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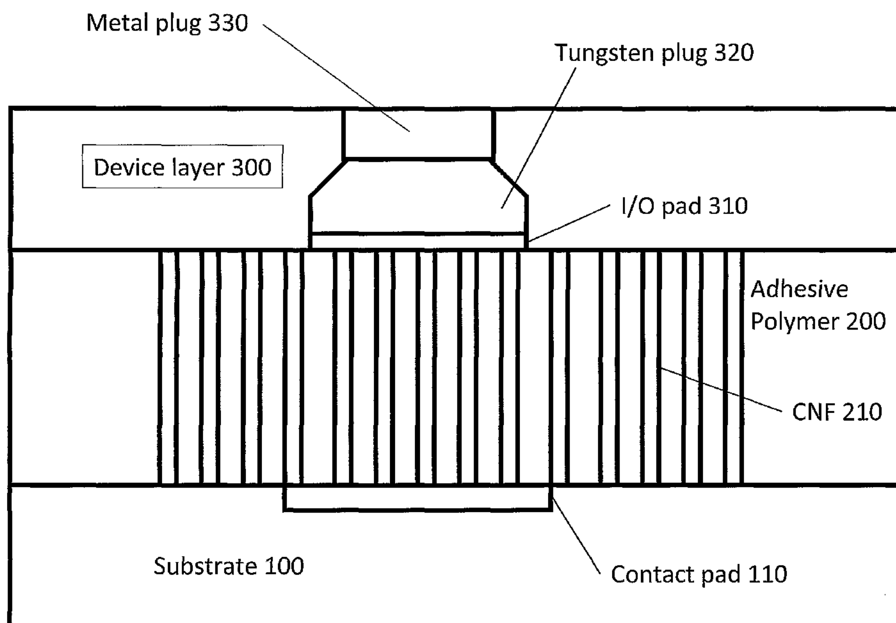
(54) Title: CONNECTING AND BONDING ADJACENT LAYERS WITH NANOSTRUCTURES



(57) Abstract: An apparatus, comprising two conductive surfaces or layers and a nanostructure assembly bonded to the two conductive surfaces or layers to create electrical or thermal connections between the two conductive surfaces or layers, and a method of making same.

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CONNECTING AND BONDING ADJACENT LAYERS WITH NANOSTRUCTURES

CLAIM OF PRIORITY

[0001] This application claims the benefit of priority to U.S. provisional patent application serial nos. 60/971,859, filed September 12, 2007, and 60/974,045, filed September 20, 2007, both of which are hereby incorporated by reference.

TECHNICAL FIELD

[0002] The technology described herein generally relates to nanostructures, and more particularly relates to use of nanostructures to connect and bond adjacent layers of conductive materials.

BACKGROUND

[0003] There are many instances in the production and manufacture of electronic devices that a layer of material, such as present in one component, is required to be attached — often at specific locations — to a substrate, such as a wafer or die. In such instances, the integrity of the attachment, whether it is mechanically, thermally or electrically, can be critical for the performance of the device.

[0004] Examples include: attaching or bonding a flip-chip to an underlayer (a substrate such as a die); fine-pitch chip-on-flex technology as used in LCD manufacture; and wafer-level bumping for creating electrical contacts at a fine pitch. In all such applications, current technologies are experiencing significant limitations, due in part to the increasing demands for miniaturization of electronic devices.

[0005] use of "flip chip" technology is growing rapidly and the technology is currently used in devices such as mobile phones, MP3-players, smart cards, displays, computer peripherals. However, in terms of complexity and product cost, flip chip technology has drawbacks, due to the requirements of complex processes that involve bonding and connecting the flip chip to the die. These processes include solder flux coating, chip/board arranging, solder bump reflow processes, flux removal processes, underfilling, and cure processes.

[0006] The techniques used in bonding and connecting flip-chips are moving towards increasingly greater numbers of I/O contacts, and finer pitches between the contacts. See, for

example, "Anisotropic Conductive Film for Flipchip Applications: An Introduction," by Peter J. Opdahl, available at www.flipchips.com/tutorial05.html, incorporated herein by reference.

[0007] As an alternative to solder bumping, anisotropic conductive film (ACF) has emerged as a lead-free, environmentally-friendly, and flux-less bonding solution consisting of conductive particles dispersed in a polymer matrix, such as an adhesive resin. ACF works by trapping conductive particles between a conductive surface, such as a conductive bump on a flip chip, and another conductive surface, such as a conductive pad on a substrate corresponding to the conductive bump on the flip chip, while insulating adjacent particles from one another.

[0008] During the last few decades, ACF has been widely used for packaging technologies in the flat panel display industry to make electrical and mechanical connections from an integrated circuit driver to a glass substrate in a display. Lately, ACF has proven to be a popular alternative to other direct chip-attach technologies, in order to satisfy requirements of finer pitch at lower dimensions. For the ACF material this means making the conductive particles as small as possible, creating high particle density, and ensuring extremely evenly distributed particles within the ACF. In addition, the flow of the polymer matrix typically has to be as well-controlled as possible. Currently, particles as small as 3.5 μm in size are used in demanding applications.

[0009] It has long been recognized that ACF suffers from a number of limitations. If the particles are too large, or if there are too many particles, there is a risk of creating a short circuit between two neighboring bumps on the flip chip. This means that there are limitations on the minimum possible pitch between particles, since a short-circuit can arise if the particles are too close to each other. This is particularly evident in, *e.g.*, the display industry, where black dots will appear when a short-circuit occurs. As there is no clear way of predicting with precision the uniformity of particle distribution within the polymer matrix, the risk of short-circuiting is always present. The impact of avoiding the risk of short-circuiting due to the particles is that the maximum possible number of contacts (I/O's) is limited, and thus the maximum possible pitch is limited when connecting a flip-chip using ACF.

[0010] Chip On Flex (COF), is a related technology that also utilizes ACF, and triggers similar issues to "flip-chip" technologies as the demand (particularly in the LCD industry) increases for finer pitch products (less than the 40 – 50 μm in current products) in order to meet cost and size requirements. There are two main issues in fine-pitch COF packaging that arise with the current bonding process: lead breakage and misalignment.

[0011] Since lead breakage during the assembly process can happen at any instance, and at any position, a visual inspection is almost impossible. Lead breakage can occur when there is a lack of trapped conductive particles between the two conductive surfaces; a trapped particle count less than one creates a high probability of an open electrical connection, which leads to electrical failure. In order to avoid that problem, the particle density must be increased, which is accomplished by reducing the diameter of the particles. If the lead pitch of the COF is 40 μm, an anisotropic conductive adhesive (ACA) with a particle diameter of less than 3 μm can be employed to achieve 99.95% chance of a good electrical connection (at least one trapped particle).

[0012] However, even at that high rate of connection integrity, the margin of error cannot be ignored. For example, for packages with 400 bumps, one out of five chips may have an open (disconnected) bump/lead joint. Moreover, if the magnitude of gap variation between bumps and leads exceeds 3 μm, an open joint failure can occur even with normal joints with trapped particles. Therefore, overall, the application of an anisotropic conducting adhesive (ACA) to fine-pitch COF interconnection requires reduced particle size and more accurate control of bump/lead height and chip/film coplanarity.

[0013] Misalignment also becomes a greater risk at finer lead pitches, since finer pitches require higher-precision control over the alignment between the film and the conductive surfaces. The existing tolerance requirement eventually needs to be replaced with a new standard for satisfactory yields. The causes of misalignment in the COF assembly process are various and may be in the film, chip, bonding equipment, and so on. The bonding tolerance relates to the nature of variation.

[0014] Thus, the main problems with ACF can be summed up as: (1) the need for uniform distributed particle size; (2) the need for control of bonding pressure to break the surface coatings of the particles and to create contacts; (3) limitations in size of the particles with respect to distribution of particles — one cannot go down to sub micron level; and (4) manufacturing limitations – one cannot manufacture at the sub micron level with good and reproducible uniformity. Accordingly, there is a need for a better way of making connections between a chip and a substrate and of attaching a chip to a substrate.

[0015] Wafer-level bumping is subject to similar considerations. The need for "bumps" for creation of the electrical contacts through distribution or contact channels with lower dimension and finer pitch demands ever greater fidelity of manufacture. Electrical connections are created by bumps, but there are limitations in the size of those bumps; it is not possible to go down to sub micron level with current manufacturing processes, which are constrained in the number of bumps

per unit area. Thus, a number of distribution channels are suffering from the constraints of creating the bumps.

[0016] The discussion of the background herein is included to explain the context of the technology. This is not to be taken as an admission that any of the material referred to was published, known, or part of the common general knowledge as at the priority date of any of the claims found appended hereto.

[0017] Throughout the description and claims of the specification the word "comprise" and variations thereof, such as "comprising" and "comprises", is not intended to exclude other additives, components, integers or steps.

SUMMARY

[0018] The present disclosure provides for an apparatus, comprising: a first conductive surface; a second conductive surface; and two or more nanostructures, wherein each of the two or more nanostructures is oriented parallel to another of the two or more nanostructures, and wherein the two or more nanostructures comprise two or more interdiffused materials, the two or more interdiffused materials including at least one material that affects a morphology of the two or more nanostructures and at least one material that affects an electrical property of an interface between the first conductive surface, and wherein a first bond exists between a first end of each of the two or more nanostructures and the first conductive surface, and wherein the two or more nanostructures are oriented perpendicular to the first conductive surface, and wherein a second bond exists between a second end of each of the two or more nanostructures and the second conductive surface, and wherein the two or more nanostructures are oriented perpendicular to the second conductive surface.

[0019] A method of connecting a first conductive surface to a second conductive surface using a nanostructure assembly, the method comprising: creating a nanostructure assembly by: depositing one or more intermediate layers on the conducting substrate, wherein at least one of the plurality of intermediate layers comprises material selected from the group consisting of amorphous silicon and germanium; depositing a catalyst layer on the one or more intermediate layers; without first annealing the substrate, causing the substrate to be heated to a temperature at which the nanostructure can form; and growing two or more nanostructures on the catalyst layer at the temperature, wherein at least one of the one or more intermediate layers are interdiffused with the catalyst layer, and wherein the catalyst layer and the at least one of the one or more intermediate layers that are interdiffused are present in the nanostructure; spincoating the

nanostructure assembly with an adhesive polymer to form a film with embedded nanostructures; polishing the film to achieve a uniform desired length for the two or more nanostructures of the nanostructure assembly; dicing the film to create one or more individual pads; lifting the pads from the conducting substrate;inserting the one or more pads between the first conductive surface and the second conductive surface; and curing the one or more pads, thereby bonding the first conductive surface to a first surface of the one or more pads and bonding the second conductive surface to a second surface of the one or more pads.

[0020] A method of connecting a first conductive surface to a second conductive surface using a nanostructure assembly, the method comprising: creating a nanostructure assembly by: depositing one or more intermediate layers on the first conductive surface, wherein at least one of the plurality of intermediate layers comprises material selected from the group consisting of amorphous silicon and germanium; depositing a catalyst layer on the one or more intermediate layers; without first annealing the substrate, causing the substrate to be heated to a temperature at which the nanostructure can form; and growing two or more nanostructures on the catalyst layer at the temperature, wherein at least one of the one or more intermediate layers are interdiffused with the catalyst layer, and wherein the catalyst layer and the at least one of the one or more intermediate layers that are interdiffused are present in the nanostructure; spincoating the nanostructure assembly with an adhesive polymer to form a film with embedded nanostructures on the first conductive surface; polishing the film to achieve a uniform desired length for the two or more nanostructures of the nanostructure assembly; dicing the film and the first conductive surface to create one or more individual pads, each pad comprising a section of the film and a section of the first conductive surface; applying one or more pads to the second conductive surface; and curing the one or more pads, thereby bonding the second conductive surface to a surface of the one or more pads.

[0021] A method of connecting a first conductive surface to a second conductive surface using a nanostructure assembly, the method comprising: creating a nanostructure assembly by: depositing one or more intermediate layers, depositing a catalyst layer on the one or more intermediate layers; without first annealing the substrate, causing the substrate to be heated to a temperature at which the nanostructure can form; and growing two or more nanostructures on the catalyst layer at the temperature, wherein at least one of the one or more intermediate layers are interdiffused with the catalyst layer, and wherein the catalyst layer and the at least one of the one or more intermediate layers that are interdiffused are present in the nanostructure; coating the nanostructures with metal deposition to form metal embedded nanostructures on the first conductive surface; spincoating the nanostructure assembly with an adhesive polymer to form a

film with embedded nanostructures on the first conductive surface; polishing the film to achieve a uniform desired length for the two or more nanostructures of the nanostructure assembly; dicing the film and the first conductive surface to create one or more individual pads, each pad comprising a section of the film and a section of the first conductive surface; applying one or more pads to the second conductive surface; and curing the one or more pads, thereby bonding the second conductive surface to a surface of the one or more pads.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] FIG. 1: bonding and electrical contacting of a die to a substrate using carbon nanofibers in a matrix – principle.

[0023] FIG. 2: bonding and electrical contacting of a die to a substrate using carbon nanofibers in a matrix, prior to curing.

[0024] FIGs. 3A, 3B: bonding and electrical contacting of a die to a substrate using carbon nanofibers in a matrix, after curing.

[0025] FIG. 4: Top view of carbon nanofibers in a matrix.

[0026] FIG. 5: Top view of carbon nanofibers in a matrix with an I/O pad.

[0027] FIG. 6: Cross-sectional view of carbon nanofibers in a matrix with an I/O pad.

[0028] FIG. 7 shows a flow-chart of a process as described herein;

[0029] FIG. 8 shows a flow-chart of a process as described herein; and

[0030] FIG. 9 shows a flow-chart of a process as described herein.

DETAILED DESCRIPTION

[0031] The instant technology is directed to methods of connecting two surfaces or layers by bonding nanostructures to contact locations on the two surfaces or layers, thereby creating mechanical, electrical, or thermal connections between the two surfaces or layers. By such methods, the pitch of the contact locations may be within the inclusive range of 2 nm to 1 mm. The instant technology further includes an apparatus comprising a first conductive surface or layer, a second conductive surface or layer, and a nanostructure assembly bonded to and positioned in between the two conductive surfaces or layers, such that the nanostructures of the nanostructure assembly are oriented perpendicular to the two conductive surfaces or layers.

[0032] In other aspects of the technology, a bonding layer is formed by growing nanostructure, such as carbon nanostructures (CNS), on metallic underlayers formed on a substrate. The substrate may comprise one or more layers of metal, semiconductive materials, or insulating materials, or combinations thereof. The nanostructures grow perpendicular to the substrate surface. The nanostructures can be coated in a carrier such as a polymer, *e.g.*, an adhesive polymer. The carrier may be a polyimide, or may be a flexible or solid material. Optionally the nanostructures, coated or not, can be polished to provide uniform length. The resulting structures can be diced into individual films. Optionally, the film of polymer and nanostructures can be lifted from the substrate. The film can then be applied to the surface of a die to provide wafer contacts.

[0033] In still other aspects of the technology, a wafer bonding layer can include nanostructures, such as carbon nanostructures (CNS), held in a polymer coating. The nanostructures extend perpendicularly to the top and bottom surfaces of the layer. The nanostructures can be grouped, with nanostructures within a group at a regular spacing, and groups at another regular (larger) spacing. Nanostructures within a group can be electrically connected, either by being placed in direct contact with a common electrode, or by being grown on metal underlayers that are electrically coupled. In contrast, nanostructures of separate groups are electrically isolated.

[0034] When "perpendicular" is used herein to describe an orientation between a nanostructure and a layer or surface, it is understood that the nanostructure is of the form of a wire, tube, or fiber, or similar structure, that has a longitudinal axis extending along its length, and it is the longitudinal axis that is disposed normal to the plane of a layer or surface. It is further to be understood that "perpendicular" encompasses small deviations from exact perpendicularity, such as for example an inclination of the longitudinal axis that is 88 – 90° with respect to the plane, or 85 – 90° with the respect to the plane.

[0035] In some embodiments, the nanostructures are generally rigid, such that the layer that contains them can be generally incompressible.

[0036] Examples of nanostructures include, but are not limited to, nanotubes, nanofibers, or nanowires. In particular, nanostructures found herein can be made of carbon based nanostructures such as carbon nanotube(s), carbon nanofiber(s), or carbon nanowire(s).

[0037] Nanostructures found herein can also be made of other materials such as metals, III-V, II-VI compounds, or combinations of elements from the periodic table of the elements. Examples

of materials include semiconductors such as GaAs, InP, InGaAs, AlGaAs, nanowires such as silicon nanowires, alloys such as ZnO, ZnAlO, and any other binary or ternary alloys from which nanostructures can be formed.

[0038] Nanostructures consistent with applications herein can be grown/formed/deposited on substrates such as silicon, polysilicon, oxidized silicon, silicon nitride, germanium, silicon-germanium, GaAs, AlGaAs, GaN, InP, glass, polyimide, polymer, metals such as W, Mo, Ti, Cr, NiCr, Al, AlOx, Pt, Pd, Au, Cu, TiN, or any other metal from the periodic table, plastics, aluminium foil, alumina, papers, and high k materials such as HfO, ZrO, etc, For growth of the nanostructures, the catalyst can be of Ni, NiCr, Pd, Pt, Fe, Au, Co, or combinations of such metals, or alloys of different materials, for example bimetallic catalysts such as Co-V, Co-Ni, Fe-Ni, etc.

[0039] Chemical Vapor Deposition (CVD) is a typical method for growth of nanostructures for use with the technology described herein. However, there are different kinds of CVD methods that can be used, *e.g.*, thermal CVD, PECVD, RPECVD, MOCVD (metallo-organic CVD), etc. or any other variants of CVD as is known by the skilled artisan. Particular methods of growth are described in U.S. Pat. Appl. Ser. No. 11/412,060, "Controlled Growth of a Nanostructure on a Substrate," filed April 25, 2006, which is incorporated herein by reference in its entirety.

[0040] Still further, the nanostructures herein can be formed from methods and materials, employing conditions, that permit control of various properties of the nanostructures once formed. Thus, the nanostructures used herein encompass nanostructures grown from substrates, and interface layers situated therebetween, having the following characteristics. The substrate is preferably a conducting layer such as a metal layer, which maybe disposed on a support. The support is typically a wafer of silicon or other semiconducting material, glass, or suitable flexible polymer used in thin film technology. The metal is preferably selected from the group consisting of molybdenum, tungsten, platinum, palladium, and tantalum. The thickness of the metal layer is preferably in the range 1 nm to 1 μm and even more preferably in the range 1 nm to 50 nm. The metal layer is preferably deposited by any one of several methods known in the art, including but not limited to: evaporative methods such as thermal or vacuum evaporation, molecular beam epitaxy, and electron-beam evaporation; glow-discharge methods such as any of the several forms of sputtering known in the art, and plasma processes such as plasma-enhanced CVD; and chemical processes including gas-phase processes such as chemical vapor deposition, and ion implantation, and liquid-phase processes such as electroplating, and liquid phase epitaxy. Examples of

deposition technologies are found in *Handbook of Thin Film Deposition*, K. Seshan, Ed., Second Edition, (William Andrew, In, 2002).

[0041] The interface layers, also called intermediate layers or an intermediate layer, comprise one or more layers, in sequence, disposed upon the substrate. On top of the interface layers is a layer of catalyst. The nanostructure is grown from on top of the catalyst layer.

[0042] The interface layers may consist simply of a single layer of material. In this circumstance, the single layer can be silicon or germanium. The layers can be deposited in amorphous or crystalline forms by techniques such as evaporation, or sputtering. The thickness typically ranges from 1 nm to 1 μm and also in the range 1 nm to 50 nm.

[0043] The interface layers may comprise several layers of different materials and may be, arbitrarily, classified according to function. For example, the layers in the vicinity of the substrate are characterized as layers that influence the electrical properties of the interface. The layers in the vicinity of the catalyst are characterized as layers that influence the composition and properties such as electrical/mechanical properties of the nanostructure.

[0044] Various configurations of interface layers are compatible with the present invention. For example, a sequence of up to 3 layers may be deposited on the substrate, for the purpose of controlling the electrical properties of the interface. Such configurations include, but are not limited to: a sequence of insulator, conductor or semiconductor, and insulator; a sequence of insulator adjacent to the substrate, and a semiconducting layer; a sequence of semiconductor, insulator, semiconductor; a sequence of two insulating barrier layers adjacent to the substrate, and a semiconductor; a single layer of a metal that is different from the metal of the substrate; and a sequence of a metal that is different from the metal of the substrate, and a semiconducting layer. In such configurations, the insulator may be selected from the group consisting of: SiO_x, Al_2O_3, ZrO_x, HfO_x, SiN_x, Al_2O_3, Ta_2O_5, TiO_2, and ITO. The semiconductor may be silicon or germanium. The metal, where present, may be palladium, platinum molybdenum or tungsten. Where two layers of the same character are present, *e.g.*, two semiconducting layers, it is not necessary that the layers have the same composition as one another.

[0045] The uppermost layer of the foregoing interface layers may itself abut against the catalyst layer. This is particularly the case where the uppermost layer is a semiconductor such as silicon or germanium. However, it is additionally possible for the foregoing interface layers to have disposed upon them a further layer or sequence of layers that lies between them and the catalyst layer. Such additional, or second, interface layers are thought of as controlling the

properties and composition of the nanostructure. The second interface layers may be a pair of layers, such as a metal layer and on top thereof a semiconductor layer adjacent to the catalyst layer. Alternatively, the second interface layers may simply consist of a single layer of semiconductor. The metal layer, where present in the second interface layers, is preferably selected from the group consisting of tungsten, molybdenum, palladium, and platinum. The semiconducting layer in the second interface layers is preferably silicon or germanium.

[0046] The catalyst layer is typically a layer of metal or metal alloy, and may contain very fine particles of metal or metal alloy instead of being a continuous film. The catalyst layer preferably comprises a metal selected from the group consisting of nickel, palladium, iron, nickel-chromium alloy containing nickel and chromium in any proportions, and molybdenum.

[0100] The nanostructures typically have a multi-stack configuration of at least one material layer between the catalyst layer and the conducting substrate, wherein the material is not of the same kind as the catalyst and conducting substrate, and wherein the material controls the chemical reactions between the various layers. Thus, the growth of the nanostructures on different conducting substrates can be controlled. Thereby the morphology and properties of the grown structures as well as the tip materials of the grown structures can be controlled. The current technology can be extended to having several stacks of materials of different kinds (semiconducting, ferroelectric, magnetic, etc.) which can be used to control the properties at base/interface, body and the tip of the nanostructure. It is also possible that the nanostructure is grown upon a conducting layer which is itself deposited on a substrate that itself can be of any kind, such as conducting, insulating or semiconducting.

[0047] Typically, during growth of such nanostructures, some diffusion of the material of the intermediate layers into the nanostructures occurs. Such interdiffusion may transport the material of the intermediate layers all the way to the tip of the grown nanostructures. In some conditions, the diffused material is present as a narrow band; in others, the diffused material is spread out through the nanostructure.

[0048] The methods described herein are applicable in any assembly techniques for electronic components that include analog and/or digital electronic circuits. For example, such components may be found in: communications engineering, car/industrial electronics goods, consumer electronics, computing, digital signal processing and integrated products. Attaching technologies such as ball grid array (BGA), flip chip (FC) modules, CSP, WLP, FCOB, TCB may utilize the methods herein. Integrated Circuit (IC) types such as RFID, CMOS, BiCMOS, GaAS, AlGAAs, MMIC, MCM, may utilize the methods described herein. Display technologies such as LCD's,

LED's, and OLED's, as used in automobiles, computers, mobile phone handsets, and televisions may also incorporate connections made by the methods described herein. Other electronic components that may similarly incorporate such technology include, but are not limited to: ASIC chips, memory devices, MCU, high frequency device modules, integrated passive components, etc.

[0049] The methods described herein can also be used to create interconnects, thermal vias or heat conductors or non-heat conductors, inductors, capacitors and resistors, to the extent that they benefit from techniques that create connections between two layers of materials. The method can further be used for optoelectronic devices such as photonic crystals, wave guides, filters, optoelectronic circuits, etc. The method can also used for biological devices, or mixed biological and silicon-based devices, such as lab-on-a-chip arrays, and probes for bio-diagnostics.

Structure

[0050] The apparatus created by the process described herein comprises a carrier with nanostructures embedded within the carrier, wherein the nanostructures were grown to have a specific morphology and functionality. The nanostructures are oriented so as to be approximately parallel to each other and perpendicular to the substrate. The nanostructures are of an approximate desired length or height.

[0051] FIGs. 1 – 8 illustrate, schematically, the methods and apparatus described herein. It would be understood that, although FIG.s 1 – 8 have been illustrated using a carbon nanofiber (CNF), other forms of nanostructures may similarly be used. Such alternative nanostructures include, but are not limited to, nanotubes, nanowires, and nanoropes. Such nanostructures may be made from carbon, doped with one or more other elements, but are not so limited.

[0052] FIG. 1 illustrates the overall principle of bonding and electrical contacting of two adjacent metal layers, such as a die to a substrate, using a pad of carbon nanofibers in a matrix. Shown in FIG. 1 are three layers: a substrate 100 having an embedded contact pad 110, on top of which is a layer of adhesive polymer 200 that surrounds a number of carbon nanofibers (CNF) 210 oriented perpendicularly to the substrate 100 and some of which are in contact with contact pad 110, and on top of the adhesive polymer layer is a device layer 300. The device layer 300 includes an I/O pad 310, to which a number of the carbon nanofibers are connected, a first metal plug 320, made from tungsten as an example, on top of the I/O pad, and a second metal plug 330, on top of the first plug. Plugs 320, 330 are different from one another, and can be made of tungsten or any other metal used in the industry such as Al, Cu, or Au.

[0053] FIG. 2 shows bonding and electrical contacting of a die to a substrate using carbon nanofibers in a matrix, prior to curing. Only a single CNF is shown in this figure, purely for ease of illustration.

[0054] FIGs. 3A, 3B show bonding and electrical contacting of a die to a substrate using carbon nanofibers (only a single CNF is shown in FIG. 3A, for ease of depiction) in an adhesive polymer matrix, after curing. Double-headed arrow 220 indicates a straightening force inducing a "spring load" in the CNF. Two single headed arrows 230 indicate a contracting adhesive force induced by curing.

[0055] FIG. 3B shows bonding and electrical contacting of a die to a substrate using carbon nanofibers in a matrix, after curing. Double-headed arrow 220 indicates a straightening force inducing "spring load" in the CNF. Two single headed arrows 230 indicate a contracting adhesive force induced by curing.

[0056] FIG. 4 shows a view from the top of an array of carbon nanofibers in a matrix. Representative spacings are shown. The pitch between adjacent nanostructures is 200 nm; the dimension of the array is 600 nm; and the nanofibers have a diameter of 50 nm.

[0057] FIG. 5 shows a view from the top of an array of carbon nanofibers in a matrix with an I/O pad overlaying a subset of the nanostructures. Representative spacings are shown. The pitch between adjacent nanostructures is 200 nm; the dimension of the array is 600 nm; and the nanofibers have a diameter of 50 nm; the diameter of the I/O pad is shown as 400 nm.

[0058] It would be understood by one skilled in the art that the spacings shown in FIGs. 4 and 5 are exemplary, and that the operation of technology herein is not dependent on the precise values of those spacings, as shown in the figures.

[0059] FIG. 6 shows a cross-sectional view of carbon nanofibers in a matrix with an I/O pad, such as that shown in FIG. 5. Certain of the nanostructures connect the contact pad and the I/O pad, whereas others are disposed outside of the area that the pads have in common and need not, as shown, extend through the entire thickness of the adhesive layer.

Example 1: Process for Creating Contacts Using Nanostructures and an ACF

[0060] This example provides a method of connecting two surfaces/layers (such as between a contact surface/layer of a first die or chip, and a contact layer/surface of a second die or chip to which the first is going to be attached). The connection is by bonding and electrically/thermally

contacting with any pitch in the range of 1 millimetre to 2 nm and typically down to 20 nm where the electrically/thermally contacting elements are based on nanostructures.

[0061] A structure consistent with this method consists of: (a) a layer of carrier (such as based on flexible, or solid material, for example polyimide), (b) nanostructures embedded in the carrier with specific morphology and functionality where they are oriented parallel with each other and perpendicular to both carrier surfaces, and (c) where the nanostructures can be grown according to methods described in international patent application PCT/SE2006/000487 (which is hereby incorporated by reference) such that control is demonstrated over morphology, dimension, length, distance, etc.

[0062] A typical nanostructure assembly for use herein comprises: a conducting substrate (such as a metal); a first catalyst layer on the conducting substrate; a nanostructure supported by the first catalyst layer; and a plurality of intermediate layers between the conducting substrate and the first catalyst layer, the plurality of intermediate layers including at least one layer that affects a morphology of the nanostructure and at least one layer to affect an electrical property of an interface between the conducting substrate and the nanostructure.

[0063] Features of the structure include: the contacting elements (nanostructures) are perpendicular to the connecting surfaces, although the nanostructures are parallel with each other. The properties of the nanostructures can be tailored according to methods of growth. Each unit can be combined with other such units for assembly into further structures, much as building blocks, like Lego, can be.

[0064] FIG. 7 illustrates steps in an exemplary process for connecting two surfaces or layers by bonding and creating electrical or thermal contacts comprising nanostructures. The steps comprise: growing a layer of carbon nanostructures on a conducting substrate with a plurality of intermediate layers between the conducting substrate and the nanostructures (701); spincoating the resulting nanostructures with an adhesive polymer to form a film with embedded nanostructures (702); polishing the film to create nanostructures of a uniform desired length (703); dicing the film to create individual pads (704); lifting the pads (705); applying each pad between a first conductive surface or layer (*e.g.*, the surface of a die) and a second conductive surface or layer (of, for example, a contact on a chip) (706); and curing the pads, such that the die is bonded to the pad and the pad is bonded to the contacting surface, thus creating electrical or thermal contacts between the die and the contacting surface by way of the nanostructures embedded within the pad (707).

[0065] The first step (701) of growing the layer of nanostructures on a conducting substrate with a plurality of intermediate layers between the conducting substrate and the nanostructures comprises growing the nanostructures, typically with a density of greater than 10 nanostructures per μm. Such a density, or the required density in a given instance, may be achieved by controlled application of catalyst dots on the substrate. Nanostructures are preferably grown using any of the various CVD-based methods, but may be grown or formed using any standard technique.

[0066] The second step (702) of spincoating the resulting nanostructures with an adhesive polymer to form a film with embedded nanostructures may be accomplished using any standard spincoating or equivalent technique of forming a carrier for the nanostructures (in a film or other layer), wherein the nanostructures are embedded within the carrier. Such a carrier may comprise an adhesive polymer or any other equivalent material that is able to adhere to a die and a contacting surface, by way of curing, pressure, heat, or other equivalent processes. The methods described herein are not limited to the exemplary embodiment of spincoating or the exemplary embodiment of use of an adhesive polymer that may be cured.

[0067] The third step (703) of polishing the carrier to achieve a uniform desired length for the nanostructures may be accomplished using any standard technique of polishing appropriate to the instant technology, whether mechanical, chemical, or otherwise. The determination of whether the nanostructures have attained the uniform desired length may, likewise, be made using any standard technique known or utilized within the art or related arts. This step is optional.

[0068] The fourth step (704) of dicing the carrier to create individual pads may be accomplished using any standard technique of dicing or otherwise creating individual pads of a desired shape and size.

[0069] The fifth step (705) of lifting the individual pads (portions of film comprised of vertically aligned carbon nanostructures embedded in adhesive polymer) may be accomplished using any standard technique of lifting such pads.

[0070] The sixth step (706) of applying each pad between a first conductive surface (of, for example, a die) and a second conductive surface (of, for example, a contact on a chip) may be accomplished using any standard technique of applying and positioning such a pad in such a location.

[0071] The seventh step (707) of curing the pads results in creation of a bond, wherein the pad is sandwiched between, and bonded to, both conductive surfaces. This bond creates electrical or

thermal contacts between the two conductive surfaces by way of the nanostructures embedded within the pad. This step is not limited to curing an adhesive polymer; it may comprise any standard technique of causing adhesion between the nanostructures embedded within the pad and the die on one side of the pad and the contacting surface on another side of the pad.

[0072] This overall process has several advantages: eliminating the need for traditional bumps, reducing the minimum possible distance between the two conductive surfaces, decreasing both the height and width of the contact points, allowing for an increase in the number and density of the contact points, eliminating complications related to the need to control the degree of pressure applied to the ACF, and enabling finer pitches by replacing particles with nanostructures, and reducing the risk of misalignment.

[0073] Consistent with the instant example, a controllable density of nanostructures (NS) per micrometer permits an increase in the effective contact points, when compared to current solutions based on spherical particles. For example, 100 NS/micrometer square (with an NS diameter of 50 nm) gives 100 individual contacting points, (see also FIGs. 4 and 5). Given dimensions of the I/O point of 20 X 20 micrometer, the number of individual contacting points can be 4,000 in that region.

Example 2: Process for Creating Spring Load Connections

[0074] A carrier (which can be based on flexible, polyimide or solid material) containing vertically aligned nanostructures (NS) (parallel oriented with each other and perpendicular to both carrier surfaces, and such as prepared by steps described in Example 1) is placed between the surface of a die and a contacting surface. See FIG. 2 and FIG. 4 as examples.

[0075] By curing of the carrier containing the vertically aligned nanostructures (using heat or chemical components or light), the carrier will contract (decreasing the distance between the die and contacting layer).

[0076] The contracting of the carrier will induce a contracting force on the vertically aligned nanostructures. The result of the contracting force on the nanostructures will be a slight bending of the nanostructures. However, due to difference in the Young modulus between the nanostructures and the surrounding materials, the nanostructures will have a tendency to straighten.

[0077] The forces described above create the "spring-load" force in the nanostructures. When the nanostructures embedded in the carrier material are placed between the two conducting

surfaces, the spring-load force will secure the contacts to the ends of the nanostructures. (See FIGs. 3A and 3B as examples.)

[0078] A process of providing a spring-loaded connection by providing bonding of the die to the substrate, creating and securing the electric contact by using the NS's embedded in carrier, is shown in FIG. 8. Steps of FIG. 8 that are common with those of FIG. 7 are described in connection with Example 1, herein, and are not repeated here.

[0079] During the sixth step (806) of curing the pads of carrier with embedded nanostructures, the curing process may use heat, or chemical components, or light to cause the carrier to contract, thereby decreasing the distance between the die and contacting layer.

[0080] The nanostructures of this example can be made according to the same methods as the nanostructures of Example 1, herein, and in particular can be grown according to methods described in international patent application PCT/SE2006/000487 (which is hereby incorporated by reference) such that control is demonstrated over morphology, dimension, length, distance, etc.

[0081] The process described in this example can be utilized to address the lead breakage and misalignment issues that can arise with Chip On Flex applications.

[0082] Similarly to the structures of Example 1, properties of the spring-loaded structure include: the contacting elements (nanostructures) are perpendicular to the connecting surfaces, although the nanostructures are parallel with each other. The properties of the nanostructures can be tailored according to methods of growth. Each unit can be combined with other such units for assembly into further structures.

[0083] This overall process has several advantages: reducing the minimum possible distance between the two conductive surfaces, decreasing both the height and width of the contact points, allowing for an increase in the number and density of the contact points thereby increasing the effective contact area, eliminating complications related to the need to control the degree of pressure applied to the ACF, enabling finer pitches by replacing particles with nanostructures, and reducing the risk of misalignment, and securing of the electric contact between two points placed on the opposite surfaces using nanostructures which are slightly bent. When the nanostructures are slightly bent it is possible to minimize gap creation due to surface roughness in the bonding surfaces.

[0084] Consistent with the instant example, a controllable density of nanostructures (NS) per micrometer permits an increase in the effective contact points, when compared to current solutions

based on spherical particles. For example, a controllable nanostructure diameter ranging from 1 nm to 200 nm) gives a predefined individual contact point and a contact area per nanometers square.

Example 3: Wafer level bumping (WLB)

[0085] This example demonstrates how wafer level bumping can be achieved by growing a matrix of nanostructures on I/O points on electronic circuits to thereby create electronic assembly for dies. The method can also be a method of connecting two surfaces/layers (contact surface/layer of the die or chip, and contact layer/surface of the die or chip to which the first layer will be connected), by bonding and electrically and/or thermally contacting with any pitch in range of 1 centimeter to 2 nm, and typically down to 1 μm, where the electrically/thermally contacting elements are based on nanostructures.

[0086] The following three cases illustrate possible embodiments.

[0087] Case 1: Vertically aligned nanostructures grown on I/O points on a integrated circuits of a wafer thereby creating a matrix structures and embedded in a curable (in UV/laser/light) material with adhesive nature, which is corresponding to the connecting points on a substrate where the die needs to be connected to.

[0088] Case 2: Vertically aligned nanostructures grown on I/O points on a integrated circuits of a wafer thereby creating a matrix structures and which is corresponding to the connection points on a substrate at which the die needs to be connected, and the attachment is made via traditional high temperature soldering process.

[0089] Case 3: Vertically aligned nanostructures grown on I/O points on an integrated circuit of a wafer creating a matrix structure, which is corresponding to the connecting points on a substrate at which the die needs to be connected.

[0090] In general, similarly to the structures of Examples 2 and 3, properties of the wafer level bumping structure include: the contacting elements (nanostructures) are perpendicular to the connecting surfaces, although the nanostructures are parallel with each other. The properties of the nanostructures can be tailored according to methods of growth. The vertically aligned nanostructures can form groups of connecting structures with a dimension from 1 millimetre down to 2 nm.

[0091] The nanostructures of this example can be made according to the same methods as the nanostructures of Examples 1 and 2, herein, and in particular can be grown according to methods

described in international patent application PCT/SE2006/000487 (which is hereby incorporated by reference) such that control is demonstrated over morphology, dimension, length, distance, etc.

[0092] A process of providing a wafer-level bump is shown in FIG. 9. Steps of FIG. 9 that are common with those of FIGs. 7 and 8 are described in connection with Examples 1 and 2, herein, and are those descriptions are not repeated here.

[0093] In current systems, bumps for can have a diameter from 500 micrometer and downwards. The method of this example permits a groups of nanostructures to be assembled, each individual group having the same dimension as today's bumps. However, the present technique also permits smaller bumps, even down to bumps that comprise a single nanostructure.

[0094] Composite bumps can also be formed by methods based on those described herein. Standard evaporation, electroplating and/or electroless plating can be carried out after the growth of nanostructures to form composites bumps where necessary. Different metals/metallic materials from periodic table such as Ti, Cr, TiW, Cu, Au or any other suitable metal can be evaporated, electroplated, and /or electroless plated after the growth of nanostructures. Standard immersion gold process can also be carried out to coat gold where necessary. Electroless plating process may consists of conditioning, acid etching, plating through different chemical compositions for different metal for example, Ni, Cu, Zn, Sn, or different alloys.

WHAT IS CLAIMED:

1. An apparatus, comprising:

a first conductive surface;

a second conductive surface; and

two or more nanostructures,

wherein each of the two or more nanostructures is oriented parallel to another of the two or more nanostructures, and

wherein the two or more nanostructures comprise two or more interdiffused materials, the two or more interdiffused materials including at least one material that affects a morphology of the two or more nanostructures and at least one material that affects an electrical property of an interface between the first conductive surface, and

wherein a first bond exists between a first end of each of the two or more nanostructures and the first conductive surface, and

wherein the two or more nanostructures are oriented perpendicular to the first conductive surface, and

wherein a second bond exists between a second end of each of the two or more nanostructures and the second conductive surface, and wherein the two or more nanostructures are oriented perpendicular to the second conductive surface.

2. The apparatus of claim 1, further comprising:

a carrier, wherein the two or more nanostructures are embedded in the carrier.

3. The apparatus of claim 2, wherein the first bond and the second bond are created by curing the carrier.

4. The apparatus of claim 3, wherein curing the carrier causes the carrier to contract, thereby compressing the two or more nanostructures and creating a spring-load force that pushes the first end of each of the two or more nanostructures against the first conductive surface and pushes the second end of each of the two or more nanostructures against the second conductive surface.

5. The apparatus of claim 1, wherein at least one material of the two or more interdiffused materials are selected from the group consisting of amorphous silicon and germanium.

6. A method of connecting a first conductive surface to a second conductive surface using a nanostructure assembly, the method comprising:

creating a nanostructure assembly by:

depositing one or more intermediate layers on the conducting substrate, wherein at least one of the plurality of intermediate layers comprises material selected from the group consisting of amorphous silicon and germanium;

depositing a catalyst layer on the one or more intermediate layers;

without first annealing the substrate, causing the substrate to be heated to a temperature at which the nanostructure can form; and

growing two or more nanostructures on the catalyst layer at the temperature, wherein at least one of the one or more intermediate layers are interdiffused with the catalyst layer, and wherein the catalyst layer and the at least one of the one or more intermediate layers that are interdiffused are present in the nanostructure;

coating the nanostructure assembly with an adhesive polymer to form a film with embedded nanostructures;

polishing the film to achieve a uniform desired length for the two or more nanostructures of the nanostructure assembly;

dicing the film to create one or more individual pads;

lifting the pads from the conducting substrate;

inserting the one or more pads between the first conductive surface and the second conductive surface; and

curing the one or more pads, thereby bonding the first conductive surface to a first surface of the one or more pads and bonding the second conductive surface to a second surface of the one or more pads.

7. The method of claim 6, wherein bonding the first conductive surface to a first surface of the one or more pads and bonding the second conductive surface to a second surface of the one or more pads thereby creates electrical or thermal contacts between the first conductive surface and the second conductive surface by way of the nanostructures embedded within the pad.

8. A method of connecting a first conductive surface to a second conductive surface using a nanostructure assembly, the method comprising:

creating a nanostructure assembly by:

depositing one or more intermediate layers on the first conductive surface, wherein at least one of the plurality of intermediate layers comprises material selected from the group consisting of amorphous silicon and germanium;

depositing a catalyst layer on the one or more intermediate layers;

without first annealing the substrate, causing the substrate to be heated to a temperature at which the nanostructure can form; and

growing two or more nanostructures on the catalyst layer at the temperature, wherein at least one of the one or more intermediate layers are interdiffused with the catalyst layer, and wherein the catalyst layer and the at least one of the one or more intermediate layers that are interdiffused are present in the nanostructure;

coating the nanostructure assembly with an adhesive polymer to form a film with embedded nanostructures on the first conductive surface;

polishing the film to achieve a uniform desired length for the two or more nanostructures of the nanostructure assembly;

dicing the film and the first conductive surface to create one or more individual pads, each pad comprising a section of the film and a section of the first conductive surface;

applying one or more pads to the second conductive surface; and

curing the one or more pads, thereby bonding the second conductive surface to a surface of the one or more pads.

9. A method of connecting a first conductive surface to a second conductive surface using a nanostructure assembly, the method comprising:

creating a nanostructure assembly by:

depositing one or more intermediate layers,

depositing a catalyst layer on the one or more intermediate layers;

without first annealing the substrate, causing the substrate to be heated to a temperature at which the nanostructure can form; and

growing two or more nanostructures on the catalyst layer at the temperature, wherein at least one of the one or more intermediate layers are interdiffused with the catalyst layer, and wherein the catalyst layer and the at least one of the one or more intermediate layers that are interdiffused are present in the nanostructure;

coating the nanostructures with metal deposition to form metal embedded nanostructures on the first conductive surface;

coating the nanostructure assembly with an adhesive polymer to form a film with embedded nanostructures on the first conductive surface;

polishing the film to achieve a uniform desired length for the two or more nanostructures of the nanostructure assembly;

dicing the film and the first conductive surface to create one or more individual pads, each pad comprising a section of the film and a section of the first conductive surface;

applying one or more pads to the second conductive surface; and

curing the one or more pads, thereby bonding the second conductive surface to a surface of the one or more pads.

FIG. 1

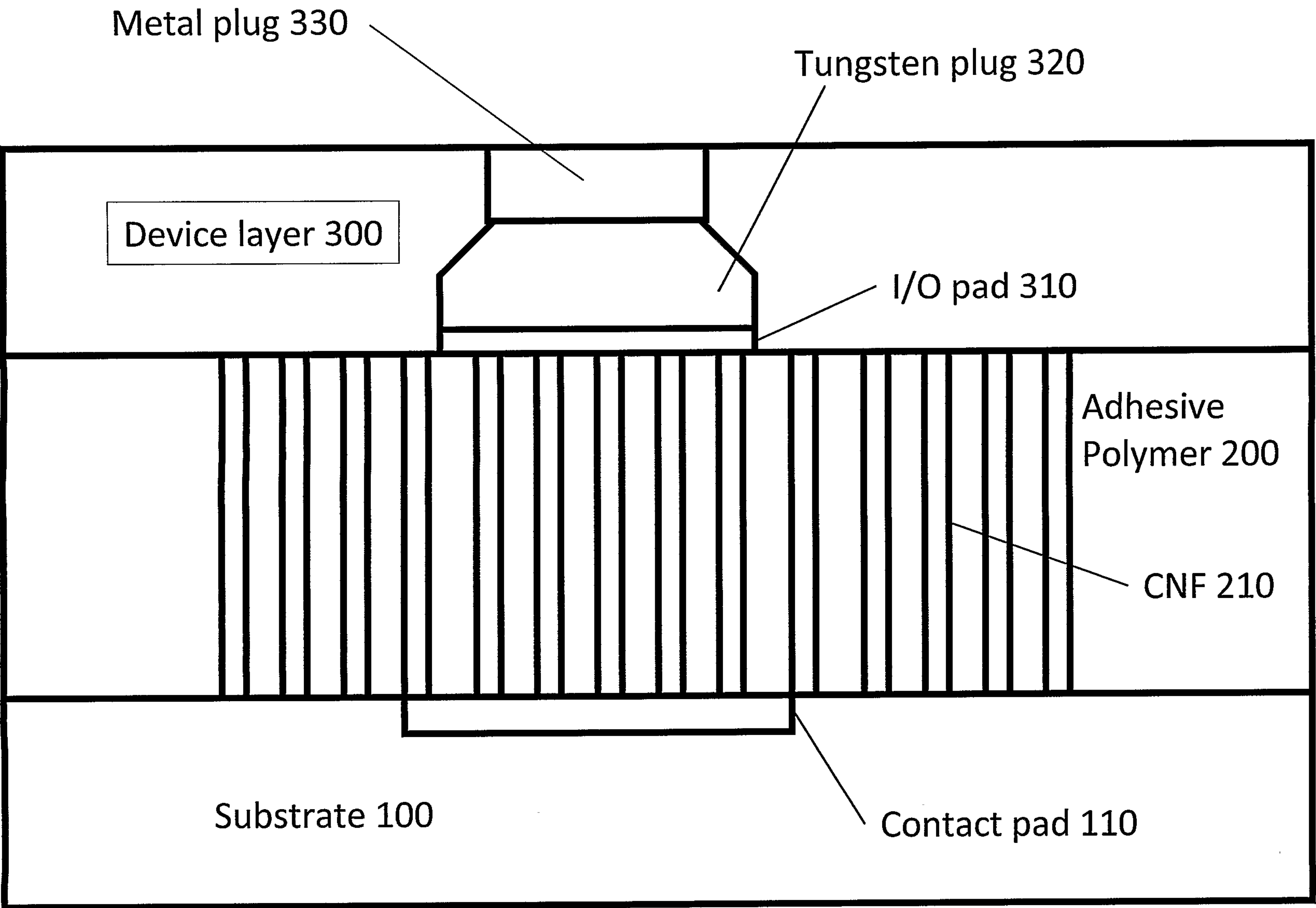
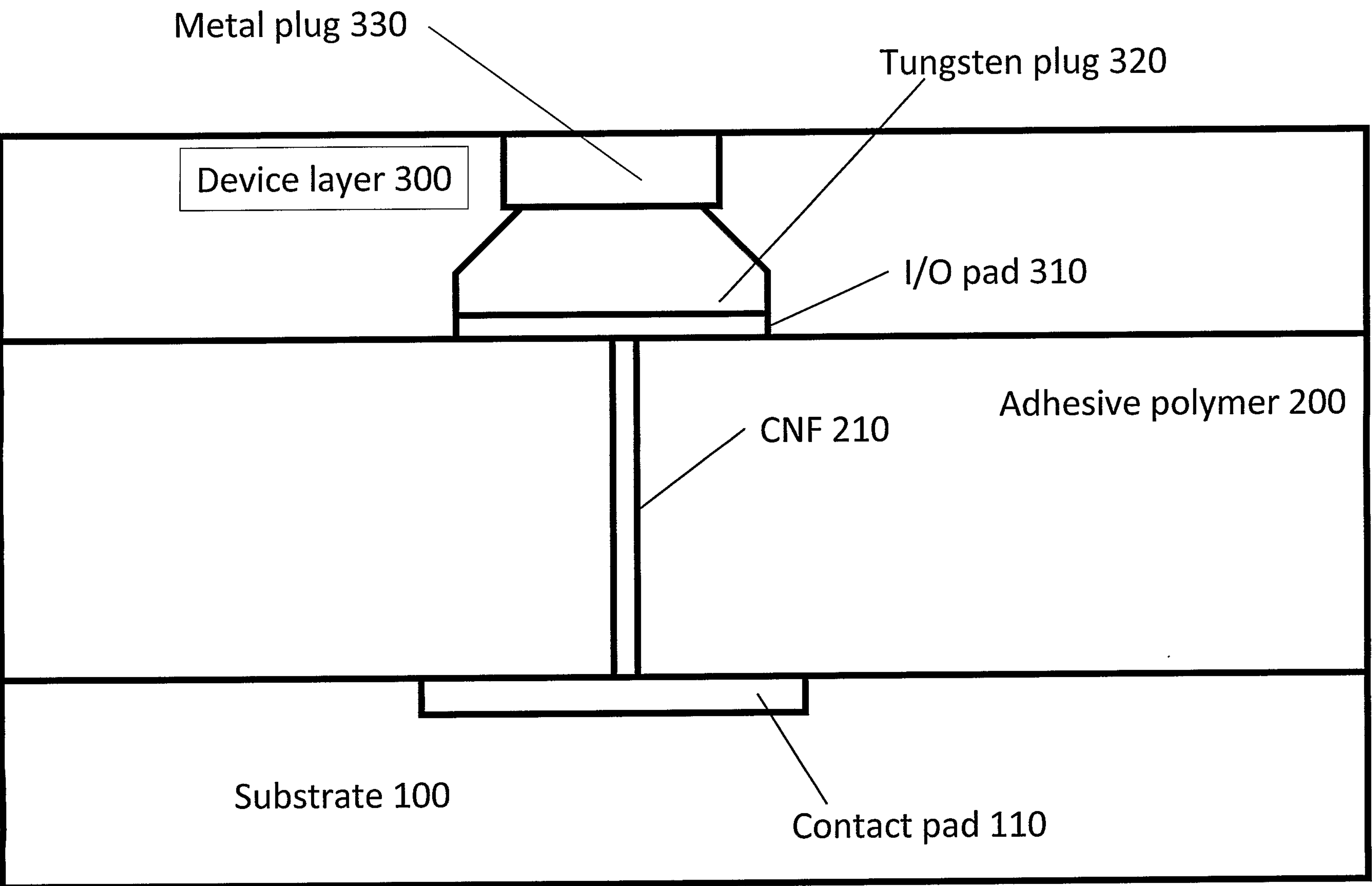


FIG. 2



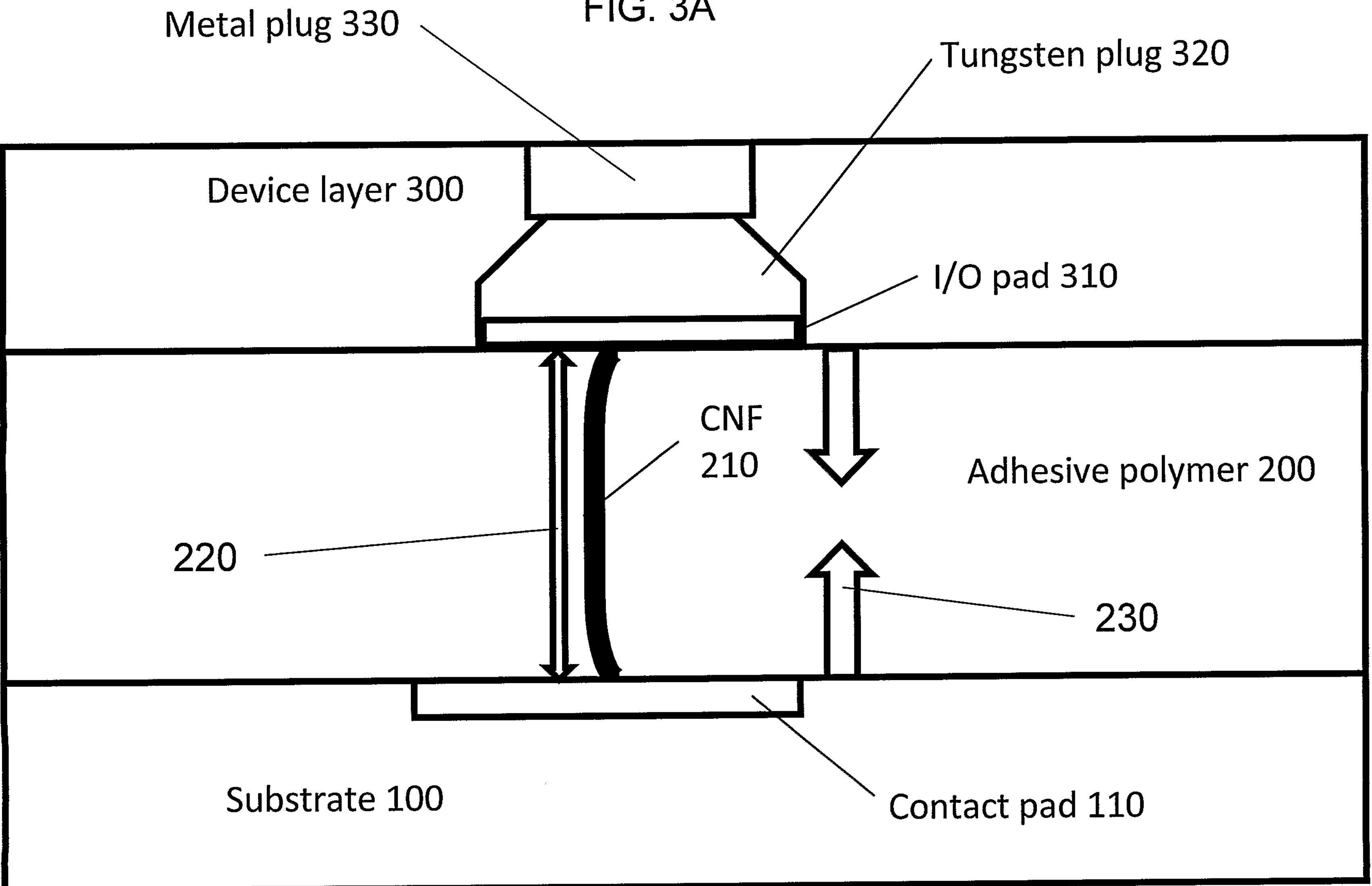


FIG. 3A

FIG. 3B

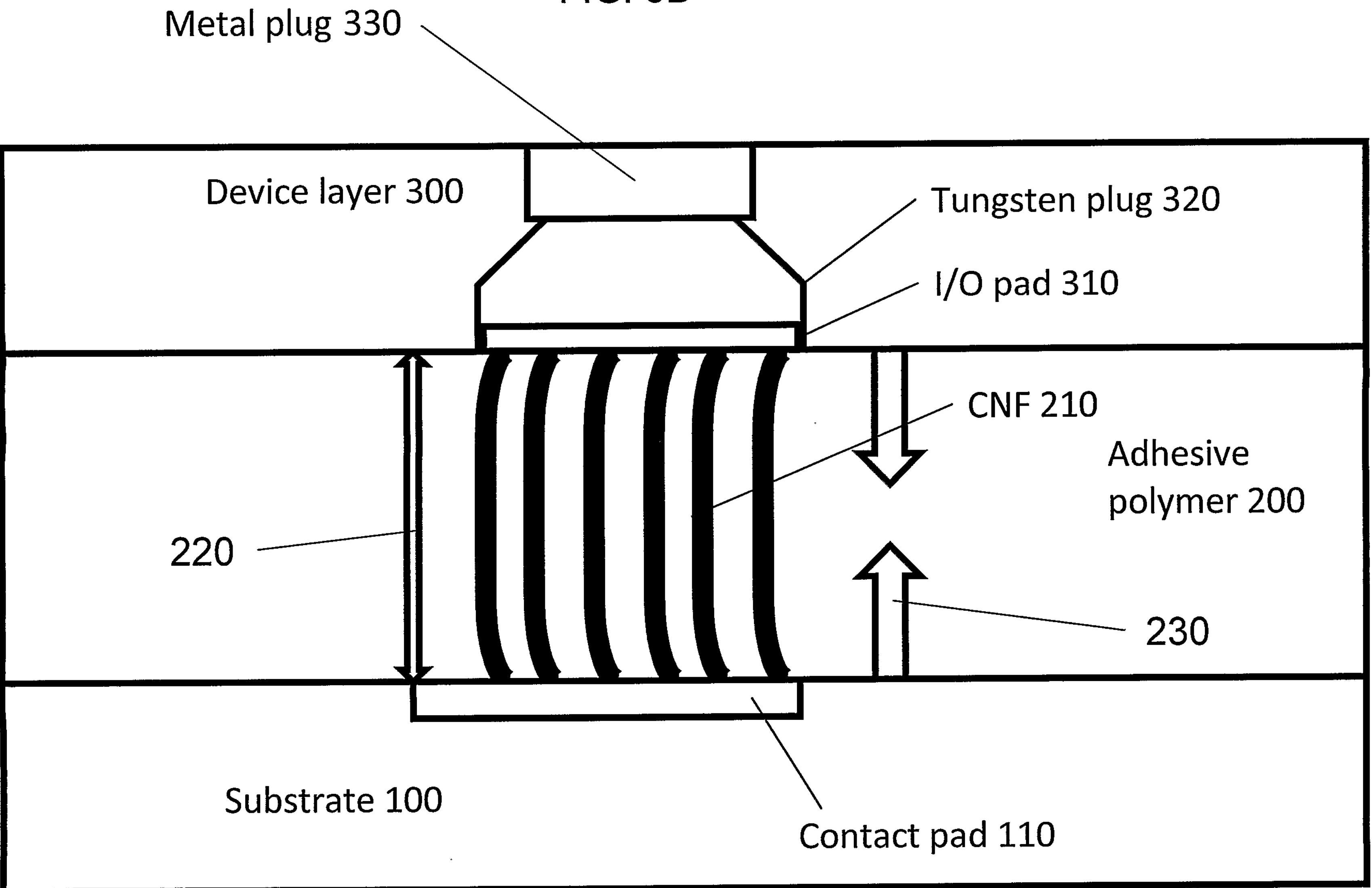


FIG. 4

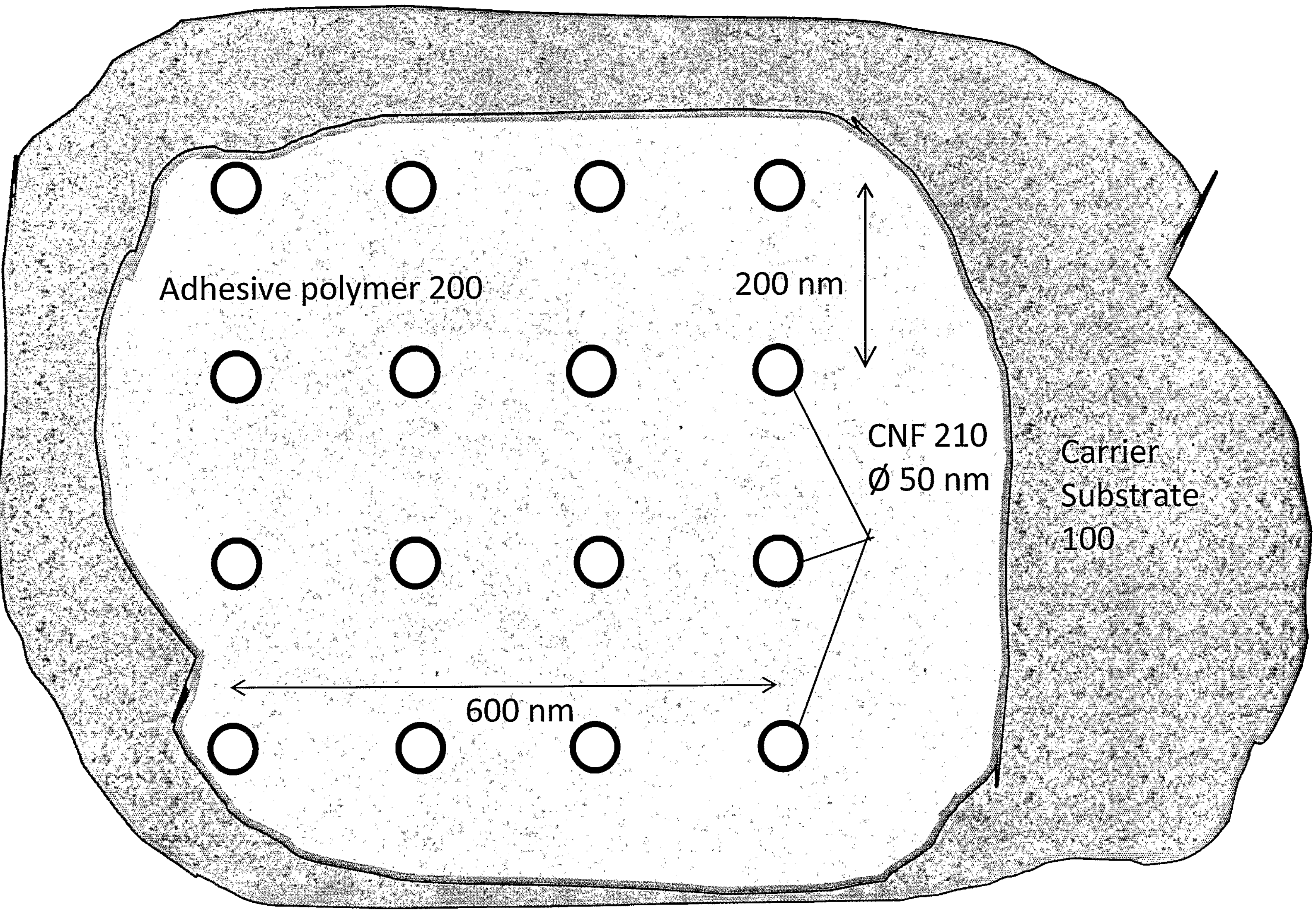
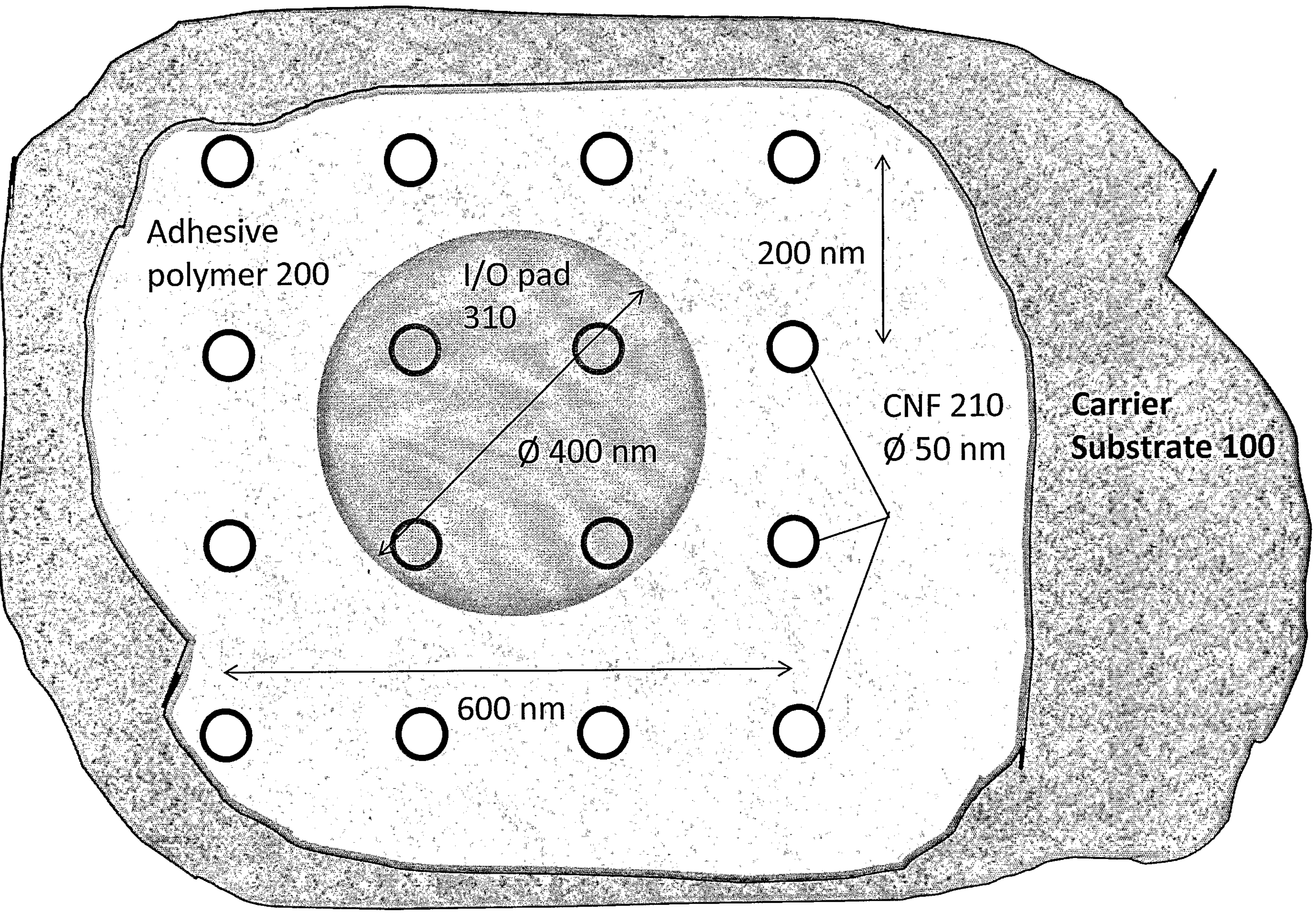


FIG. 5



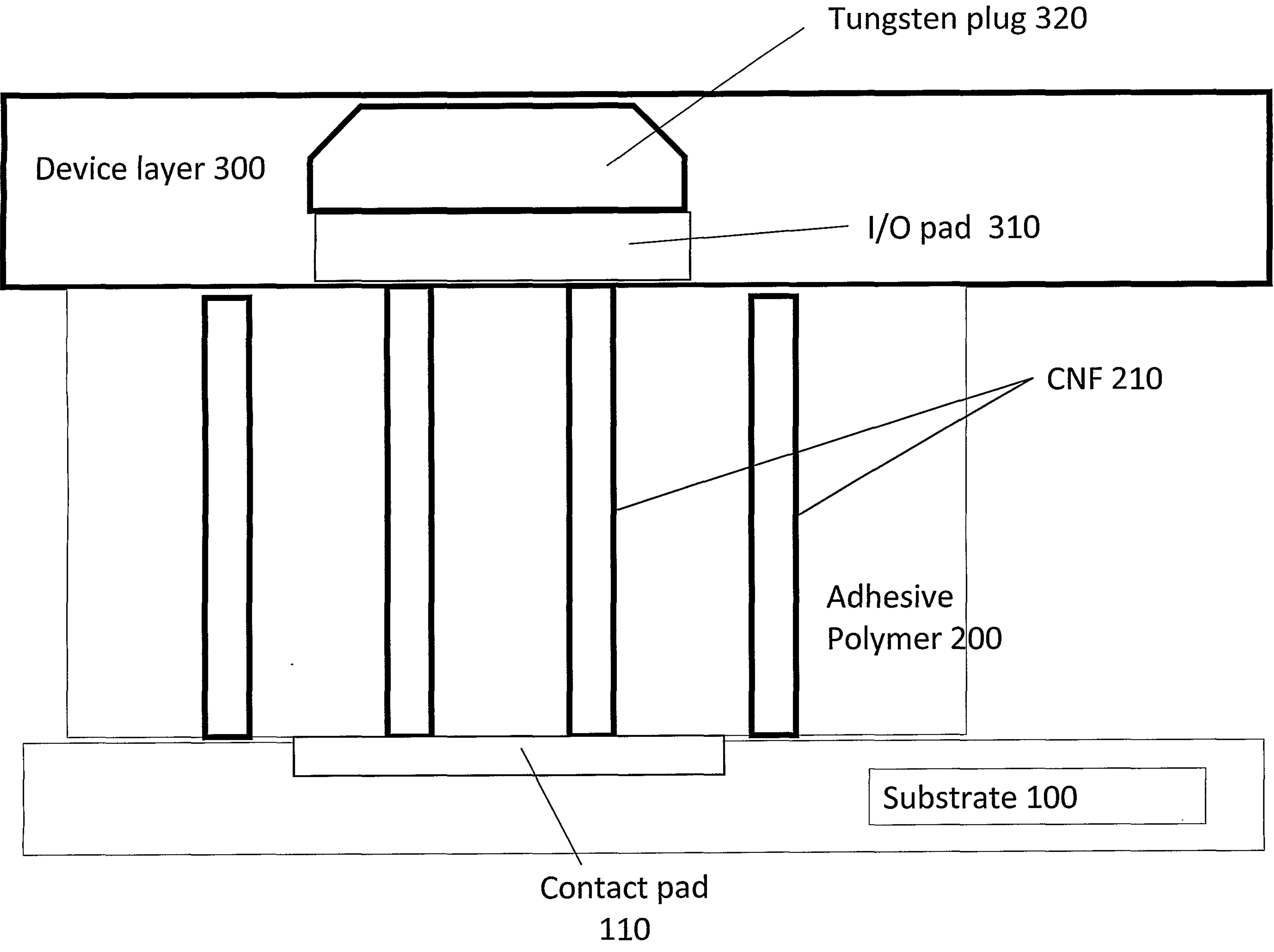


FIG. 6
Tungsten plug 320
Device layer 300
I/O pad 310
CNF 210
Adhesive
Polymer 200
Substrate 100
Contact pad
110

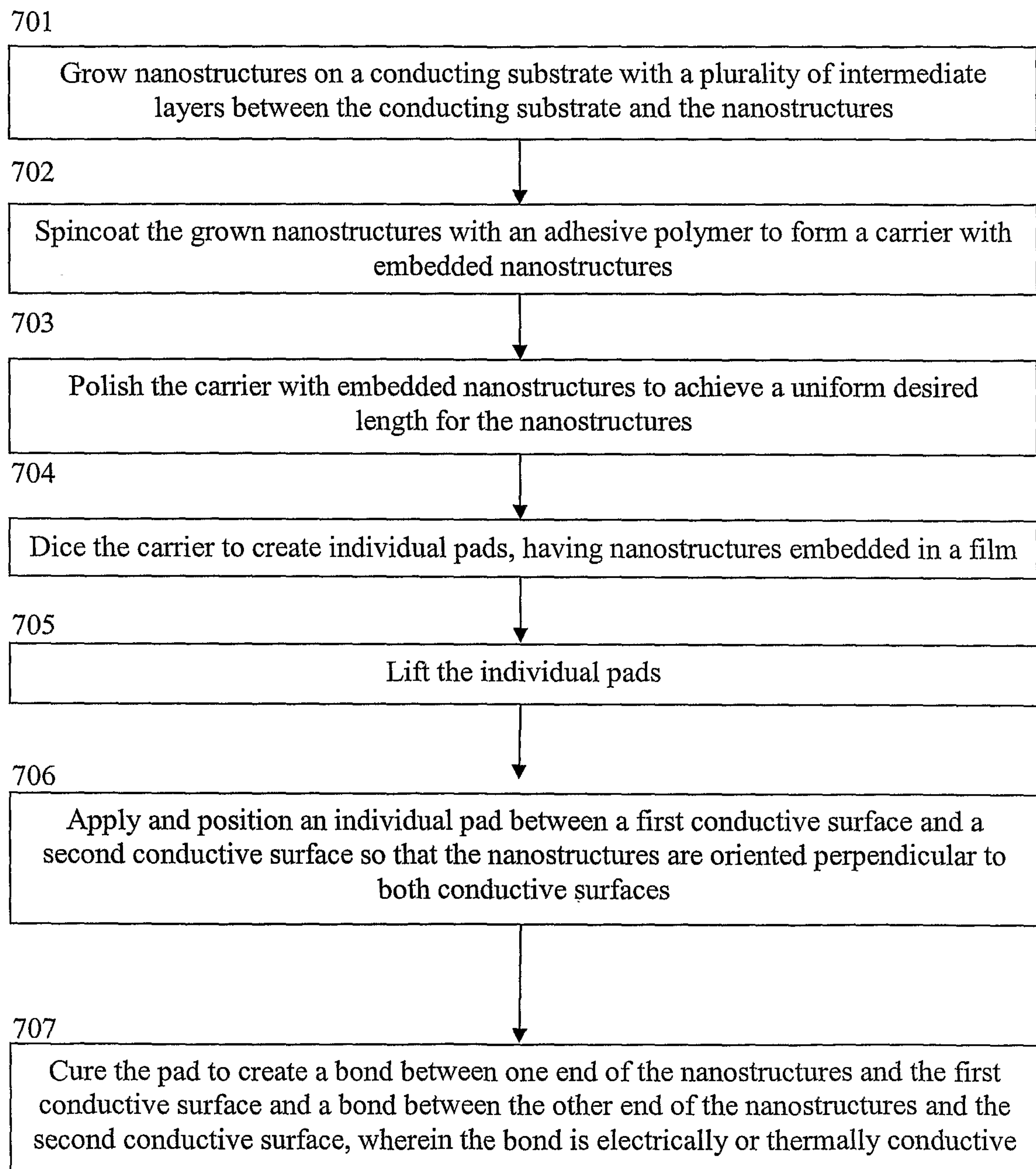


FIG. 7

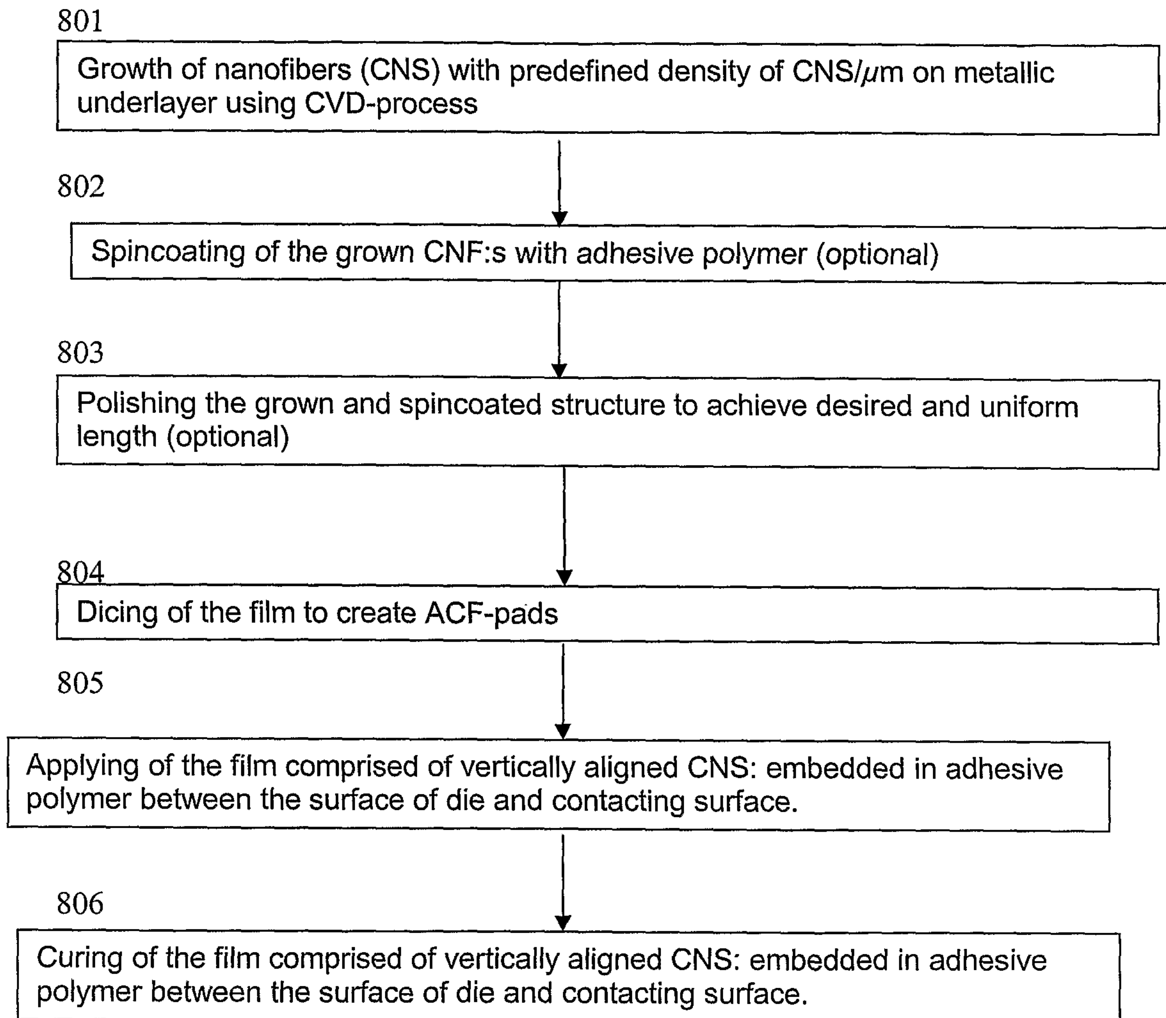


FIG. 8

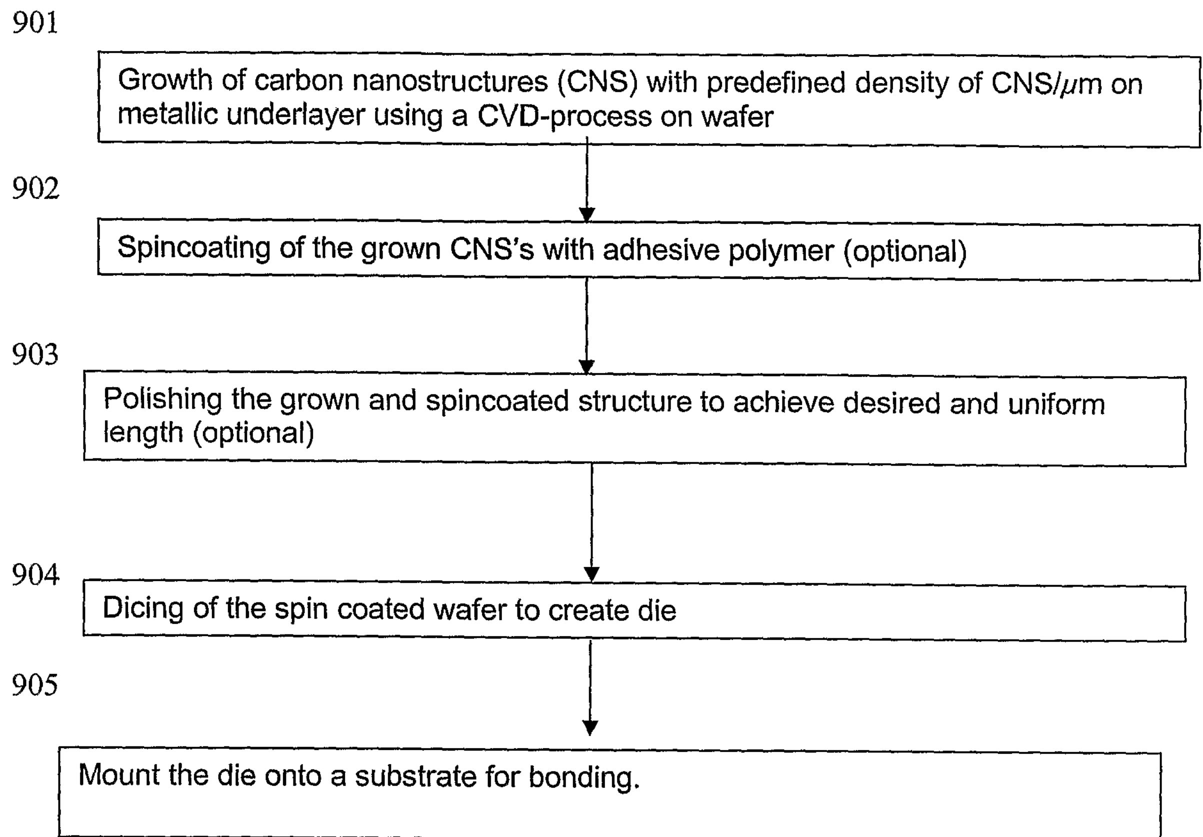


FIG. 9

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE2008/000506

A. CLASSIFICATION OF SUBJECT MATTER

IPC: see extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: H01L, B82B, C23C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-INTERNAL, WPI DATA, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 20040182600 A1 (KAWABATA ET AL), 23 Sept 2004 (23.09.2004), figures 2,4, abstract, paragraphs [0007]-[0008]; [0018]-[0020]; [0044]; [0047] --	1-2,5
A	US 20030117770 A1 (MONTGOMERY ET AL), 26 June 2003 (26.06.2003), figures 2,6, abstract, paragraphs [0014]-[0015]; [0019]-[0021] --	1-9
A	WO 2006115453 A1 (SMOLTEK AB), 2 November 2006 (02.11.2006), figure 3, paragraphs [0027]; [0035]-[0040]; [0203]-[0205] -- --------	1-9

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
28 January 2009	30-01-2009

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C23C 16/22 (2006.01)
H01L 21/285 (2006.01)
H01L 21/768 (2006.01)
H01L 23/52 (2006.01)
H01L 23/538 (2006.01)

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Paper copies can be ordered at a cost of 50 SEK per copy from PRV InterPat (telephone number 08-782 28 85).

Cited literature, if any, will be enclosed in paper form.

Patent document	Kind	Publication date	Family member		Kind	Publication date
US 20040182600	A1	23/09/2004	JP	2004288833	A	14/10/2004
			JP	2004292181	A	21/10/2004
US 20030117770	A1	26/06/2003	CN	1623230	A	01/06/2005
			EP	1329953	A	23/07/2003
			JP	2003249613	A	05/09/2003
			US	6965513	B	15/11/2005
			WO	03054958	A	03/07/2003
WO 2006115453	A1	02/11/2006	CN	101189372	A	28/05/2008
			EP	1874986	A	09/01/2008
			JP	2008538854	T	06/11/2008
			KR	20080009729	A	29/01/2008
			CN	101313092	A	26/11/2008
			EP	1945840	A	23/07/2008
			KR	20080064797	A	09/07/2008
			US	20070096304	A	03/05/2007
			WO	2007024186	A	01/03/2007
			WO	2007119123	A	25/10/2007