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(71) Applicant: NCR CORPORATION [US/US]; World Headquarters, Dayton, OH 45479 (US).

(72) Inventor: SCHUCK, David, Burton ; 1640 Queenston Drive, Escondido, CA 92027 (US).

(74) Agents: DUGAS, Edward et al.; Patent Division, NCR Corporation, World Headquarters, Dayton, OH 45479 (US).

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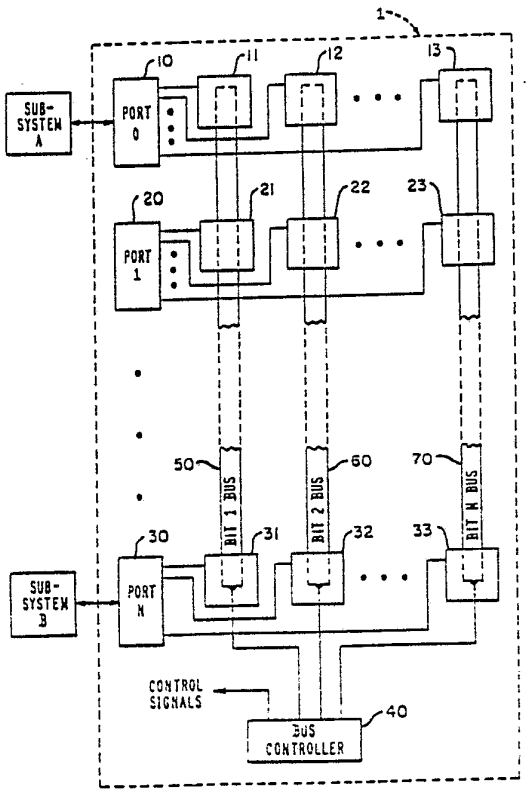
(54) Title: DATA COMMUNICATION BUS STRUCTURE

(57) Abstract

In order to provide fast data transfers and to ensure that the capacitive loading remains fixed, a data communication bus structure for interconnecting a desired number of subsystems of a data processing system comprises an integrated circuit (1) having bus conductors (50, 60, 70) of fixed length and a fixed number of ports (10, 20, 30) for connecting the subsystems. Each port comprises the control and data terminals for a group of driver/receiver circuits (11-13, 21-23, 31-33), each driver/receiver circuit of a group being connected to a respective bus conductor. Each driver/receiver circuit comprises a driver circuit having address and data output latches and driver gates, and a receiver circuit having address and data input latches.



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DATA COMMUNICATION BUS STRUCTURE

Technical Field

This invention relates to a data communication bus structure.

Background Art

Buses of data processing systems generally comprise the path over which information is transferred between the various subsystems of the data processing system, the bus itself generally comprising the conductor or plurality of conductors. Subsystems interface with each other via the bus by an established communication protocol. The subsystems are generally coupled to the bus through an adapter and/or bus driver circuitry. Additionally, the adapter generally contains the logic for interfacing the subsystem such that it is compatible with the established protocol. This arrangement thereby allows additional subsystems to be added easily. As each subsystem is added, the capacitive loading added to the bus by the added adapter/driver circuits tends to have a slowing up effect of the transmission speed of the bus.

U. S. Patent 4,085,448 discloses a data communication bus structure wherein a bus is connected to subsystems of the data processing system. Subsystems may be added, increasing the capacitive loading on the bus.

Disclosure of the Invention

It is an object of the present invention to provide a bus structure between the subsystems of a data processing system which permits fast data transfers and wherein subsystems may be added without increasing the capacitive loading on the bus.

The present invention provides a data communication bus structure comprising at least one bus conductor and a plurality of driver/receiver circuit means

characterized in that said bus structure is formed on an integrated circuit, each of said driver/receiver circuit means has a data terminal adapted to receive and transmit data and further has a first control terminal and a second control terminal for receiving a second control signal and a receive control signal respectively, the plurality of driver/receiver circuit means are grouped in a manner such that there exists a plurality of groups, such that the or each bus conductor has a driver/receiver circuit means within each group operatively connected thereto, the first control terminal of each driver/receiver circuit means within each group being operatively connected one to another forming a first control input terminal, the second control terminal of each driver/receiver circuit means within each group operatively connected one to another forming a second control input terminal and, for each group, said first control input terminal, said second control input terminal, and said data terminal of each driver/receiver circuit means collectively forming a port for coupling a subsystem thereto.

In accordance with the invention, the bus structure is embodied in an integrated circuit and therefore has fixed length bus conductors and a fixed number of ports for selective coupling to the bus structure of a desired number of subsystems. The ports act to isolate the bus structure from the capacitive load of the subsystems coupled to the ports. Thus the speed of operation of the bus structure is unaffected by the number of subsystems that may be connected to the ports and hence fast data transfers are permitted.

Brief Description of the Drawings

A preferred embodiment of the invention will now be described with reference to the accompanying drawings, wherein:

Fig. 1 is a block diagram of the integrated

circuit chip of the bus structure of the present invention;

Fig. 2 is a logic diagram of the driver/receiver circuits attached to the bus for bit 1 for port 0 and port N;

Fig. 3 is a timing diagram of the logic of Fig. 2 showing a transmission sequence between port 0 and port N; and

Fig. 4 shows the word formats utilized in the preferred embodiment of the present invention.

Best Mode for Carrying Out the Invention

The integrated circuit bus structure 1 of the present invention is shown in Fig. 1. The integrated circuit bus structure 1, which resides completely on an integrated circuit chip, comprises a plurality of bus conductors 50, 60, 70, the bus conductors being part of the integrated circuit, and a plurality of driver/receiver circuits, 11, 12, 13, 21, 22, 23, 31, 32, 33. The driver/receiver circuits are grouped (11,12,13), (21,22,23), (31,32,33) such that there exists a plurality of groups, the control terminals for each group forming ports 10, 20, 30. Within a group each driver/receiver circuit therein is connected to a corresponding bus conductor. Therefore, a first driver/receiver circuit 11 is connected to the bit 1 bus conductor 50, a second driver/receiver circuit 12 is connected to the bit 2 bus conductor 60, ..., and a last driver/receiver circuit of the group (the $M^{\underline{th}}$ driver/receiver circuit 13) is connected to the bit M bus conductor 70. Subsystem A is shown connected to port 0 and subsystem B is shown connected to port N.

More specifically, the integrated circuit bus structure 1 shown in Fig. 1 contains N ports and M bus conductors, N and M being whole numbers. In the preferred embodiment of the present invention, the value of N is 5 and the value of M is 9, thereby providing an integrated circuit bus structure of 9-bits

wide and 5 ports. This permits the integrated circuit bus structure 1 to reside on a substrate carrier with 68 pins, 45 being required to support the 9-bit data for each of the 5 ports, the remainder of the pins being utilized for providing the requisite control signals for each port. Bus controller 40, also included on the integrated circuit chip of integrated circuit bus structure 1, provides the general bus control functions and bus control signals, including routing and port enabling logic, logic for resolving conflicts, and priority logic when applicable. Bus controller 40 is coupled to the bus elements 50, 60, 70, for monitoring the data information thereon. The system timing may be provided by a clock generator which is on the same chip but separate from the bus controller 40, included in the logic of the bus controller 40, or by an external clock (i.e., external to the integrated circuit chip of integrated circuit bus structure 1, or as sometimes referred to herein as the integrated circuit chip).

The logic of the driver/receiver circuits will now be explained by describing a sample data transfer between two subsystems in conjunction with Figs. 2 and 3. Fig. 2 shows the logic of two driver/receiver circuits, and Fig. 3 is a timing diagram of the driver/receiver circuits of Fig. 2, including the timing and control signals. Fig. 2 shows port 0 and port N, 10 and 30, respectively, which are associated with driver/receiver circuits, 11, 31, respectively. The driver/receiver 11 and driver/receiver 31 are connected to bus conductor 50, for the word or byte designated as bit 1. It will be understood by those skilled in the art that the transfer of bit 1 information between port 0 and port N, which will now be described, is applicable for all the bits, bit 1 through bit M, of ports 0 and N, the bit transfers occurring in parallel. Furthermore, it will also be understood by those skilled in the art that the driver/receiver circuits forming the port 0 group

utilize the same control signals for that port; however, each driver/receiver circuit within the group has its own data line. The ports are shown in Fig. 2 as blocks 10, 30 which receive the RECEIVE and SEND signals from the attached subsystems, and which further receive the respective control signals OUTPUT READY and INPUT READY from bus controller 40. Thus each port comprises a set of data terminals 100, 300, one data terminal for each driver/receiver circuit of the group of driver/receiver circuits served by the port, and a first control input terminal 150 for receiving a send control signal SEND and a second control input terminal 151 for receiving a receive control signal RECEIVE. The first control input terminal is connected to first control terminals, one for each driver/receiver circuit, and the second control input terminal is connected to second control terminals, one for each driver/receiver circuit. System timing signals are transmitted to the driver/receiver circuits and the subsystems in order to coordinate the transfer of information between subsystems.

The bus system of the present invention employs a two-phase gate and two-phase clock timing signals as shown in Fig. 3, waveforms A-D. Gate A (GA) and gate D (GD) are two non-overlapping gates which gate data onto the bus. Clock A (CKA) and clock D (CKD) clock data into the corresponding address and data latches. The GA and GD signal waveforms are shown by waveforms A and C, respectively, in Fig. 3. The CKA and CKD signal waveforms are shown by waveforms B and D, respectively in Fig. 3.

When subsystem A (not shown in Fig. 2) coupled to port 0 wishes to communicate with subsystem B (not shown in Fig. 2) attached to port N, the subsystem A detects OUTPUT 0 READY is high (waveform E of Fig. 3) prior in time to time t_o, signifying subsystem A may output. The OUTPUT O READY signal is a control signal from the bus controller 40. Subsystem A then outputs a SENDO send control signal (waveform F of Fig. 3) to a

first control terminal 150 coincident with the start of the bus cycle as defined by the GA (gate A) signal (waveform A of Fig. 3), the start being denoted in Fig. 3 as time t_o. The SENDO signal will be high for one bus cycle (cycle 1). During phase A of cycle 1, subsystem A outputs the address information DATA0 on data terminal 100 in accordance with a predefined word format which will be described hereinunder. During phase B of cycle 1, subsystem A outputs the data information on DATAO terminal, the DATAO output during cycle 1 depicted by waveform G of Fig. 3. Bus controller 40, being on line with the buses, captures the destination address from the address word for subsequent control signal generation.

Output address (OA) latch 101, and output data (OD) latch 102 together with output AND gates 103, 104 form the output buffer of the driver/receiver circuit 11. The SENDO signal being high during cycle 1 partially enables AND gate 103 and 104. When CKA goes high during phase A of cycle 1, AND gate 103 is totally enabled, thereby clocking into OA latch 101, bit 1 of the address information initially on DATAO line 100 during phase A of cycle 1. During phase B of cycle 1 when CKD is high, AND gate 104 is totally enabled thereby clocking into OD latch 102 the data information on DATAO line 100 during phase B of cycle 1.

Bus controller 40 monitors the output buffers to ascertain the transmitting ports and to determine the destination. During cycle 1, bus controller 40 having decoded the control portion of address word, and determined the destination to be port N, sets up to generate a select data control signal SDN high during cycle 2 and the SSO control signal high during cycle 2 (waveforms I and H respectively of Fig. 3). During phase A of cycle 2, GA is high and a send select control signal from controller 40 (SSO) is high, thereby totally enabling output address gate (OAG) 105 which comprises an AND driver gate. The output of gate 105 is connected

to bus conductor 50 so that the address information stored in OA latch 101 is gated onto bus 50 during this time. Still during cycle 2, SDN is high and when CKA goes high, input AND gate 310 of driver/receiver circuit 31 is enabled, thereby clocking the address information into input address latch (IA) 312. Similarly during phase B of bus cycle 2, when GD goes high, output data gate (ODG) 106, which comprises an AND driver gate is enabled gating the data information onto bus 50. Also, during the second phase of cycle 2, CKD goes high enabling input AND gate 311, thereby clocking the data information from bus 50 into input data latch (ID) 313. The address and data information on the bit 1 bus 50 is depicted by waveform J of Fig. 3. The latches 1A 312 and ID 313 together with input AND gates 310, 311 form the input buffer of driver/receiver circuit 31. Gates OAG 105 and ODG 106 are the bus drivers.

During cycle 2, bus controller 40 generates the INPUT N READY control signal for subsystem B, shown as waveform K of Fig. 3. Subsystem B in this manner knows that on the next bus cycle, it can receive data (i.e. the input buffer is full).

During cycle 3 subsystem B generates a receive control signal RECEIVEN signal as shown in waveform L of Fig. 3 which is received by a second control terminal 151. The RECEIVEN signal partially enables input address gate (IAG) 314 and input data gate (IDG) 315. During phase A of cycle 3, GA is high totally enabling IAG 314, thereby permitting the address information contained in IA 312 to be inputted over DATAN lines 300 of port N 30. Likewise, during phase B of cycle 3, GD is high totally enabling IDG 315 permitting the data information stored in ID 313 to be inputted to subsystem B via DATAN line, 300 as shown by waveform M of Fig. 3.

The word format utilized in the preferred embodiment of the invention is shown in Fig. 4. The address word, shown in Fig. 4A, contains 22-bit address

information and 10-bits of control information. SW indicates a single word transfer, i.e., no data word is transmitted. This allows the receiving subsystem to ignore the data word. OP signifies an operation code, S signifies a source address, and D signifies a destination address. The data word, shown in Fig. 4B, is 32 bits long and is made up by utilizing four integrated circuit chips in parallel as described hereinunder.

It is to be understood that the output address (OA) and output data (OD) latches 101, 102 together with output AND gates 103, 104 form the output buffers for the respective driver/receiver circuit. Likewise, the OAG and ODG gates form the output driver gates, the output driver gates and the output latches constituting the driver circuit part of the driver/receiver circuit. The input latches 312, 313 and input AND gates 310, 311 form the input buffers and together with input gates 314, 315 constitute the receiver circuit part of the driver/receiver circuit 31.

It will be recognized by those skilled in the art that since the bus permits a transfer every cycle, there may be a bus transfer between any two other non-busy subsystems during cycle 1 and cycle 3. Also, the loading of the output buffers from each port may occur simultaneously. The bus controller 40 can then determine on a priority basis, rotational basis, etc. which data is to be transferred on the bus 50 first. As a result of that determination, the bus controller generates the respective SS(X) and SD(Y) control signals, X being the transmitting port and Y being the receiving port. The logic required to perform the priority or the rotational determination, and the logic required for the generation of the control signals by the bus controller 40 is well-known within the art and is not discussed further herein. Further, it is to be understood that once the data is transferred on the bus into the respective input buffer, the receiving subsystem can accept

the data at any time, not necessarily in the next bus cycle. The bus controller 40 determines which input buffers and output buffers contain data in order to set OUTPUT READY high (signifying to the subsystem that the output buffer is empty), and in order to set INPUT READY high (signifying to the subsystem that the input buffer contains information therein).

It can also be recognized by those skilled in the art that the information transfer may consist of more than two parts, i.e. address information and data information. For information transfer which contains a plurality of component parts, the system timing will include a phased clock having a number of phases corresponding to the plurality of component parts.

As mentioned above, OAG and ODG are the bus drivers. It can be seen that the capacitive loading of the bus remains fixed. The addition of subsystems to the bus is achieved by adding subsystem to an available port. It can further be seen that the bus can be expanded to 32-bits (i.e., 32 data bits and 1 or 4 parity bits) by combining four integrated circuit chips having the configuration of the preferred embodiment as described above, utilizing the bus controller 40 from a single chip. The driver/receiver circuits would be grouped to form five ports, each port having 32 data lines. The control signals of a port would be tied in parallel to all the driver/receiver circuits of the group constituting a port.

A bus conductor 50,60,70, for a single bit always resides on a single integrated circuit (IC). It is understood that, in order to increase the number of ports, the number of buses (i.e., the value of M) is decreased for the same number of pins of the carrier. Design changes of N and M can be made with a carrier of increased pin capacity within the scope of the invention.

It can be seen that the capacitive loading of the bus is fixed and the bus length is very short, in

the order of a hundred thousandths of an inch, resulting in a bus having high speed transmission rates.

While there has been shown what is considered to be the preferred embodiment of the invention, it will be manifest that many changes and modifications can be made therein without departing from the essential spirit and scope of the invention. It is intended, therefore, in the annexed claims, to cover all such changes and modifications which fall within the true scope of the invention.

CLAIMS:

1. A data communication bus structure comprising at least one bus conductor (50, 60, 70) and a plurality of driver/receiver circuit means (11-13, 21-23, 31-33), characterized in that said bus structure is formed on an integrated circuit, each of said driver/receiver circuit means has a data terminal (100, 300) adapted to receive and transmit data (DATAN) and further has a first control terminal (150) and a second control terminal (151) for receiving a send control signal (SEND N) and a receive control signal (RECEIVE N), respectively, the plurality of driver/receiver circuit means are grouped in a manner such that there exists a plurality of groups, such that the or each bus conductor has a driver/receiver circuit means (11-13, 21-23, 31-33) within each group operatively connected thereto, the first control terminal of each driver/receiver circuit means within each group being operatively connected one to another forming a first control input terminal (150), the second control terminal of each driver/receiver circuit means within each group operatively connected one to another forming a second control input terminal (151) and, for each group, said first control input terminal, said second control input terminal, and said data terminal of each driver/receiver circuit means collectively forming a port (10, 20, 30) for coupling a subsystem thereto.

2. A bus structure according to claim 1, characterized in that each said driver/receiver circuit means comprises a driver circuit (101-106) operatively connected to the associated bus conductor (50), which is operatively connected to said data terminal to receive data (DATAN) and operatively connected to said first control input terminal to receive said send control signal (SEND N) and a receiver circuit (310-315)

2. (concluded)
operatively connected to the associated bus conductor which is operatively connected to said second control input terminal to receive said receive control signal (RECEIVE N) and operatively connected to said data terminal to provide data (DATAN) thereto.

3. A bus structure according to claim 2, characterized in that said driver circuit (101-106) includes output buffer means (101-104) which is operatively connected to said data terminal to receive said data signal (DATAN) and to said first control input terminal to receive said control signal, and output gate means (105, 106) having an output operatively connected to the bus conductor and further operatively connected to receive the contents of said output buffer means (101-104).

4. A bus structure according to claim 3, characterized in that said output buffer means (101-104) includes at least one output latch circuit (101, 102), the or each latch output latch circuit (101, 102) having a data input (D), a clock input (K), and a data output (Q), the data input of the or each output latch circuit (101, 102) being operatively connected to said data terminal and at least one output AND gate (103, 104), the or each output AND gate having a first input, a second input, and an output, the first input of each output AND gate (103, 104) being operatively connected to said first control input terminal the second input of the or each of said output AND gate being operatively connected to receive an individual phased clocking signal (CKA, CKD) and the output of the or each output AND gate being operatively connected to the clock input of a corresponding output latch circuit.

5. A bus structure according to claim 4, characterized in that said output gate means includes

5. (concluded)
at least one AND driver gate (105, 106) the or each AND driver gate having a first, second and third input and an output, said output being operatively connected to the bus conductor, said first input being operatively connected to a corresponding data output of a said output latch circuit, said second input being operatively connected to an individual phased gating signal (GA,GD) and said third input being operatively connected to receive a send select control signal (SSN).

6. A bus structure according to claim 2, characterized in that said receiver circuit (310-315) includes input buffer means (310-313) operatively connected to the bus conductor and input gate means (314, 315) operatively connected between said data terminal and said input buffer means.

7. A bus structure according to claim 6, characterized in that said input buffer means includes at least one input latch circuit (312, 313), the or each input latch circuit having a data input (D), a clock input (CK) and a data output (Q), the data input of the or each input latch circuit being operatively connected to the bus conductor and at least one input AND gate (310, 311) the or each input AND gate (310, 311) having a first input, a second input, and an output, said first input being operatively connected to receive a select data control signal (SDN), said second input being operatively connected to receive an individual phased clocking signal (CKA, CKD) and said output being connected to a said clock input of a corresponding said input latch circuit.

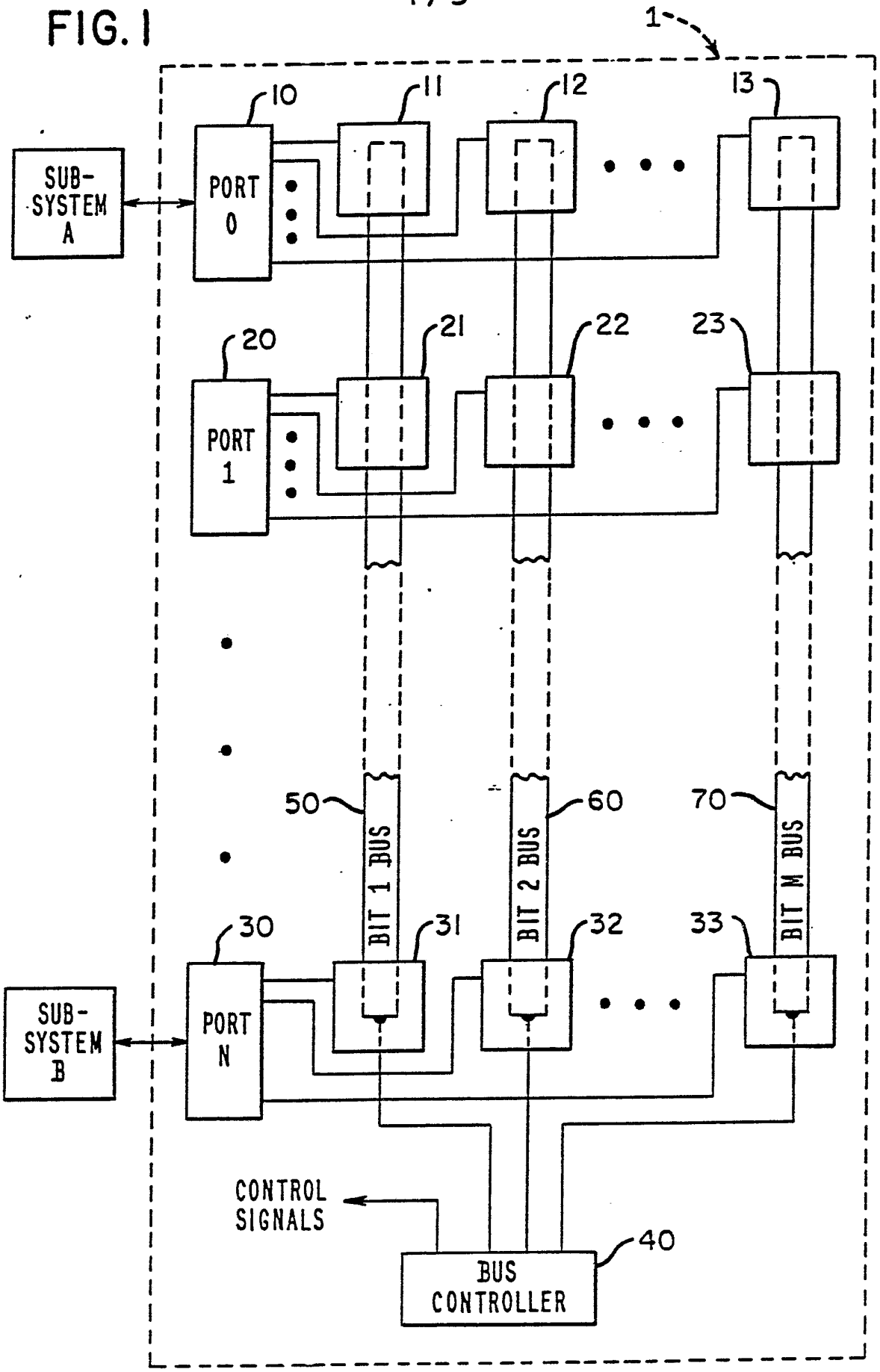
8. A bus structure according to claim 7, characterized in that said input gate means (314, 315) includes at least one input AND driver gate (314, 315) the or each input AND driver gate having a first, second,

8. (concluded)
and third input, and an output, said output being operatively connected to said data terminal, said first input being operatively connected to a corresponding said data output of a said input latch circuit, said second input being operatively connected to receive an individual phased gating signal, (GA,GD) and said third input being operatively connected to said second control input terminal.

9. A bus structure according to claim 1, characterized by bus controller means for controlling the information transfer on the or each bus conductor (50, 60, 70).

10. A bus structure according to any preceding claim characterized by clock means (40) for generating bus turning signals.

FIG. 1



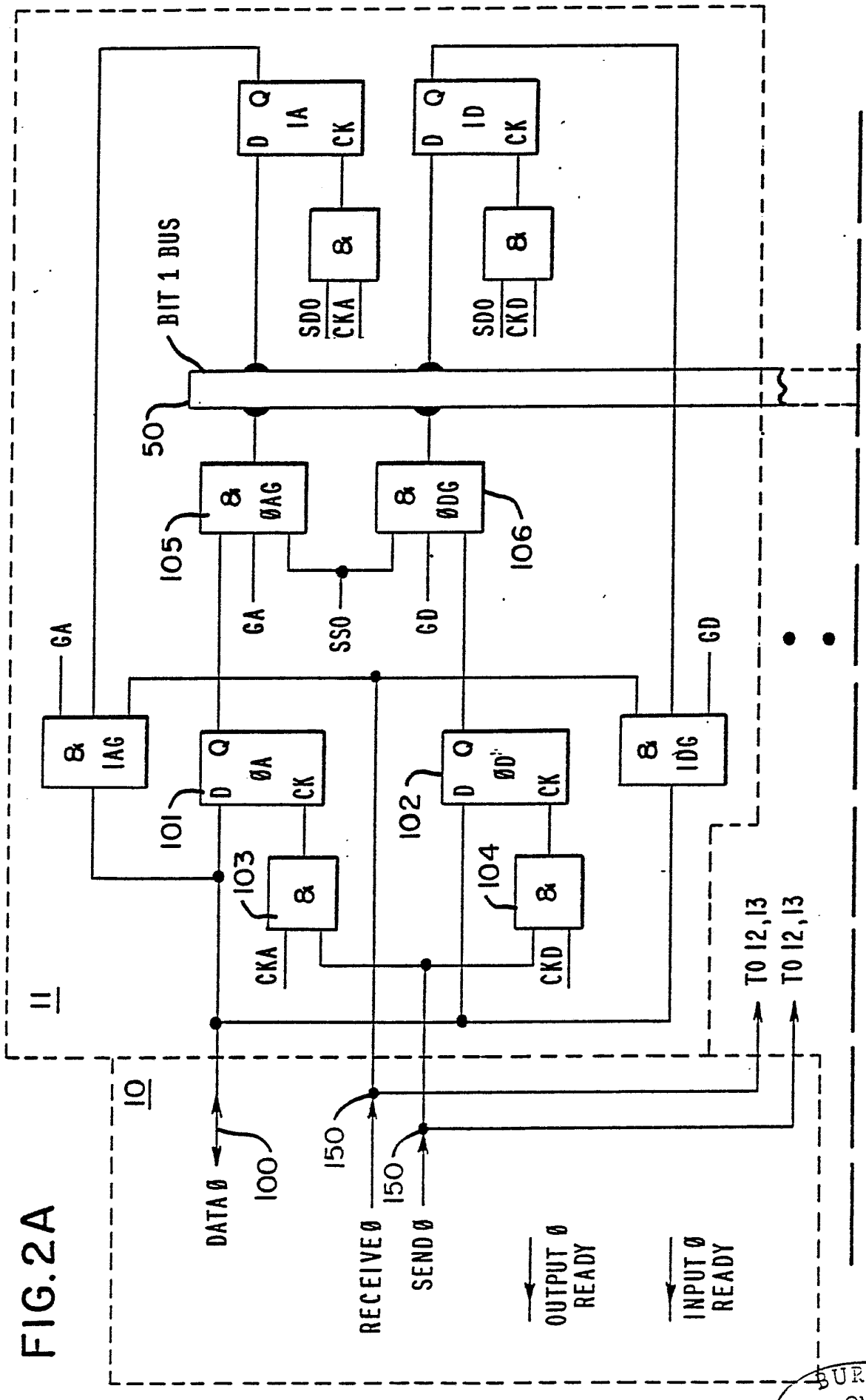


FIG. 2A

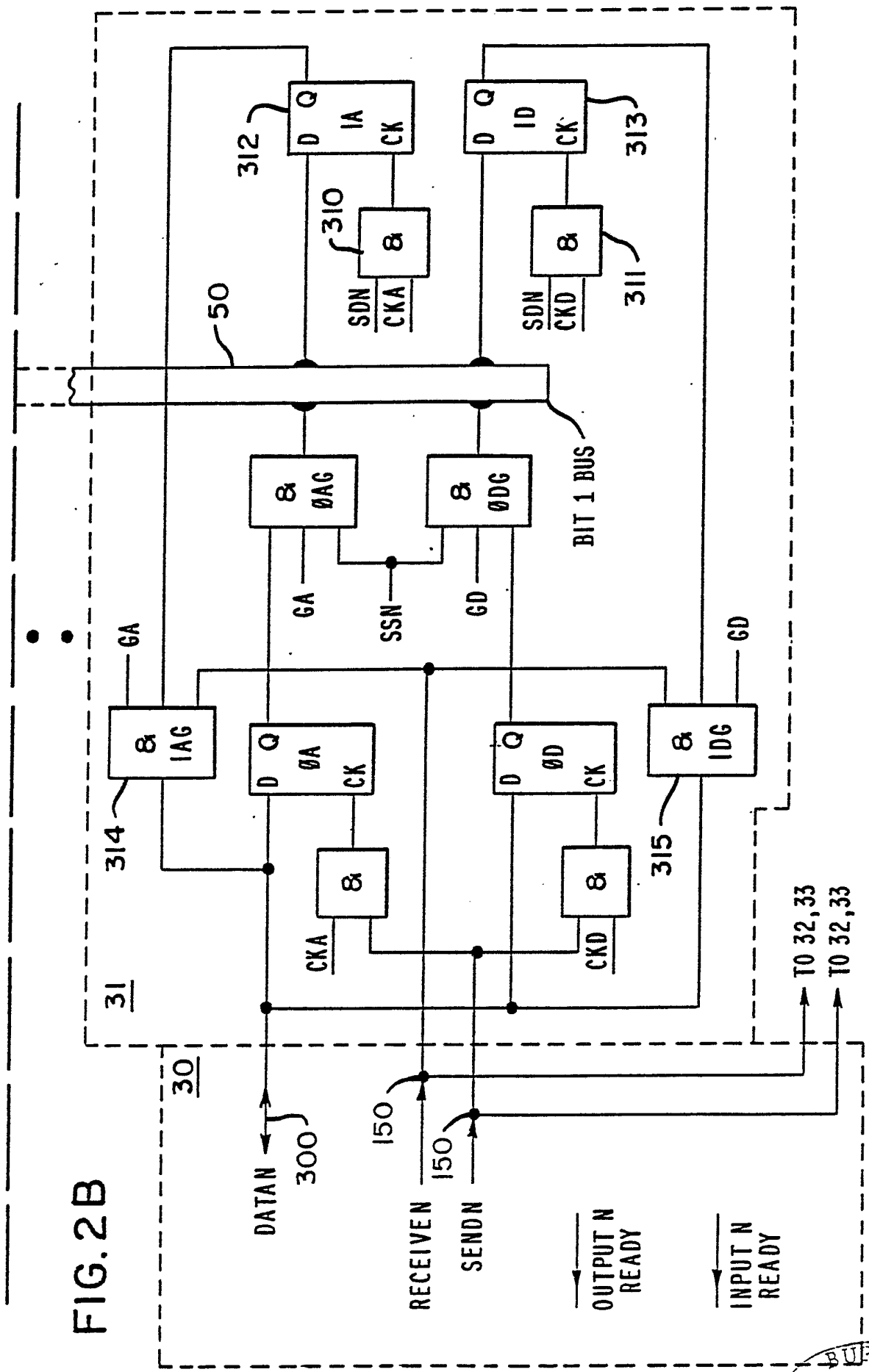


FIG. 2B

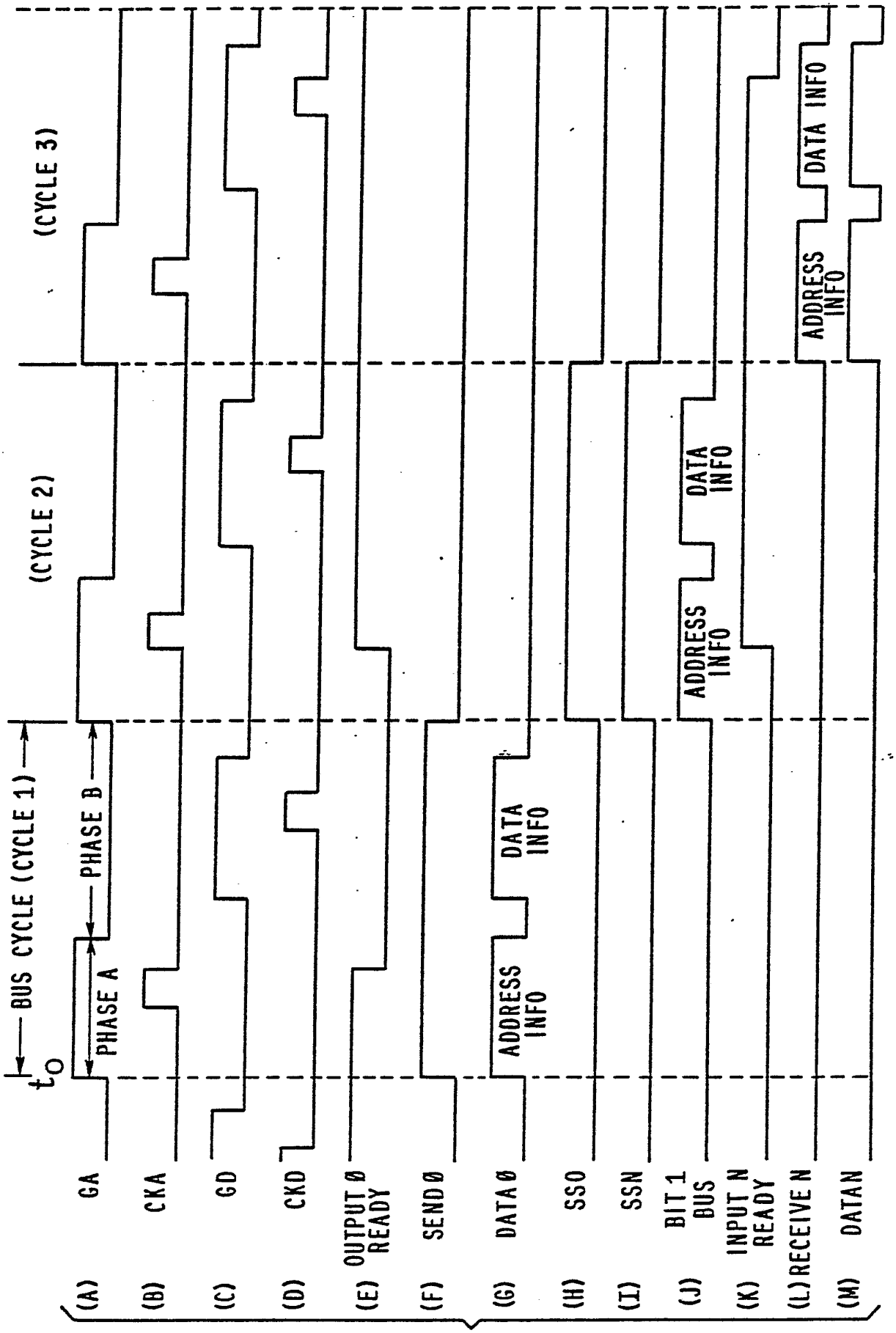


FIG.3

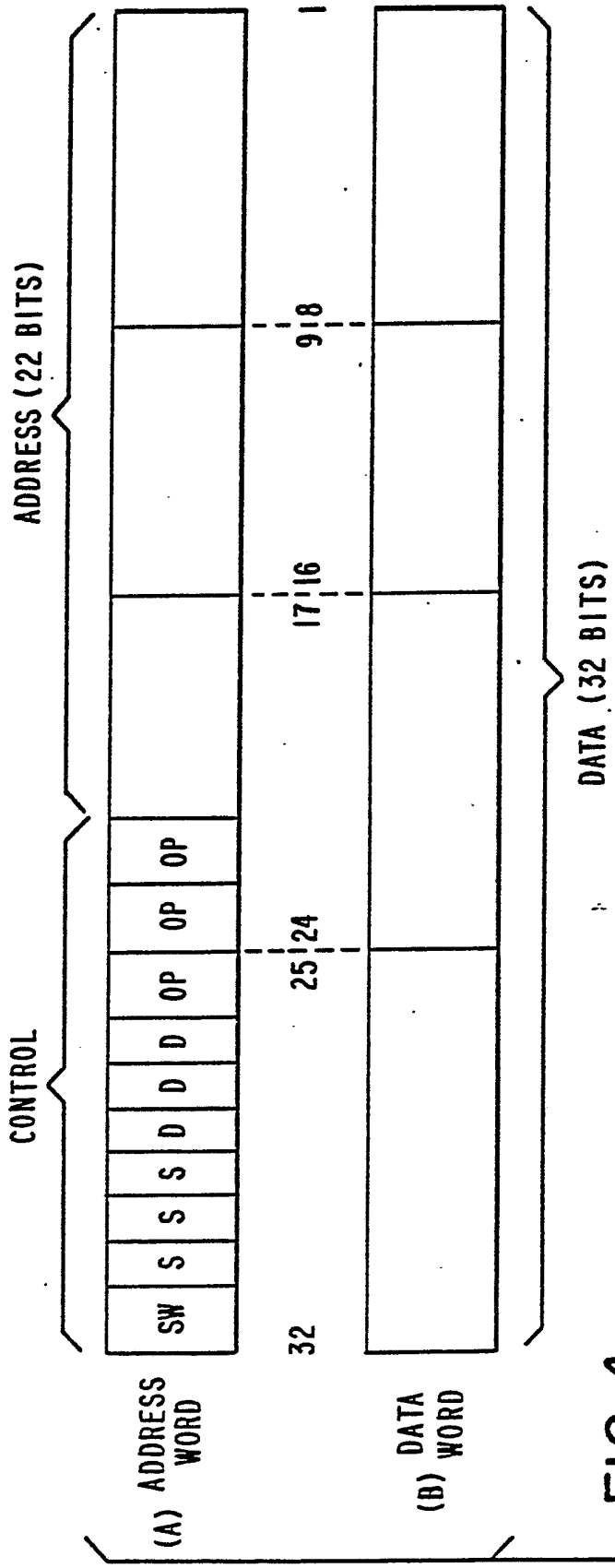


FIG. 4

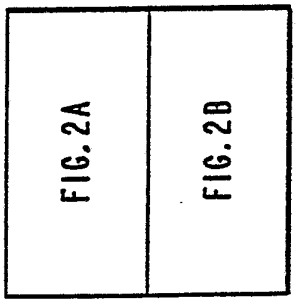


FIG. 5

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 81/01396

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

INT. CL.[3] G 06F 13/00
U.S. CL. 364/900

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
U.S.	364/200,900; 370/24,32,85; 340/147R,147LP

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
X	U.S.,A, 4,085,448, Published 18 APR. 1978 P.KOGGE (see Fig's 7,8,10)	1-10
X	U.S.,A, 4,213,177, Published 15 JULY 1980 R. SCHMIDT	1-10
X	U.S.,A, 4,050,097, Published 20 SEPT. 1977 M.MIU (see Fig. 16)	1-10
A	U.S.,A, 3,737,861, Published 5 JUNE 1973 W.O'NEILL	1-10
A	U.S.,A, 4,034,346, Published 5 JULY 1977 C.HOSTEIN	1-10

* Special categories of cited documents: [15]

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"L" document cited for special reason other than those referred to in the other categories

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"T" later document published on or after the international filing date or priority date and not in conflict with the application, but cited to understand the principle or theory underlying the invention

"X" document of particular relevance

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
29 DEC. 1981	12 JAN 1982
International Searching Authority [1]	**Signature of Authorized Officer [20]**
ISA/US	DAVID Y. ENG

Form PCT/ISA/210 (second sheet) (October 1977)

FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

A	U.S.,A, 4,067,059 Published 3 JAN. 1978 N. DERCHAK	1-10

V. ☐ OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE [10]

This international search report has not been established in respect of certain claims under Article 17(2) (a) for the following reasons:

1. ☐ Claim numbers _____, because they relate to subject matter [12] not required to be searched by this Authority, namely:

2. ☐ Claim numbers _____, because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out [13], specifically:

VI. ☐ OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING [11]

This International Searching Authority found multiple inventions in this international application as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application.

2. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:

3. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:

Remark on Protest

☐ The additional search fees were accompanied by applicant's protest.

☐ No protest accompanied the payment of additional search fees.