(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
5 November 2015 (05.11.2015)

WIPO | PCT

(10) International Publication Number
WO 2015/167351 A1

(51) International Patent Classification:
H01L 45/00 (2006.01)

(21) International Application Number:
PCT/RU2014/000316

(22) International Filing Date:
30 April 2014 (30.04.2014)

(25) Filing Language: English

(26) Publication Language: English

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

(54) Title: MEMRISTOR AND METHOD OF PRODUCTION THEREOF

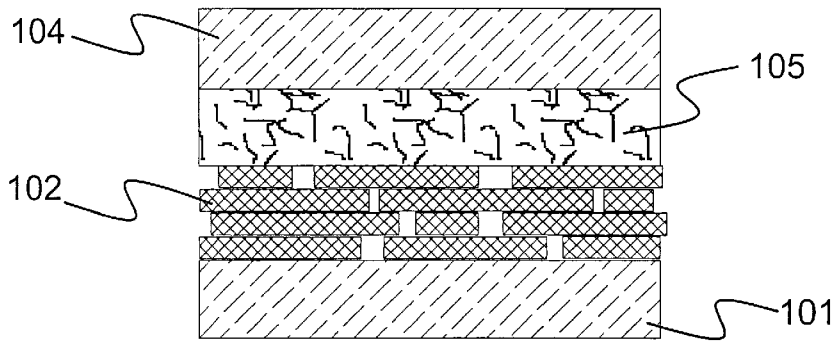

Figure 1b

(57) Abstract: A device is disclosed which comprises a first electrode (101) and a second electrode (104) spaced from the first electrode, a switching region (102) positioned between the first electrode and the second electrode, and an intermediate region (103) positioned between the switching region and the second electrode, wherein the intermediate region is in electrical contact with the switching region and the second electrode. Preferably, the device is a memristor, the intermediate region comprising metal nanowires (105) embedded in an insulating polymer matrix to provide sporadic physical and electrical contacts to the switching material.

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MEMRISTOR AND METHOD OF PRODUCTION THEREOF

TECHNICAL FIELD

[0001] The present application relates to microelectronics. In particular, the present application relates to variable resistance devices and methods of production thereof.

BACKGROUND

[0002] Neuromorphic electronics that mimic the working principles of neuron and synapse behavior may change the computing paradigm, providing cognitive data processing capabilities. Artificial neuromorphic systems are highly productive due to parallel computing and thus tolerant to defects in circuits, consume low energy due to short spike-like electric pulses, and have reduced circuit complexity due to two terminal structures. Analog adaptive electronics may outperform currently used digital computing platforms in tasks such as image recognition, classification, cognitive computation and sensor data processing.

[0003] The memristor, a basic component of neuromorphic systems, is an electrical resistance switch with the capability to retain a state of resistance based on the history of applied voltage and flowing current. Memristor devices can store and process information in contrast to conventional integrated circuit technology where switching transistors and memory are separated. There are several classes of memristors, for example two-terminal vertical-stack, two-terminal planar, or three-terminal resistance switches. Based on the switching mechanism the materials can be grouped into two main categories – chemical and physical switches. The first class includes ionic switching materials where anions or cations are considered to be the mobile species utilizing the principles of redox reactions and nanoionics. Anion motion induced by an electric field leads to valence changes of the metal causing the resistance change of the material (such as metal oxides, metal nitrides, metal iodides and metal chalcogenides), while cation-based devices are driven by electrochemically active metals such as copper or silver with the capability of forming an atomic bridge between

electrodes. A second category of memristors based only on physical changes include devices relying on magnetic, ferroelectric, electron/hole trapping and phase-change processes. However, both chemical and physical switching mechanisms can also be realized in a single device.

SUMMARY

[0004] In this section, the main embodiments of the present invention as defined in the claims are described and certain definitions are given.

[0005] According to a first aspect of the present invention, a device is disclosed. The device comprises: a first electrode; a second electrode spaced from the first electrode; a switching region positioned between the first electrode and the second electrode, the switching region comprising one or more materials; and an intermediate region positioned between the switching region and the second electrode, wherein the intermediate region is in electrical contact with the switching region and the second electrode.

[0006] The device according to the embodiment may be a variable resistance device, for example a memristive device. A memristive device is a device that has a current-voltage (I-V) pinched-hysteresis loop that has a frequency dependent size. The first and second electrodes may comprise any conductive material. The intermediate region is positioned between the switching layer and the second electrode. As it is clear to a skilled person, the electrodes are numbered as "first" and "second" electrodes for clarity purposes only. They may be interchangeable, have similar or different conductive properties and comprise the same or different materials. In the production of this device the electrodes may be deposited in any order.

[0007] The intermediate region may be advantageous in providing electrical contact with the switching region and the second electrode, while at the same time preventing unwanted electrical contact between the first and the second electrodes.

[0008] According to an embodiment, the device is a memristor.

[0009] According to an embodiment, the switching region is in electrical contact with the first electrode via physical contact with the first electrode, and in electrical contact with the second electrode via physical contact with the intermediate region.

[0010] The physical contact can also mean a physical proximity sufficient for establishment of an electrical contact.

[0011] According to an embodiment, the switching region comprises one or more materials selected from the group of: transition metal dichalcogenides (TMD), partially oxidized TMD, fully oxidized transition metal oxides (TMO) and graphene-like materials.

[0012] The TMD materials may be selected from the group of materials with the following chemical formulas: WX_2, MoX_2, ScX_2, TiX_2, HfX_2, ZrX_2, VX_2, CrX_2, MnX_2, FeX_2, CoX_2, NiX_2, NbX_2, TcX_2, ReX_2, PdX_2 and PtX_2 wherein "X" may be S, Se or Te. The TMO materials may be selected from the group of materials with the following chemical formulas: WO_n, MoO_n, ScO_n, TiO_n, HfO_n, ZrO_n, VO_n, CrO_n, MnO_n, FeO_n, CoO_n, NiO_n, NbO_n, wherein "n" has a value of 2 or 3. The graphene-like materials may be selected from the group including graphene oxide and materials with the following chemical formulas: hexagonal BN, AlN, GaN, InN, InP, InAs, BP, BAs, GaP. All of the above materials may be provided into the switching region as combinations of few-layer flakes or other few-layer structures. As a result, the switching region may comprise one or more few-layer materials selected from the groups listed above. For the purposes of this specification, the term "few-layer" refers to a layered structure with 1-10 layers of atoms. The material may be an insulator, a *p*-type or an *n*-type semiconductor.

[0013] It is clear to a skilled person that the switching region can comprise these materials in any combination, e.g. in homogenous composites or as separate hybrid layers. In an exemplary embodiment, the switching regions comprise materials in a stack.

[0014] According to an embodiment, the switching region has a thickness between 10 and 1000 nanometers.

[0015] According to an embodiment, the intermediate region comprises: metal nanowires (NW), polymers or a combination thereof. Metal nanowires may have a solids content in the range of 1–50 weight percent.

[0016] The materials according to this embodiment may be used in any combination or individually. For example, the intermediate region may comprise a conducting polymer selected from the group of: polyanilines (PANI), poly(pyrrole)s (PPY), poly(thiophene)s (PT), poly(3,4-ethylenedioxythiophene) (PEDOT), poly(p-

phenylene sulfide) (PPS), poly(acetylene)s (PAC), poly(p-phenylene vinylene) (PPV). Alternatively, but not limited to, the intermediate region may comprise metal nanowires embedded in an insulating polymer matrix. The insulating polymer may be acrylic, polyurethane, polysiloxane, epoxy resins, or other suitable organic media.

[0017] According to an embodiment, the intermediate region is in electrical contact with the second electrode and with the switching region via one or more electrical contact points.

[0018] In an embodiment, these contact points may be sporadic. For example, if metal nanowires are used in the intermediate region, they can provide sporadic contact points throughout interfaces of the intermediate region. Such sporadic electrical contacts can support nanoscale ionic motion channels. The resistance switching may thereby be localized to a small area of the interface.

[0019] The intermediate region may serve as a physical barrier providing sporadic contact points or as a barrier for charge carriers tuning the work function of the second electrode and thus changing the Schottky barrier height.

[0020] According to an embodiment, the elements of the device are arranged to form a vertical stack. For example, the elements of the device may be arranged to form a vertical stack few-layer based memristor.

[0021] In an embodiment, the device may have a first interface between the first electrode and the switching region, and a second interface between the switching region and the intermediate region . One interface of the device may be an ohmic interface with a large density of dopants (e.g. defects or structural imperfections) while the other interface may be electrically resistive with fewer dopants. A large fraction of applied voltage can drop on the resistive interface providing switching, whereas the ohmic interface always remains highly conductive. The functioning of a resistive switch can be based on the Schottky barrier at the interface insulator/metal or semiconductor/metal. The resistance switching mechanism may rely on nano-ionic transport processes associated with redox reactions, or charge trapping/detrapping, or a mixture of these.

[0022] According to an embodiment, the switching region comprises one or more defects including structural defects, pores and/or cavities. For example, the defects may be formed during the deposition or at a later stage, e.g. by partial or full oxidation of the materials. Structural defects may affect the switching properties and be

advantageous in a memristive device. Stoichiometry of the materials can be further disturbed by a number of different techniques including thermal annealing, UV treatment, electron beam bombardment, etc. In an embodiment, the structural defects may improve ionic motion involving the oxygen anions.

[0023] According to an embodiment, the intermediate region at least partially fills the pores and/or cavities in proximity to the interface between the intermediate region and the switching region. The pores and/or cavities are fabrication defects that occur during deposition or at a later stage and may affect the functioning of the device negatively.

[0024] In an exemplary embodiment, the intermediate region can comprise metal nanowires embedded in an insulating polymer matrix and fill the cavities or pores of the switching region near the interface of the two regions. This provides for sporadic contact points by means of the metal nanowires.

[0025] According to a second aspect of the present invention, a method is disclosed. The method comprises: providing a first electrode; depositing on the first electrode a switching region comprising one or more materials; depositing on the switching region an intermediate region comprising metal nanowires and/or polymers; and depositing on the intermediate region a second electrode.

[0026] The method according to this embodiment may be, but not limited to, a method for producing or fabricating a variable resistance device, or a method for producing or fabricating a memristor.

[0027] As it is clear to a skilled person, the first and second electrodes are numbered only for clarity purposes. According to an alternative embodiment, the method comprises: providing a first electrode; depositing on the first electrode an intermediate region comprising metal nanowires and/or polymers; depositing on the intermediate region a switching region comprising one or more materials; and depositing on the switching region a second electrode.

[0028] The one or more materials according to the method may be, but not limited to, few-layer materials.

[0029] According to an embodiment, the method further comprises providing a substrate, wherein the first electrode is provided by depositing said first electrode on the substrate. In other words, according to this embodiment a substrate is provided, and the first electrode is deposited on the substrate, followed by depositing a switching

region on the first electrode etc. The substrate can be either rigid or flexible including plastic foils.

[0030] According to an embodiment, the method further comprises at least partially oxidizing the switching region comprising one or more materials prior to depositing an intermediate region.

[0031] Partial or full oxidation may be performed to modify the interface between the one or more materials of the switching region and the intermediate region. A less conductive oxide layer may be formed at the interface of the switching region by oxidation, and thus the electronic switching properties of the resulting device can be improved. Since, for example, transition metal oxides can be difficult to provide as a material to be deposited, the method according to this embodiment may be beneficial for producing such oxides in-situ during deposition.

[0032] In an exemplary embodiment, the method comprises at least partially oxidizing the switching region at various temperatures in a range between 100°C and 500°C.

[0033] According to an embodiment, the switching region comprising one or more materials is deposited on the first electrode by at least one of the following deposition techniques: spray-coating, slot-die coating, inkjet printing, thin film transfer, spreading technique, CVD and sputtering.

[0034] According to an embodiment, the intermediate region comprising metal nanowires and/or polymers is deposited on the switching region by dispensing, drop-casting, screen printing, offset printing, gravure printing, flexography, inkjet printing, and the similar techniques.

[0035] According to an embodiment, the first and second electrodes are deposited by at least one of the following deposition techniques: sputtering, CVD, PVD and printing. In this embodiment, a substrate is provided and the first electrode is deposited on the substrate.

[0036] According to an embodiment, at least partially oxidizing the switching region comprises oxidizing the switching region in an environment comprising oxygen by at least one of the following techniques: thermal annealing, laser, plasma, and xenon flash lamp treatment.

[0037] As it is clear to a skilled person, the methods according to these embodiments are not limited to the mentioned techniques, and they are indicated for exemplary purposes only.

[0038] According to a third aspect of the present invention, an apparatus is disclosed. The apparatus comprises: at least one processor; at least one memory coupled to the at least one processor, the at least one memory comprising program code instructions which, when executed by the at least one processor, cause the apparatus to perform the methods according to any of the abovementioned embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

[0039] For a more complete understanding of example embodiments of the present invention, reference is now made to the following descriptions taken in connection with the accompanying drawings in which:

[0040] FIGURES 1a and 1b show devices according to embodiments of the present invention;

[0041] FIGURE 2 shows a method according to an embodiment the present invention;

[0042] FIGURES 3a to 3c are graphs of Current against Voltage for devices according to exemplary embodiments of the present invention;

[0043] FIGURES 4a to 4b are graphs of Current against Time for MoS_2/MoO_x and WS_2/WO_x based memristors according to an exemplary embodiment of the present invention.

DETAILED DESCRIPTON OF THE EMBODIMENTS

[0044] Exemplary embodiments of the present invention and its potential advantages are understood by referring to Figures 1 through 4 of the drawings.

[0045] Fig. 1 shows a device according to an embodiment of the present invention. It is clear to a skilled person that the device shown in this figure is an exemplary implementation of the present invention, and the claimed device is not limited to the structure shown herein. The device may be a memristor or another variable resistance device. The device comprises a first electrode 101 which can be made of any appropriate conductive material, for example a metal. The first electrode 101 may be a planar electrode, a wire or any other appropriate type of an electrode. In

this implementation, the switching region 102 is positioned on top of the first electrode. The switching region 102 is in electrical contact with the first electrode 101. The switching region 102 is shown as a stack of materials, which can be, for example, few-layer materials such as few-layer transition metal dichalcogenides (TMD), few-layer transition metal oxides (TMO), few-layer TMD-TMO composites (mixtures of sulfides and oxides, sulfoxides, selenoxides, telluroxides, etc) and other graphene-like materials. Few-layer materials may demonstrate high anisotropy in electrical properties due to the large difference of intra- and interlayer bonding. These materials may comprise a plurality of defects such as structural defects, pores and cavities, as schematically shown by spaces in the layers of materials in the switching region 102. When constructed in a single- or few-layer form, materials may experience defect generation, especially at the edge of crystals, resulting in highly active nonstochiometric areas. For example oxygen, sulfur, selenium or tellurium anions (or equivalently positively charged vacancies) can act as mobile species and thus anionic motion can lead to valence change of the metal, which causes the resistance change of the material. The defects may also be responsible for charge trapping and de-trapping providing an alternative mechanism of resistance switching.

[0046] The device further comprises an intermediate region 103 and a second electrode 104. The intermediate region 103 is in electrical contact with the second electrode 104 and the switching region 102. The intermediate region 103 can comprise, for example, metal nanowires, or a variety of conducting polymers (described above), composite polymers with different conductive fillers such as Carbon Nanotubes, graphene, graphite, metal particles etc. In an exemplary implementation of the device shown in Fig. 1b, the intermediate region comprises metal nanowires 105 embedded in an insulating polymer matrix. The intermediate region of Fig. 1b can be in electrical contact with the second electrode 104 and with the switching region 102 via one or more electrical contact points. These contact points can be provided via sporadic physical contact or proximity of the metal nanowires to the other regions. The intermediate region 103 may be advantageous in providing electrical contact with the switching region 102 and the second electrode 104, while at the same time preventing unwanted electrical contact between the first 101 and the second electrode 104.

[0047] Typically, a variable resistance device (such as a memristor) is built from a metal/insulator/metal or metal/semiconductor/metal thin-film stack. Due to the

nature of some insulators that exhibit memristive properties, the bottom and top electrodes might be shorted in conventional devices, which can potentially render the device unusable. This risk is even more significant when few-layer materials are used in the switching region 102. The intermediate region 103 can prevent this unwanted electrical contact between the electrodes 101 and 104. For example, metal nanowires embedded in polymer matrix can act as a separator that partially fills the pores and cavities in proximity of the interface between the intermediate and the switching regions with insulating polymer, and provides sporadic electrical contacts by nanowires which support ionic motion channels at nanoscale. Therefore, with the intermediate region 103 (for example, comprising metal nanowires 105) unwanted connection between the electrodes of the device is unlikely, and the performance of the device is improved at the same time. According to an embodiment, the intermediate region may be used for tuning of the Schottky barrier properties at the interface between semiconductor and metal.

[0048] A classical approach to memristor fabrication usually requires a high-precision mask alignment and an involvement of high temperatures and low vacuum processes. With the growth of printed electronics industry aligned with the advantages of reducing manufacturing costs, there is a need for solution-processable materials and low-cost technologies that can be applied to manufacturing of memristor arrays.

[0049] Fig. 2 shows a method according to an embodiment of the present invention. This method is suitable for production or fabrication of variable resistance devices such as memristors. According to the method, a first electrode 201 is provided. It can be deposited on a substrate (not shown) by any suitable technique such as dispensing, screen printing, offset printing, gravure printing, flexography, slot-die coating, inkjet printing, chemical vapor deposition (CVD) and sputtering; or the electrode 201 can be pre-manufactured. A switching region 212 is then deposited onto the electrode, resulting in a structure 202 with one electrode and an exposed switching region 212. The switching region 212 may be deposited by different techniques such as spray-coating, slot-die coating, inkjet printing, thin film transfer, CVD and others. The switching region 212 can comprise a variety of different materials, as described in the embodiments above. The method of Fig. 2 further comprises depositing an intermediate region 213 onto the switching region 212, which results in a structure 203. The intermediate region 213 can be deposited by any suitable technique such as dispensing,

drop-casting, screen printing, offset printing, gravure printing, flexography, inkjet printing, etc. Then, a second electrode 214 is deposited by any suitable technique, resulting in the final structure 204. In an alternative embodiment, the intermediate region may be deposited onto the first electrode, and deposition of the switching region and the second electrode may follow.

[0050] The method according to the present invention may include an additional step of partial or full oxidation of the materials of the switching region. After the oxidation is performed, the intermediate region 213 is deposited onto a partially or fully oxidized switching region 215 of the structure 205 and the method continues similarly to the embodiment described above. A variety of oxidation techniques can be used including, but not limited to, thermal annealing, laser, plasma, and xenon flash lamp treatment. The gaseous atmosphere of the oxidation can be, for example air, oxygen, ozone or a mixture of an inert gas with oxygen. Ozone atmosphere may enhance the rate and the degree of oxidation during the treatment. Masking may also be used during oxidation in any of the above gaseous atmospheres.

[0051] A less conductive oxide layer may be formed at the interface of the switching region 212 by oxidation, which allows improving the electronic switching properties of the resulting device. The partial or full oxidation of materials may also significantly increase the number of defects in the material, which can be beneficial for producing enhanced ionic motion involving the oxygen anions. This allows using, for example, few-layer materials as anion-driven memristors wherein the resistance switching is governed by a variety of defects in the materials that alter electronic transport. While bulk material memristors often require forcible disturbance of stoichiometry in order to achieve sufficient ionic motion, few-layer materials may have natural defects due to their unique structure.

[0052] "Memristance", or memristive property, can be expressed as a charge-dependent rate of magnetic flux φ with charge q by the following formula $M(q) = d\varphi/dq$. Due to the fact that voltage V is a time function of magnetic flux and current I is a time function of charge, the following expression can be obtained: $M(q(t)) = V(t)/I(t)$. This shows that memristance is essentially a charge-dependent resistance. With little changes in M(q(t)) under pulsating current conditions the memristor may behave as a resistor. Usually, three main properties of a memristor are considered: 1 – pinched I-V (current-voltage) hysteresis loop; 2 – hysteresis lobe area decrease with increase in

frequency; and 3 – hysteresis loop shrinks to a single-valued function at infinite frequency. The devices described in the following examples are memristors based on few-layer WS_2 and MoS_2 with a metal nanowire interlayer, deposited by different methods and at different conditions. According to a first exemplary implementation of the method, the first electrodes used in these examples were planar gold electrodes. WS_2 and MoS_2 flakes dispersed in ethanol solution were spray-coated over the electrode at different temperatures (150°C, 250°C and 400°C), and then dried in vacuum. The lateral size of WS_2 flakes was 50-150 nm, the thickness was 1-4 monolayers. The lateral size of MoS_2 flakes was 100-400 nm, the thickness was 1-8 monolayers. The overall thickness of the switching region was in the range of 50–300 nm. Then, an intermediate region of silver nanowires (NW) dispersed in an organic media was drop-casted. The top electrode was printed using a silver paste. According to the second exemplary implementation of the method, the first electrode was fabricated by screen printing or inkjet printing of silver ink on a polyethylene naphthalate (PEN) substrate. The WS_2 and MoS_2 thin films were deposited over the electrode by a spreading technique, in particular a modified Langmuir-Blodgett method, where the inorganic film is collected at a polar-nonpolar liquid interface by mixing and then, utilizing a tendency of the interface film to spread or cover any available area, it was transferred to the plastic foil with the printed electrode. The film transfer procedure can be repeated 2-10 times depending on the required film thickness. The overall thickness of the switching region was in the range of 30–300 nm. Then the films were dried in vacuum and annealed at 180-200 °C for 3 hours in air. This led to the formation of an ultrathin oxide layer (~2-10 nm) at the top surface of the film, resulting in WS_2/WO_x ($x<3$) and MoS_2/MoO_x ($x<3$) films, respectively. Then, an intermediate region of silver nanowires (NW) dispersed in an organic media was drop-casted. The top electrode was screen printed using a silver paste.

[0053] Figs. 3a to 3c are graphs of current against voltage for the example devices. The materials are called herein WS_2/WO_x ($x<3$) instead of WS_2/WO_3 and MoS_2/MoO_x ($x<3$) instead of MoS_2/MoO_3 because the stoichiometry may not be accurate for few-layer materials in a deficient phase. Fig. 3a shows I-V characteristics of the few-layer MoS_2/MoO_x memristor deposited by spray-coating at 250°C with a silver nanowires intermediate layer. Fig. 3b shows I-V characteristics of the few-layer MoS_2/MoO_x memristor deposited by the spreading technique at room temperature, and

Fig. 3c shows the few-layer WS_2/WO_x memristor deposited by the spreading technique at room temperature. The few-layer stacks exhibit a typical hysteresis loop of I-V curve at positive and negative direct current (DC) voltages. The threshold voltage of below 1 V and low switching power of less than 0.1 μW along with high resistance change of up to 10^6 can be beneficial for the purposes of ultra-low power electronics.

[0054] One application of memristors is their function as an analogue of a biological synapse where the strength of the synaptic connection can be precisely changed to perform information processing, learning and memorization in accordance with pre-synaptic and post-synaptic neuron actions. Similarly to synapse terminology, two types of memristor plasticity can be identified: short-term plasticity (STP), in which the changes in resistance last for only seconds and then the memristor returns to the original state, and long-term plasticity (LTP), in which the resistance change can last from hours to years. Memristance is managed by the pulse amplitude, the number of pulses, and input frequency, which all cumulatively change the "synaptic weight" of memristor.

[0055] Figs. 4a and 4b are current-time graphs that show resistance switching behavior and memorization of MoS_2/MoO_x and WS_2/WO_x based memristors fabricated by the spreading technique and spray-coating, respectively. Fig. 4a illustrates STP of MoS_2/MoO_x memristor obtained by applying a train of electric pulses with amplitude of 150mV for 606ms with a pulse interval of about 6s, with the base voltage of 50mV. Fig. 4b shows LTP obtained for the WS_2/WO_x memristor by applying a sequence of electric pulses with amplitude of 200mV for 66ms with a pulse interval of 66ms (solid curve) and 606ms with a pulse interval of 606ms (dashed curve), the base voltage was 50mV. As shown in these Figures, the memristive devices possess both STP and LTP properties when the interval between pulses varies. Low-frequent pulsed DC voltage decreases the resistance temporary while high-frequent DC voltage leads to long-term potentiation. In other words, a spike timing-dependent plasticity (STDP), in which the changes in resistance depend on the interval between spikes, is demonstrated.

[0056] An apparatus in accordance with the invention may include at least one processor in communication with a memory or memories. The processor may store, control, add and/or read information from the memory. The memory may comprise one or more computer programs which can be executed by the processor. The processor may also control the functioning of the apparatus. The processor may control other

elements of the apparatus by effecting control signaling. The processor may, for example, be embodied as various means including circuitry, at least one processing core, one or more microprocessors with accompanying digital signal processor(s), one or more processor(s) without an accompanying digital signal processor, one or more coprocessors, one or more multi-core processors, one or more controllers, processing circuitry, one or more computers, various other processing elements including integrated circuits such as, for example, an application specific integrated circuit (ASIC), or field programmable gate array (FPGA), or some combination thereof. Signals sent and received by the processor may include any number of different wireline or wireless networking techniques.

[0057] The memory can include, for example, volatile memory, non-volatile memory, and/or the like. For example, volatile memory may include Random Access Memory (RAM), including dynamic and/or static RAM, on-chip or off-chip cache memory, and/or the like. Non-volatile memory, which may be embedded and/or removable, may include, for example, read-only memory, flash memory, magnetic storage devices, for example, hard disks, floppy disk drives, magnetic tape, etc., optical disc drives and/or media, non-volatile random access memory (NVRAM), and/or the like. If desired, the different functions discussed herein may be performed in a different order and/or concurrently with each other. Furthermore, if desired, one or more of the above-described functions may be optional or may be combined.

[0058] Although various aspects of the invention are set out in the independent claims, other aspects of the invention comprise other combinations of features from the described embodiments and/or the dependent claims with the features of the independent claims, and not solely the combinations explicitly set out in the claims.

[0059] It is also noted herein that while the above describes example embodiments of the invention, these descriptions should not be viewed in a limiting sense. Rather, there are several variations and modifications which may be made without departing from the scope of the present invention as defined in the appended claims.

WHAT IS CLAIMED IS

1. A device, comprising:
a first electrode;
a second electrode spaced from the first electrode;
a switching region positioned between the first electrode and the second electrode, the switching region comprising one or more materials; and
an intermediate region positioned between the switching region and the second electrode, wherein the intermediate region is in electrical contact with the switching region and the second electrode.

2. The device of claim 1, wherein the device is a memristor.

3. The device of any of claims 1 and 2, wherein the switching region is in electrical contact with the first electrode via physical contact with the first electrode, and in electrical contact with the second electrode via physical contact with the intermediate region.

4. The device of any of claims 1 to 3, wherein the switching region comprises one or more materials selected from the group of: transition metal dichalcogenides (TMD), partially oxidized TMD, fully oxidized transition metal oxides (TMO) and graphene-like materials.

5. The device of any of claims 1 to 4, wherein the switching region has a thickness between 10 and 1000 nanometers.

6. The device of any of claims 1 to 5, wherein the intermediate region comprises: metal nanowires, polymers or a combination thereof.

7. The device of any of claims 1 to 6, wherein the intermediate region is in electrical contact with the second electrode and with the switching region via one or more electrical contact points.

8. The device of any of claims 1 to 7, wherein the elements of a device are arranged to form a vertical stack.

9. The device of any of claims 1 to 8, wherein the switching region comprises one or more defects including: structural defects, pores and/or cavities.

10. The device of claim 9, wherein the intermediate region at least partially fills the pores and/or cavities in proximity to the interface between the intermediate region and the switching region.

11. A method, comprising:
providing a first electrode;
depositing on the first electrode a switching region comprising one or more materials;
depositing on the switching region an intermediate region comprising metal nanowires and/or polymers; and
depositing on the intermediate region a second electrode.

12. The method of claim 11, further comprising providing a substrate, wherein the first electrode is provided by depositing said first electrode on the substrate.

13. The method of any of claims 11 and 12, further comprising at least partially oxidizing the switching region comprising one or more materials prior to depositing an intermediate region.

14. The method of any of claims 11 to 13, wherein the switching region comprising one or more materials is deposited on the first electrode by at least one of the following deposition techniques: spray-coating, slot-die coating, inkjet printing, thin film transfer, chemical vapor deposition (CVD) and sputtering.

15. The method of any of claims 11 to 14, wherein the intermediate region comprising metal nanowires and/or polymers is deposited on the switching region by dispensing, drop-casting, screen printing, offset printing, gravure printing, flexography, inkjet printing, and the similar techniques.

16. The method of claim 13, wherein the first and second electrodes are deposited by at least one of the following deposition techniques: sputtering, chemical vapor deposition (CVD), physical vapor deposition (PVD) and printing.

17. The method of claim 13, wherein at least partially oxidizing the switching region comprises oxidizing the switching region in an environment comprising oxygen by at least one of the following techniques: thermal annealing, laser, plasma, and xenon flash lamp treatment.

18. An apparatus, comprising:
at least one processor;
at least one memory coupled to the at least one processor, the at least one memory comprising program code instructions which, when executed by the at least one processor, cause the apparatus to perform the methods according to any of claims 11 to 17.

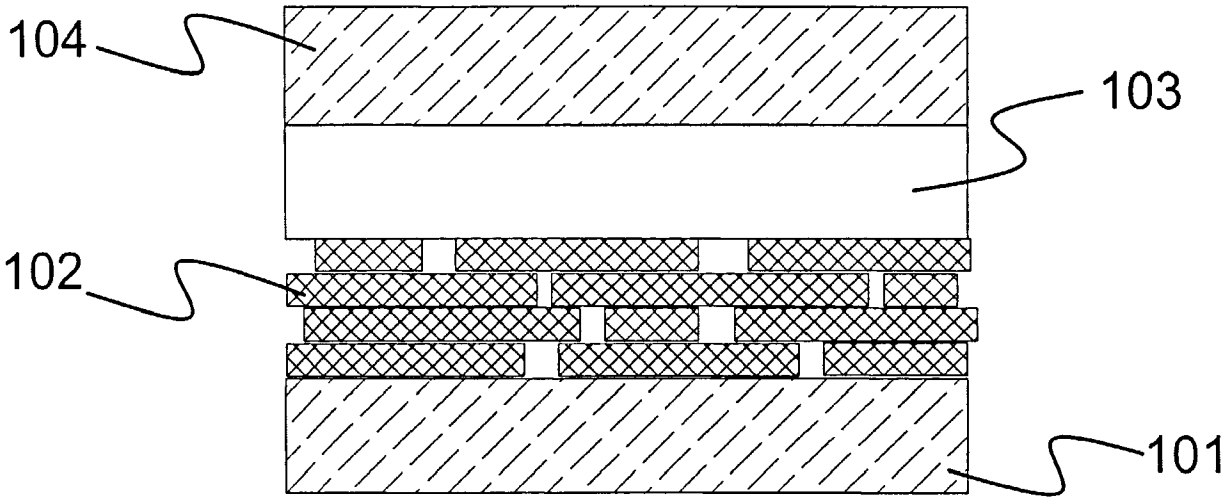

Figure 1a

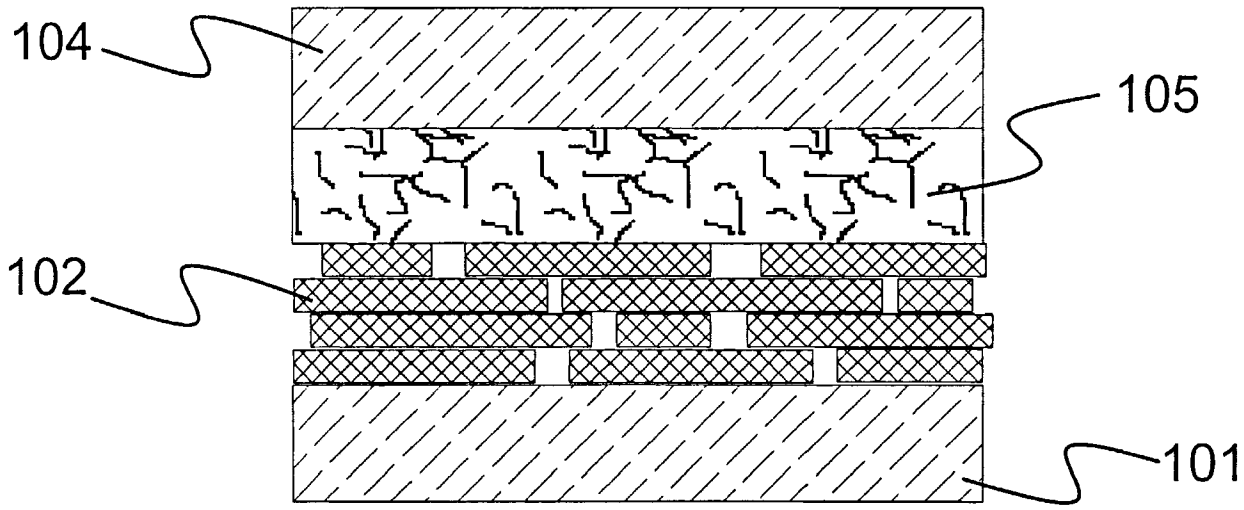

Figure 1b

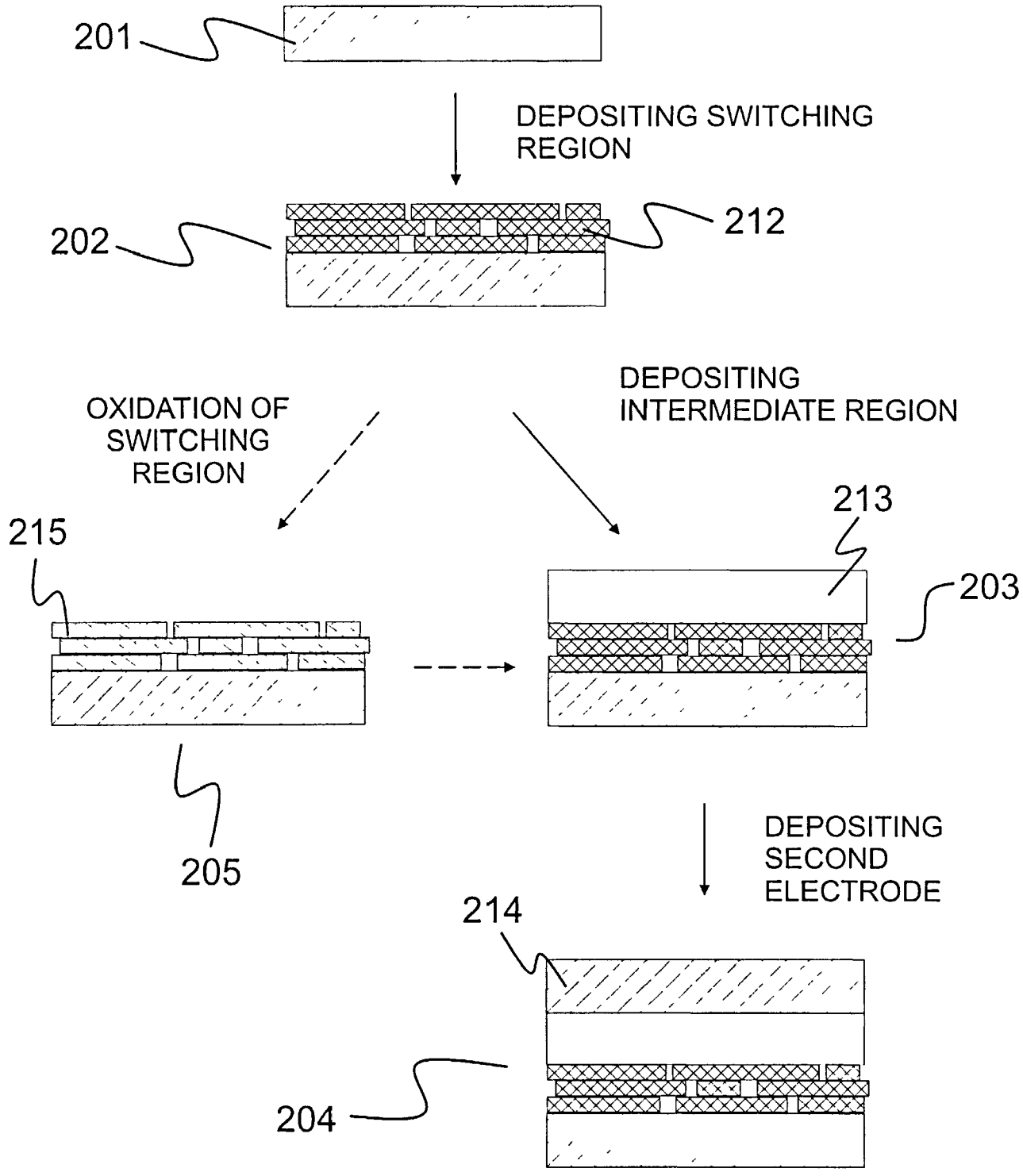
201
DEPOSITING SWITCHING REGION
202
212
OXIDATION OF SWITCHING REGION
DEPOSITING INTERMEDIATE REGION
215
213
203
205
DEPOSITING SECOND ELECTRODE
214
204

Figure 2

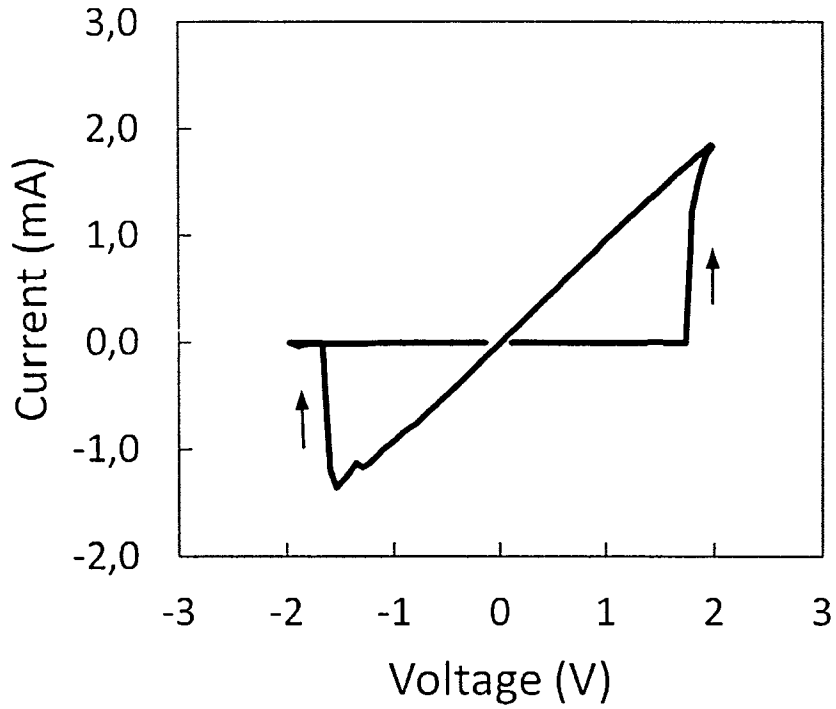

Figure 3a

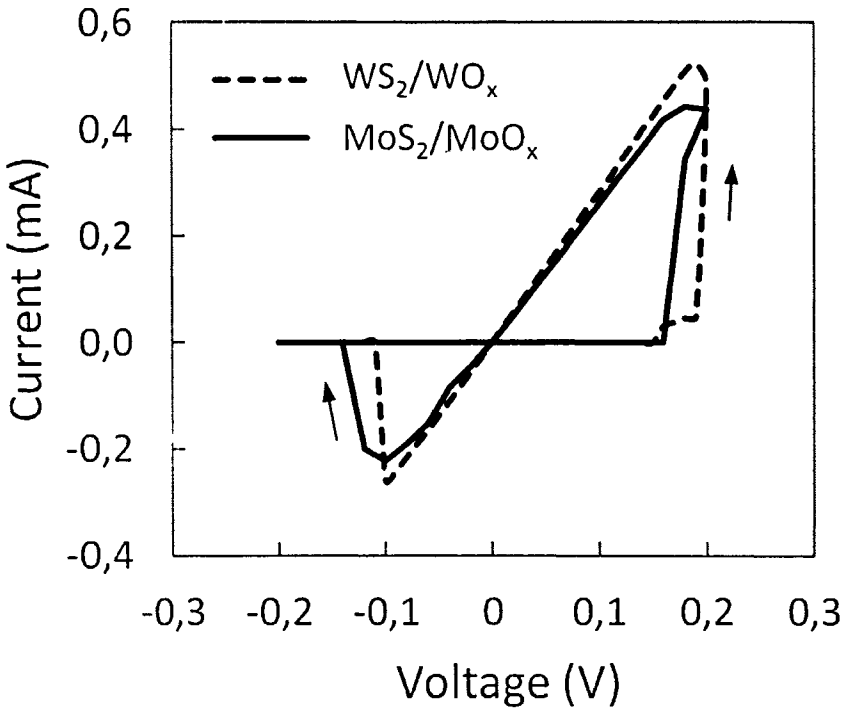
0,6
0,4
0,2
0,0
-0,2
-0,4
Current (mA)
WS_2/WO_x
MoS_2/MoO_x
-0,3
-0,2
-0,1
0
0,1
0,2
0,3
Voltage (V)

Figure 3b

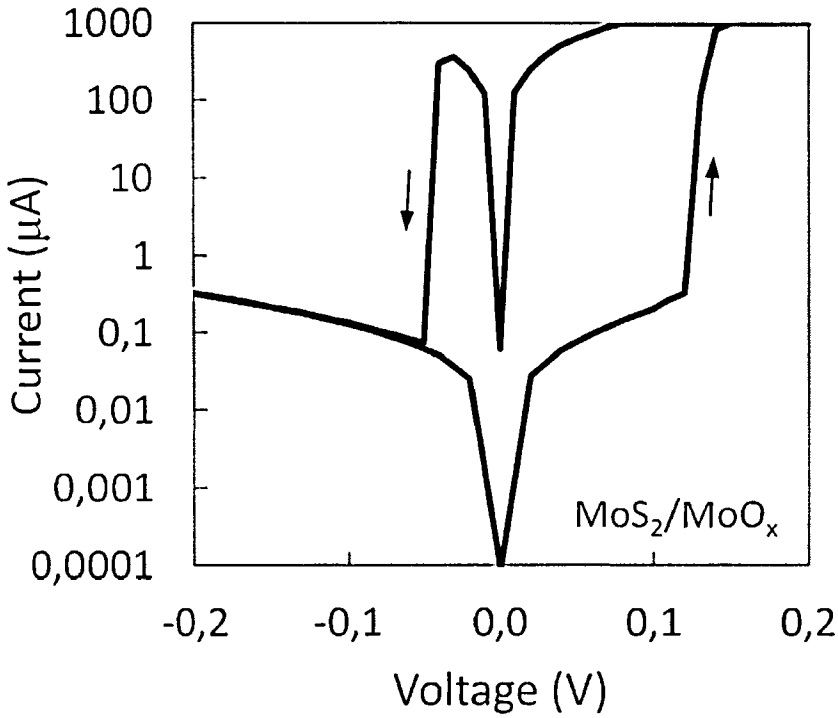
1000
100
10
1
0,1
0,01
0,001
0,0001
Current (μA)
-0,2
-0,1
0,0
0,1
0,2
Voltage (V)
MoS2/MoOx

Figure 3c

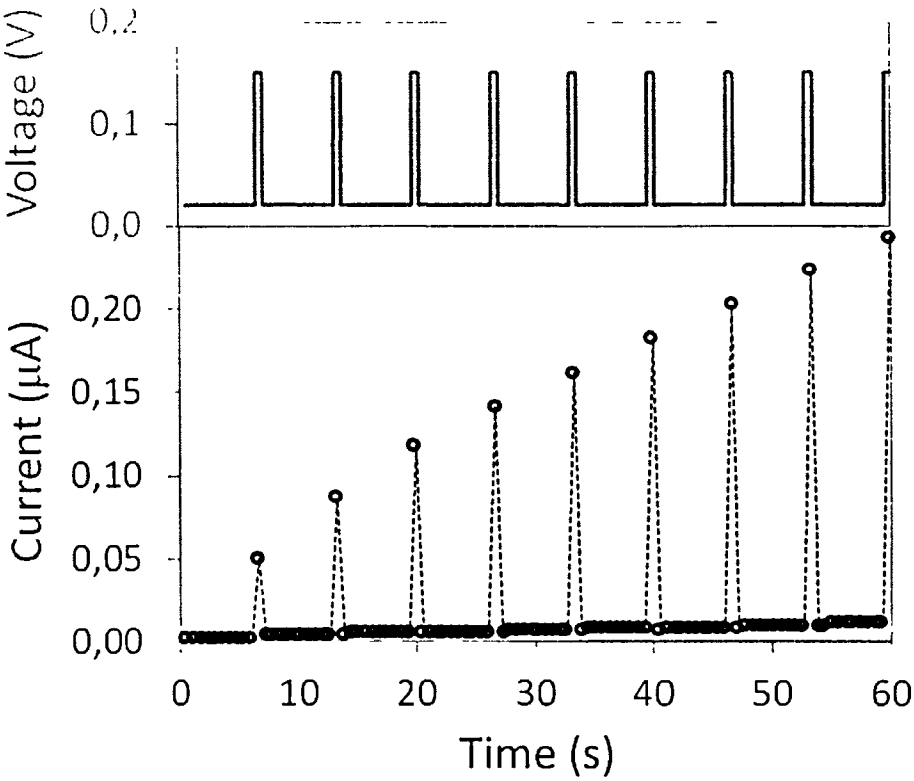
Voltage (V)
0,2
0,1
0,0
Current (μA)
0,20
0,15
0,10
0,05
0,00
0
10
20
30
40
50
60
Time (s)

Figure 4a

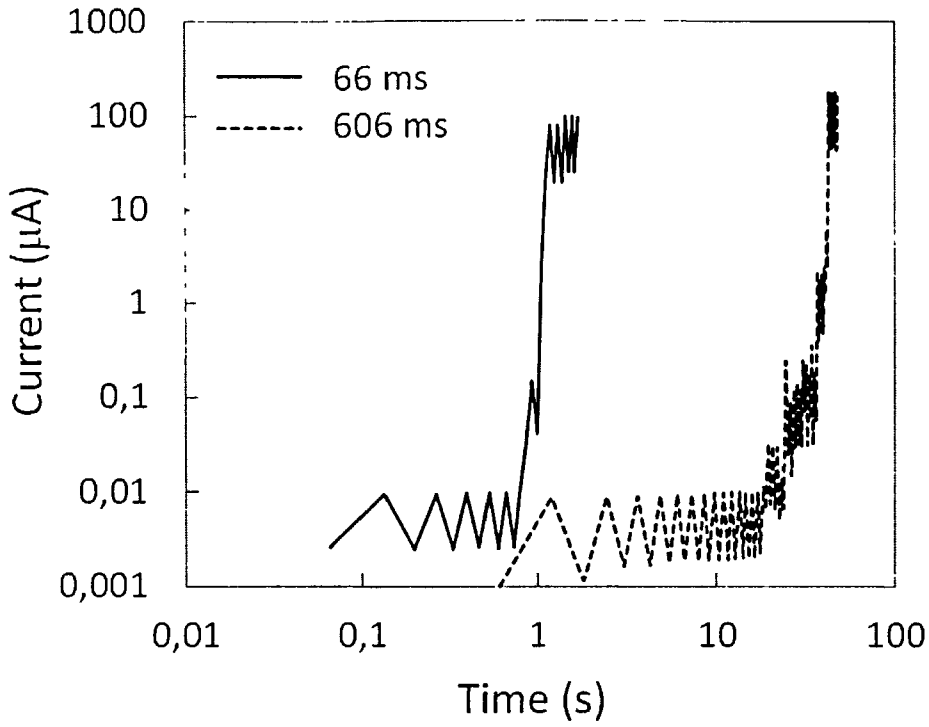
1000
100
10
1
0,1
0,01
0,001
Current (μA)
66 ms
606 ms
0,01
0,1
1
10
100
Time (s)

Figure 4b

INTERNATIONAL SEARCH REPORT

International application No
PCT/RU2014/000316

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L45/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data, INSPEC, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2010/117051 A1 (TIAN WEI ET AL) 13 May 2010 (2010-05-13) paragraphs [0022] - [0061]; figures 1, 2, 5, 6	1-8,11, 12,14, 15,18
X	US 2011/186799 A1 (KAI JAMES ET AL) 4 August 2011 (2011-08-04) paragraphs [0015] - [0035], [0040]; figures 1-3, 5A	1-8,11, 12,14, 15,18
X	EP 2 141 753 A2 (GWANGJU INSTITUTE OF SCIENCE AND TECHNOLOGY) 6 January 2010 (2010-01-06) paragraphs [0014] - [0030]; figures 1-3	1-5,7,8

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 January 2015	01/04/2015

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Köpf, Christian

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Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/RU2014/000316

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-9, 11, 12(completely); 14, 15, 18(partially)

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-9, 11, 12(completely); 14, 15, 18(partially)

   (Electronic switching) device comprising an intermediate region positioned between, and being in electrical contact with, a (resistance) switching material region and one of two electrodes, wherein said intermediate region comprises metal nanowires and/or polymers; corresponding fabrication method and apparatus

   ---

2. claim: 10

   (Electronic switching) device comprising an intermediate region positioned between, and being in electrical contact with, a (resistance) switching material region and one of two electrodes, wherein said intermediate region at least partially fills pores and/or cavities of the switching region in proximity to the interface between said regions

   ---

3. claims: 13, 16, 17(completely); 14, 15, 18(partially)

   (Electronic switching) device fabrication method comprising depositing a switching material region on a first electrode, depositing an intermediate region comprising metal nanowires and/or polymers thereon, and depositing a second electrode, further comprising at least partially oxidizing said switching region prior to depositing said intermediate region; corresponding processing apparatus

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INTERNATIONAL SEARCH REPORT

International application No
PCT/RU2014/000316

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2006/003620 A1 (KONINKLIJKE PHILIPS ELECTRONICS NV; VAN SCHAIJK ROBERTUS T F ET AL) 12 January 2006 (2006-01-12) page 20, line 10 - page 22, line 5; figure 9	1-3,5-8, 11,12, 14,18
X	TANAKA H ET AL: "Electrical Switching Phenomena in a Phase Change Material in Contact with Metallic Nanowires", JAPANESE JOURNAL OF APPLIED PHYSICS, vol. 41, no. 12B, part 2, 15 December 2002 (2002-12-15), pages L1443-L1445, XP001162410, ISSN: 0021-4922, DOI: 10.1143/JJAP.41.L1443 page L1443; figure 1	1-3,5-8
X	US 8 298 891 B1 (CHIANG TONY ET AL) 30 October 2012 (2012-10-30) column 3, lines 41-67; figure 1C	1-3,5,8, 9

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/RU2014/000316

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2010117051 A1	13-05-2010	NONE	
US 2011186799 A1	04-08-2011	TW 201140813 A	16-11-2011
		US 2011186799 A1	04-08-2011
		WO 2011097389 A1	11-08-2011
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		KR 20100004363 A	13-01-2010
		US 2010002491 A1	07-01-2010
WO 2006003620 A1	12-01-2006	CN 101010793 A	01-08-2007
		JP 2008505476 A	21-02-2008
		KR 20070028604 A	12-03-2007
		TW I386940 B	21-02-2013
		US 2009200536 A1	13-08-2009
		WO 2006003620 A1	12-01-2006
US 8298891 B1	30-10-2012	US 8298891 B1	30-10-2012
		US 2013140511 A1	06-06-2013
		US 2014014892 A1	16-01-2014