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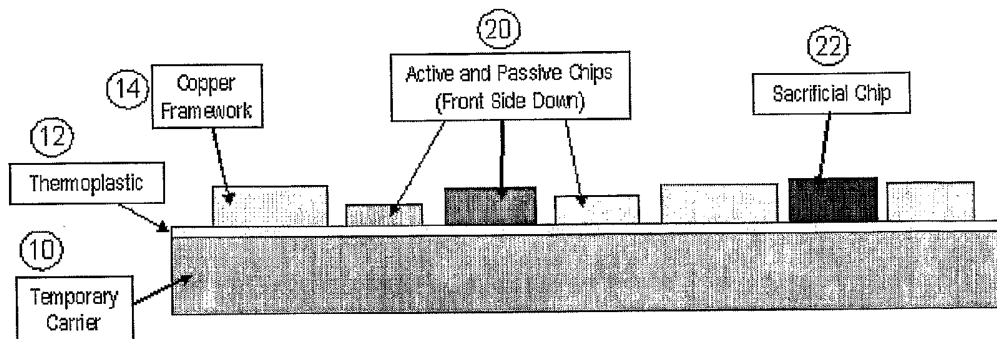
(54) Title: A METHOD FOR PRODUCING A MULTI COMPONENT ELECTRONIC MODULE AND A MODULE PRODUCED BY THE METHOD



(57) Abstract: A method of manufacturing an integrated electronic module, comprising the step of providing a framework with openings arranged to receive components, the openings being arranged to locate the components in a predefined configuration.

WO 2006/105586 A1

A METHOD FOR PRODUCING A MULTI COMPONENT ELECTRONIC MODULE AND A MODULE PRODUCED BY THE METHOD

FIELD OF THE INVENTION

The present invention relates to a method for producing a multi-component electronic module, and particularly, but not exclusively, to a method for integrating multiple electronic components into a single module which is particularly suited for applications in the 40GHz and above frequency range.

BACKGROUND OF THE INVENTION

Conventional multi-component integration into a single module, particularly for modules which are arranged to operate with signal frequencies of 40GHz and above, is a time consuming and expensive process, since conventional manufacturing techniques require the components (such as chips) to be placed into a metal package and then wire-bonded to each other to form connections. Moreover, the connections formed by wire-bonding do not function as correct transmission lines at high frequencies and may cause loss of the electrical signal.

Another method utilised to produce multi-component modules is to "flip-chip" the active chips into a carrier to avoid wire-bonding. This method has disadvantages, as there are inherent difficulties in modelling up-side-down chips for applications in the frequency range above 40 GHz. Structural problems may also arise when the chips are in a vibrating environment, including problems with heat transfer.

SUMMARY OF THE INVENTION

In a first aspect, the present invention provides a method of manufacturing an integrated electronic module, comprising the step of providing a framework with openings arranged to receive components, the openings being arranged to locate the components in a predefined configuration.

In one form, the framework may be made from a thermally conductive material, and/or from an electrically conductive material.

In one form, the method may include the further step of manufacturing the framework by etching openings into a sheet of metal.

The method may comprise the further steps of bonding the framework to a temporary carrier to facilitate the positioning of the components.

The temporary carrier may be provided with a layer of a thermoplastics material, whereby the framework is bonded to the layer of thermoplastics material. Furthermore, after inserting the components into the openings provided in the framework, the framework and the components may be coated with an electrically conductive material to form a common ground connection for all the components.

In one embodiment the total surface area of the openings is minimised to minimise the volume of the electrically conductive material required to avoid unnecessary structural stress.

After applying the electrically conductive coating, the method may include the further step of processing the module to produce a flat surface.

The temporary carrier layer may be removed and a dielectric material may be coated in place of the removed temporary carrier. A pattern may be etched into the dielectric layer, the pattern defining the via hole electrical connections to the components.

Once the pattern is etched into the dielectric layer, a conductive material may be provided into the etched area and onto the dielectric. The conductive material is patterned to create an electrically conductive
5 interconnection between the components.

In one form, the method may comprise the further step of inserting at least one sacrificial component in the at least one opening, whereby the sacrificial component is removable to define a waveguide cavity. In particular,
10 the at least one sacrificial component may be of a dimension whereby the step of processing the module to provide a flat surface causes the sacrificial component to be exposed to facilitate removal (by etching) of the sacrificial component.

15 The temporary carrier may be made from a Silicon Aluminium alloy that has a thermal coefficient substantially similar to the thermal coefficient of the framework, and the framework may be formed from a material having a thermal coefficient substantially similar to the
20 thermal coefficient of the electronic components. In a particular embodiment, the framework may be made from one of copper or copper molybdenum. The components may be GaAs, SiGe or other devices.

In a second aspect, the present invention provides an
25 integrated electronic module when manufactured in accordance with a first aspect of the invention.

In a third aspect, the present invention provides an integrated electronic module comprising a framework with openings arranged to receive components, the openings
30 being arranged to locate the components in a predefined configuration.

In a fourth aspect, the present invention provides a wafer comprising a plurality of integrated electronic modules in accordance with a third aspect of the
35 invention.

In a fifth aspect, the present invention provides an electronic device including an integrated electronic module in accordance with a third aspect of the invention.

In a sixth aspect, the present invention provides a method of manufacturing a plurality of integrated electronic modules comprising the steps of providing a wafer capable of containing a plurality of frameworks, each framework being usable to form an integrated electronic module, each framework further comprising openings arranged to receive components and locate the components in a predefined configuration.

DETAILED DESCRIPTION OF THE DRAWINGS

Further features of an embodiment of the present invention will now be described, by way of example only, with reference to the following figures in which:

Figures 1 to 15 are illustrations of the method steps carried out when manufacturing a multi-component module in accordance with an embodiment of the present invention;

Figure 16 depicts a top view of a multi-component module produced in accordance with an embodiment of the present invention; and

Figure 17 depicts a top view of a wafer containing a plurality of multi-component modules in accordance with an embodiment of the present invention.

DESCRIPTION OF AN EMBODIMENT

Referring to Figures 1 through 15, there is described a series of method steps for manufacturing a multi-component module in accordance with an embodiment of the present invention.

At Figure 1, there is shown a Si/Al temporary carrier 10 that has a matching temperature coefficient to a conductive framework (Figure 3).

The temporary carrier 10 is coated with approximately 14 μm (or other thickness) of a thermoplastic material 12 (Figure 2). The coating of thermoplastic material 12 serves as a base onto which there is temporarily fixed to a framework. In the specific embodiment disclosed herein, the framework is a copper sheet 14 (Figure 3). The framework 14 is sized to hold a number of components which may include active and passive chips, waveguides, antennas, via-holes, air-bridges, thin film capacitors, resistors or any other component which may be formed or placed in a module. In the embodiment described, the framework 14 is thicker than the thickest chip that will be placed into the multi-component module. In the example given, the framework is 250 μm thick.

The framework may preferably be made of any electrically and/or thermally conductive material such as copper or copper molybdenum. Moreover, in the embodiment described the framework will preferably have a matching temperature coefficient to GaAs, InP, SiGe or Si, which may be the materials from which most semi-conductor components are manufactured for electronics which operate in the frequency range of 40 GHz and above. In other words, the framework should preferably have thermal properties similar to the thermal properties of the components which form part of the module. It will be understood that for high power operation or any other extreme ambient temperature operation such as cryogenic operation, copper molybdenum or similar thermally matched conductive material may be utilised in place of a simple copper framework.

Once the framework 14 has been fixed to the temporary carrier 10, openings 16 may be patterned and subsequently etched into the framework, to allow for the insertion of components (Figure 4). Openings 18, which may subsequently be used to form waveguide connections, may also be etched into the stencil at this time.

Once the openings 16 and 18 have been etched into the framework 14, components 20 are placed in an "up side down" configuration into the openings using a flip-chip bonder or any other equipment that is suitable for aligning and thermally bonding up-side-down components (Figure 5).

Where a waveguide connection 18 is required, a sacrificial chip 22 is placed in the opening for the waveguide connection 18. The sacrificial chip is of the same dimensions as the desired waveguide port 42, although it is slightly thicker than the framework 14, such that it protrudes beyond the framework 14.

Once all components 20 and sacrificial chips 22 have been placed into the openings in the framework 14, ground metal 24 is sputtered over framework 14, and components 20 and sacrificial chip 22 (Figure 6). In addition, ground metal 26 is also subsequently plated over sputtered ground metal 24 (Figure 7).

The sputtering and plating process generally produces a stepped surface 28, due to the varying heights of the modules 20 and chips 22. The stepped surface 28 is turned into a substantially flat surface by filling in the gaps in the stepped surface with a conductive epoxy (such as Epotek TM H20E) 30, and the resulting module is then lapped to produce a flat top surface 32 (Figure 8). If a sacrificial chip 22 is fitted, the lapping exposes the upper surface of the sacrificial chip 22, so that the sacrificial chip 22 may be suitably removed, thereby creating a waveguide port.

Once the surface is lapped flat, the module may be turned, and the temporary carrier 10 (including the thermoplastics layer 12) may be removed from the framework 14, thereby exposing the "front" side of the module (Figure 9).

The exposed surface (i.e. the surface which was bonded to the temporary carrier 10) is covered with a

10 μm (or other thickness) BCB (Benzocyclobutene) or other suitable dielectric 34. The dielectric layer 34 is applied utilising a spinning technique, followed by curing at a temperature of approximately 200°C. The dielectric
5 34 may be applied to any appropriate thickness, which may vary depending on application (Figure 10).

Once the dielectric 34 is applied, holes 36 may be patterned and etched into the dielectric 34 (Figure 11).

Once the holes 36 are etched, 3 μm (or other
10 thickness) of metal 38 is sputtered over the whole face of the dielectric 34 to form connections to the components (Figure 12). As can be seen in Figure 13, the metal 38 can also be patterned and etched to form the inter component connections.

15 It is possible to add additional layers of dielectric 34 and other materials to form additional connections and/or components (such as thin film capacitors, resistors or antennas) 40 (Figure 14).

Furthermore, the sacrificial chip 22, if fitted, may
20 be etched away to form a waveguide connection 42 with smooth walls (Figure 15).

Figure 16 depicts an example of a completed multi-chip module, highlighting the positioning of each of the major components, including the provision of
25 connectors 44 which may be utilised to interface and connect to other electronic modules, and the provision of a waveguide probe 46, which is an input/output device from the waveguide to the other components on the multi-chip module. The completed multi-chip module may be
30 incorporated into another device, such as an electronic communications device, via the connectors 44.

Figure 17 illustrates a plurality of multi-chip modules when manufactured on a wafer. It will be appreciated that a plurality of multi-chip modules may be
35 produced simultaneously on a single wafer utilising the method described herein.

The resulting multi-component module is suitable for high frequency applications (frequencies over 40 GHz), since the active and passive components are provided with a continuous ground (metallised) connection at the back (bottom) of the module, and a signal (metallised) connection at the front (top) of the module that can be designed using standard printed transmission line techniques. A good electrical connection to the back of each component is desirable for components that are designed for high frequency operation.

A good thermal connection is also provided, which in turn provides for better heat transfer and hence an improved lifetime of the module. Furthermore, by providing a framework which is thicker than all components (other than sacrificial chips), it is possible to create a module which can integrate components that have different thicknesses and that are made from different materials.

The use of a framework also provides rigidity to the module as a whole and reduces stress in the module.

Generally, the total area of openings provided for components will be kept to a minimum, to minimise the structural stress in the conductive filling material and to ensure that a certain level of rigidity is retained in the module.

It will be understood that the inter-chip connections can have several layers of metallisation. In addition, other components such as via-holes, air-bridges, thin film capacitors, resistors, antennas and other suitable passive components can be made during the module manufacturing process to form a complete high frequency module.

It will be further understood that in a particular embodiment, a copper framework, or a framework made out of other electrically and thermally conductive material such as copper molybdenum, is used. However, any material that has a temperature coefficient similar to the material of the chips and electronic components that are being

integrated may be utilised to surround the components and form part of the final package of the module.

In the particular embodiment described herein, a copper or copper molybdenum framework is convenient as a final carrier, as it can support waveguide, coaxial or other connections to the electronic module. Waveguide holes above 40 GHz require smooth walls, which are provided in at least a specific embodiment of the present invention.

It will be appreciated by persons skilled in the art that numerous variations and/or modifications may be made to the invention as shown in the specific embodiments without departing from the spirit or scope of the invention as broadly described. The present embodiments are, therefore, to be considered in all respects as illustrative and not restrictive.

CLAIMS:

1. A method of manufacturing an integrated electronic module, comprising the step of providing a framework with openings arranged to receive components, the openings being arranged to locate the components in a predefined configuration.

2. A method in accordance with Claim 1 comprising the further step of providing a framework made from a thermally conductive material.

3. A method in accordance with Claim 1 or 2, comprising the further step of providing a framework made from an electrically conductive material.

4. A method in accordance with any one of Claims 1, 2 or 3, whereby the total surface area of the openings and the total volume of the conductive filler are kept to a minimum to prevent structural stress in the conductive material.

5. A method in accordance with any one of Claims 1 to 4, comprising the further step of manufacturing the framework by etching openings into a sheet of material.

6. A method in accordance with any one of Claims 1 to 5, comprising the further step of bonding the framework to a temporary carrier to facilitate the positioning of the components.

7. A method in accordance with Claim 6, comprising the further step of providing the temporary carrier with a layer of a thermoplastics material, whereby the framework is bonded to the layer of thermoplastics material.

8. A method in accordance with any one of Claims 1 to 7, comprising the further step of, after inserting the components into the openings provided in the framework, coating the framework and the components with an electrically conductive material to form a common ground connection for all the components.

9. A method in accordance with Claim 8, wherein the total surface area of the openings is minimised to minimise the volume of the electrically conductive material required to avoid unnecessary structural stress.

10. A method in accordance with Claim 8 or Claim 9, comprising the further step of processing the module to produce a flat surface.

11. A method in accordance with Claim 9 or Claim 10, comprising the further step of removing the temporary carrier layer and depositing a dielectric material in place of the removed temporary carrier.

12. A method in accordance with Claim 11, comprising the further step of etching a pattern into the dielectric layer, the pattern defining the via-hole-connections to the components.

13. A method in accordance with Claim 12, comprising the further step of coating a conducting layer onto the dielectric layer and patterning the conductive layer to create an electric interconnection between the components.

14. A method in accordance with any one of Claims 1 to 13, comprising the further step of providing at least one sacrificial component in the at least one opening, whereby the sacrificial component is removable to define a waveguide cavity.

15. A method in accordance with Claim 14, whereby the at least one sacrificial component is of a dimension whereby the step of processing the module to provide a flat surface causes the sacrificial component to be exposed to facilitate removal of the sacrificial component.

16. A method in accordance with any one of the preceding claims, whereby the temporary carrier is made from a Silicon Aluminium or other alloy.

17. A method in accordance with any one of the preceding claims, whereby the framework is formed from a material having a thermal coefficient substantially similar to the thermal coefficient of the electronic components.

18. A method in accordance with any one of the preceding claims, whereby the framework is made from one of copper or copper molybdenum.

19. A method in accordance with any one of the preceding claims, whereby the components are one of GaAs or SiGe devices.

20. An integrated electronic module when manufactured in accordance with any one of Claims 1 to 19.

21. An integrated electronic module comprising a framework with openings arranged to receive components, the openings being arranged to locate the components in a predefined configuration.

22. An integrated electronic module in accordance with Claim 21 wherein the framework is made from a thermally conductive material.

23. An integrated electronic module in accordance with Claim 21 or 22, wherein the framework is made from an electrically conductive material.

5 24. An integrated electronic module in accordance with any one of Claims 21, 22 or 23, wherein the total surface area of the openings and the total volume of the conductive filler are kept to a minimum to prevent structural stress in the conductive material.

10

25. An integrated electronic module in accordance with any one of Claims 21 to 24, wherein the framework and the components are coated with an electrically conductive material to form a common ground connection for all the

15 components.

26. An integrated electronic module in accordance with Claim 25, wherein the total surface area of the openings and the total volume of the electrically conductive

20 material is minimised to optimise the structural stress in the conductive material.

27. An integrated electronic module in accordance with any one of Claims 21 to 26, comprising at least one

25 sacrificial component in the at least one opening, wherein the sacrificial component is removable to define a waveguide cavity.

28. An integrated electronic module in accordance with

30 any one of Claims 21 to 27, wherein the temporary carrier is made from a Silicon Aluminium or other alloy that has thermal properties substantially similar to the framework.

29. An integrated electronic module in accordance with

35 any one of Claims 21 to 28, wherein the framework is formed from a material having a thermal coefficient

substantially similar to the thermal coefficient of the electronic components.

30. An integrated electronic module in accordance with any one of Claims 21 to 29, wherein the framework is made from one of copper or copper molybdenum.

31. An integrated electronic module in accordance with any one of Claims 21 to 30, wherein the components are one of GaAs or SiGe devices.

32. A wafer comprising a plurality of integrated electronic modules in accordance with any one of Claims 21 to 31.

33. An electronic device including an integrated electronic module in accordance with any one of Claims 21 to 31.

34. A method of manufacturing a plurality of integrated electronic modules comprising the steps of providing a wafer capable of containing a plurality of frameworks, each framework being usable to form an integrated electronic module, each framework further comprising openings arranged to receive components and locate the components in a predefined configuration.

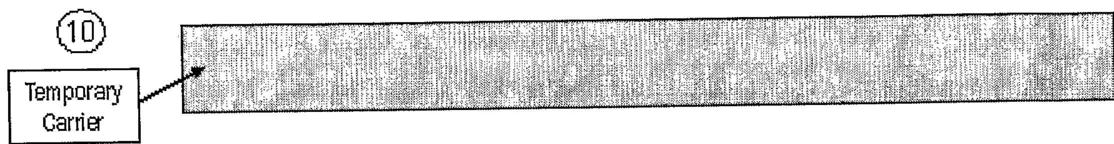


FIGURE 1

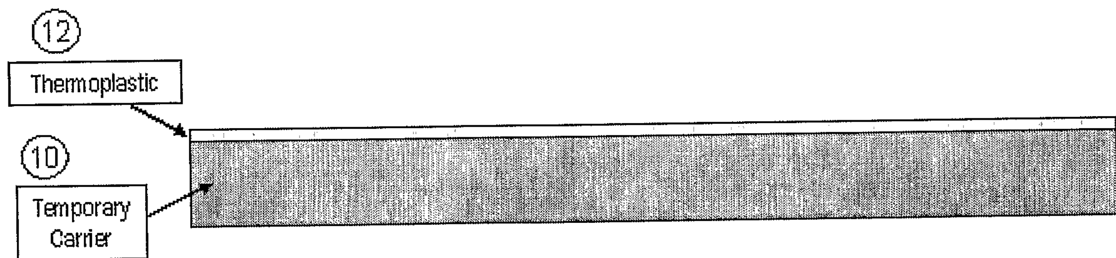


FIGURE 2

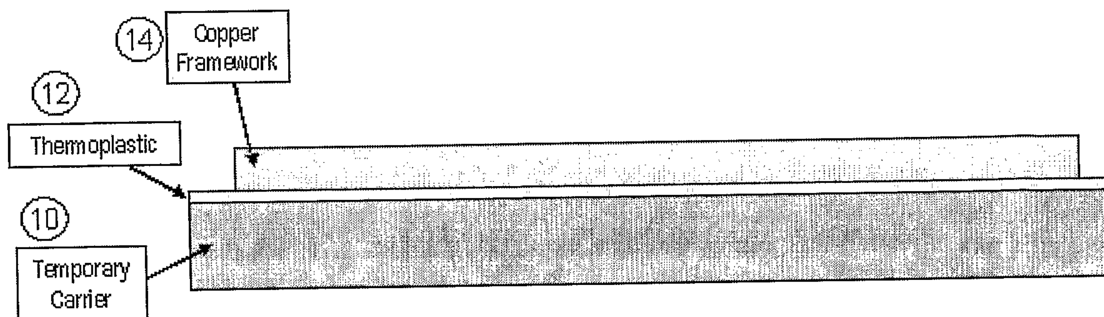


FIGURE 3

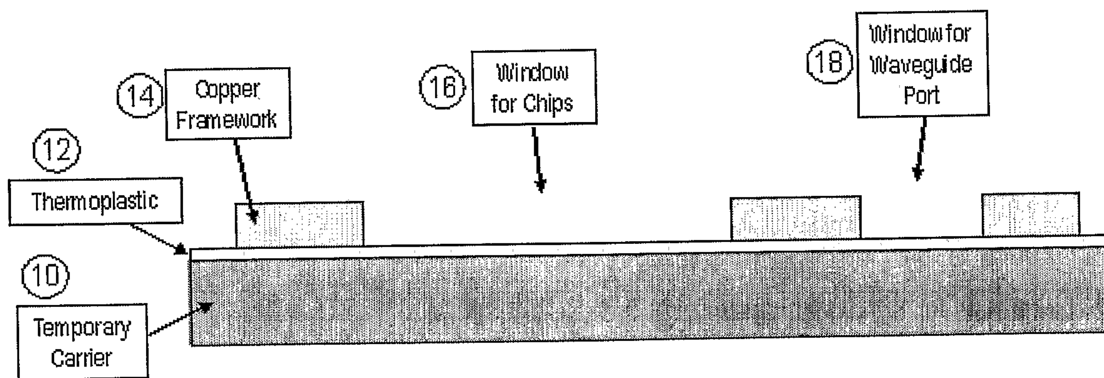


FIGURE 4

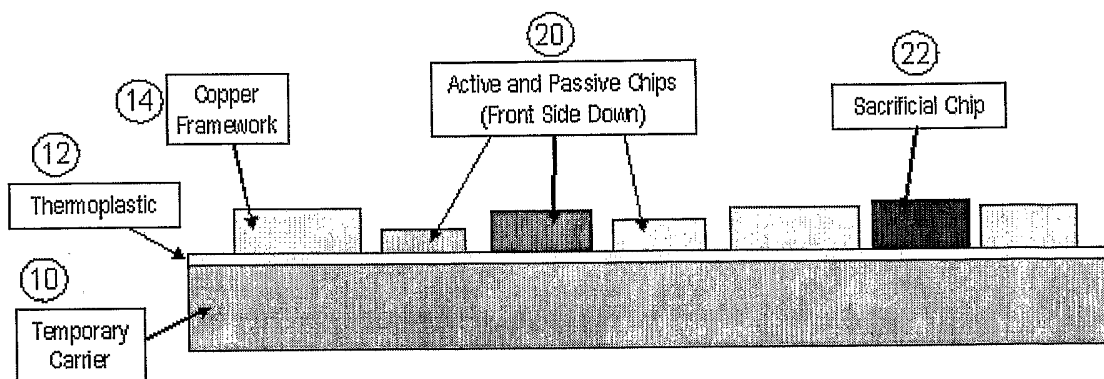


FIGURE 5

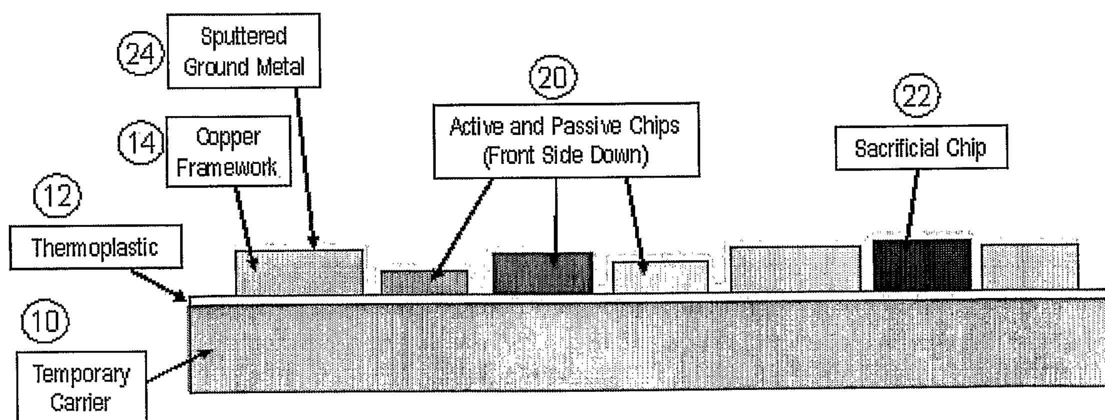


FIGURE 6

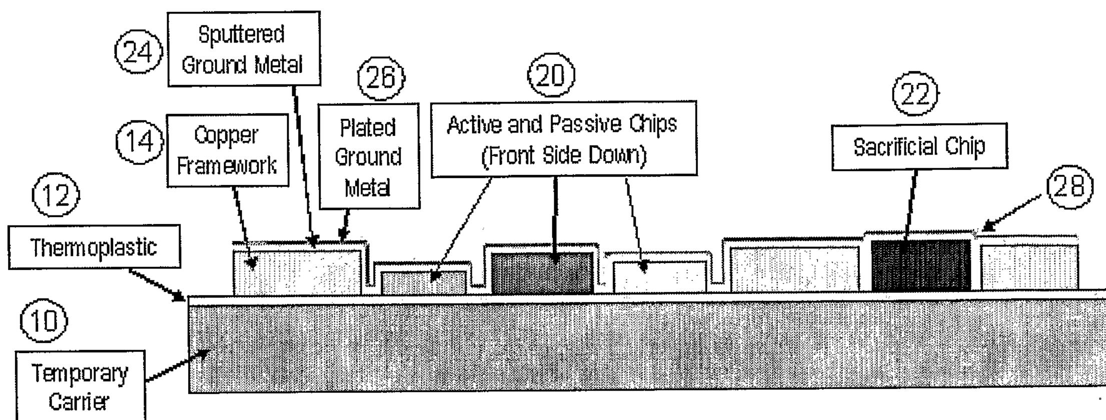


FIGURE 7

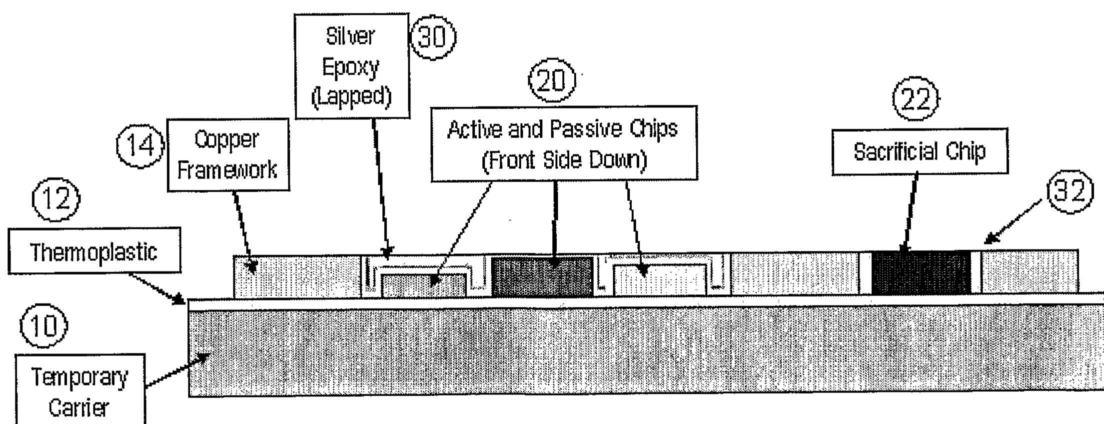


FIGURE 8

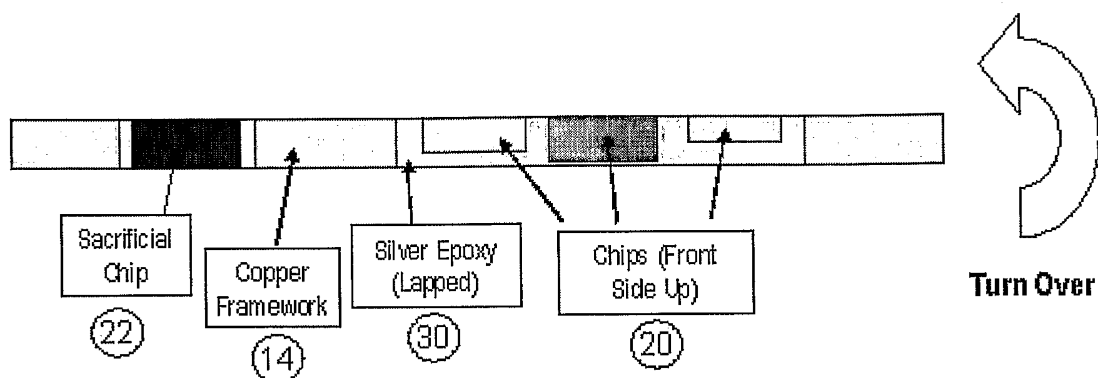


FIGURE 9

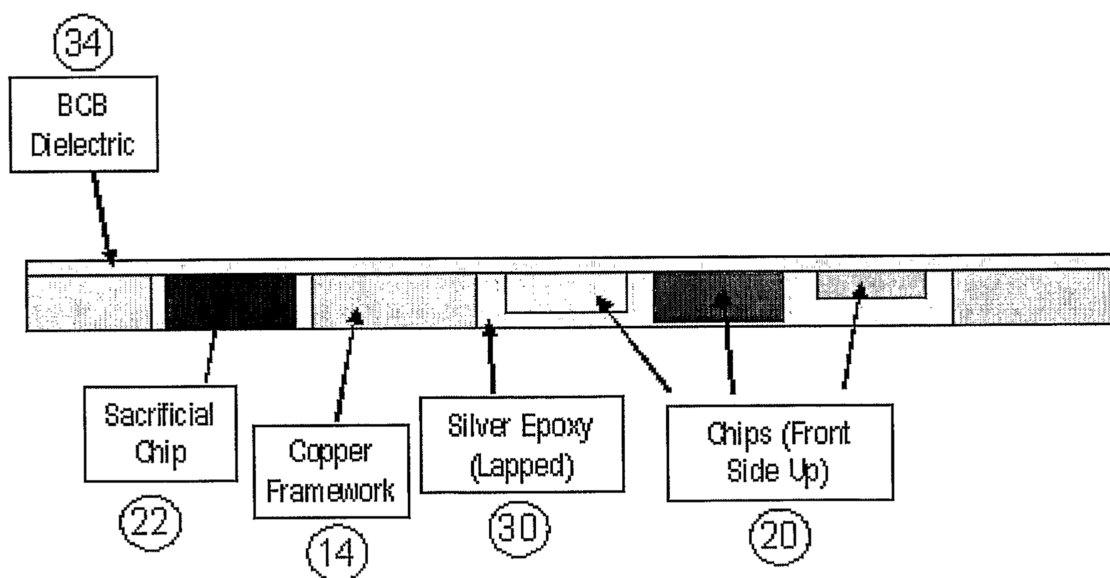


FIGURE 10

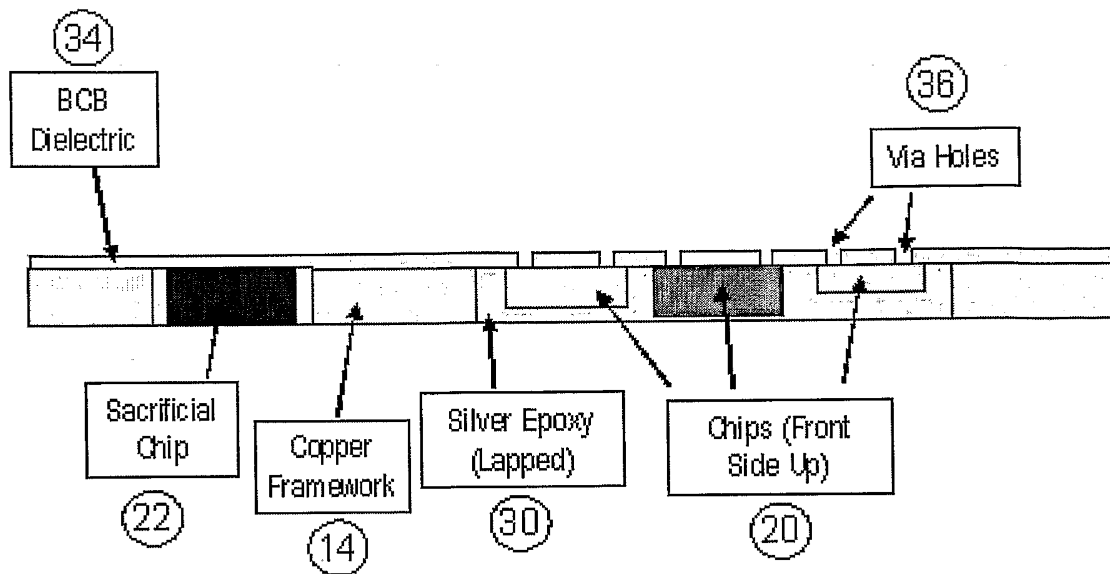


FIGURE 11

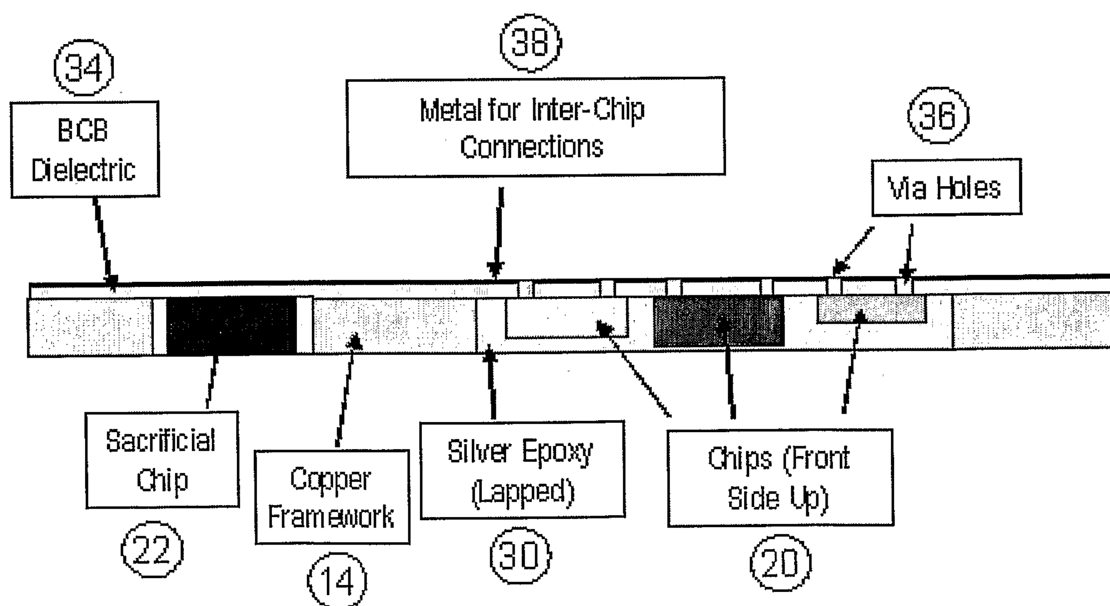


FIGURE 12

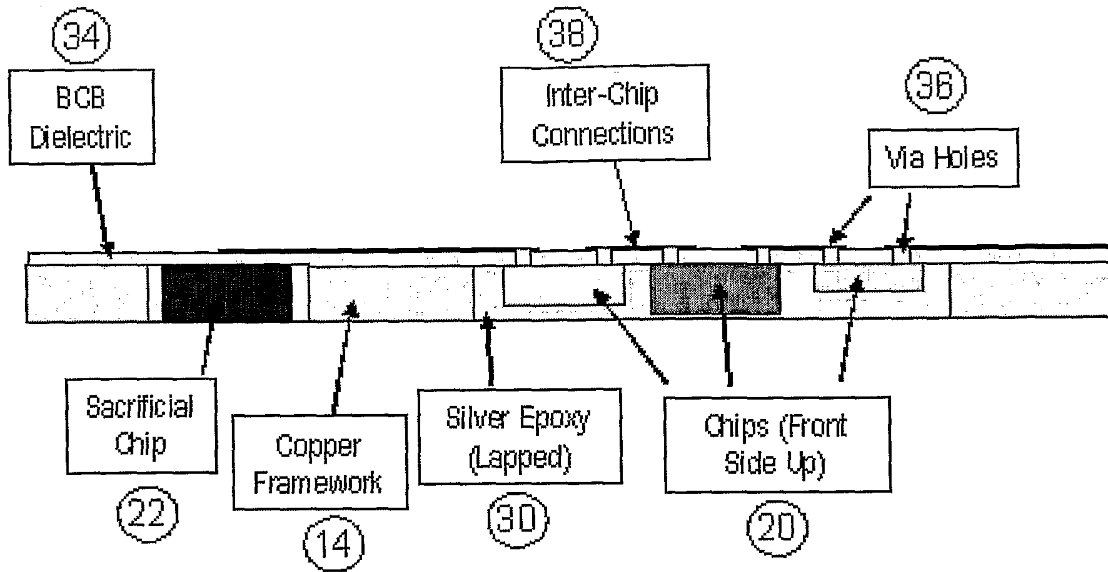


FIGURE 13

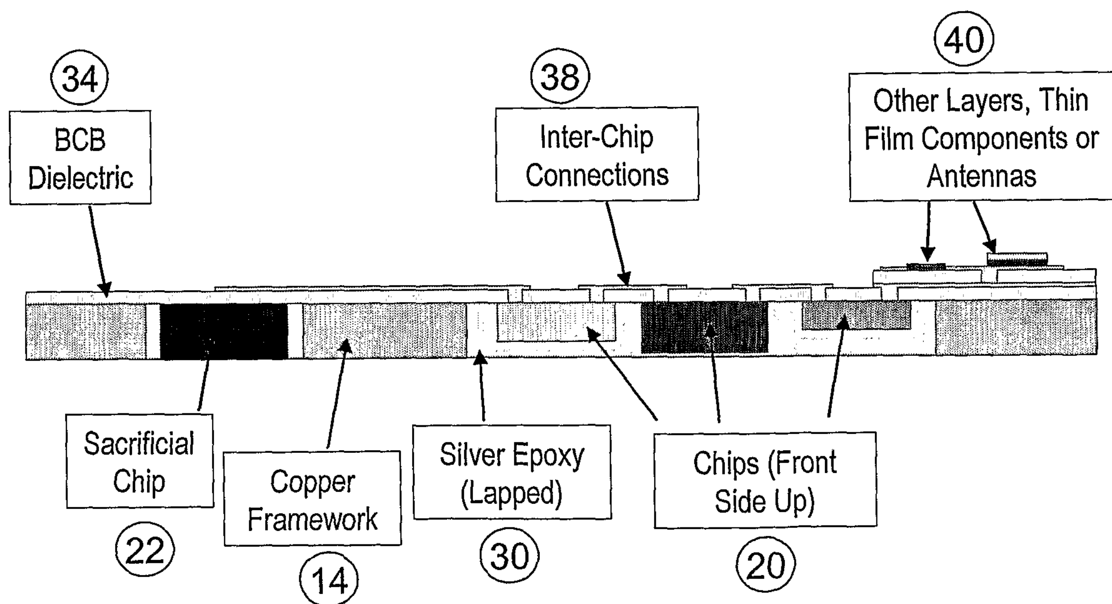


FIGURE 14

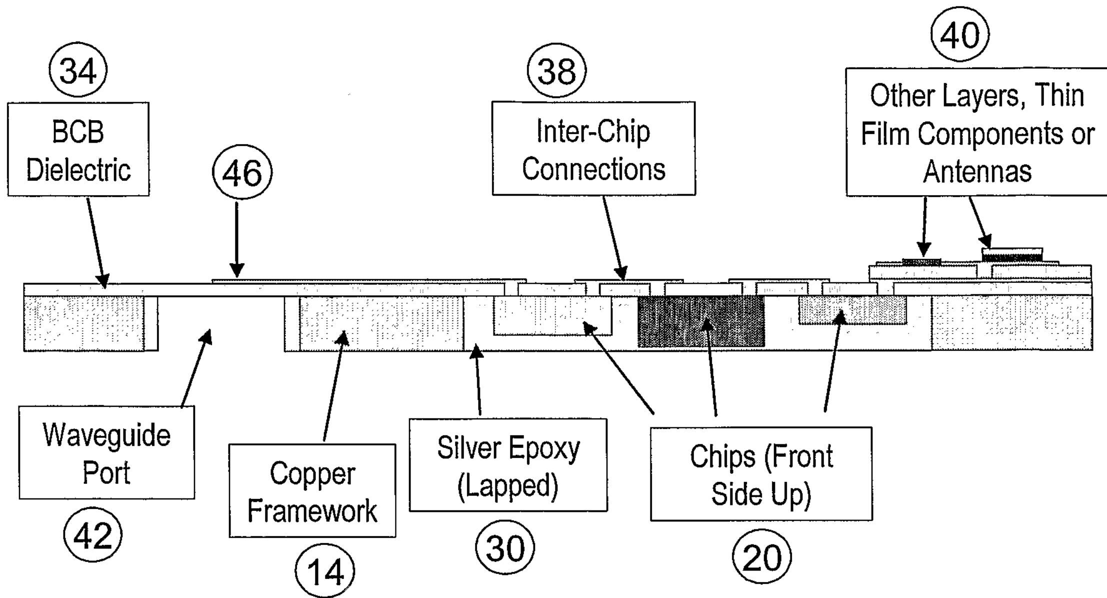
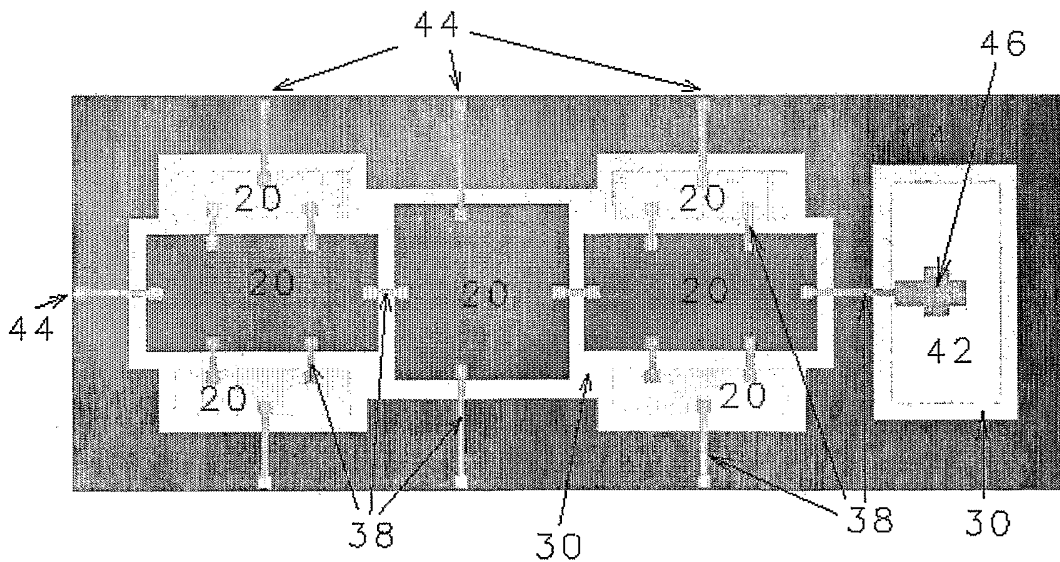


FIGURE 15

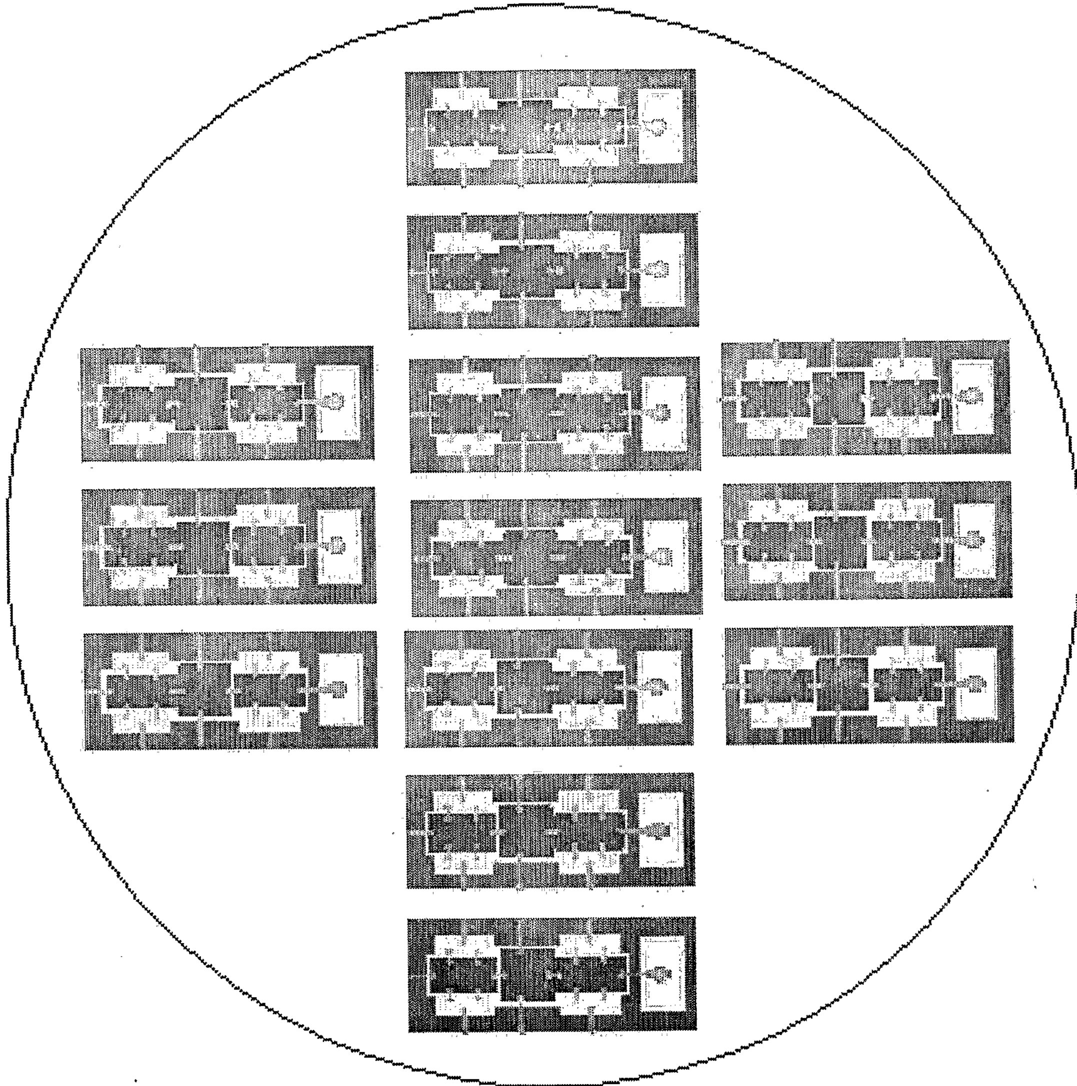


Basic Multi-Chip Module Top View

44: Connector or other input/output to MCM

46: Waveguide probe (Waveguide input/output to MCM) (extension of 38, i.e. conductive metal printed on dielectric)

FIGURE 16



Basic MCM Wafer Top View
Many MCMs are processed at the same time as a wafer, and then diced into separate modules.

FIGURE 17

INTERNATIONAL SEARCH REPORT

International application No.
PCT/AU2006/000438

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl.

H05K 1/18 (2006.01) *H01L 23/28* (2006.01) *H05K 1/02* (2006.01)
H01L 23/16 (2006.01) *H01L 25/065* (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
DWPI, JAPIO

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 1087434 A2 (NEC CORP) 28 March 2001 See figures	1-34
X	FR 2818804 A1 (THOMSON CSF SA) 28 June 2002 See figures	1-34
A	US 2004017668 A1 (SIEGEL et al) 29 January 2004 See figures	

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Date of the actual completion of the international search	Date of mailing of the international search report
19 May 2006	16 JUN 2006
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This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member			
EP	1087434	JP	2001094003	US	6518093
FR	2818804				
US	2004017668	US	6769174	US	2004200062

Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.

END OF ANNEX