(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
23 December 2004 (23.12.2004)

PCT

(10) International Publication Number
WO 2004/112127 A1

(51) International Patent Classification[7]: H01L 21/84, 27/12, 21/336

(21) International Application Number: PCT/EP2004/006498

(22) International Filing Date: 16 June 2004 (16.06.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/463,023 16 June 2003 (16.06.2003) US

(71) Applicant *(for all designated States except US)*: **INFINEON TECHNOLOGIES AG** [DE/DE]; St.-Martin-Str. 53, 81669 Munich (DE).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: **KANG, Woo-Tag** [KP/US]; 2013 Walden Glade Run, Apex, NC 27523 (US).

(74) Agent: **EPPING HERMANN FISCHER PATENTANWALTSGESELLSCHAFT MBH**; Ridlerstrasse 55, 80339 Munich (DE).

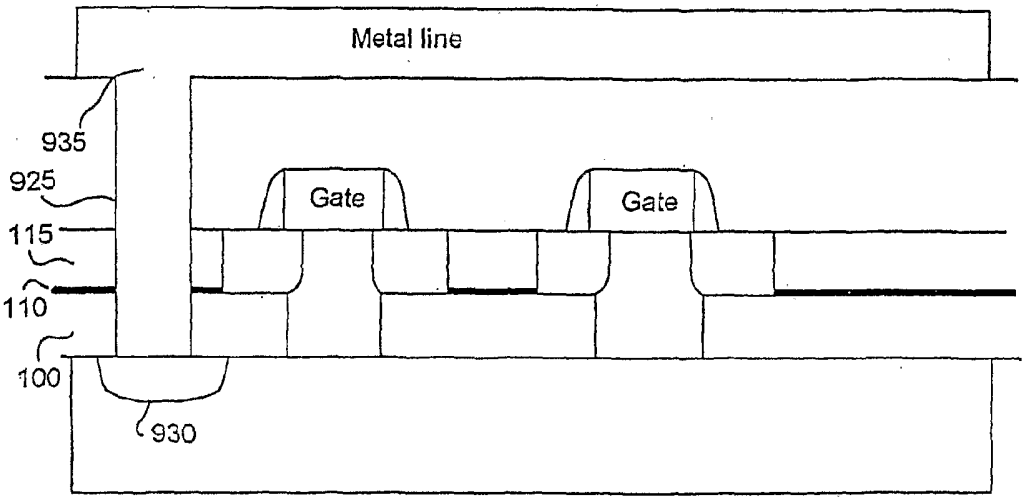
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

**Published:**
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

(54) Title: SOI SHAPED STRUCTURE




(57) Abstract: A silicon on insulator shaped structure formed to reduce floating body effect comprises a T-shaped active structure and a body contact for back bias. Etching a T-shape through two layers of oxide will form the T-shaped active areas. A back bias is formed when a metal line is dropped through the SOI structure and reaches a contact plug. This contact plug is doped with N+ or P+ dopant and is embedded in a Si sub-strate. The T-active shaped structure is used to reduce the short channel effects and junction capacitance that normally hinder the effectiveness of bulk transistors. The back bias is used as a conduit for generated holes to leave the SOI transistor area thus greatly reducing the floating effects generally associated with SOI structures.

WO 2004/112127 A1

# SOI Shaped Structure

## Field of the Invention

The present invention relates generally to field effect transistors and, in particular, to field effect transistors with silicon on insulator ("SOI") structures.

## Background

Over time, SOI has become a popular design in field effect transistor ("FET") technology. In prior years, the FET's large junction capacitance hindered its performance. For example, in NMOS transistors where doped N regions are embedded in silicon P substrates, depletion regions form in the substrate. These depletion regions are located at each area between the P and N regions (called a PN junction) and are characterized by a depleted number of majority carriers. Consequently, depletion regions must be charged with majority carriers before the NMOS can properly work. Recharging the depletion region with majority carriers can take so long that the time to charge the depletion region exceeds the time to switch the NMOS to the desired voltage. SOI rectifies this problem because it places a sheet of insulation between the P and N regions, thus eliminating the large depletion region and junction capacitance. Compared to a regular bulk transistor, SOI is advantageous to the extent it has low junction leakage, junction capacitance, and power consumption.

Nevertheless, SOI also has disadvantages. One drawback to the SOI structure is the floating body effect, which can degrade current flow. The floating body effect occurs when, at NMOS operation, electrons in the source terminal are drawn to a high electric field in the drain terminal and experience impact ionization. Impact ionization occurs when high speed carriers, like electrons, collide with atoms in a semiconductor lattice, like atoms in a drain. The impact ionization

creates electron-hole pairs in the drain region. The low potential active Si bottom region draws these generated holes towards its bottom region. In a bulk transistor, the holes collecting at the Si bottom region exit through a low potential body contact. But, in an SOI structure, insulator separates the active Si region from the body. Therefore, without any body contact, generated holes collect at the active Si bottom and increase the potential of the active Si bottom. This creates a forward-bias between the source and the active Si bottom. As a result of the forward bias, electron injection occurs from the source to the active Si bottom. This, in turn, creates a parasitic NPN bipolar transistor junction, which lowers the threshold voltage and drain breakdown voltage of the NMOS.

An unmet need therefore exists for creating a body contact in a SOI structure that is useable as an exit for generated holes.

## Summary of the Invention

Structures according to the present invention provide a solution to the problems described above by combining an SOI structure with a body contact able to flush out generated holes collecting at the Si bottom region.

In one embodiment according to the present invention, a method is provided for fabricating an SOI active structure on a wafer in an integrated circuit where an interruption is formed in the insulator and silicon is deposited in the interruption.

Another embodiment according to the present invention provides for an SOI active structure on a wafer in an integrated circuit in which an interruption is formed in the insulator and a body contact is coupled to the insulator and is in communication with the interruption.

In yet another embodiment according to the present invention, an SOI active structure on a wafer in an integrated circuit has an SOI T-shaped structure. It also provides a means for producing a back bias formed in the SOI T-shaped structure in which extra generated holes may exit a transistor.

Another embodiment according to the present invention provides for a transistor in an integrated circuit having a SOI structure with a gate, a source, and a drain. The drain is in communication with the source via a channel. The insulator has an interruption adjacent the channel through which excess change can be conducted away from the channel.

Brief Description of Drawings

Figure 1 is a diagram showing nitride and oxide layers deposited on a wafer to form an intermediate structure in an embodiment of the present invention.

Figure 2 is a diagram showing photoresist deposited over the intermediate structure of Figure 1, and also showing the photoresist having been etched to form a further intermediate structure, in an embodiment of the present invention.

Figure 3 is a diagram showing the intermediate structure of Figure 2, having been further etched, to produce another intermediate structure, in an embodiment of the present invention.

Figure 4 is a diagram showing photoresist deposited over the intermediate structure of Figure 3, a further etch of the deposited photoresist, and a further intermediate structure, in an embodiment of the present invention.

Figure 5 is a diagram showing the intermediate structure of Figure 4 having been further etched, to produce another in-

termediate structure, in an embodiment of the present invention.

Figure 6 shows an oxidation over the intermediate structure in Figure 5, and a further intermediate structure in an embodiment of the present invention.

Figure 7 shows Si growth over the intermediate structure of Figure 6, and a further intermediate structure in an embodiment of the present invention.

Figure 8 is a diagram showing a smoothing of the intermediate structure of Figure 7, an oxidation of the intermediate structure of Figure 7, and a further intermediate structure in an embodiment of the present invention.

Figure 9 is a diagram showing an implantation of a well in the intermediate structure of Figure 8, and a further intermediate structure in an embodiment of the present invention.

Figure 10 shows formation of a gate over the intermediate structure of Figure 9, and a further intermediate structure in an embodiment of the present invention.

Figure 11 shows implantation of a source or drain in the intermediate structure of Figure 10, and a further intermediate structure in an embodiment of the present invention.

Figure 12 is a diagram showing formation of gate spacer and dielectric, deposition of oxide over the gate structure, and formation of a body contact in the intermediate structure of Figure 11, and a further intermediate structure, in an embodiment of the present invention.

Figure 13 is a diagram showing implantation of a contact plug in the intermediate structure of Figure 12, and a further in-

termediate structure in an embodiment of the present invention.

Figure 14 is a diagram showing deposition of metal in the intermediate structure of Figure 13 to produce a back bias in an embodiment of the present invention.

Figure 15 shows another embodiment of the present invention.

Figure 16 is a diagram showing an alternative embodiment of the present invention.

Detailed Description

Figure 1 shows a first step in an embodiment of a method, and an intermediate IC structure, according to the present invention. This and the subsequently related steps describe one embodiment of a method for creating an SOI-shaped structure according to the present invention. A first layer of oxide 100 is deposited over a Si substrate 105. In this example, but without limitation, the thickness of oxide layer 100 is 1000 Å (Ångstrøm). After the first oxide layer is set, a layer of nitride ("SiN") 110 having, in this example, but without limitation, a width of 100 Å is deposited over oxide layer 100. Acting as a stopping liner, SiN layer 110 stops the oxide etch process and prevents it from reaching material underneath SiN 110. SiN 110 permits formation of a vertical T-shaped SOI structure in this embodiment. In a final step of Figure 1, a second layer of oxide 115, in this embodiment having with a width of 1000 Å , is deposited over the nitride layer.

Figure 2 shows the intermediate structure of Figure 1, where that intermediate structure has been etched. Photoresist 200 is deposited over oxide layer 115, after which active photolithography, as known in the art, is used to etch holes in photoresist 200. Photolithography, as known in the art, is

used to create openings in the photoresist that can eventually be used for Si epitaxial growth, for example. An oxide etch is then performed to etch away any oxide not underneath the photoresist. As described above, the oxide etch cannot penetrate SiN layer 110; thus only oxide layer 115 is etched. Oxide layer 100, located underneath nitride layer 110, remains unaffected.

Figure 3 is a diagram showing the intermediate structure of Figure 2 following further etching. Photoresist layer 200 has been etched completely away, leaving behind a patterned oxide layer 115. Photoresist can be removed by use of a so-called ashing process.

In Figure 4, a layer of photoresist 400 has been deposited over the intermediate structure of Figure 3. Openings in photoresist 400 have been created by a photolithographic step, leaving areas of SiN layer 110 exposed.

Figure 5 shows the intermediate structure of Figure 4 where that intermediate structure has been etched. A nitride etch is performed on the nitride 110 layer exposed by the procedure of Figure 4, leaving portions of oxide layer 100 exposed. Oxide etching is then performed to etch that portion of oxide layer 100 that is exposed. No other layer is affected, because photoresist 400 blocks the oxide etch from reaching materials located underneath photoresist 400. Ashing processes are then performed on photoresist 400 to remove the remaining photoresist. Following the ashing process, a nitride etch is performed to remove any portion of nitride layer 110 exposed after photoresist 400 is removed. After the nitride etch, clean active T-shaped areas 500 and 502, according to an aspect of the present invention, remain in the wafer.

Referring to Figure 6, a thermal oxidization (not deposition) step is performed according to known methods. The T-shaped

holes or interruptions 500, 502 will eventually be filled with Si-epitaxy; however, for Si epitaxial growth, a clean and damage-free surface is preferred. It is possible that, while etching oxide layer 100, the oxide etch could damage the surface at the bottom of the T-shaped interruptions 500, 502. To properly cure the Si surface at the bottom of oxide layer 100, thermal oxidation of the surface may be performed, followed by removal of the resulting thin thermal oxide 600. Thin thermal oxide 600, in this example, but without limitation is about 100 Å wide.

Figure 7 shows Si epitaxy regions grown over the T-shaped interruptions 500, 502 in Figure 6 to form T-shaped transistor structures 700, 702.

Structures formed using Si epitaxy may grow in an uneven manner. Thus, in Figure 8, chemical mechanical polishing ("CMP") or other suitable methods may be used to even out any non-even portions of structures 700, 702 from the intermediate structure shown in and described with reference to Figure 7. CMP processes ensure a smooth and even Si surface. After structures 700, 702, are smoothed and evened, a thermal oxidation step is performed over the Si epitaxy. The thermal oxidation forms oxide layers 800, 802, which, in this example, but without limitation, are about 100 Å in thickness. This oxidation is used to cure Si surface damage which can occur during the CMP process.

Referring to Figure 9, after the CMP and oxide processes shown in Figure 8, a well 900 is implanted into substrate 105 (not shown). Well 900 is used for CMOS processes, for example, to have NFET and PFET isolation. For a PFET, an N well is used; whereas for an NFET, a P well is used.

To form a transistor, a gate is placed over the T-shaped structures. Therefore, in the illustrated embodiment, as

shown in Figure 10, gates 902, 904 are formed according to known methods, over the T-shaped structures 700, 702.

Turning to Figure 11, sources and drains 910, 912 (or vice versa) are formed, according to known methods, e.g., by implantation on either side adjacent to gates 902, 904. With the implantation of a source and a drain, e.g., 910, 912, T-shaped transistor structures 700, 702 are formed according to the present invention.

Figure 12 shows the formation of gate spacer layers 915 and dielectric layers in the illustrated embodiment. Lightly doped drains ("LDD") are used in many transistors because LDDs reduce transistors' short channel effects. Nevertheless, LDDs of separate transistors should be electrically isolated from each other. Gate spacers 915 electrically isolate separate LDDs from each other. A third layer of oxide 920 is then deposited over the transistors with gate spacer and dielectric layers.

According to an aspect of the present invention, a back bias is created in order to remove extra holes that collect at the bottom of T-shaped structure 500, 502. Therefore, as shown in Figure 12, body contact 925 is formed, extending to Si substrate 105 (as shown in Figure 1). To form body contact 925, a layer of photoresist is first deposited over oxide layer 920. Photolithography, as known in the art, is then used to open a hole in the photoresist. A dry oxide etch is applied to oxide layer 920, etching out any portion of oxide layer 920 and oxide layer 115 not underneath the photoresist. The nitride stopper layer 110 is then etched, followed by an oxide etch of oxide layer 100, yielding body contact 925 that reaches Si substrate 105 (as shown in Figure 1).

In Figure 13, contact plug 930 is implanted, as shown. Contact plug 930 is implanted with N+ dopant for an N well and P+ dopant for a P well. Thermally generated holes in the

drains (910 or 912) exit through contact plug 930, thus addressing, and preferably alleviating, the floating body effect.

Figure 14 shows a process for completing body contact 925 in an embodiment of the invention, in which a conductor, such as metal line 935, is deposited to complete body contact 925. Also, metal line 935 may be deposited over oxide layer 920. Metal line 935, which forms body contact 925 and contact plug 930, in this embodiment, is inside the N+ or P+ region, leading to lower contact leakage current.

In another embodiment of this aspect of the present invention, formation of an "easy" body contact is shown in Figure 15. In Figure 14, the contact plug 930 was deep in the body contact and, therefore, a contact plug implantation was needed. But the embodiment shown in Figure 15 has a contact plug that is shallow. A contact plug implantation is thus not necessary, since the N+ or P+ contact plug implantation is simultaneously formed during the N+ or P+ source/drain implantation. Instead, Si is grown, for example using epitaxy, in body contact 925'. Furthermore, in a preceding formation step analogous to the one in Figure 2, where the T shaped structures are initially formed, an additional hole is formed, as shown in Figure 15. A process analogous to the process shown in Figures 3 through 9 is carried out, and a lower portion of body contact 925' is formed with Si as shown in Figure 15, for example through epitaxy processes, and an upper portion of a body contact 925' is also formed with a conductor, such as metal line 935, in a process analogous to that shown in Figures 10 to 14. For contact plug implantation, the additional hole in the Si surface in Figure 15 is implanted with N+ or P+ when the N+ or P+ source/drain implantation is formed after the gate process. This additional Si epitaxial hole process reduces the contact plug implantation step and makes an easy contact process due to the shallow contact hole.

Figure 16 shows another embodiment according to the present invention. In this embodiment, both an easy body contact 925' and a trench capacitor storage poly 940 are used. Storage poly 940 has a trench storage poly insulator 941 and a trench capacitor oxide 943. The top of the storage poly 940 is attached to a transistor source or drain region 910, 912. To achieve good contact attachment between the N type source/drain 910, 912 of the cell transistor 945, 947 and a N+ storage poly 940, the top of trench capacitor storage poly 940 has a high concentration of N-type dopant. This high concentration of N-type dopant degrades the cell transistor's short channel effects because of N-dopant source/drain depletion region increase by the lateral diffusion of N-dopant from the attached high N-dopant trench storage poly region 965 to channel center region 950. In this embodiment according to the present invention, the N-dopant diffusion is reduced since an oxide region 952, 954 blocks N-dopant diffusion from the attached high N-dopant trench capacitor region 965. Therefore, the short channel effects are greatly improved.

While the invention has been particularly shown and described with reference to particular embodiments, those skilled in the art will understand that various changes in form and details may be made without departing form the spirit and scope of the invention as set forth in the appended claims.

What is claimed is:

1. A method of fabricating a silicon on insulator active structure on a wafer in an integrated circuit, the method comprising the steps of:

forming an interruption in the insulator; and

depositing silicon in the interruption formed in the insulator.

2. The method according to claim 1, further comprising forming a second interruption in the insulator.

3. The method according to claim 2, further comprising forming a body contact in communication with the second interruption.

4. The method according to claim 3, wherein the body contact and second interruption comprise metal.

5. The method according to any of claims 1 to 4, further comprising:

depositing a trench capacitor in the insulator, wherein the trench capacitor is in communication with the deposited silicon; and

depositing at least on oxide region in the silicon.

6. The method according to claim 3, further comprising depositing silicon in the second interruption.

7. The method according to claim 6, wherein the body contact comprises metal.

8. The method according to any of claims 1 to 7, wherein the deposited silicon comprises a T-shape.

9. An integrated circuit comprising:

a silicon-on-insulator active structure on a wafer, the insulator having an interruption formed therein; and

a body contact coupled to the insulator and in communication with the interruption.

10. The circuit according to claim 9, further comprising a contact plug in the wafer.

11. The circuit according to claim 10, wherein the body contact comprises a conductor.

12. The circuit according to claim 11, wherein the conductor comprises a metal layer.

13. The circuit according to claim 10, further comprising silicon residing in the interruption.

14. The circuit according to claim 13, wherein the body contact comprises a conductor.

15. The circuit according to claim 14, where conductor comprises a metal layer.

16. The circuit according to any of claims 9 to 15, wherein the interruption comprises a cross-section having T-shape.

17. The circuit according to any of claims 9 to 16, further comprising a trench capacitor in communication with the interruption.

18. The circuit according to claim 10, wherein the contact plug comprises one of the group consisting of N+ and P+ doping.

19. A silicon on insulator active structure on a wafer in an integrated circuit, comprising:

a silicon on insulator T-shaped structure; and

means for producing a back bias formed in the silicon on insulator T-shaped structure in which extra generated holes may exit a transistor.

20. A transistor in an integrated circuit having a silicon on insulator active structure, comprising:

a gate;

a source;

a drain in communication with the source via a channel;

the insulator having an interruption adjacent the channel through which excess charge can be conducted away from the channel.

21. The transistor according to claim 20, further comprising a body contact, in electrical communication with the interruption in the insulator, for conducting excess charge distally from the channel.

22. The transistor according to claim 20 or 21, further comprising a second interruption in the insulator through which excess charge escapes.

23. The transistor according to claim 22, further comprising a metal line which forms the body contact and the second interruption.

24. The transistor according to any of claims 20 to 23 further comprising:

a trench capacitor, wherein the trench capacitor is in communication with at least one of the source and drain; and

oxide, wherein the oxide is dispersed in at least one of the source and drain.

25. The transistor according to 22 further comprising silicon which resides in the second interruption.

26. The transistor according to 25 further comprising a metal line which resides in the body contact.

27. The transistor according to any of claims 20 to 26 wherein the silicon on insulator structure comprises a T-shape.

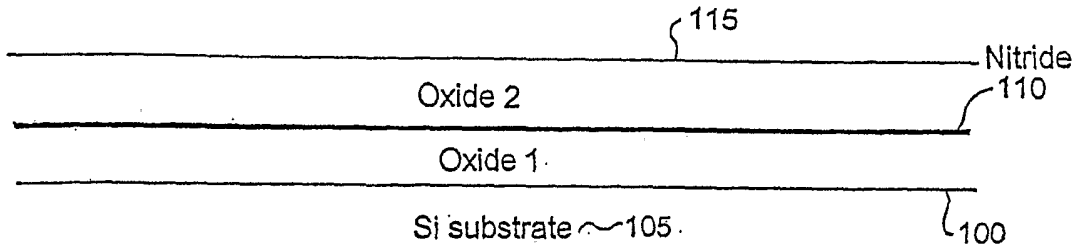



FIG. 1

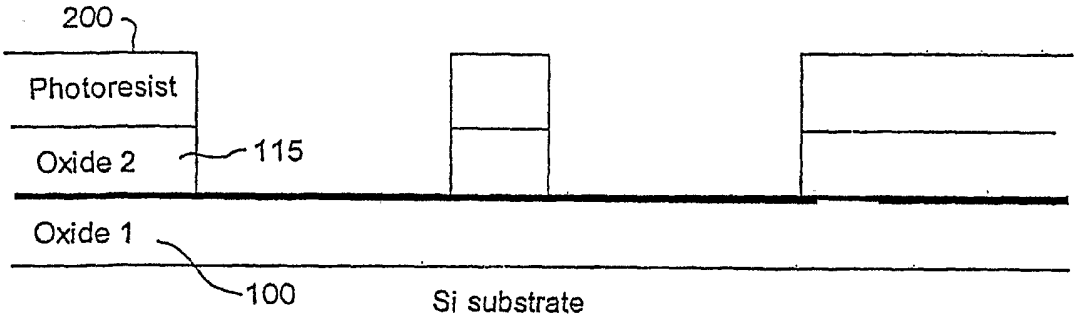



FIG. 2

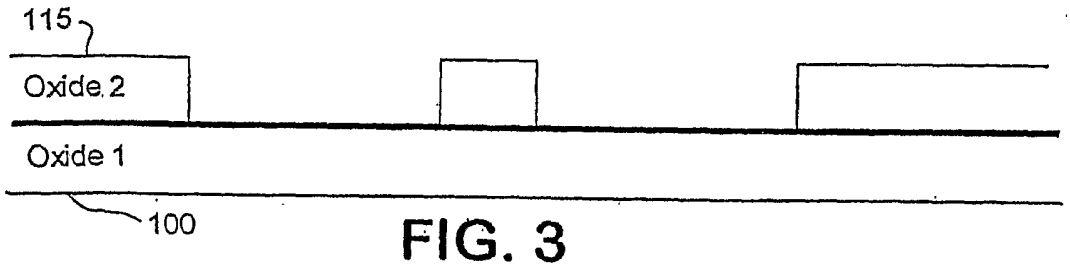



FIG. 3

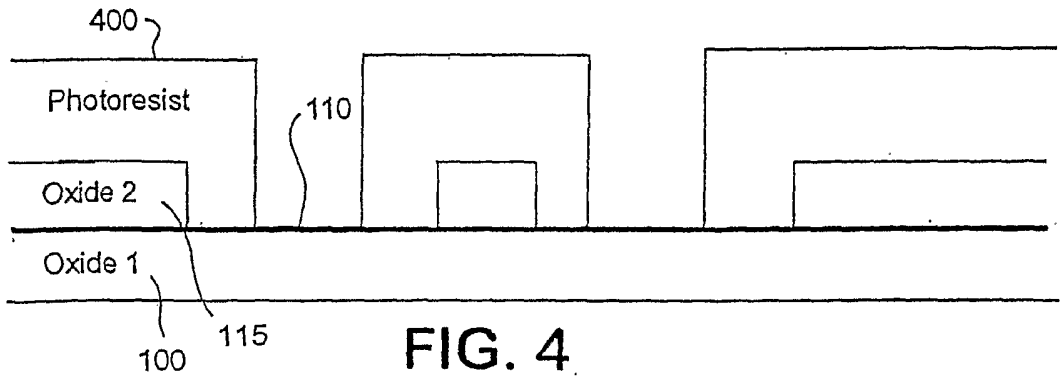



FIG. 4

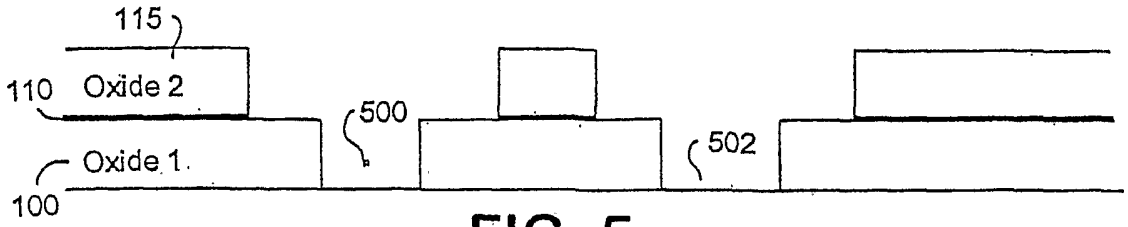



FIG. 5

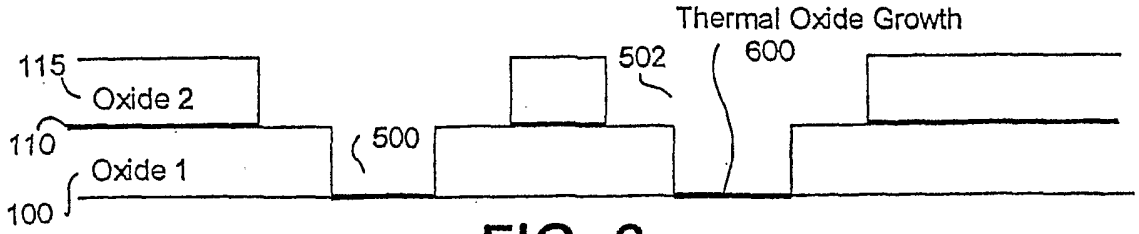



FIG. 6

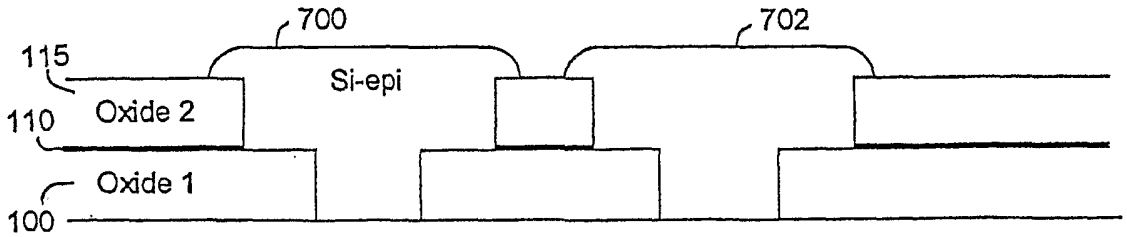



FIG. 7

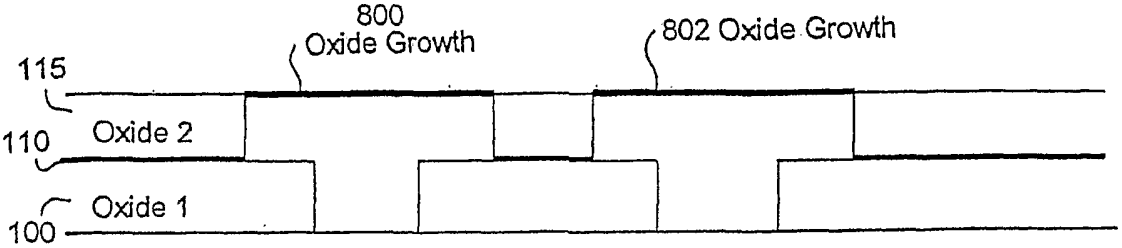



FIG. 8

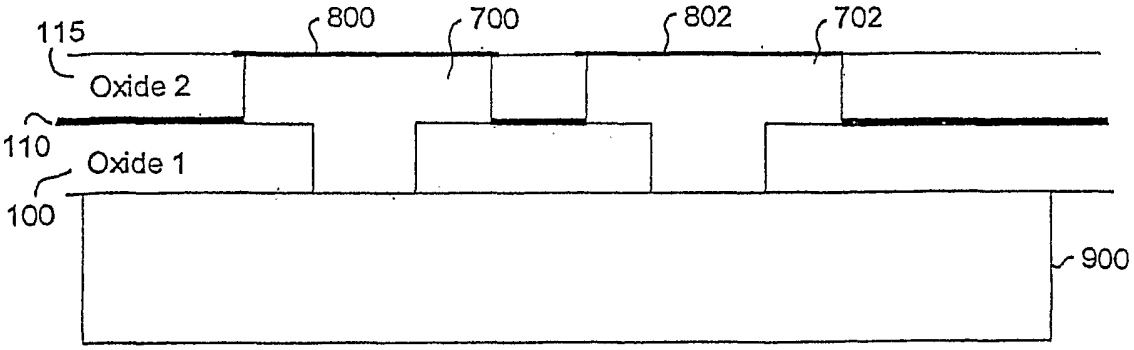



FIG. 9

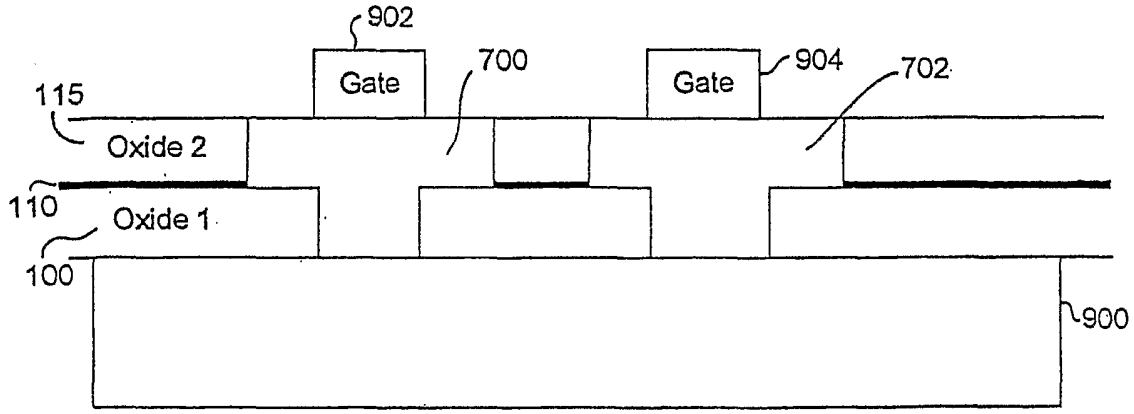



FIG. 10

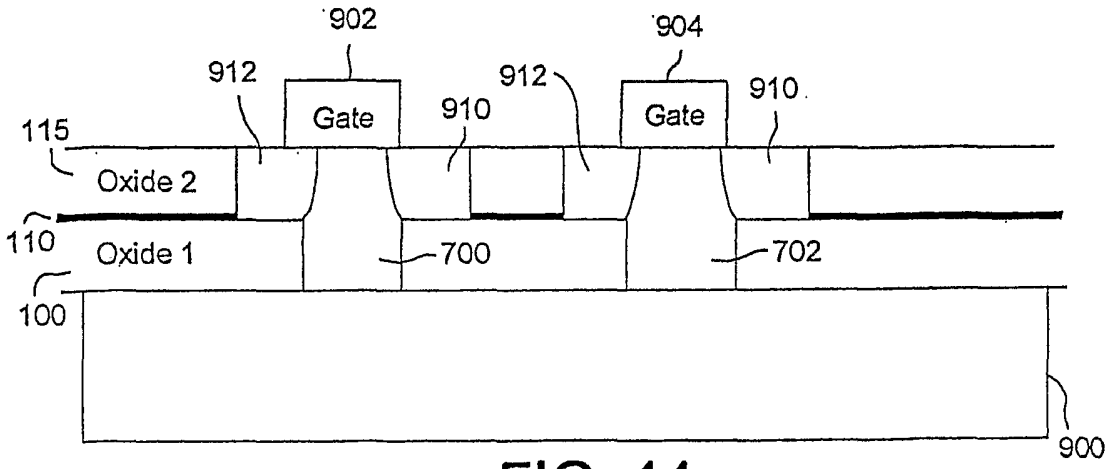



FIG. 11

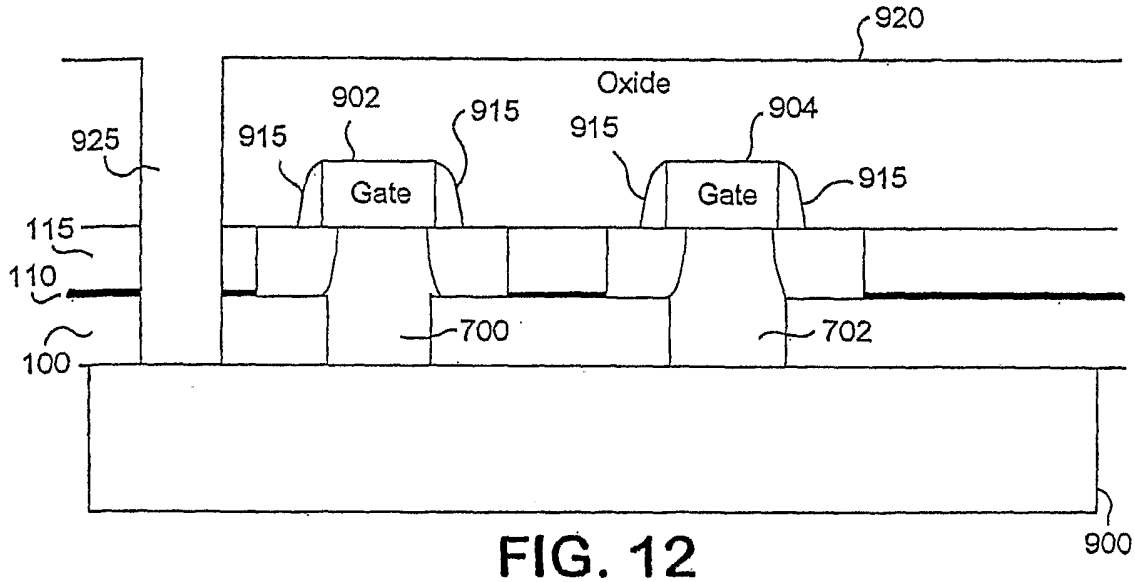

920
Oxide
902
915
915
915
904
925
Gate
Gate
915
115
110
700
702
100
900

FIG. 12

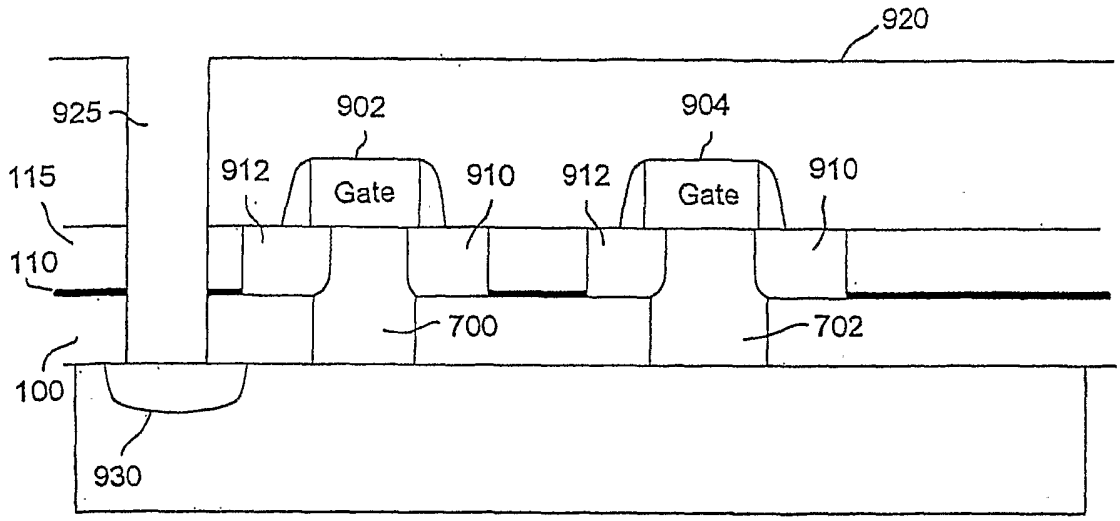

920
925
902
904
912
Gate
910
912
Gate
910
115
110
700
702
100
930

FIG. 13

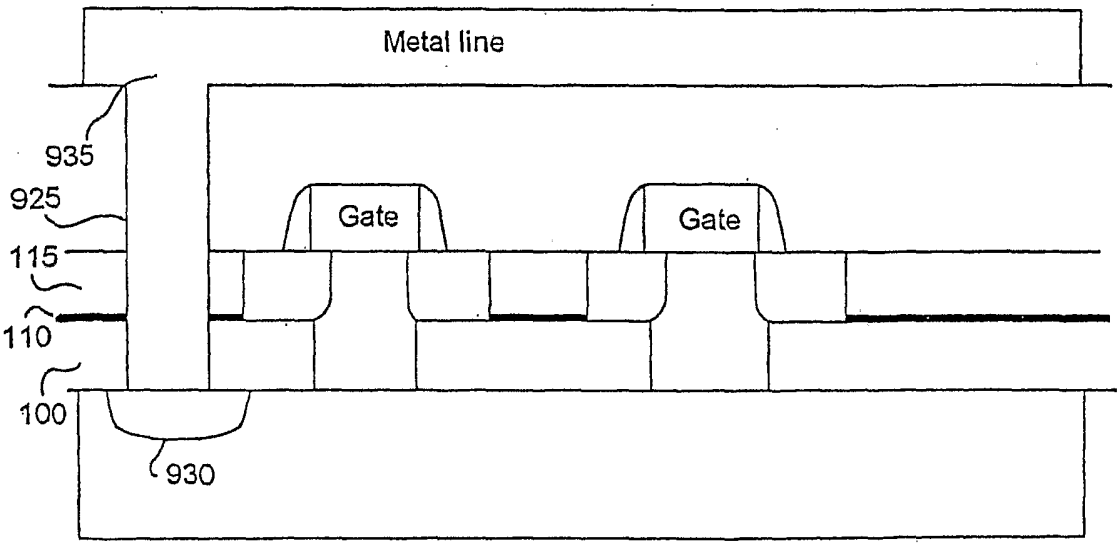

Metal line
935
925
Gate
Gate
115
110
100
930

FIG. 14

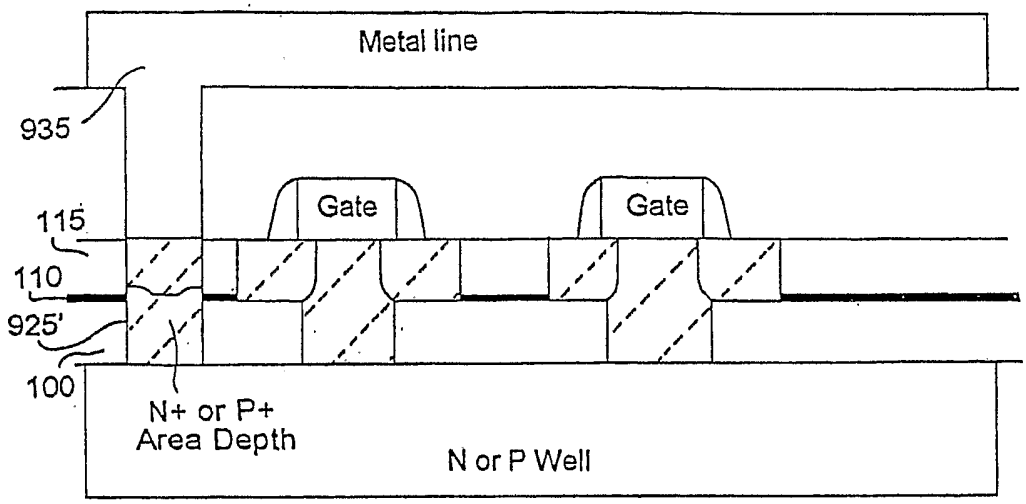

Metal line
935
Gate
Gate
115
110
925'
100
N+ or P+
Area Depth
N or P Well

FIG. 15

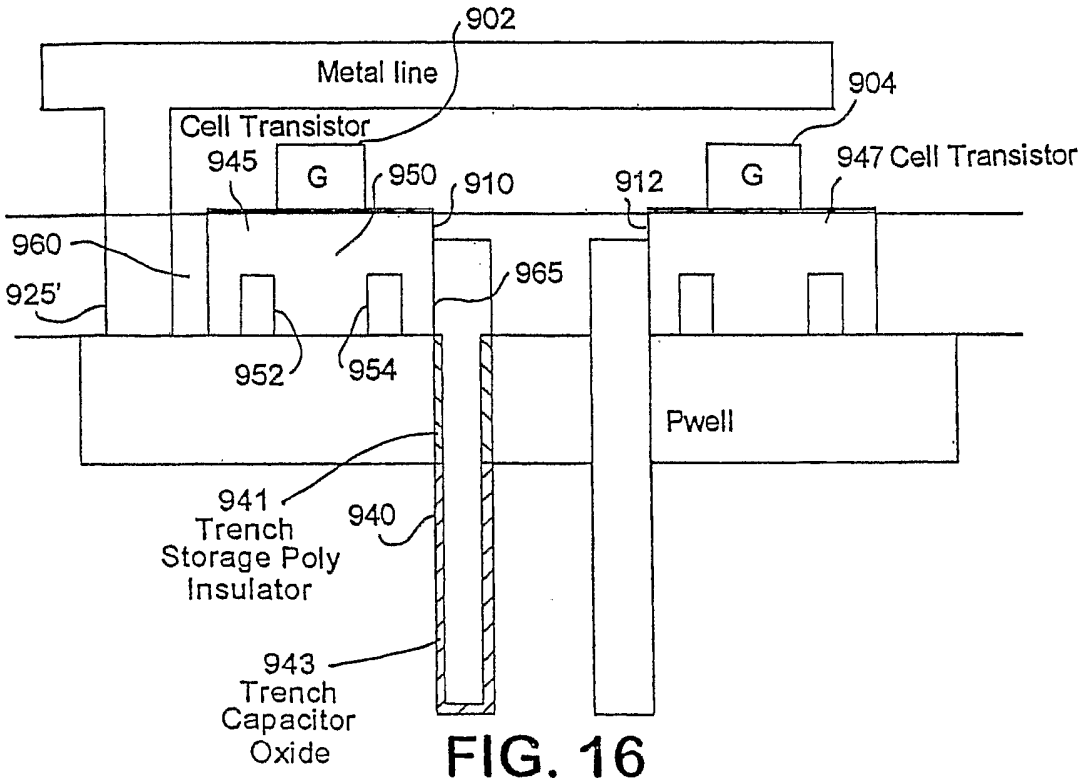

902
Metal line
904
Cell Transistor
945
G
950
910
912
G
947 Cell Transistor
960
925'
965
952
954
Pwell
941
Trench
Storage Poly
Insulator
940
943
Trench
Capacitor
Oxide

FIG. 16

# INTERNATIONAL SEARCH REPORT

International Application No
PCT/EP2004/006498

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/84 H01L27/12 H01L21/336

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category ° | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | US 2002/163041 A1 (KIM MIN-SU) 7 November 2002 (2002-11-07) | 1-4, 6-16, 18-23, 25-27 |
| Y | paragraph '0006! - paragraph '0042!; figures 2-9 | 5,17,24 |
| X | US 6 429 099 B1 (CHRISTENSEN TODD ALAN ET AL) 6 August 2002 (2002-08-06) | 1-4, 6-16, 18-23, 25-27 |
| Y | column 1, line 20 - column 4, line 17 column 4, line 35 - column 5, line 32 figures 3-6 | 5,17,24 |

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 26 October 2004 | 03/11/2004 |

| Name and mailing address of the ISA | Authorized officer |
|---|---|
| European Patent Office, P.B. 5818 Patentlaan 2<br>NL – 2280 HV Rijswijk<br>Tel. (+31–70) 340–2040, Tx. 31 651 epo nl,<br>Fax: (+31–70) 340–3016 | Bernabé Prieto, A |

Form PCT/ISA/210 (second sheet) (January 2004)

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

| Category ° | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | PATENT ABSTRACTS OF JAPAN<br>vol. 1998, no. 02,<br>30 January 1998 (1998-01-30)<br>-& JP 09 283766 A (MATSUSHITA ELECTRIC IND CO LTD), 31 October 1997 (1997-10-31) | 1-16,<br>18-23,<br>25-27 |
| Y | abstract<br>figure 2 | 5,17,24 |
| X | WO 01/43198 A (IBM ; INFINEON TECHNOLOGIES CORP (US)) 14 June 2001 (2001-06-14)<br><br>page 8, paragraph 3 - page 33, paragraph 1<br>figures 19,32 | 1-3,<br>9-11,13,<br>14,16,<br>18-23,<br>25,27 |
| X | US 6 174 754 B1 (LEE JIN-YUAN ET AL)<br>16 January 2001 (2001-01-16)<br><br>column 6, line 56 - column 9, line 58;<br>figures 7-12 | 1,8,9,<br>16,19,<br>20,27 |
| Y | US 5 593 912 A (RAJEEVAKUMAR THEKKEMADATHIL V)<br>14 January 1997 (1997-01-14)<br>abstract<br>figure 1 | 5,17,24 |
| Y | US 5 606 188 A (BRONNER GARY B ET AL)<br>25 February 1997 (1997-02-25)<br>figure 6 | 5,17,24 |
| X | US 6 284 594 B1 (CHU SHAO-FU SANFORD ET AL) 4 September 2001 (2001-09-04)<br>the whole document<br>figure 9 | 1,9,19,<br>20 |

# INTERNATIONAL SEARCH REPORT

International Application No
PCT/EP2004/006498

| Patent document cited in search report | Publication date | Patent family member(s) | Publication date |
|---|---|---|---|
| US 2002163041 A1 | 07-11-2002 | KR 2001095471 A<br>US 2001025991 A1 | 07-11-2001<br>04-10-2001 |
| US 6429099 B1 | 06-08-2002 | US 2002030229 A1 | 14-03-2002 |
| JP 09283766 A | 31-10-1997 | NONE | |
| WO 0143198 A | 14-06-2001 | WO 0143198 A2 | 14-06-2001 |
| US 6174754 B1 | 16-01-2001 | NONE | |
| US 5593912 A | 14-01-1997 | JP 2994239 B2<br>JP 8116037 A<br>KR 187868 B1<br>US 5869868 A | 27-12-1999<br>07-05-1996<br>01-06-1999<br>09-02-1999 |
| US 5606188 A | 25-02-1997 | NONE | |
| US 6284594 B1 | 04-09-2001 | SG 87932 A1 | 16-04-2002 |