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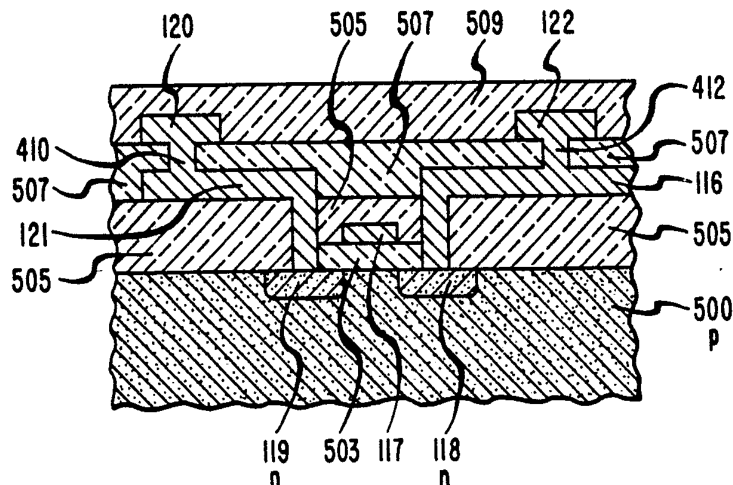

(57) Abstract

A region of a semiconductor MOS integrated circuit consists essentially of mutually parallel and spaced-apart cell rows with three successive levels of interconnections: (1) a first level (117), typically polysilicon, in which conducting stripes are confined essentially to areas overlying the cell rows; (2) a second level (116, 121), typically aluminum, in which conducting stripes run perpendicular to the cell row direction; and (3) a third level (120, 122), typically aluminum, in which conducting stripes run parallel to the row direction. In this way, the lengths of all (relatively high resistivity) first level interconnections can be made relatively short, without either crowding or complicating the layout of the second and third levels.

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THREE-LEVEL INTERCONNECTION SCHEME FOR INTEGRATED CIRCUITS

1. Field of the Invention

This invention relates to semiconductor
5 integrated circuits and more particularly to schemes for the interconnection of MOS (metal oxide semiconductor) devices therein, such as three level interconnection schemes with a single level of polysilicon stripes and two levels of metal stripes.

10 ## Background of the Invention

In prior art, semiconductor integrated circuits have typically taken the form of a plurality of MOS (metal oxide semiconductor) transistors, numbering as high as several hundred thousand, all integrated at a
15 top planar major surface of a silicon chip. Electrical interconnections between transistors, as mandated by the desired electrical circuit to be achieved, have typically taken the form of two "levels" of interconnections, i.e., electrical conducting stripes
20 running along two mutually insulated essentially planar surfaces that are mutually parallel to, and insulated from, the top planar surface of the chip.

In more recent prior art, as integrated circuits have increased greatly in complexity, the
25 problem of crowding of interconnections has increased in severity, and the scheme of two levels of interconnection has been modified by adding a third level of interconnections--for example, metal stripes, running in the direction perpendicular to the underlying
30 second level stripes, and hence running parallel to the first level stripes. These third level stripes are separated and insulated from the second level stripes by means of a third insulating layer, located between the

second and third levels of interconnections, in which at various points there are windows that are filled with metal (plugs) to connect third level stripes with second level stripes. The third level interconnections serve
5 especially to relieve crowding on the first level and to supply relatively low resistance interconnections across relatively long distances across the chip. The resulting scheme of three level interconnections (one level of polysilicon stripes plus two levels of metal
10 stripes), however, suffers from a problem arising from the fact that a direct connection from first to third level by means of a plug in a single window running vertically from first to third level through both the second and the third insulating layers is beyond
15 present-day commercially feasible window alignment techniques. Therefore, in order to interconnect two mutually remote polysilicon stripes (e.g., stemming from two widely separated MOS devices) by a long third level metal stripe, it is necessary both to connect each of
20 the two polysilicon stripes through a separate window in the second insulating layer to a separate auxiliary second level stripe and to connect each such separate auxiliary second level stripe separately through a separate window in the third insulating layer to the
25 long third level stripe to complete an interconnection. Thus in addition to added fabrication complexity, the scheme suffers from the introduction of undesirable sidewise detours ("jogs") in the second level routing (even when the two first level polysilicon stripes to be
30 interconnected happen to be aligned along the same straight line). These detours thus add a requirement of extra auxiliary second level stripes which undesirably reduce the remaining available space in the second level and undesirably complicate the routing of the remaining
35 second level stripes required for other interconnections, whereby various routing channels must be made larger, thereby undesirably consuming extra

semiconductor area for a given circuit.

These problems are alleviated by this invention.

Summary of the Invention

5 This invention involves a semiconductor integrated circuit which has a region thereof comprising two or more mutually parallel and spaced apart elongated cell rows, all running parallel to a given direction in each of which is located a separate plurality of 10 transistors--typically, MOS transistors--integrated at a major surface of a semiconductor body, such transistors being interconnected and accessed by three levels of interconnection stripes, the first level consisting essentially of stripes for electrically connecting the 15 control electrodes of the transistors to the rest of the circuit, the second level consisting essentially of stripes running perpendicular to the given direction of the elongated rows, and the third level consisting essentially of stripes running parallel to the given 20 direction. In this way the first level stripes, typically polysilicon (doped with suitable impurities) which may or may not be overlaid with metal silicide, can be confined to cell row areas, and more importantly all the ends (terminations) of every first level stripe 25 are confined to a single cell row area: in other words, no contact between first and second level stripes occurs in any channel area.

Brief Description of the Drawing

This invention together with its features, 30 advantages, and characteristics can be better understood from the following detailed description when read in conjunction with the drawing in which:

FIG. 1 is a top view diagram of a region of a semiconductor integrated circuit with three level 35 interconnections in accordance with an illustrative embodiment of the invention;

FIG. 2 is an equivalent logic diagram of the circuitry of the region shown in FIG. 1;

FIG. 3 is a top view diagram of another region of a semiconductor integrated circuit with three level
5 interconnections in accordance with another illustrative embodiment of the invention; and

FIG. 4 is a side view in cross section of an indicated portion of FIG. 1.

First level interconnection stripes are
10 indicated by hatched lines; second level by solid lines; and third level by dashed lines. Specific cell areas are demarcated by dot-dashed lines. Connections (contacts through windows) between first and second level stripes are indicated by encircled dots;
15 connections between second level stripes and the top surface of the underlying semiconductor body are indicated simply by (unencircled) dots; and connections between second and third level stripes are indicated by crosses. Arrows indicate the directions of propagation
20 of signals during operation.

Detailed Description

As shown in FIG. 1, a region 5 of a silicon chip basically comprises a first pair of third level, parallel VDD and VSS power line stripes 11 and 12,
25 respectively, defining a first rectangular cell row 10 therebetween; a second pair of third level power line stripes, 110 and 120, respectively, defining a second row 100 therebetween; and a routing channel located in the space between the VSS power line 12 of the first
30 pair and the VDD power line 110 of the second pair. All transistors that are integrated in the upper half of each cell row are PMOS (p-channel); all in the lower half therof are NMOS (n-channel). As known in the CMOS integrated circuit art, all transistors located in the
35 region 5--as well as all those located in the other regions (not shown)--are integrated in a single silicon semiconductor body (not shown).

Input signals IN1, IN2, and IN3 are brought into the region 5 along third level stripes 91, 92, and 93, respectively, and the output signal OUT of the region 5 is brought out along second level stripe 160,
5 as well as third level stripes 161 and 162. For purposes of the illustrative embodiment, the input signal IN1 passes successively through four inverters 125, 130, 60, 70 and then is fed through a second level interconnection stripe 181 as one of three
10 inputs A1, IN2, and IN3 to a three-input NAND gate 140; whereas the input signals IN2 and IN3 are fed directly through second level interconnection stripes 182 and 183, respectively, to this same NAND gate 140 (See, also, FIG. 2).

15 In particular, the third level stripe 91 contacts a second level stripe 111 which, in turn, contacts a pair of first level stripes 112 and 117. The first level stripe 112 extends as a gate electrode over a PMOS transistor whose source region 113 is connected
20 through a second level stripe 114 to the VDD power line 110 and whose drain region 115 is connected to a second level stripe 116. The source region 113 and the drain region 115 together with the transistor channel located between them, form a PMOS-GASAD (gate and source
25 and drain) area, as known in the CMOS art.

The first level stripe 117 extends as a gate electrode over an NMOS transistor whose source region 119 is connected through a second level stripe 121 to the VSS power line 120 and whose drain
30 region 118 is contacted by the second level stripe 116. This second level stripe 116 is also connected to a third level stripe 122 which carries the output of the inverter 125. The source region 119 and the drain region 118, together with the transistor channel located
35 between them, form an NMOS-GASAD area, as known in the CMOS art.

The source and drain regions 113 and 115, respectively, are both p-type silicon semiconductor and the source and drain regions 119 and 118 respectively, are both n-type silicon semiconductor, as known in the
5 art of CMOS integrated circuit technology.

The third level stripe 122 is also connected, at its right-hand extremity, to a second level stripe 131 which delivers input for the inverter 130 much in the same manner as the second level stripe 111
10 delivers input for the inverter 125 described above, and therefore the inverter 125 will not be described in detail any further. Output from the second inverter 130 is delivered through a third level stripe 132 and thence through a second level stripe 133 into the routing
15 channel where the output is further delivered successively through a third level stripe 134 a second level stripe 135, and a third level stripe 136 to a second level stripe 51.

The second level stripe 51 contacts a pair of
20 first level stripes 61 and 62 whose extensions serve as gate electrodes for a pair of complementary MOS transistors that are interconnected to form an inverter 60 in similar manner as previously described in conjunction with the inverter 125. Output of the
25 inverter 60 is delivered along a third level stripe 63 to another inverter 70 in similar manner as previously described in conjunction with the inverter 130. In turn, output of the inverter 70 is delivered as an input signal A1 to the NAND gate 140 through the path formed
30 by third level stripe 71, a second level stripe 72, another third level stripe 73, and another second level stripe 181 to the three-input NAND gate 140.

The NAND gate 140 is composed of three PMOS and three NMOS transistors, where the PMOS transistors
35 are mutually connected in parallel and the three NMOS transistors are mutually connected in series, as required in (full) CMOS technology. In particular, the

input signal A1 is brought to the PMOS and NMOS transistor GASAD areas, respectively, along a pair of first level stripes 171 and 174; the input signal IN2, along first level stripes 172 and 175, respectively, and 5 the input signal IN3, along first level stripes 173 and 176, respectively. In particular, the first level stripe 171 has a right-hand portion serving as a gate electrode for a PMOS transistor whose source region 141 is connected by a top portion of second level stripe 151 10 to the VDD power line 110 and whose drain is supplied by diffused p-type impurity region 142 connected at its extreme right-hand portion to a second level stripe 160. This impurity region 142 also serves as source region for another PMOS transistor whose drain is supplied by 15 another p-type impurity region 143, which is also connected to the second level stripe 151, and whose gate electrode is supplied by a right-hand portion of the first level stripe 172. The impurity region 143 in turn also supplies the source of yet another PMOS transistor 20 whose drain is supplied by yet another p-type impurity region 144 connected at its extreme right-hand portion to the second level stripe 160.

The three PMOS transistors, whose gate electrodes are thus 171, 172, and 173 (by inspection of 25 FIG. 1) thus have their source-drain paths (i.e., their electrical current paths) all connected in parallel, as is desired in the PMOS portion of a three-input NAND gate. These gate electrodes thus receive as inputs the signals A1, IN2, and IN3, respectively, for these three 30 PMOS transistors. The (shared) source and drain supplied by regions 142 and 143, together with the connection of regions 142 and 144 to the second level stripe 160 and the connection of regions 141 and 143 through the second level stripe 151 to the VDD power 35 line 110, results in a structure formed by the three PMOS transistors plus their interconnections that functions as the desired PMOS portion of the three-input

NAND gate 140 with inputs A1, IN2, and IN3--the output of this NAND gate being delivered to the second level stripe 160.

For the NMOS portion of the NAND gate 140, the input signal A1 on the second level stripe 181 is also delivered to first level stripe 174, where right-hand portion serves as a gate electrode for an NMOS transistor having as its drain an n-type impurity region 145 and having as its source an n-type impurity region 146. The region 145 is connected through a second level stripe 153 and thence through a third level stripe 152 to the second level stripe 160. The impurity region 146 also serves as drain for another NMOS transistor where gate electrodes are supplied by a right-hand portion of the first level stripe 175, which brings in the input signal IN2, and whose source is supplied by another n-type impurity region 147. This n-type region 147 also serves as drain of yet another NMOS transistor whose gate electrode is supplied by first level stripe 176 which brings in the input signal IN3, and whose source is supplied by yet another n-type impurity region 148. This n-type region 148 is connected through a second level stripe 154 to the VSS power line 120.

The three NMOS transistors whose gate electrodes are 174, 175, and 176 (by inspection of FIG. 1) thus have their source-drain paths connected in series between power lines VDD and VSS, as is desired in the NMOS portion of the three-input NAND gate 140, the output of which is supplied through the second level stripe 153 and thence through third level stripe 152 to the second level stripe 160. Note that when and only when all three signals A1, IN2, and IN3 are at the high voltage signal level, then all three NMOS transistors in the NAND gate 140 are on, so that then and only then there is a complete current path through the three transistors from the second level output stripe 160 to

the VSS power lines 120, and hence then and only then the three NMOS transistors pull down the voltage on this stripe 160 toward VSS (typically ground). At the same time, then and only then all three PMOS transistors are off, so that the PMOS portion of the three-input NAND gate 140 then does not pull up the voltage on the stripe 160 toward VDD (typically 5 volts in present-day art). In response to any other signal combinations of A1, IN2, and IN3, at least one of the three PMOS transistors is on and hence pulls up the voltage in the stripe 160 toward VDD while the three NMOS transistors do not pull down the stripe 160 toward VSS (typically ground) since at least one of them is then off--all as desired in the NAND gate 140.

The second level stripe 160 is connected to a pair of third level stripes 161 and 162, located in different routing channels, in order to bring the output of the NAND gate 140 to other cells (not shown) located in the cell rows adjacent to these channels.

The second level stripe 153 and the third level stripe 152 can both be omitted if the impurity region 145 is extended in the right-hand direction and its right-hand extremity is connected directly to the second level stripe 160. The use of the third level stripe 153 as shown in FIG. 1, however, enables easier testability of the NAND gate output by an external probe coming down from above the surface of the region 5, since third level stripes are the easiest of all levels to access by such a probe. Similarly the outputs of inverters 125, 130, 60 and 70 are easily accessible by probes connected to third level stripes 122, 132, 63 and 71, respectively.

As indicated in FIG. 3, the three-input NAND gate 140 (FIG. 1) can be expanded into a five-input NAND gate 300 (FIG. 3)--to accommodate five input signals I1, I2, I3, I4, and I5--by adding two NMOS transistors and two PMOS transistors on the right-hand side as indicated

in FIG. 3. Notice that this expansion from a three-input into a five-input NAND gate does not entail extra space between the VDD and VSS power lines but entails extra space only along the row direction, so that there
5 is no need to increase the distance between the VSS and VDD power lines to accommodate the five-input gate. Such an increase would cause undesirable waste of space elsewhere in the rows.

In particular, the inputs I1, I2, I3, I4, and
10 I5 are brought to the five-input NAND gate 300 along second level stripes 301, 302, 303, 304, and 305, respectively. The second level stripes 301, 302, and 303 are connected to first level stripes 311, 312, and 313, respectively, in the PMOS area and to first level
15 stripes 321, 322, and 323, respectively, in the NMOS area. These first level stripes at their right-hand portions serve as gate electrodes overlying PMOS-GASAD area 310 and NMOS-GASAD area 320, as shown in FIG. 3. On the other hand, second level stripes 304 and 305 are
20 connected to first level stripes 334 and 335, respectively, in the PMOS area and to first level stripes 344 and 345, respectively, in the NMOS area. These first level stripes serve at their left-hand portions as gate electrodes overlying PMOS-GASAD
25 area 310 and NMOS-GASAD area 340, also as shown in FIG. 3. The third level power line VDD is connected to the PMOS-GASAD area 310 through second level stripes 315 and 336 through four windows: a window located between first level stripes 312 and 313, a window located at the
30 left-hand top extremity of the PMOS-GASAD area 310 (just above first level stripe 311), a window located at the right-hand top extremity of this PMOS area 310 (just above first level stripe 335), and a window located at the bottom right-hand extremity of this area 310 (just
35 below first level stripe 334). The third level power line VSS is connected to NMOS-GASAD area 320 through second level stripes 325 as shown in FIG. 3.

The NMOS-GASAD areas 320 and 340 are respectively interconnected at their top extremities by second level stripes 326 and 342, through a third level stripe 341. The output Z of the five-input NAND gate 5 300 is delivered along second level stripe 350 by virtue of its connection through third level stripe 346 and second level stripe 343 to the bottom extremity of the NMOS-GASAD area 340 and its direct contacts to an elongated portion of the bottom of the left-hand portion 10 of PMOS-GASAD area 310 and to an interconnecting portion (between imaginary extensions toward the right of first level stripes 311 and 312, and to the left of first level stripes 334 and 335) of this PMOS-GASAD area 310.

A six-input NAND gate can be laid out 15 similarly as the above-described five-input NAND gate 300, likewise without increasing the distance between power lines VDD and VSS, by adding one more first level stripe to the right-hand side of PMOS-GASAD area 310 between first level stripes 334 and 335, and adding one 20 more first level stripe to the NMOS-GASAD area 340 between first level stripes 344 and 345, both such added first level stripes being contacted by a second level input stripe for bringing in the sixth input signal.

Note that in FIGS. 1 and 3 all the power lines 25 VDD and VSS are advantageously mutually parallel everywhere in the region 5, in accordance with the ordinary cell row layout technique, in order to have a simple and orderly layout pattern of rectangular row areas. In cases of clocked (dynamic) gates, one or more 30 clock lines should be added, in the appropriate channel(s) adjacent to the row(s) containing the clocked gates, running in the third level parallel to, and located proximate to, one or more of the power lines.

Turning to the cross section labeled 4-4 in 35 FIG. 1, as shown in crosssection in FIG. 4, upon a top major surface of a portion of an underlying p-type semiconductor body 500 is located a first insulating

layer 503 (gate oxide) extending over a transistor channel region located at the top surface of the body 500 between the n-type source region 119 and the n-type drain region 118, as known in the art of CMOS transistors. Upon the first insulating layer 503 is located first level stripe 117 serving there as the gate electrode. The drain and source regions 118 and 119 are contacted by second level stripes 116 and 121, respectively. The stripes 116 and 121 are both separated and insulated from the body and from the first level stripe 117 by a second insulating layer 505 located on the first insulating layer. In turn, the third level stripes 120 and 122 are separated and insulated from the second level stripes 121 and 116 respectively, by a third insulating layer 507, except that the third level stripes 120 and 122 contact the second level stripes 121 and 116, respectively, through windows 410 and 412 in this third insulating layer 507. A protective insulating cap layer 509 is located on the third insulating layer 507 and on the third level stripes 120 and 122.

Illustratively, the insulating layers are made of known material(s), or of other materials as they become available in the CMOS art. The first level stripe 117 is essentially doped or undoped polysilicon, and may be overlaid with metal silicide for greater conductivity if needed. It is also feasible to dope the polysilicon stripes 117 serving as gate electrodes for the PMOS transistors differently from the stripes serving as gate electrodes for the NMOS transistors. The second and third level stripes 120, 122, 121, and 116 are all essentially aluminum or other metal(s) or combination(s) thereof. It should be understood that at areas of the circuit region 5 (FIG. 1) removed from transistors--i.e., located in the cell row area and the channel area away from the gate and source and drain (GASAD) areas--the first insulating layer is made

thicker than at (gate) areas overlying transistor channel regions located between sources and drains; and the second insulating layer may also be made correspondingly thicker at areas removed from the GASAD
5 areas. Thus the first, second, and third levels of interconnections are planar except for transition areas overlying the boundaries of GASAD areas (and perhaps also overlying the edges of first and second level stripes). Although the invention has been described in
10 terms of specific embodiments, various modifications can be made without departing from the scope of the invention. For example, NOR gates can be fabricated by interchanging the PMOS and NMOS layouts. Also, programmed logic arrays and/or memories can be
15 fabricated in other regions of the circuit using the above-described three levels of interconnection without using the cell row arrangement of the kind described above--i.e., without having elongated rows dedicated to transistors plus some interconnections but while still
20 using three levels of interconnections, for example, one polysilicon and two aluminum levels.

It is further noted that when using the three level interconnection scheme of this invention, insofar as routing (layout) of interconnection from one cell to
25 another whether located in the same row or in different rows, the routing of interconnections in the channel can be the same as in the case of the two level scheme of prior art simply by considering the first prior art level (of polysilicon) as the new second level (of
30 metal), and the second prior art level (of metal) as the new third level (also of metal). Accordingly, the same computer-aided routing tools can be used for layout of routing when implementing interconnections in accordance with this invention as were used in the prior art.
35 Also, in using the present invention for CMOS (complementary MOS, containing PMOS and NMOS transistors) circuits, the gate electrode of an NMOS

transistor in a given cell can be directly (i.e., without running into the channel) interconnected to the gate electrode of a PMOS transistor within the same cell via a second level (metal) stripe located within the
5 polycell instead of via solely first level (polysilicon) stripes--an advantage of special importance in the case of submicron transistor feature sizes where the close proximity of the PMOS to the NMOS gates runs the risk of undesirable diffusion of the significant impurities in
10 the PMOS gate electrode through the prior art first level polysilicon interconnection to the NMOS gate electrode (and/or vice versa) whereby the significant impurity concentrations (desirably different in type and amount in NMOS vs. PMOS gate electrodes) and hence the
15 transistor threshold voltages would be uncontrollably changed. Also, because of the relatively short required lengths of the first level polysilicon stripes when implementing them in accordance with the invention, the requirement to reduce their resistivities by using a
20 first level metal silicide overlay as in prior art is correspondingly relaxed, and hence the first level stripes can be polysilicon doped with impurities but not containing any metal silicide.

Claims

1. A semiconductor integrated circuit having a region (5) thereof comprising mutually parallel and spaced-apart elongated separate cell rows that run parallel to a first direction, in each of which is located a separate plurality of transistors integrated at a major surface of a semiconductor body, such transistors being interconnected and accessed by three successive levels of interconnection stripes,

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the first level (FIG. 4, 117) being located closest among the three levels to the major surface of the body and consisting essentially of stripes for electrically connecting the control electrodes of the transistors to the rest of the circuit, the second level (116, 121) consisting essentially of stripes running perpendicular to the first direction, and the third (120, 122) being located farthest among the three levels from the major surface of the body and consisting essentially of stripes running parallel to the first direction.

2. A circuit according to claim 1 in which the transistors are all MOS transistors and in which the first level stripes are confined to areas directly overlying the cell rows.

3. A semiconductor integrated circuit according to claim 1 in which the transistors are all MOS transistors and in which first level stripes are separated and insulated from the major surface of the body by a first insulating layer (503), the second level stripes are separated and insulated from the first level stripes by a second insulating layer (505) having first windows at selected first locations thereof through which second level stripes contact first level stripes and having second windows at selected second locations thereof through which second level stripes contact the major surface of the body, and the third level stripes

major surface of the body, and the third level stripes are separated and insulated from the second level stripes by a third insulating layer (507) having third windows at selected locations thereof through which
5 third level stripes contact second level stripes.

4. A semiconductor integrated circuit in accordance with claim 3 in which some of the first windows of the second insulating layer are located in areas directly overlying cell rows.

10 5. A semiconductor integrated circuit in accordance with claim 4 in which at least some of the third windows in the third insulating layer are located in areas directly overlying cell rows.

6. A semiconductor integrated circuit in
15 accordance with claim 3 in which at least some of the third windows in the third insulating layer are located in areas directly overlying cell rows.

7. A circuit according to claim 2 in which the first level stripes consist essentially of
20 polysilicon doped with impurities.

8. A circuit according to claim 1 in which every first level stripe has all of its ends located within a cell row.

9. A circuit according to claim 8 in which
25 the first level stripes consist essentially of polysilicon doped with impurities.

FIG. 1

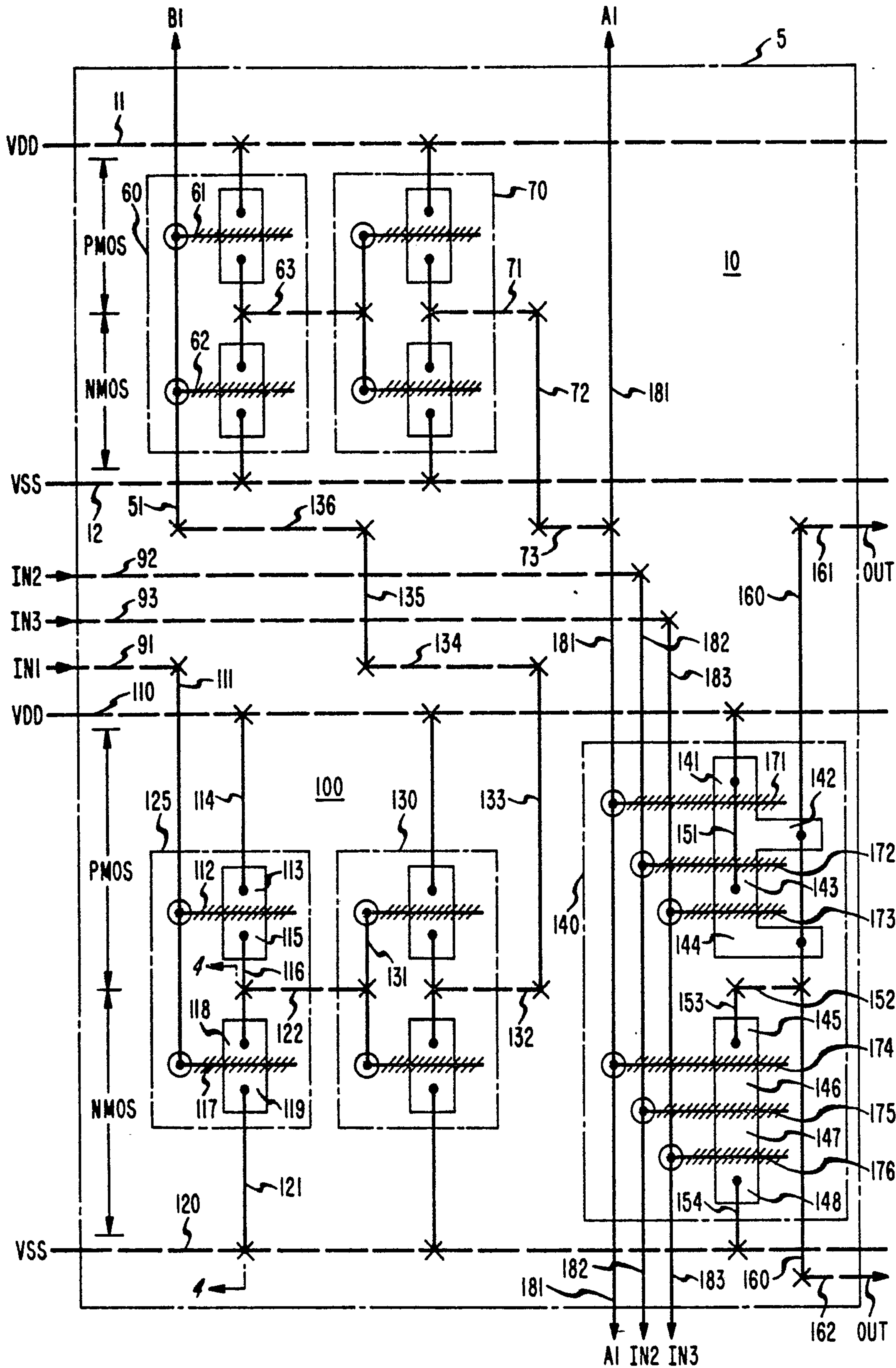


FIG. 2

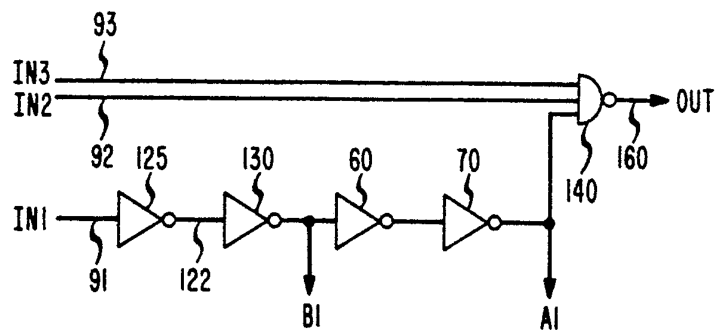


FIG. 4

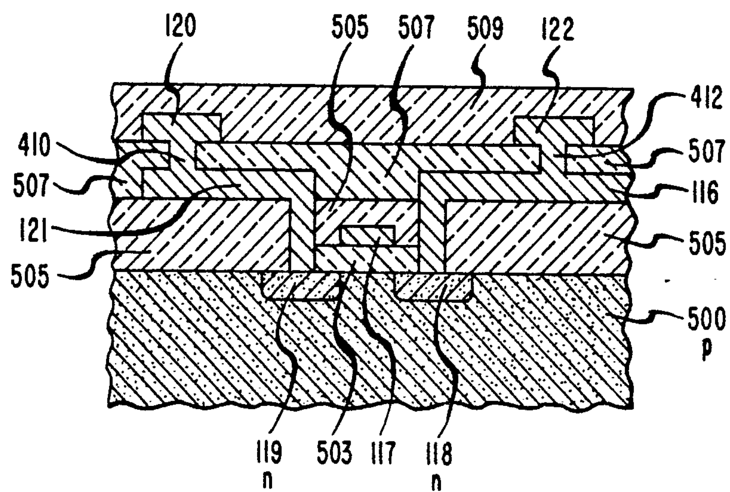
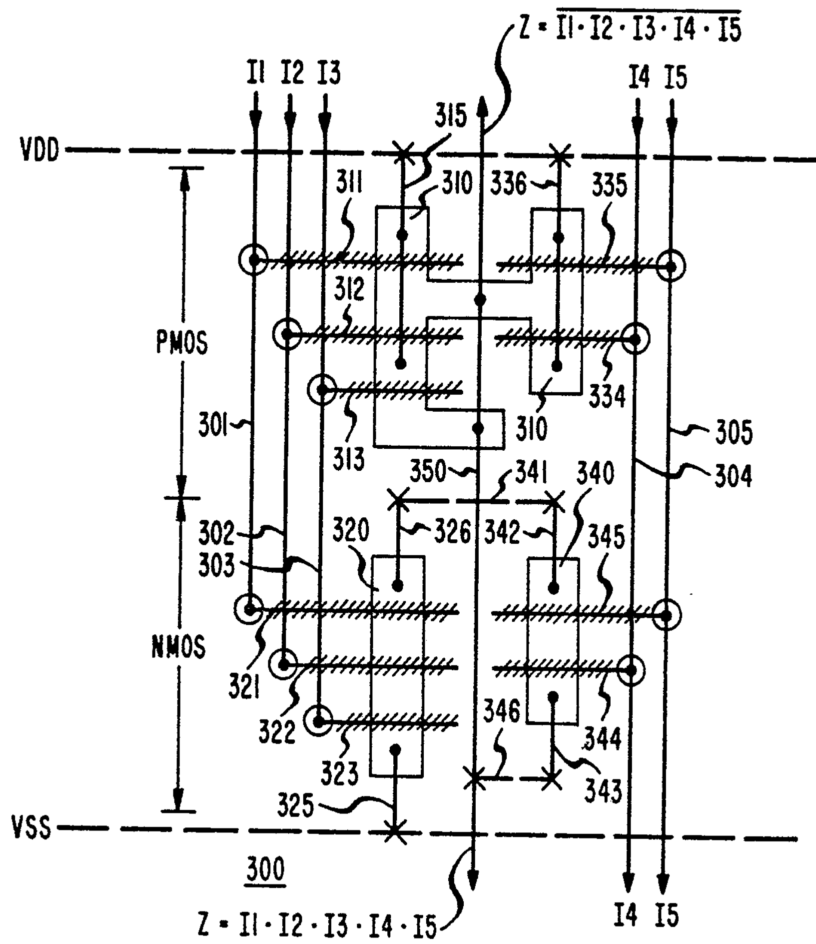
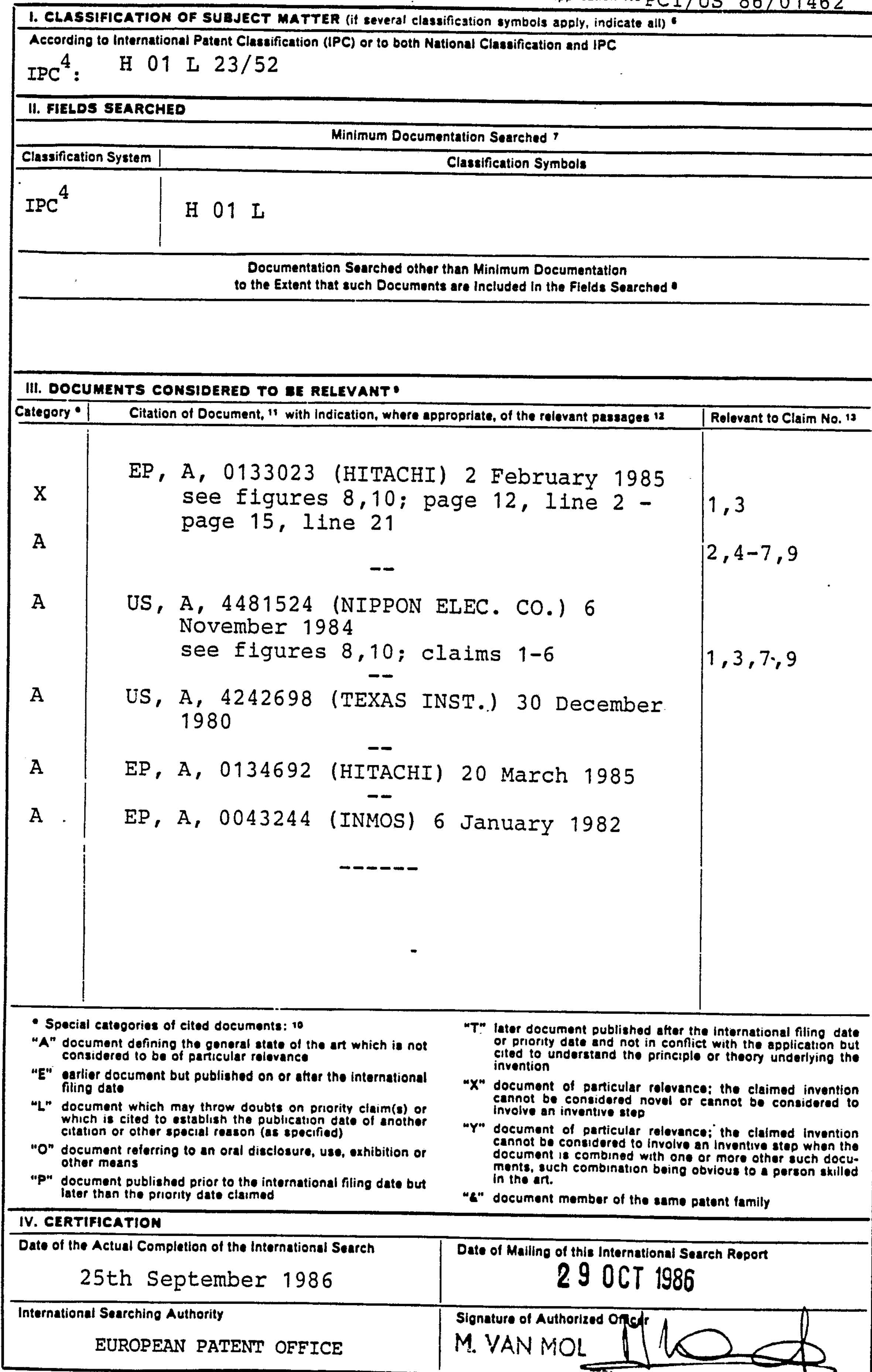


FIG. 3





INTERNATIONAL SEARCH REPORT

International Application No PCT/US 86/01462

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC^4: H 01 L 23/52

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC^4	H 01 L

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category *	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
X A	EP, A, 0133023 (HITACHI) 2 February 1985 see figures 8,10; page 12, line 2 - page 15, line 21 --	1,3 2,4-7,9
A	US, A, 4481524 (NIPPON ELEC. CO.) 6 November 1984 see figures 8,10; claims 1-6 --	1,3,7-,9
A	US, A, 4242698 (TEXAS INST.) 30 December 1980 --	
A	EP, A, 0134692 (HITACHI) 20 March 1985 --	
A	EP, A, 0043244 (INMOS) 6 January 1982 ------	

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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
25th September 1986	29 OCT 1986
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	M. VAN MOL

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ANNEX TO THE INTERNATIONAL SEARCH REPORT ON

INTERNATIONAL APPLICATION NO. PCT/US 86/01462 (SA 13851)

This Annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 09/10/86

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