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(54) **MICRO INERT ANODE ARRAY FOR DIE LEVEL ELECTRODEPOSITION THICKNESS DISTRIBUTION CONTROL**

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§ 371 (c)(1),
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(51) **Int. Cl.**

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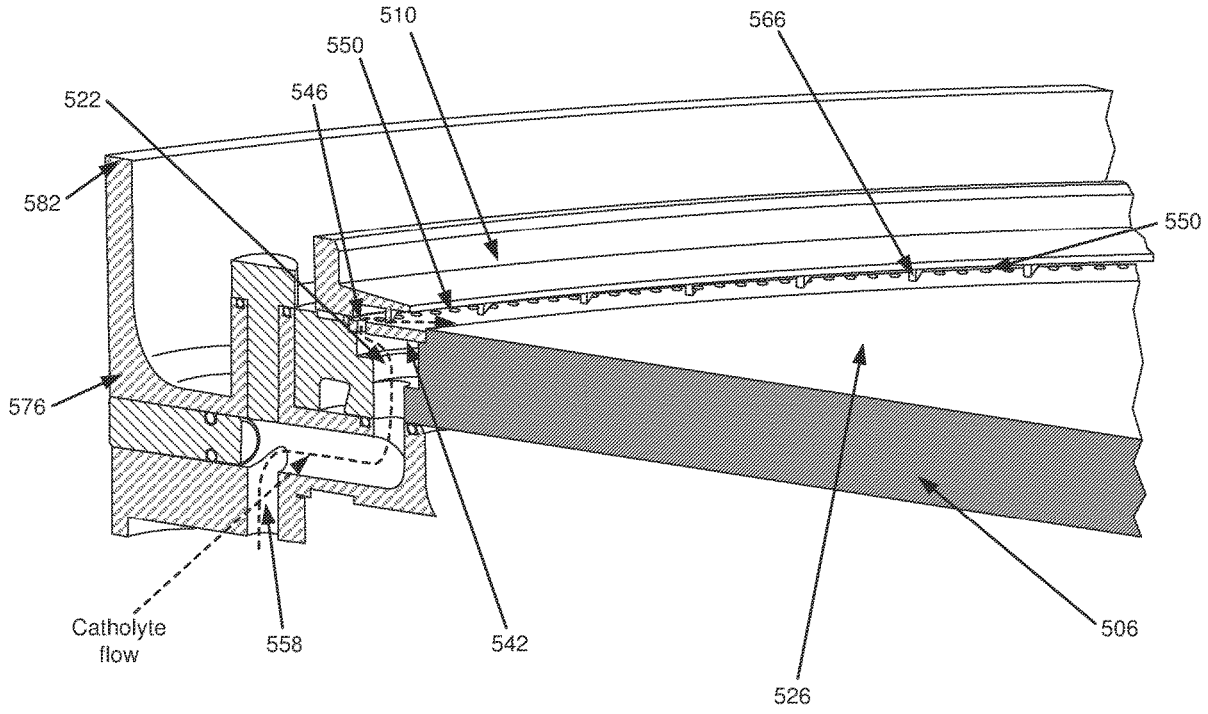
C25D 7/12	(2006.01)
C25D 17/00	(2006.01)
C25D 21/14	(2006.01)
C25D 21/18	(2006.01)

(52) **U.S. Cl.**

CPC ***C25D 17/12*** (2013.01); ***C25D 5/022*** (2013.01); ***C25D 5/08*** (2013.01); ***C25D 7/123*** (2013.01); ***C25D 17/001*** (2013.01); ***C25D 17/007*** (2013.01); ***C25D 21/14*** (2013.01); ***C25D 21/18*** (2013.01)

(57) **ABSTRACT**

Metal may be electroplated on a semiconductor substrate in an electroplating chamber with a micro inert anode array positioned proximate to the semiconductor substrate having one or more die. The micro inert anode array includes a plurality of micro inert anode elements that are independently controllable. Current applied to the micro inert anode elements provides a current distribution in the array that may be based at least in part on a die layout in the semiconductor substrate or based at least in part on global within-wafer corrections. The current distribution may achieve uniform plating thickness even with a non-uniform distribution of features in the die of the semiconductor substrate. In some implementations, current distribution may be adjusted in the array during substrate rotation according to a rotational path of the semiconductor substrate.



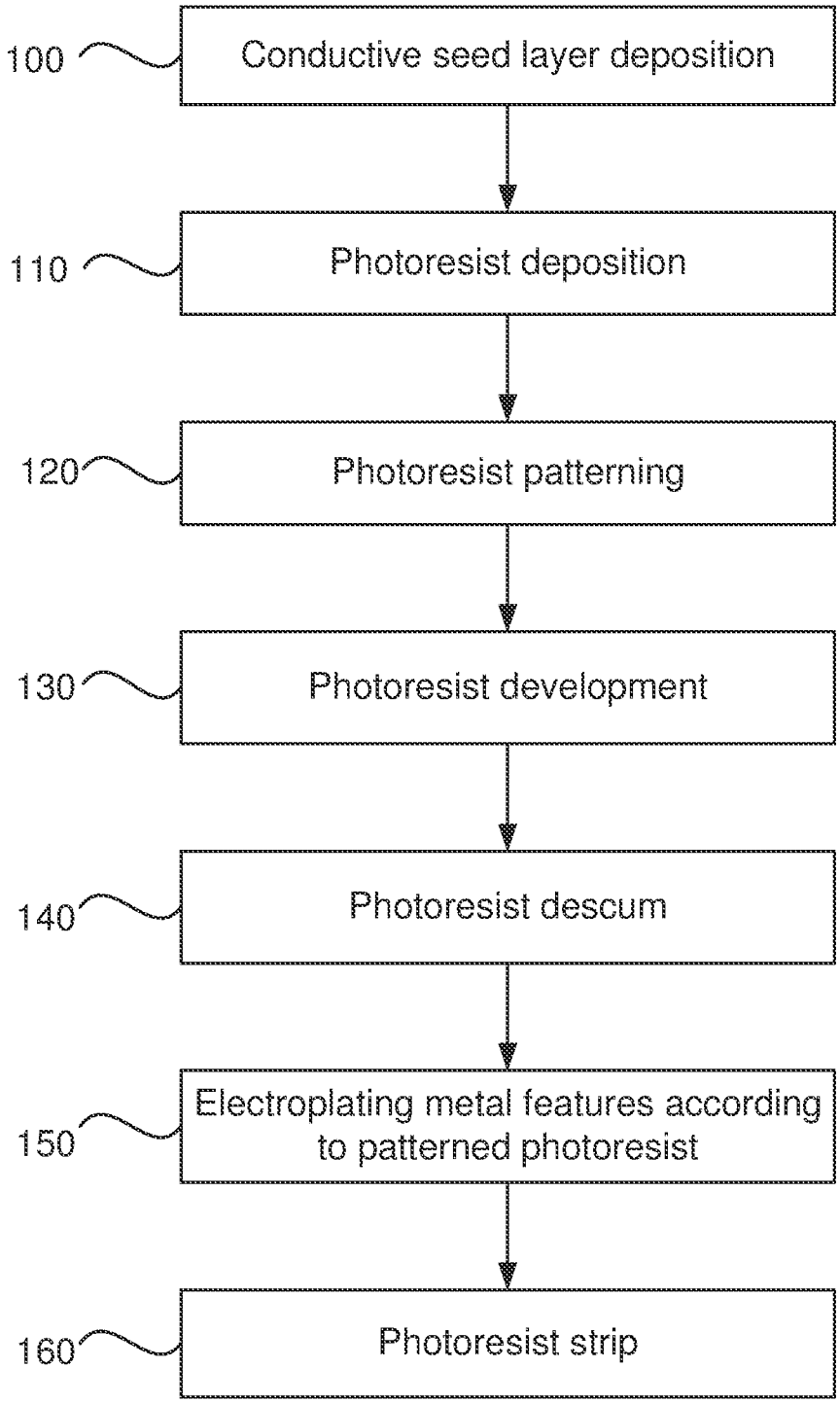

100
Conductive seed layer deposition
110
Photoresist deposition
120
Photoresist patterning
130
Photoresist development
140
Photoresist descum
150
Electroplating metal features according to patterned photoresist
160
Photoresist strip

FIG. 1

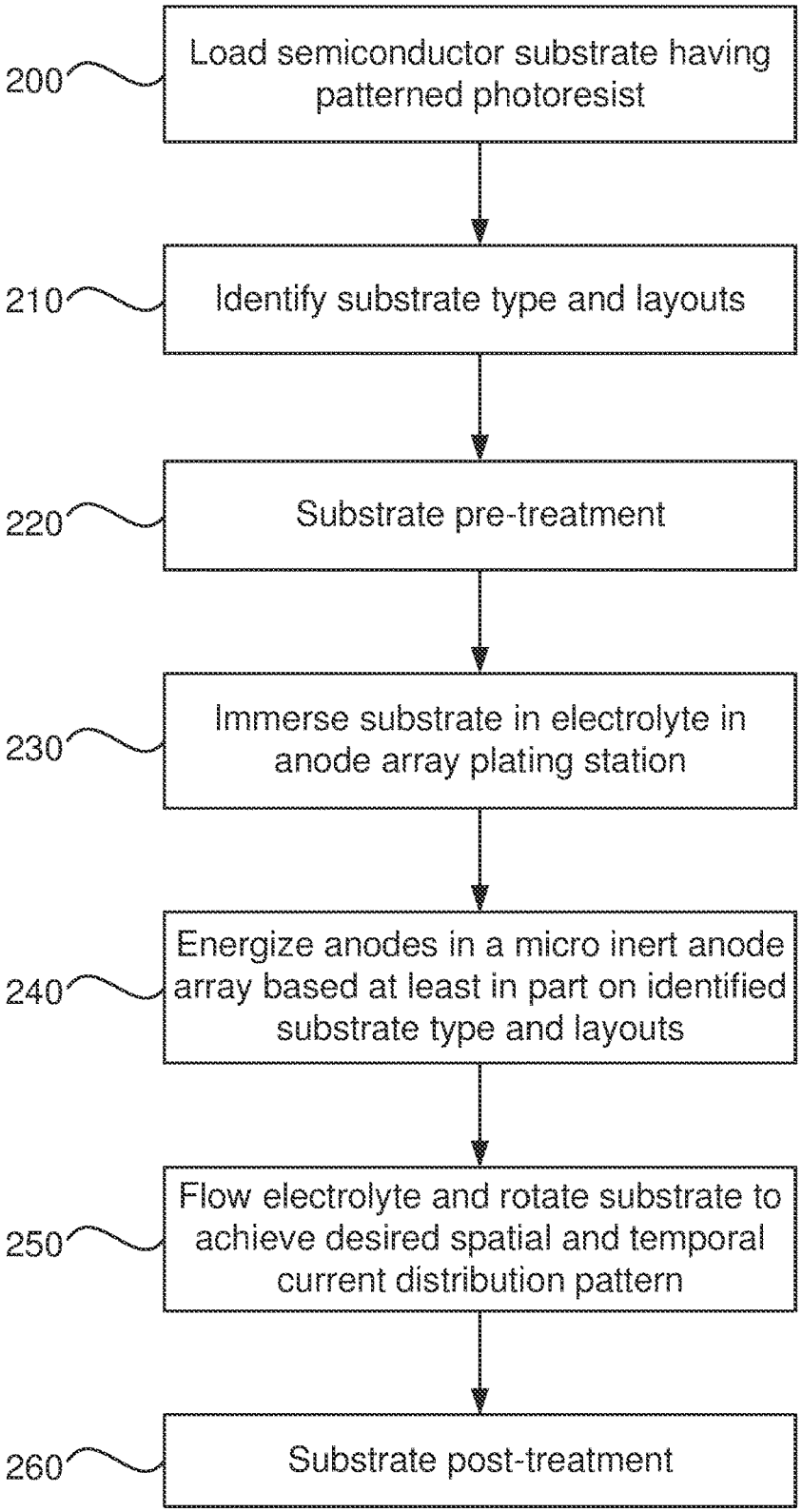

200
Load semiconductor substrate having patterned photoresist
210
Identify substrate type and layouts
220
Substrate pre-treatment
230
Immerse substrate in electrolyte in anode array plating station
240
Energize anodes in a micro inert anode array based at least in part on identified substrate type and layouts
250
Flow electrolyte and rotate substrate to achieve desired spatial and temporal current distribution pattern
260
Substrate post-treatment

FIG. 2

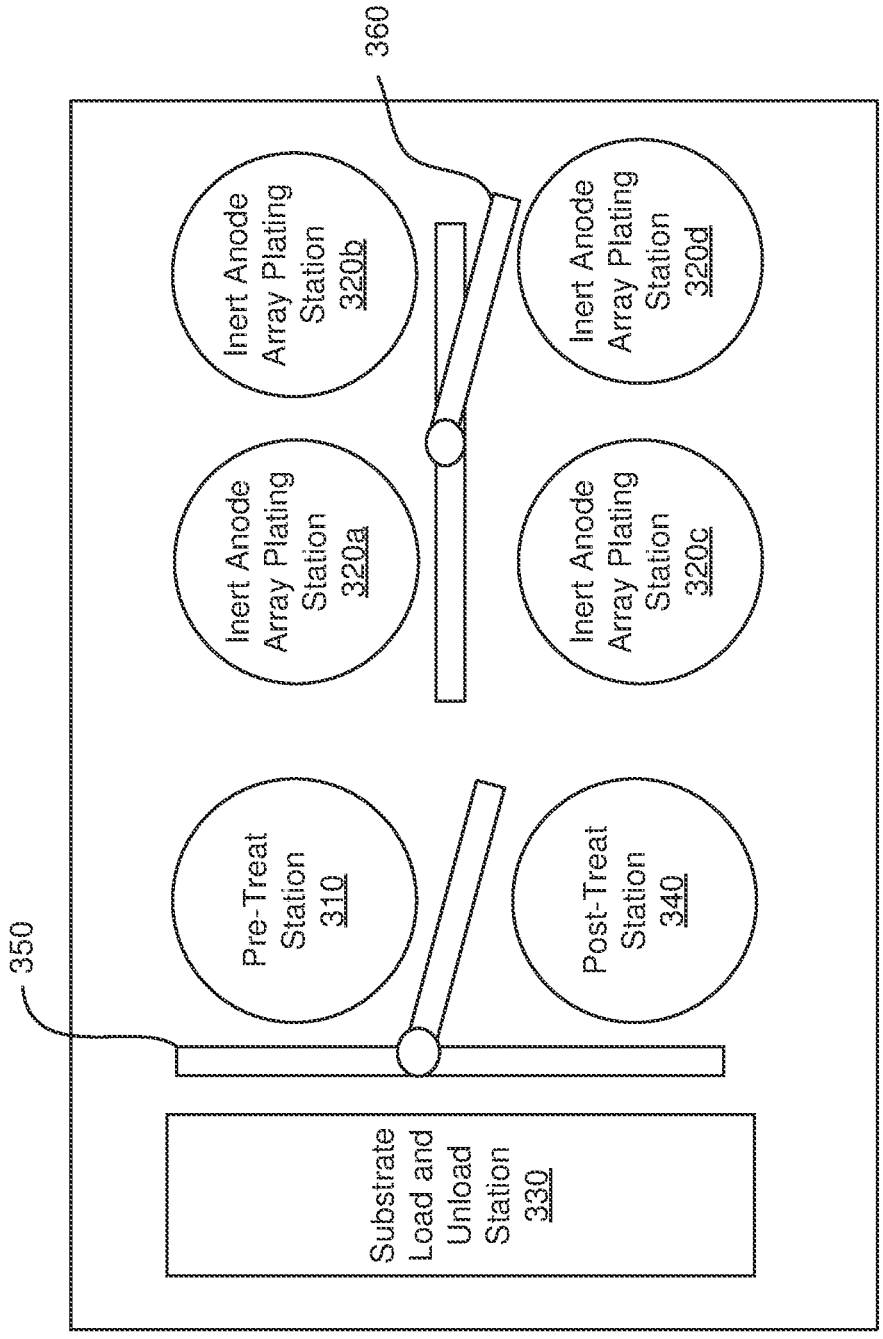

360
Inert Anode Array Plating Station 320b
Inert Anode Array Plating Station 320d
Inert Anode Array Plating Station 320a
Inert Anode Array Plating Station 320c
Pre-Treat Station 310
Post-Treat Station 340
350
Substrate Load and Unload Station 330

FIG. 3

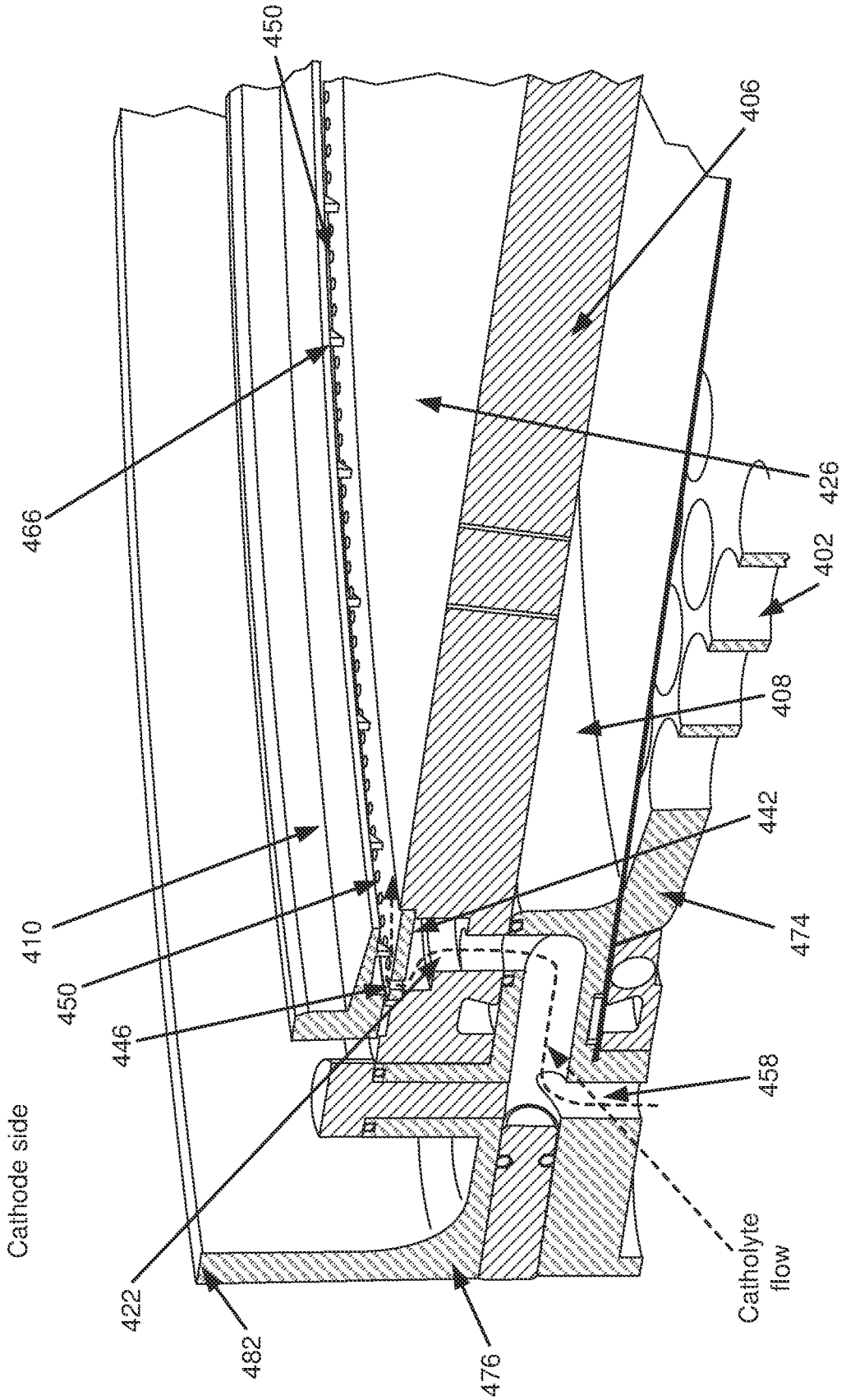

450
406
466
426
402
408
410
442
450
474
446
458
Catholyte flow
422
482
476
Cathode side
Anode side

FIG. 4A

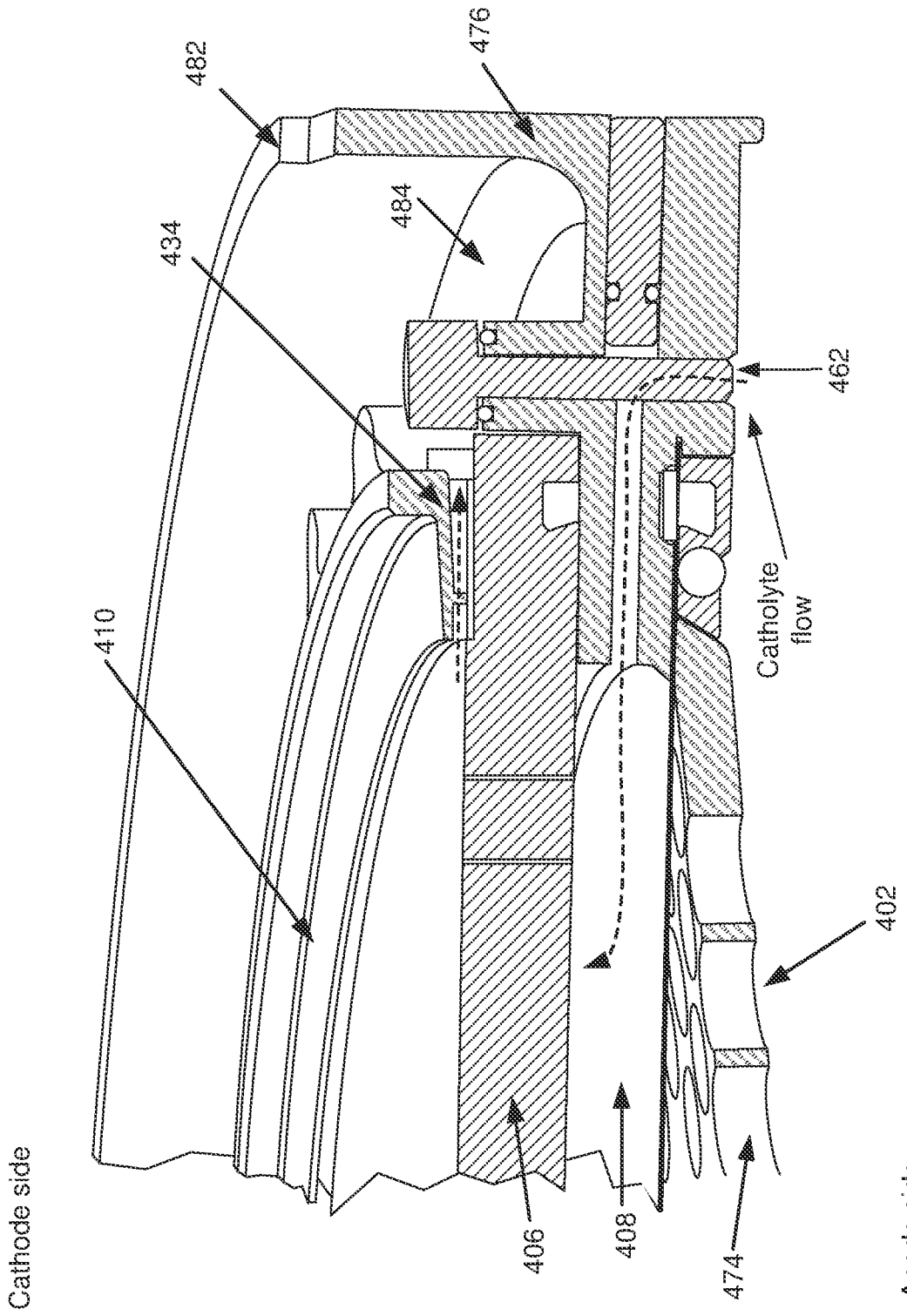

482
476
484
434
462
Catholyte flow
410
402
406
408
474
Cathode side
Anode side

FIG. 4B

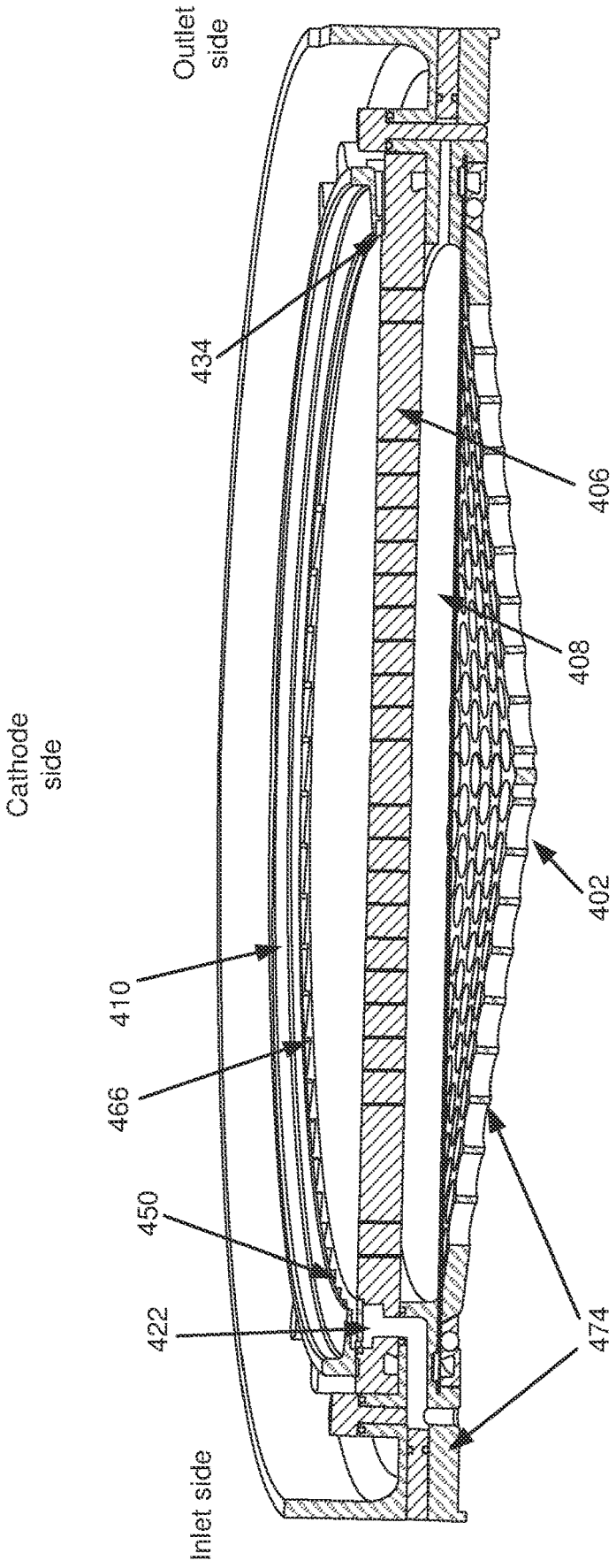

Outlet side
434
406
408
Cathode side
Anode side
402
410
466
450
422
474
Inlet side

FIG. 4C

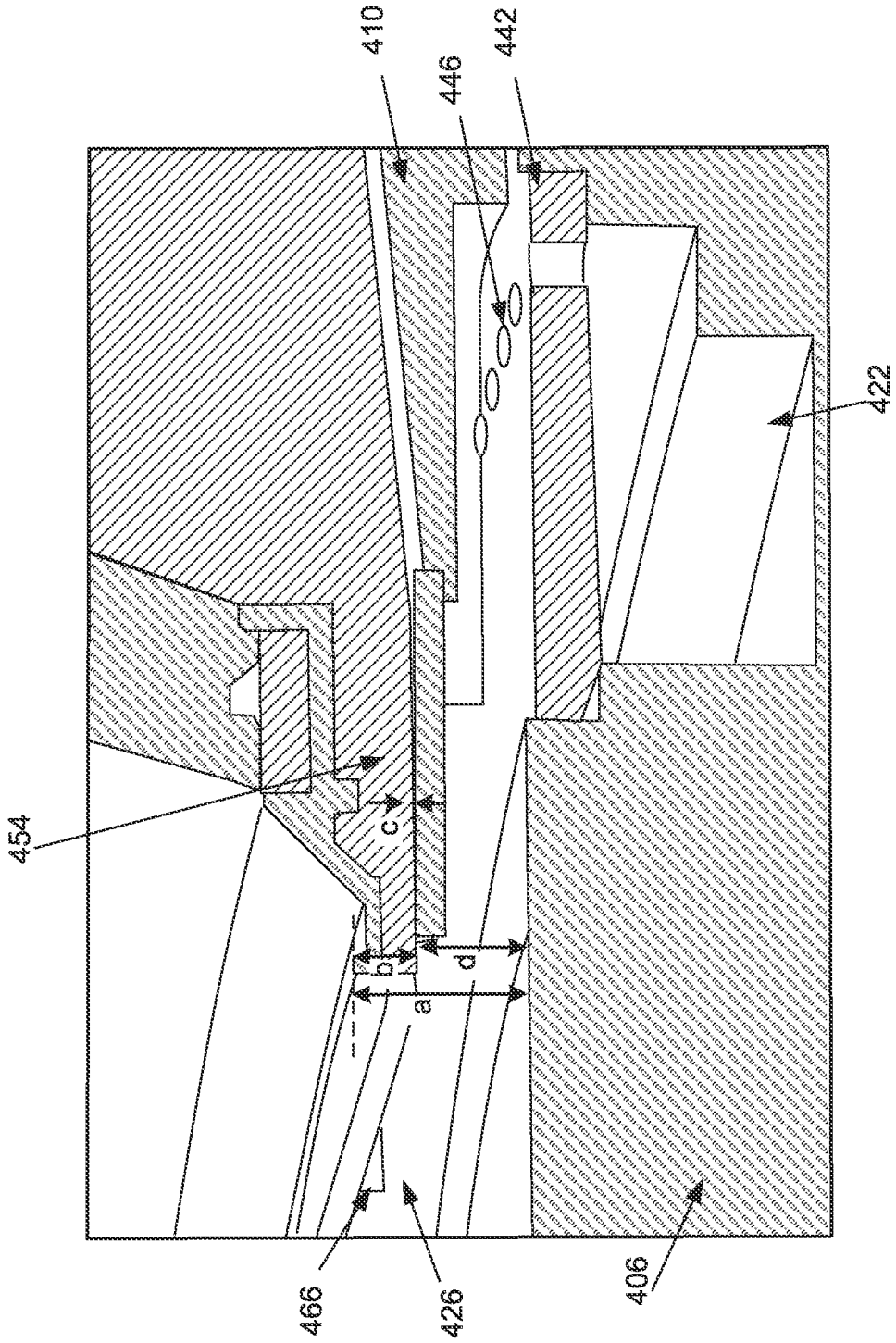


FIG. 4D

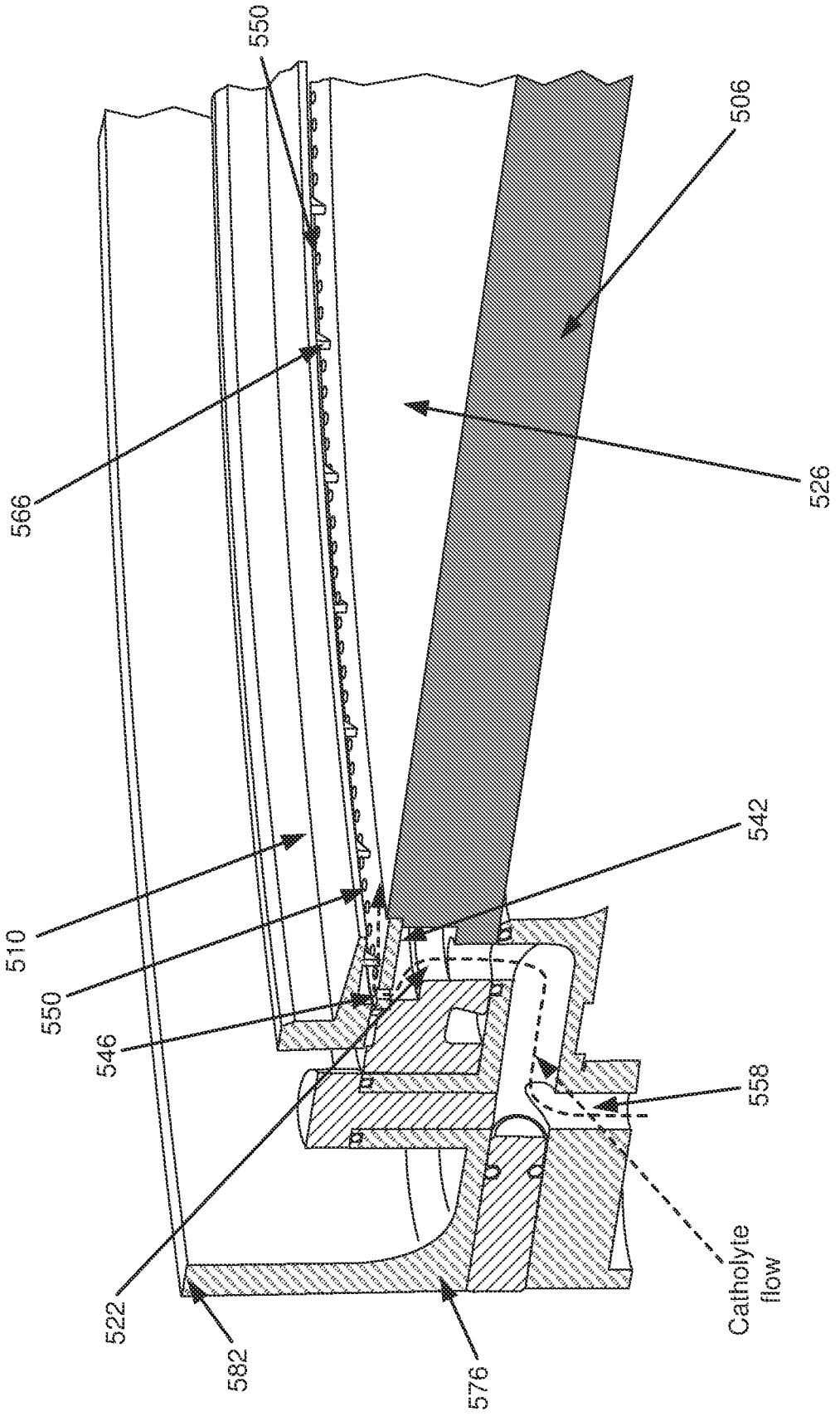


FIG. 5A

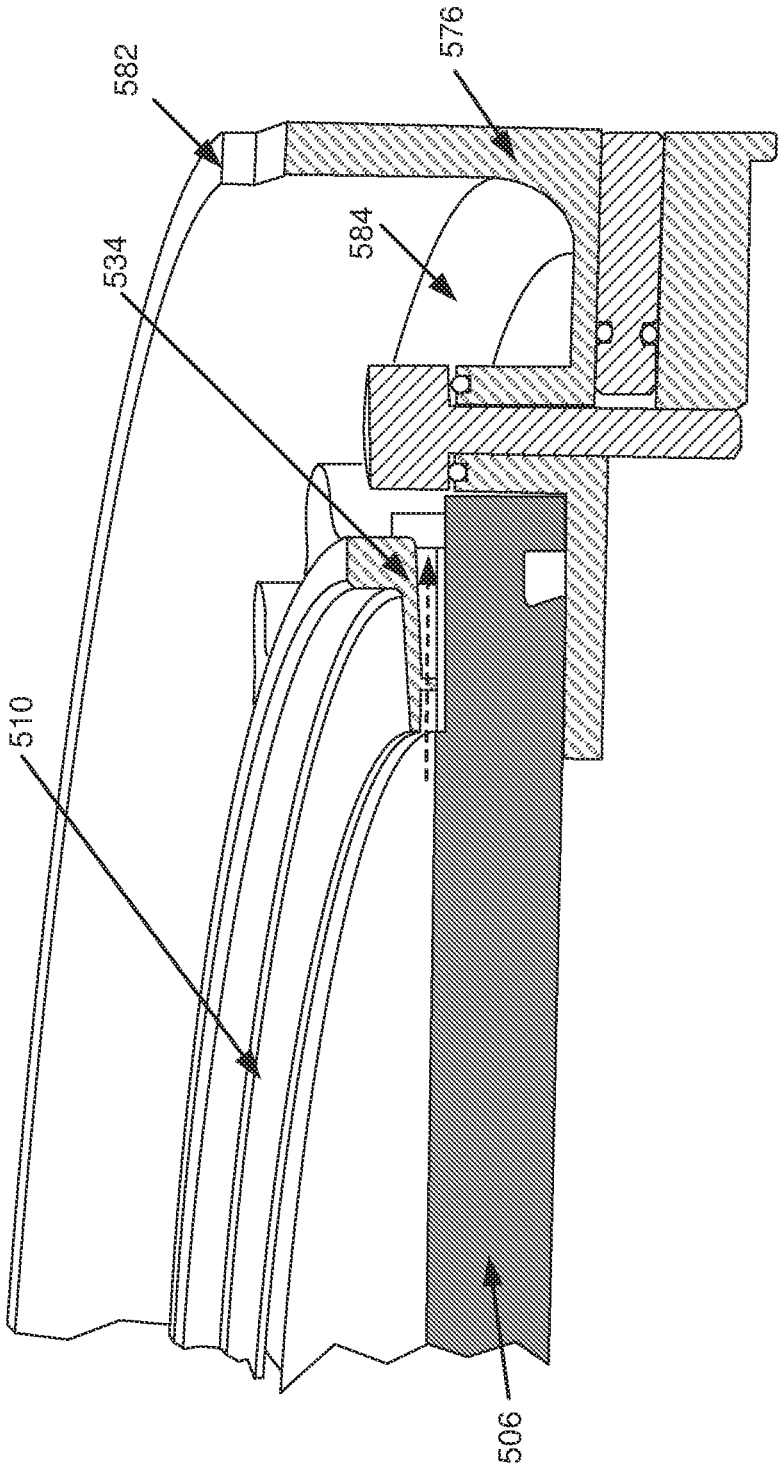


FIG. 5B

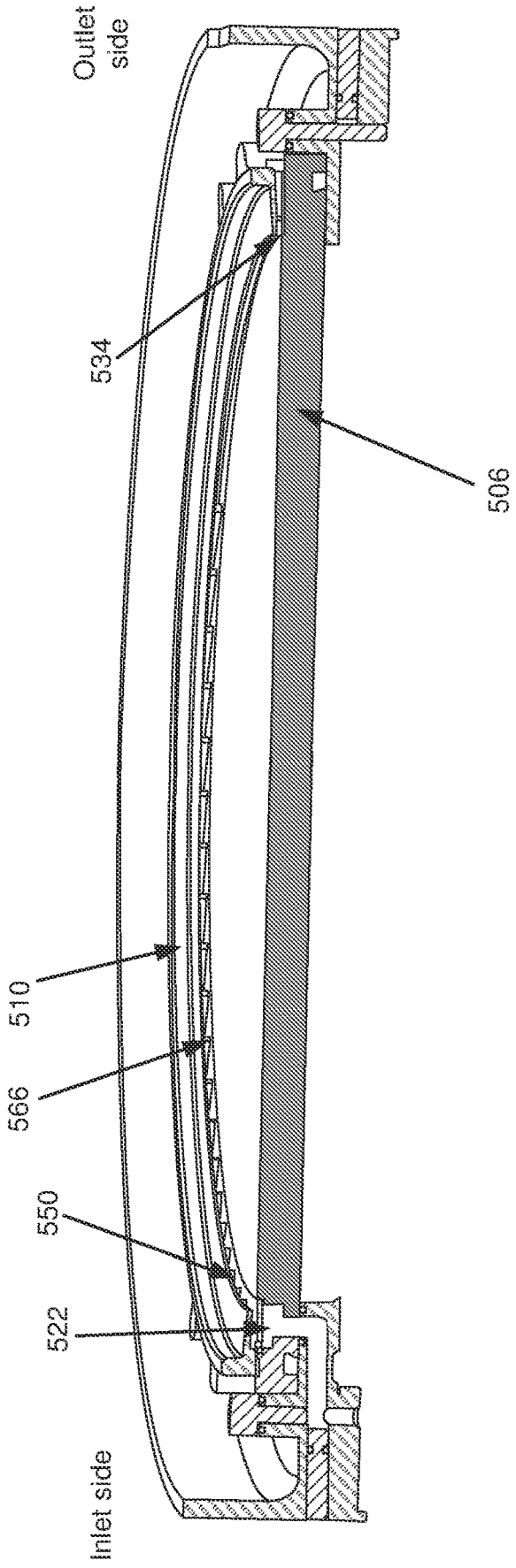


FIG. 5C

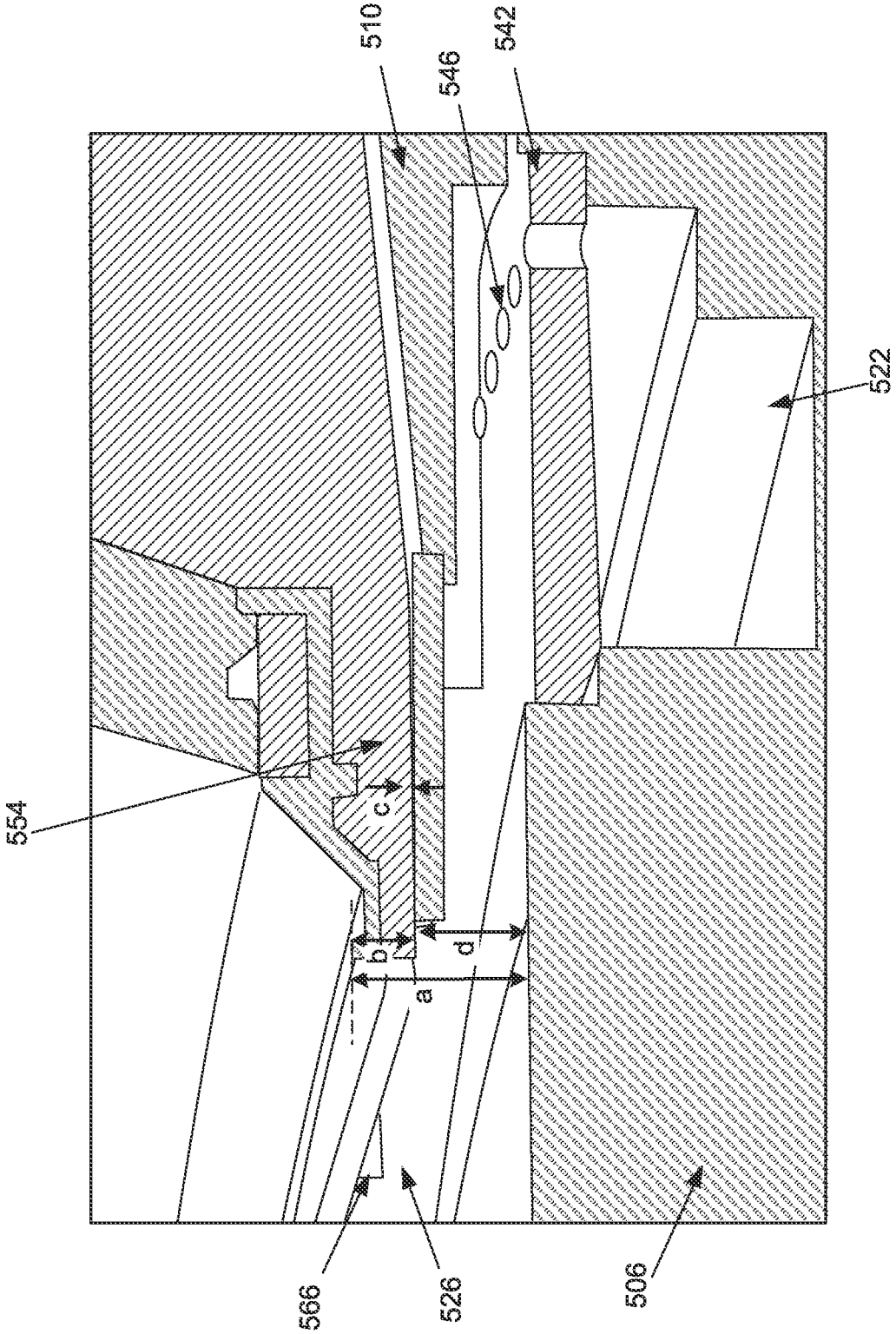


FIG. 5D

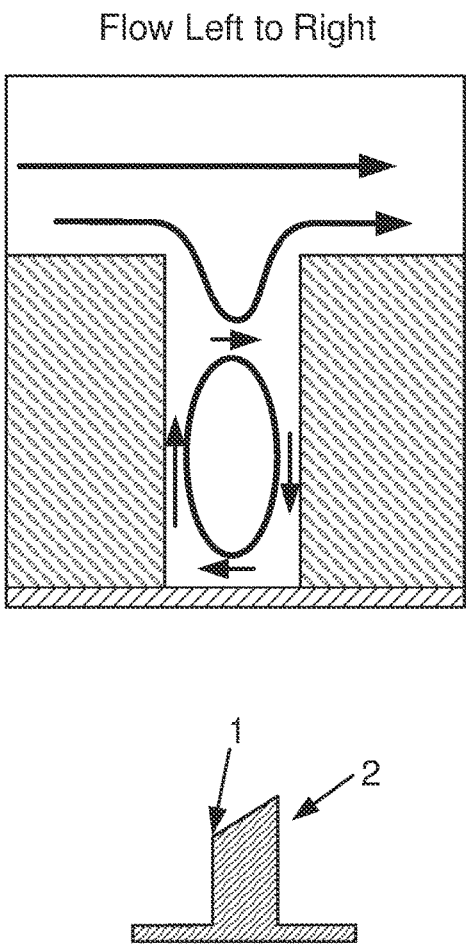


FIG. 6A

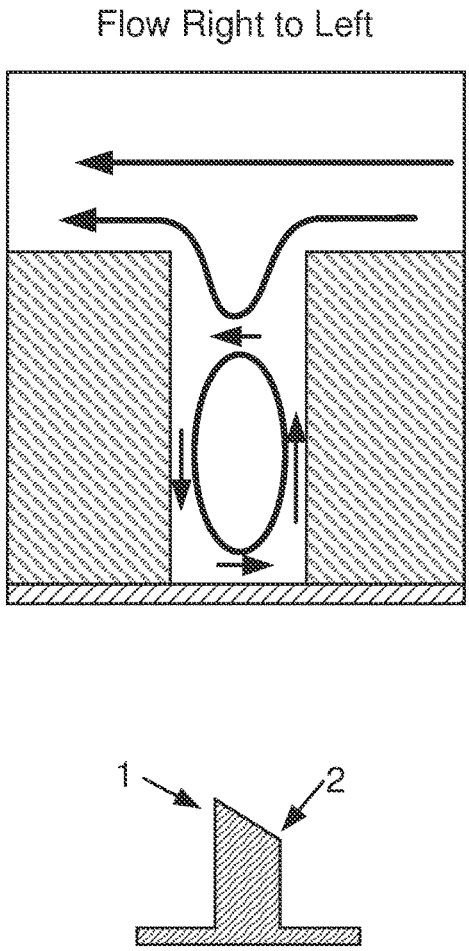


FIG. 6B

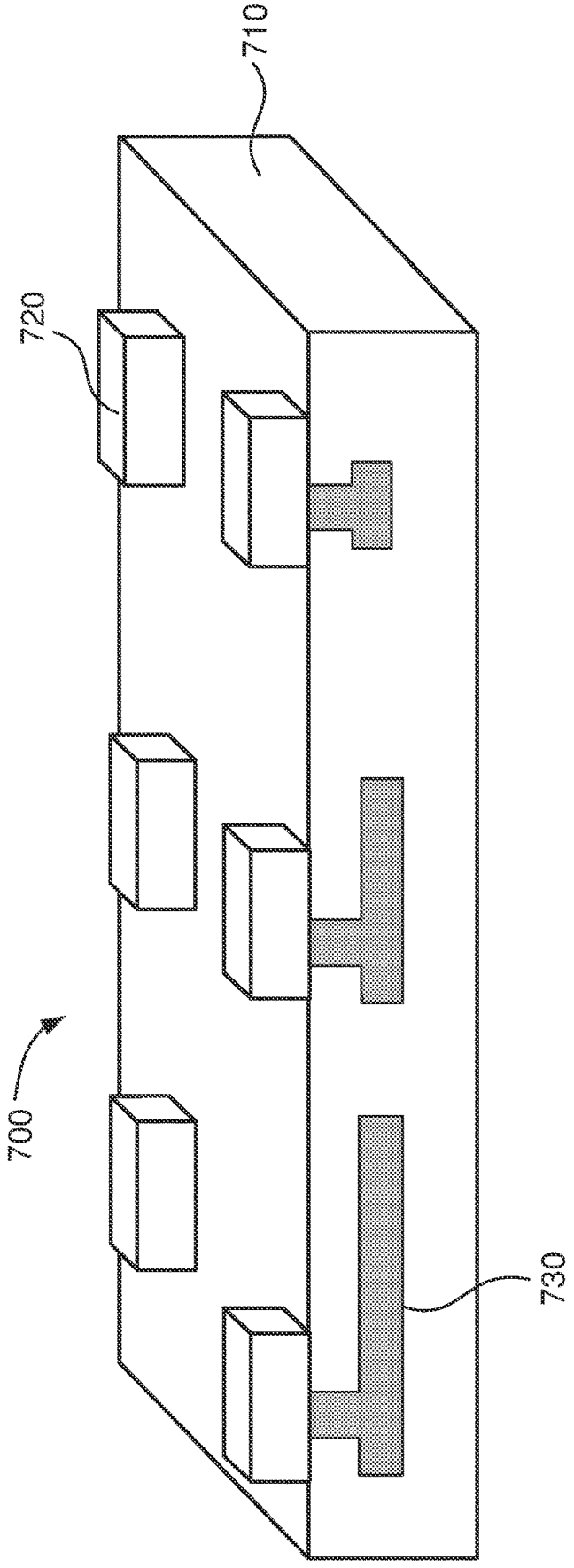


FIG. 7A

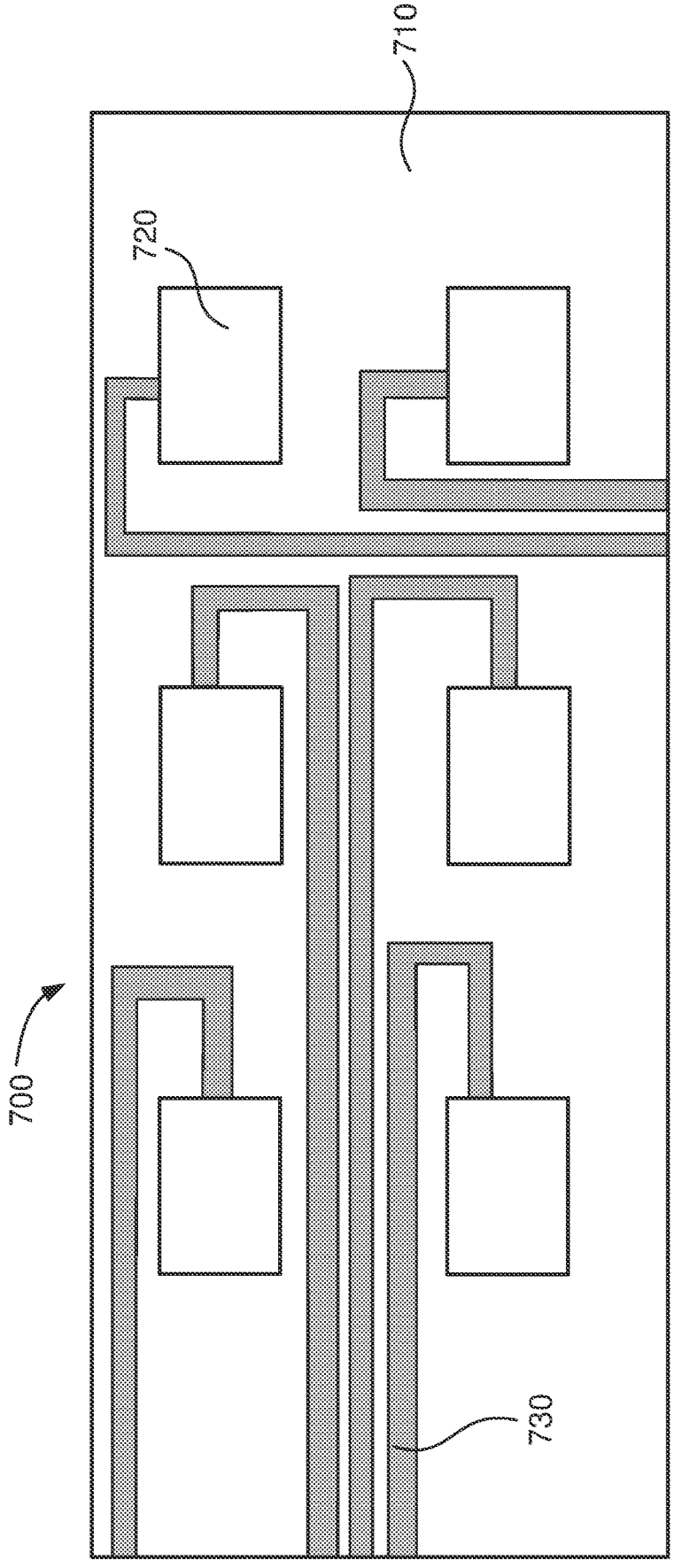


FIG. 7B

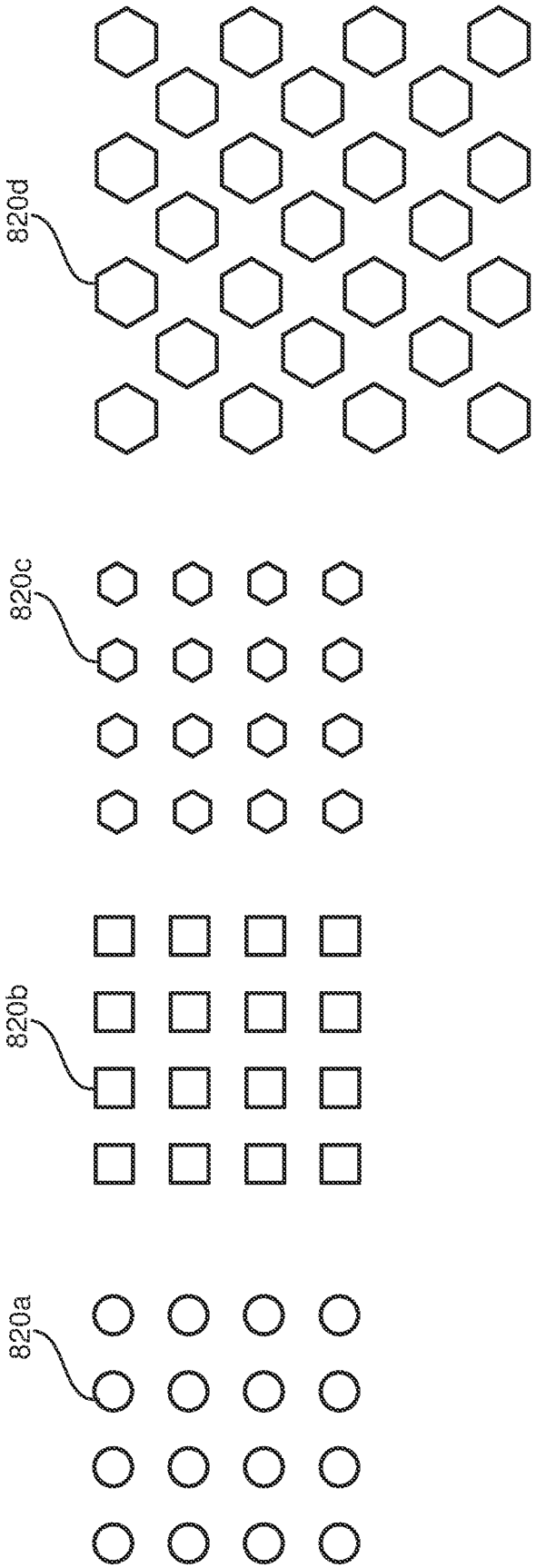


FIG. 8

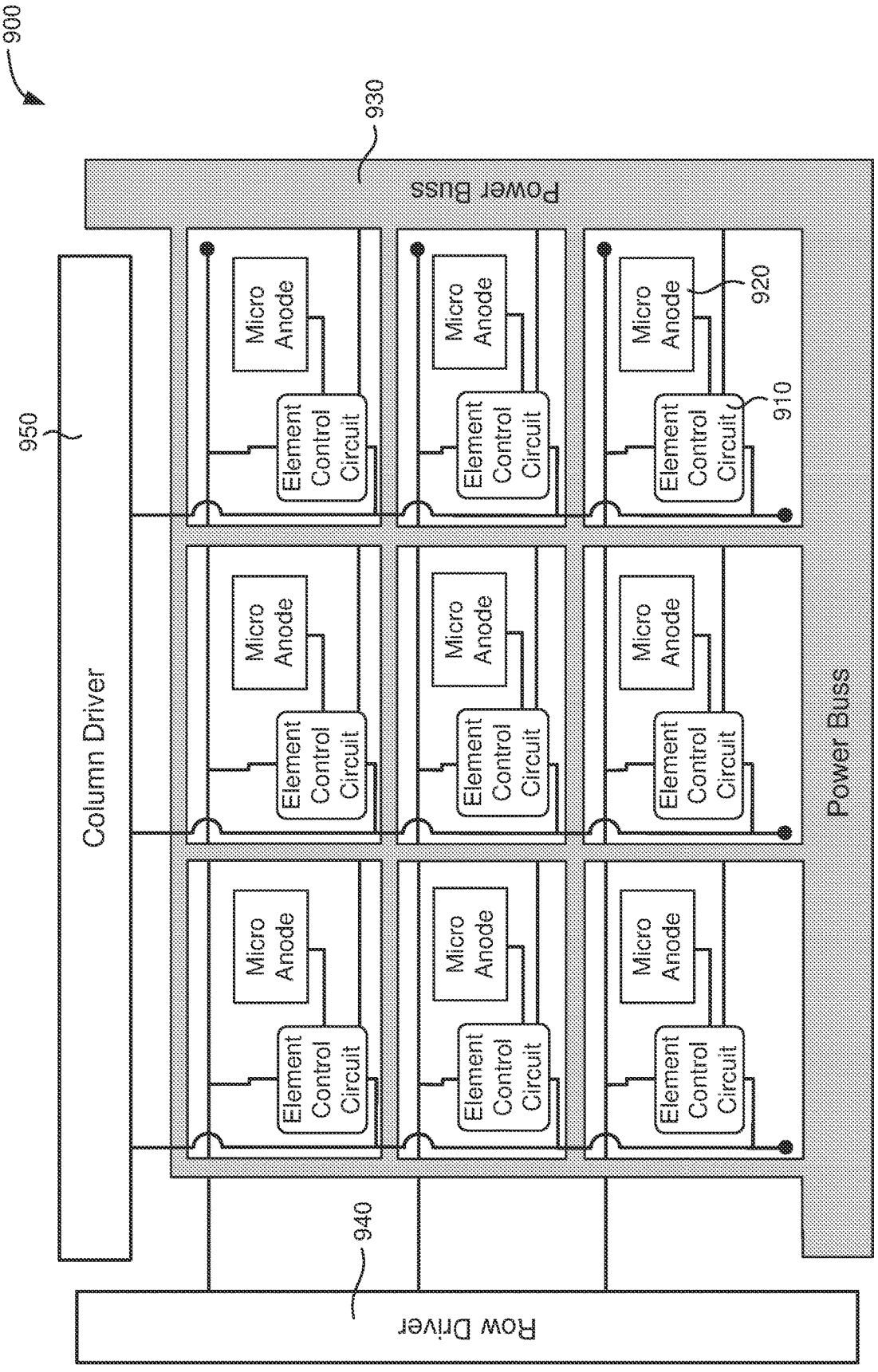

900
930
Power Buss
950
Column Driver
Micro Anode
Element Control Circuit
920
910
Power Buss
940
Row Driver

FIG. 9

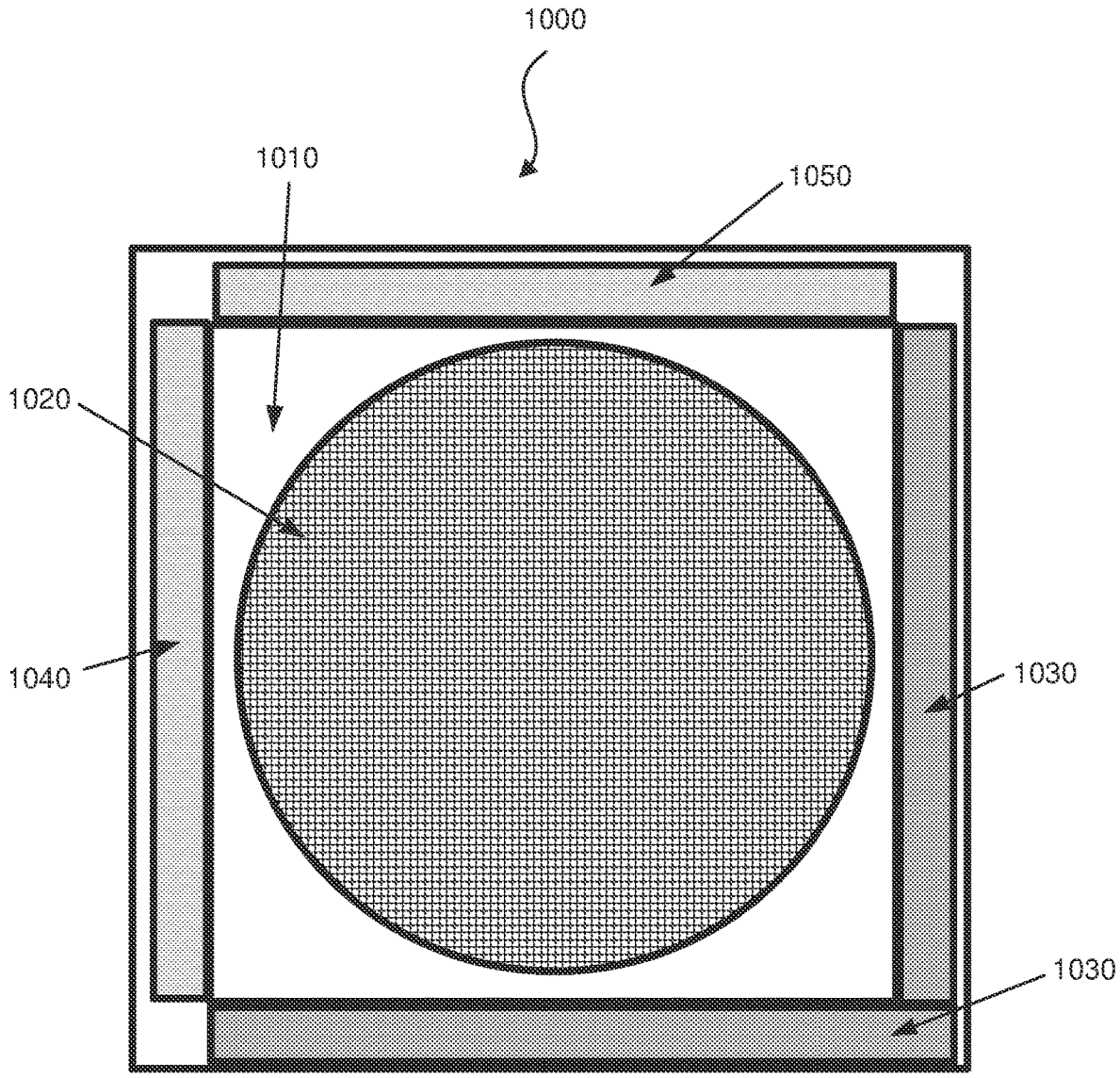


FIG. 10

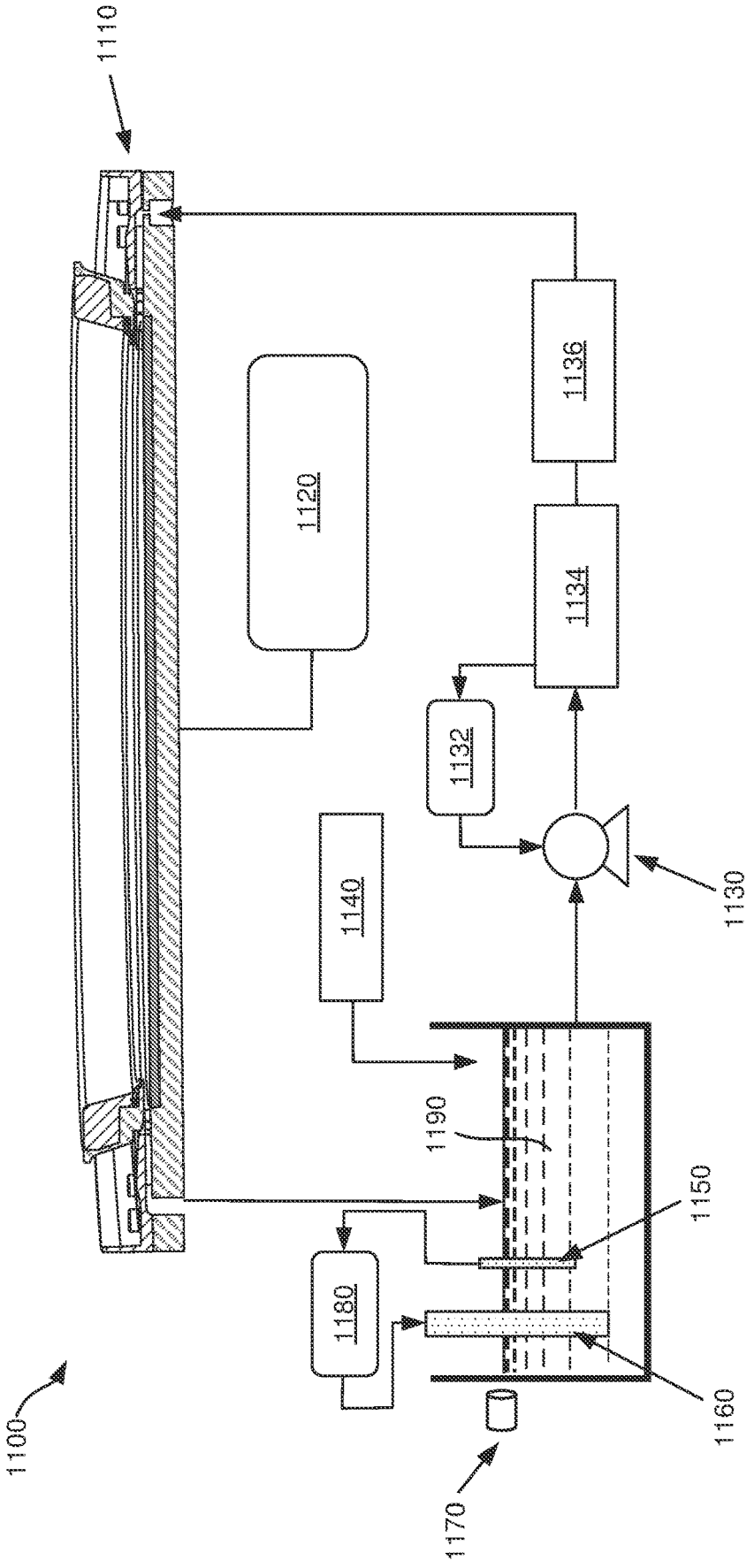

1110
1120
1136
1134
1132
1130
1140
1190
1150
1180
1160
1170
1100

FIG. 11A

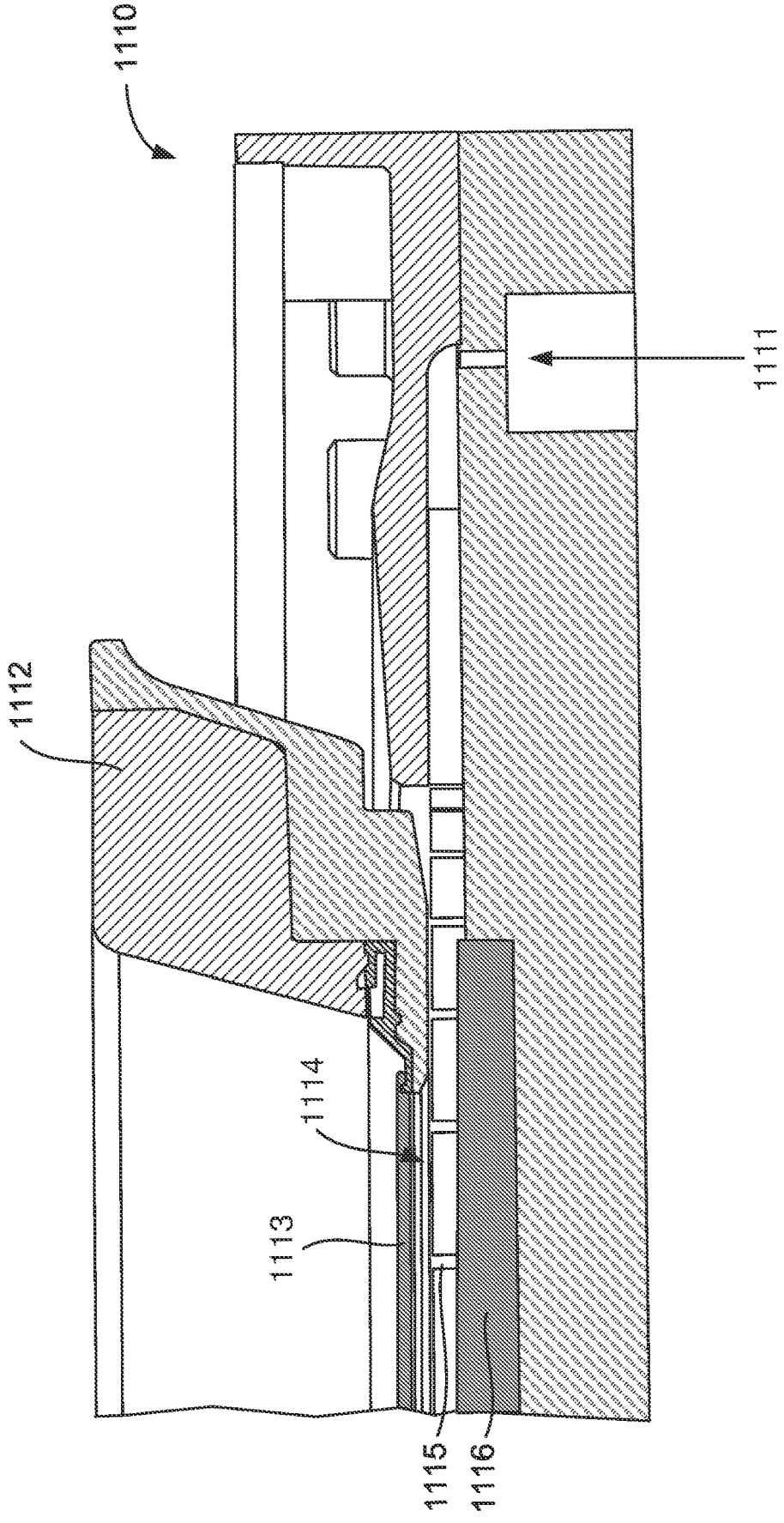


FIG. 11B

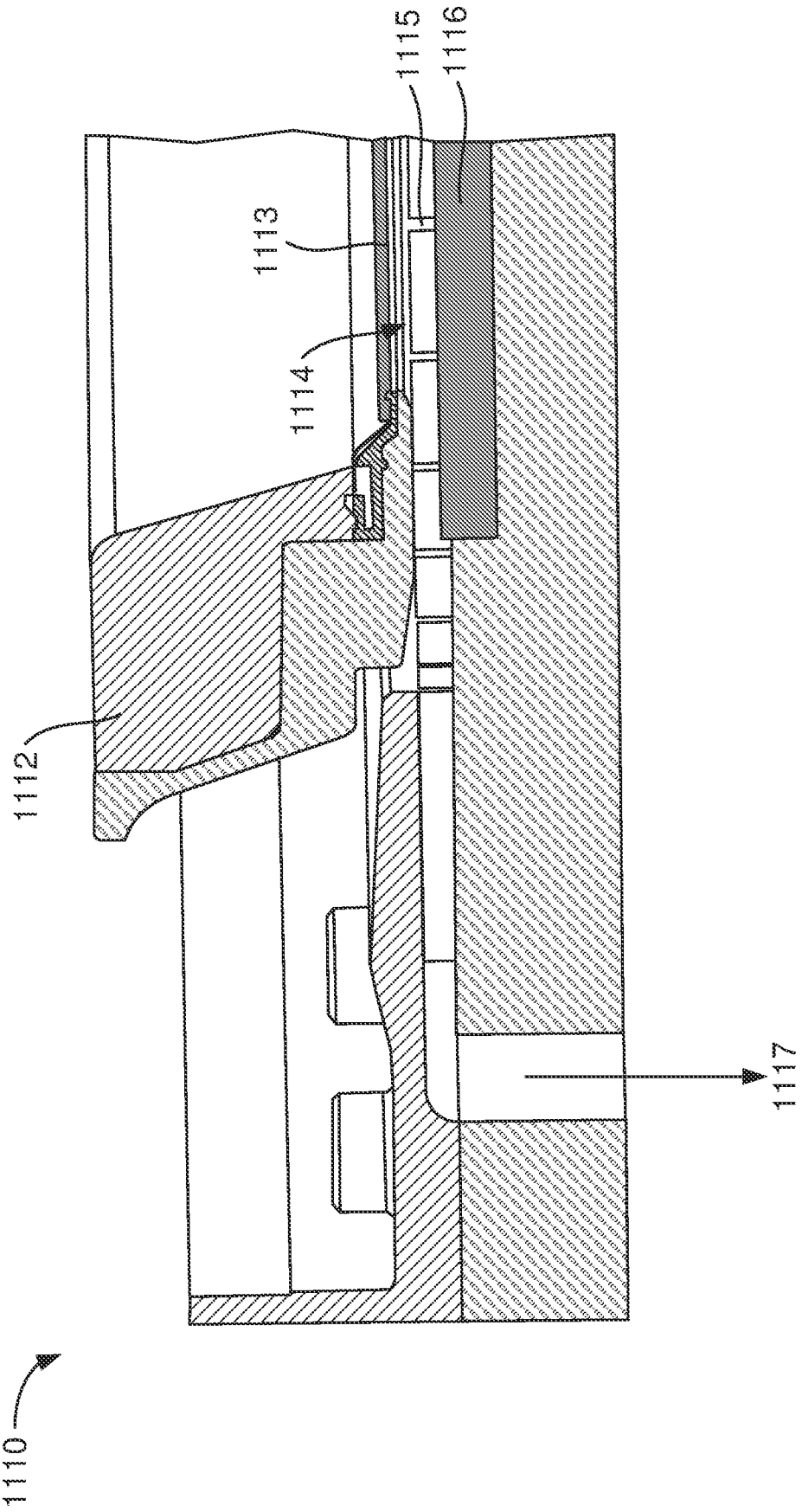


FIG. 11C

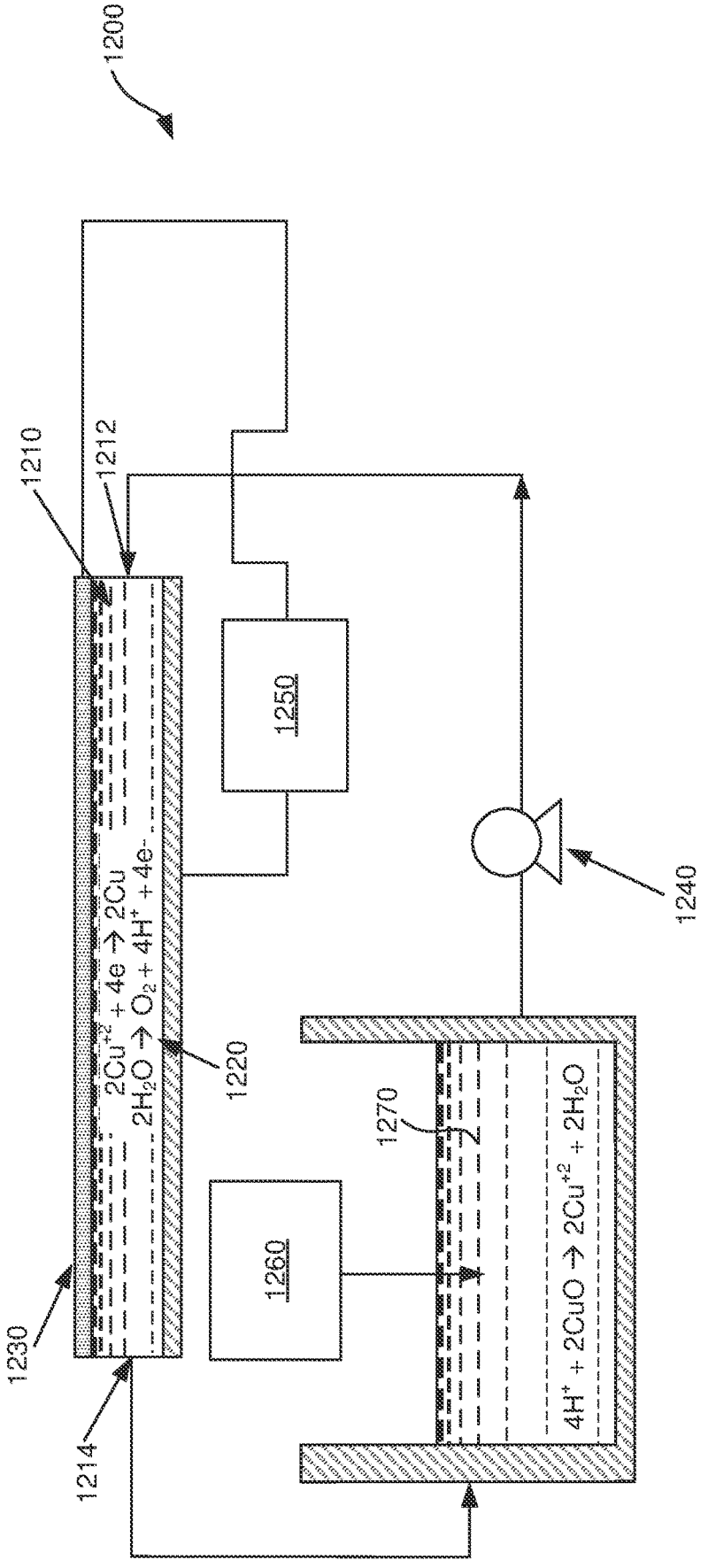

1200
1210
1212
1250
1240
1230
1214
1220
1260
1270
$2Cu^{+2} + 4e \rightarrow 2Cu$
$2H_2O \rightarrow O_2 + 4H^+ + 4e^-$
$4H^+ + 2CuO \rightarrow 2Cu^{+2} + 2H_2O$

FIG. 12

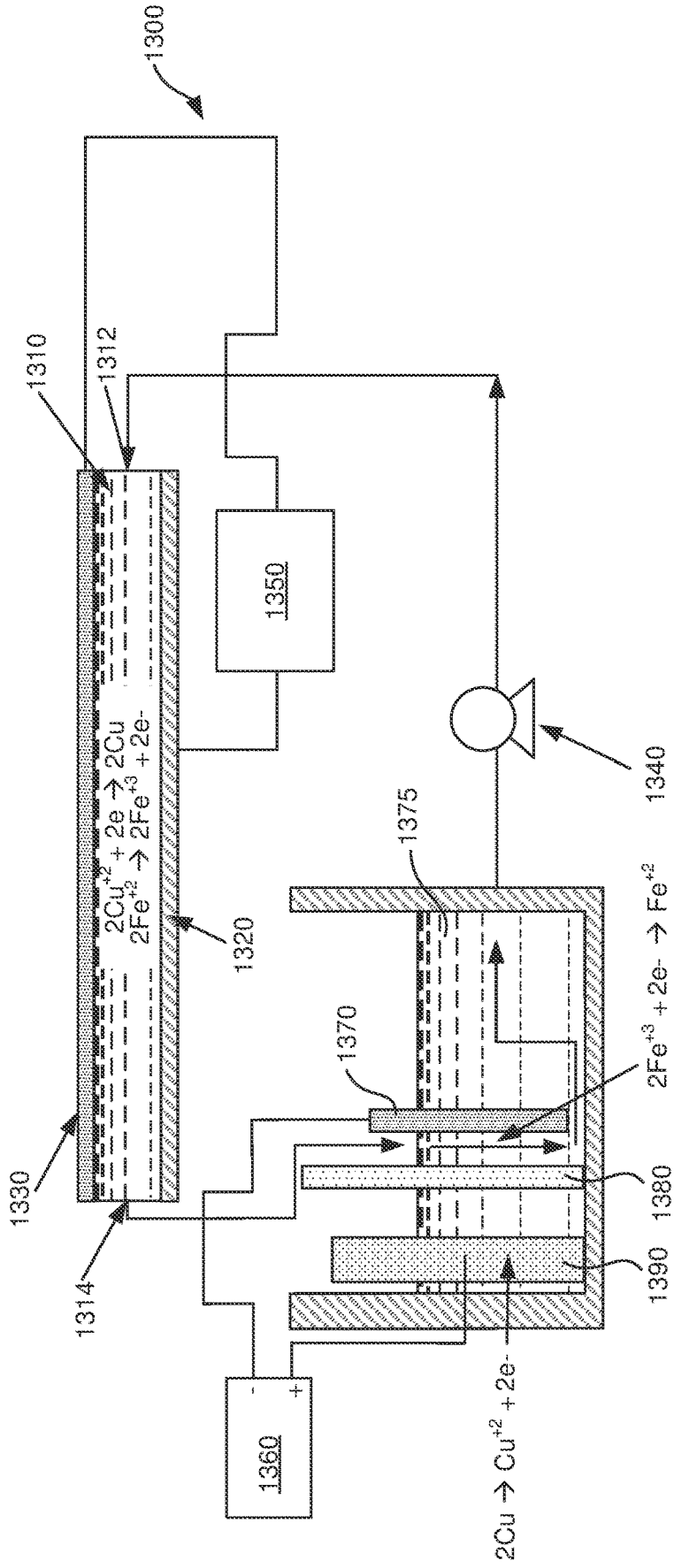

1300
1310
1312
1350
1340
1375
1320
1370
1330
1380
1314
1390
1360
$2Cu^{+2} + 2e \rightarrow 2Cu$
$2Fe^{+2} \rightarrow 2Fe^{+3} + 2e-$
$2Fe^{+3} + 2e- \rightarrow Fe^{+2}$
$2Cu \rightarrow Cu^{+2} + 2e-$

FIG. 13

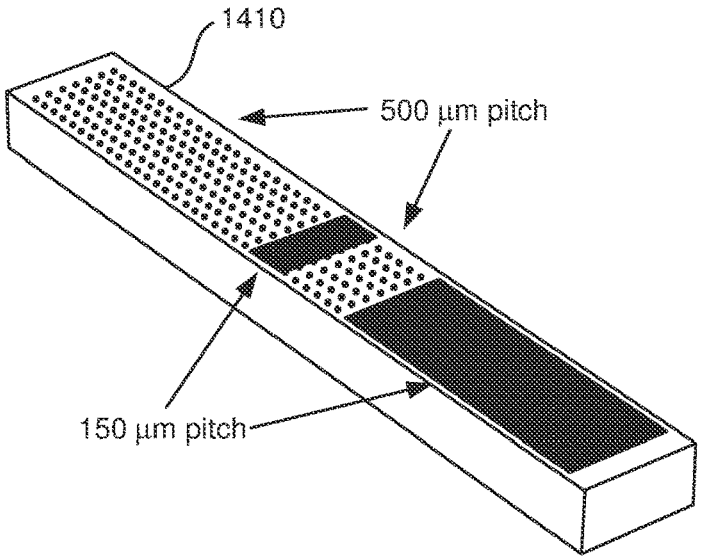


FIG. 14A

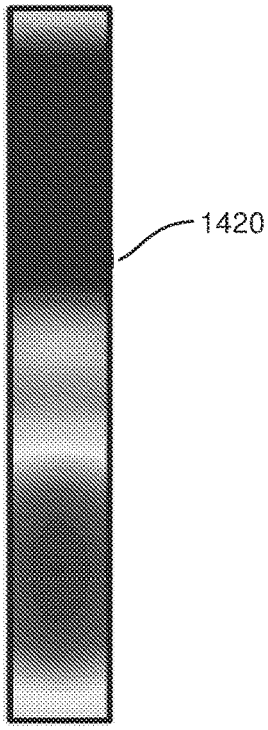


FIG. 14B

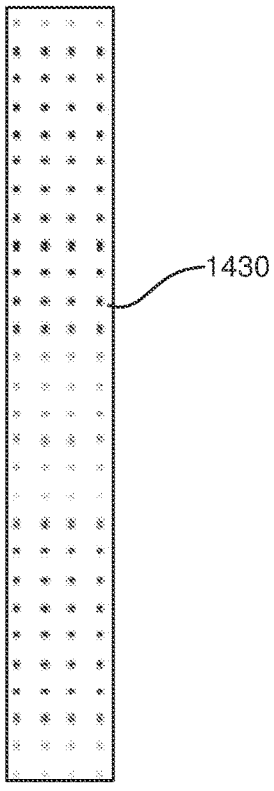


FIG. 14C

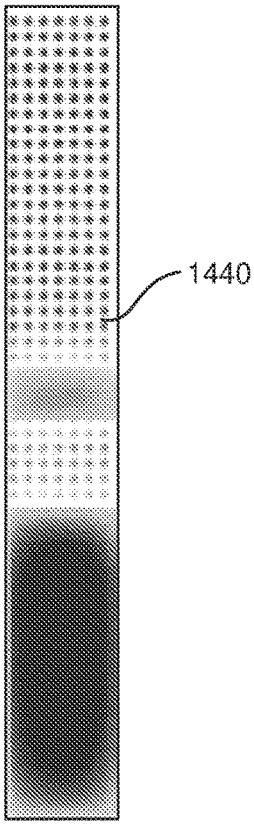


FIG. 14D

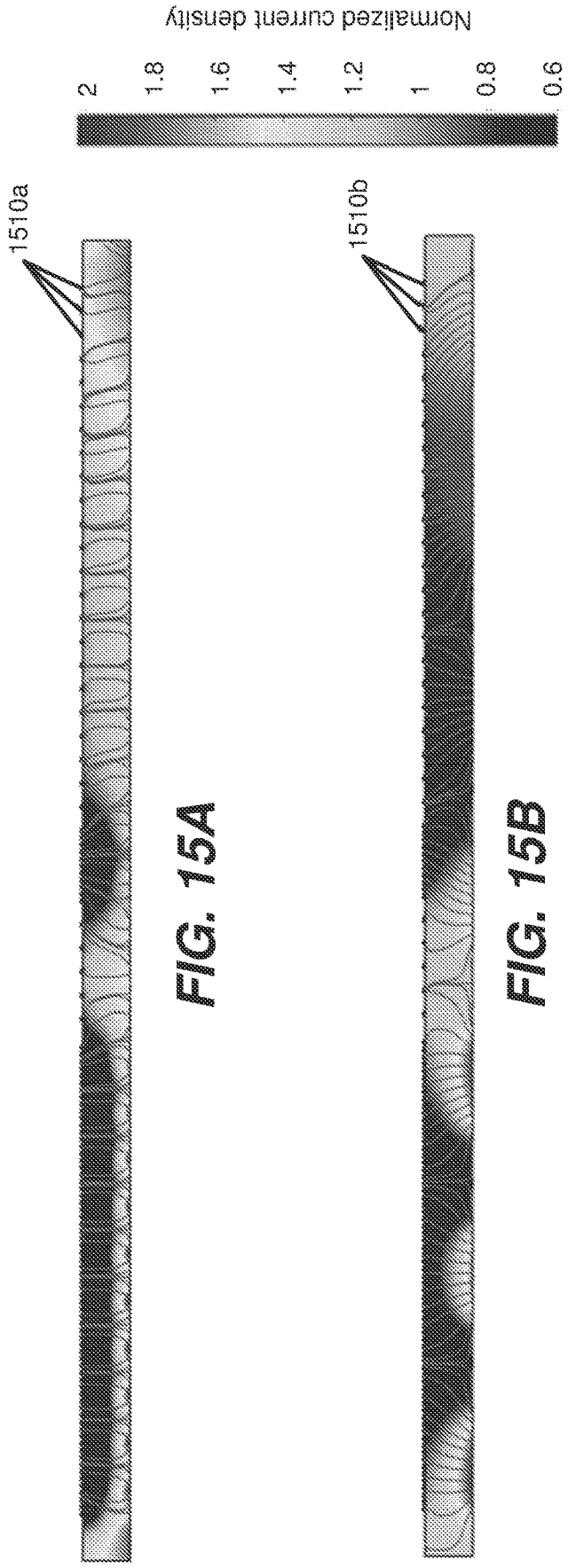


FIG. 15A

FIG. 15B

FIG. 15C

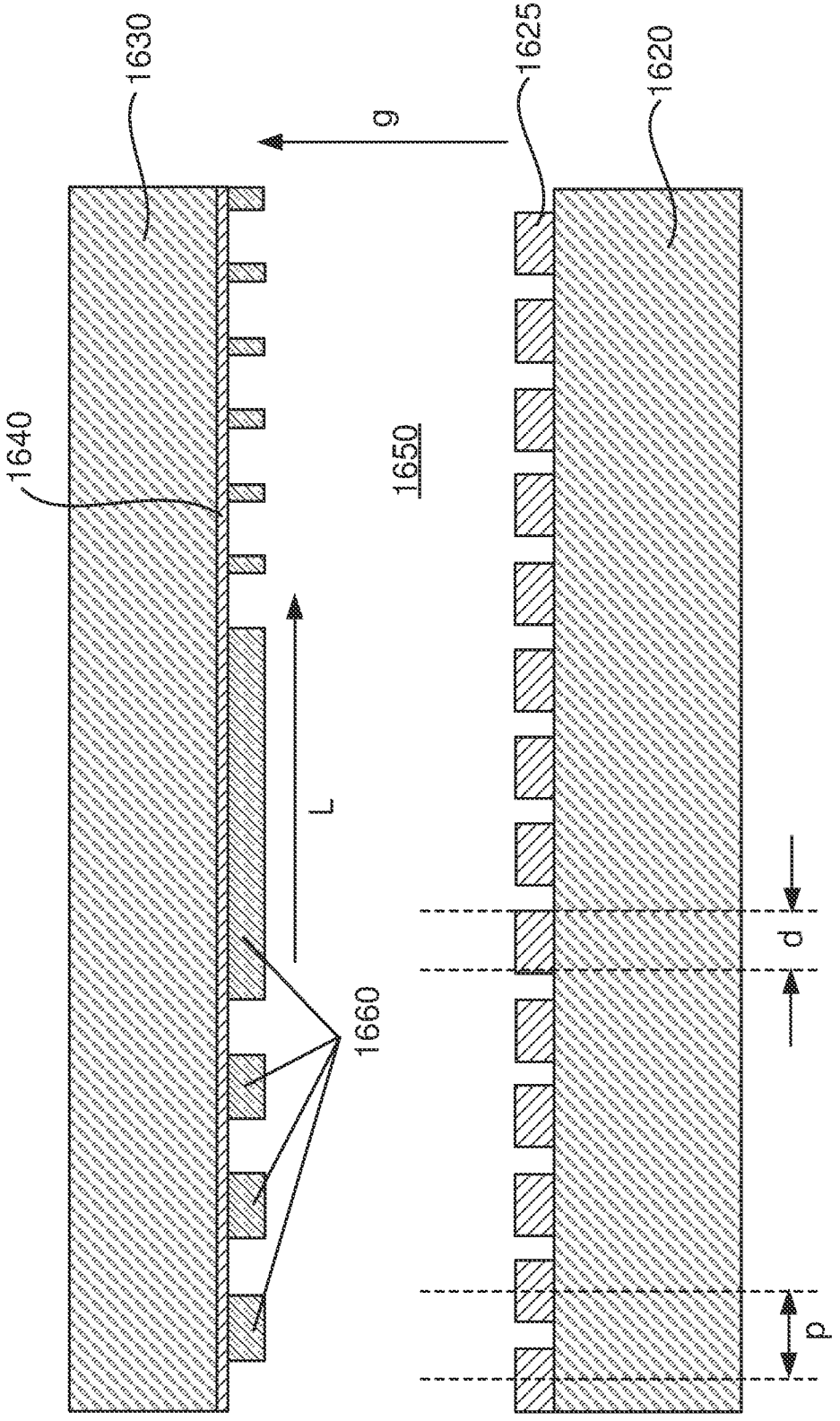


FIG. 16

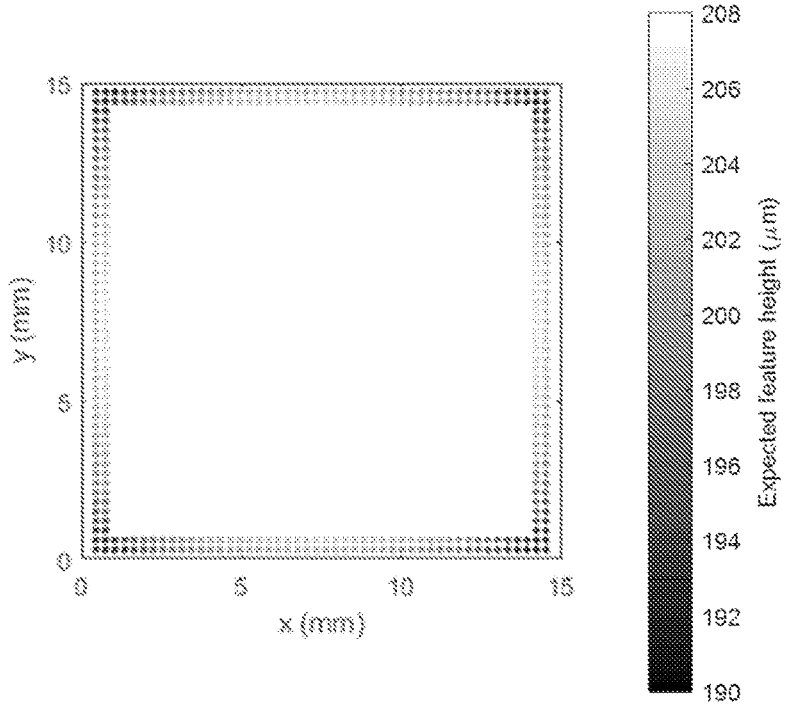


FIG. 17A

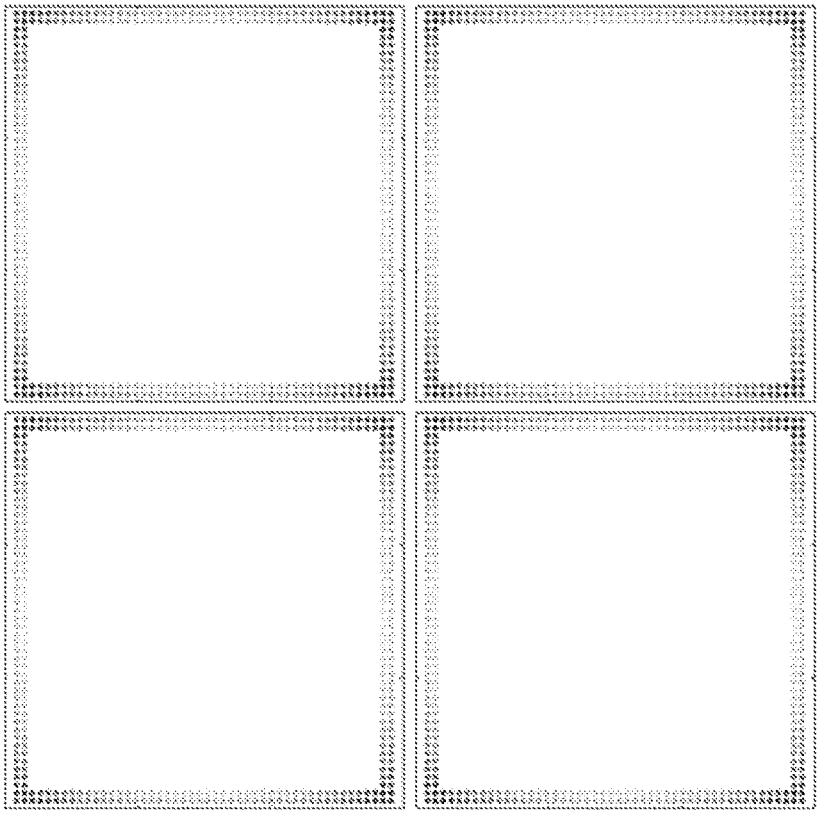


FIG. 17B

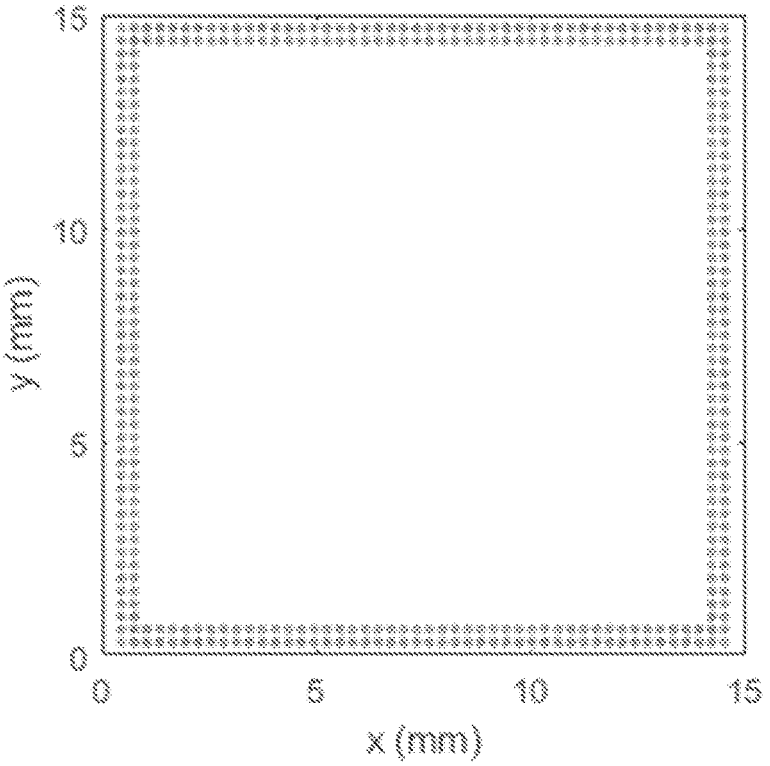


FIG. 17C

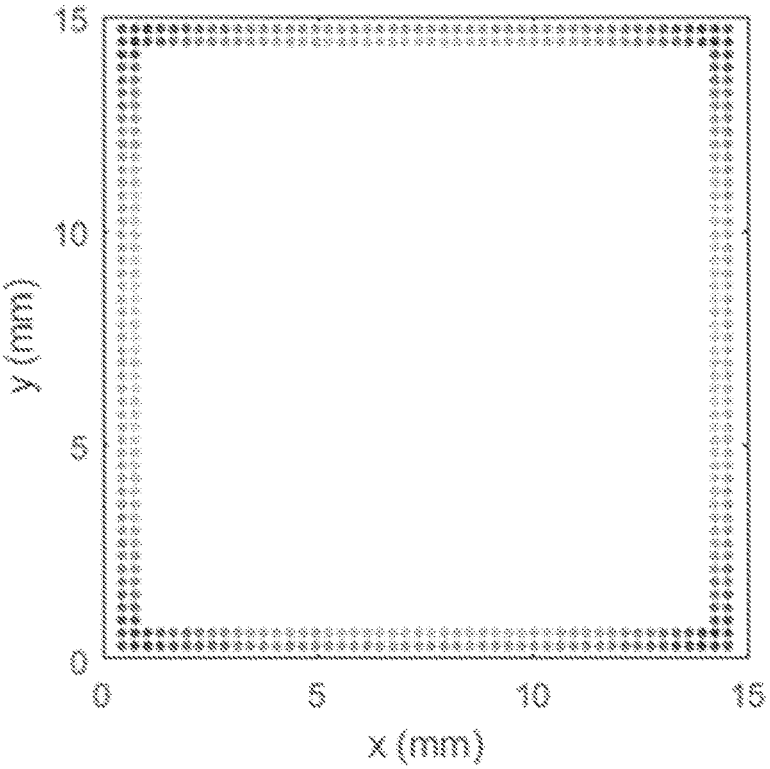


FIG. 17D

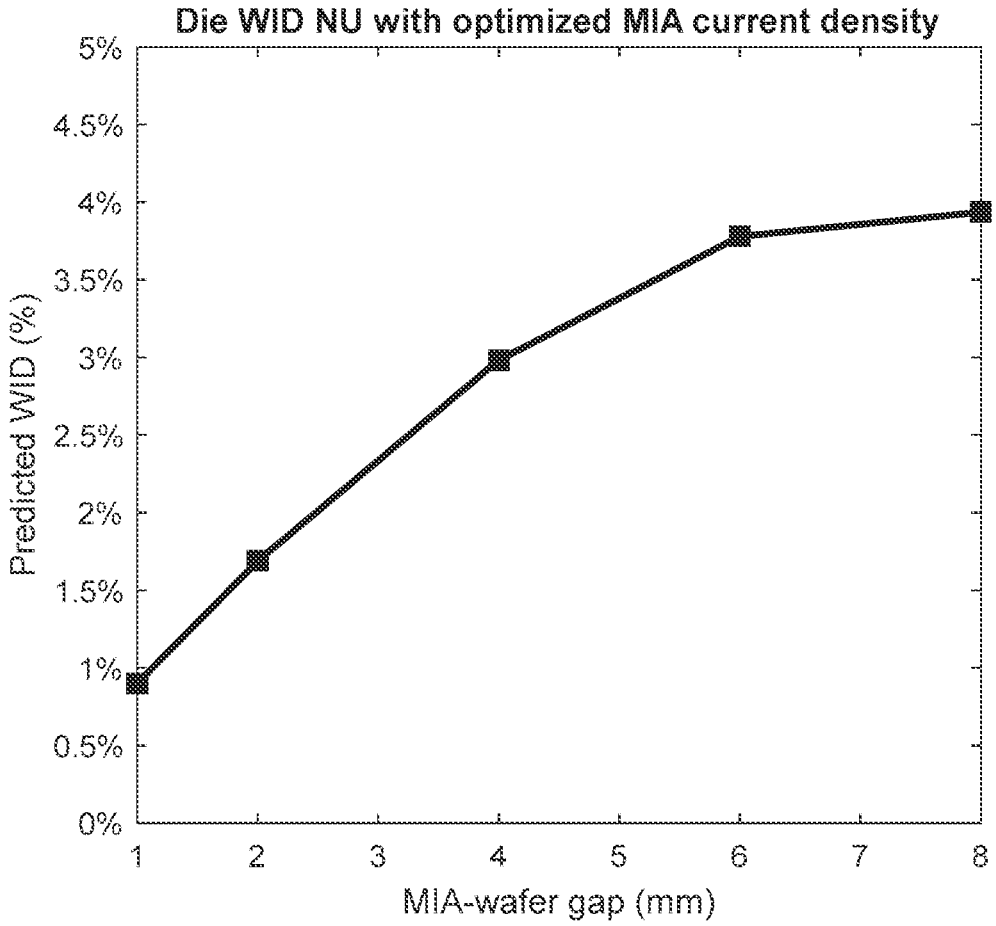

Die WID NU with optimized MIA current density
Predicted WID (%)
5%
4.5%
4%
3.5%
3%
2.5%
2%
1.5%
1%
0.5%
0%
1
2
3
4
5
6
7
8
MIA-wafer gap (mm)

FIG. 18

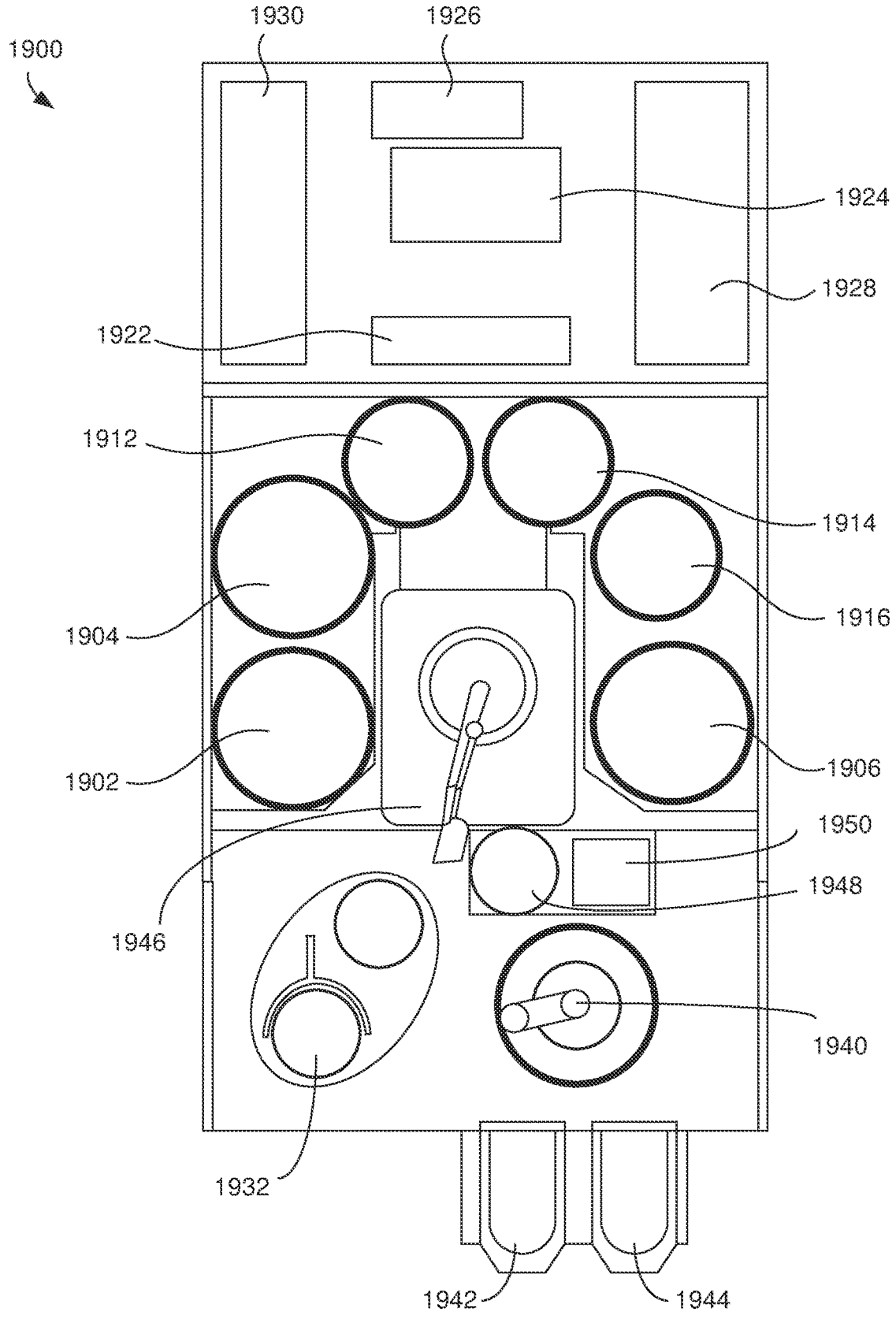

1900
1930
1926
1924
1928
1922
1912
1914
1904
1916
1902
1906
1950
1948
1946
1940
1932
1942
1944

FIG. 19

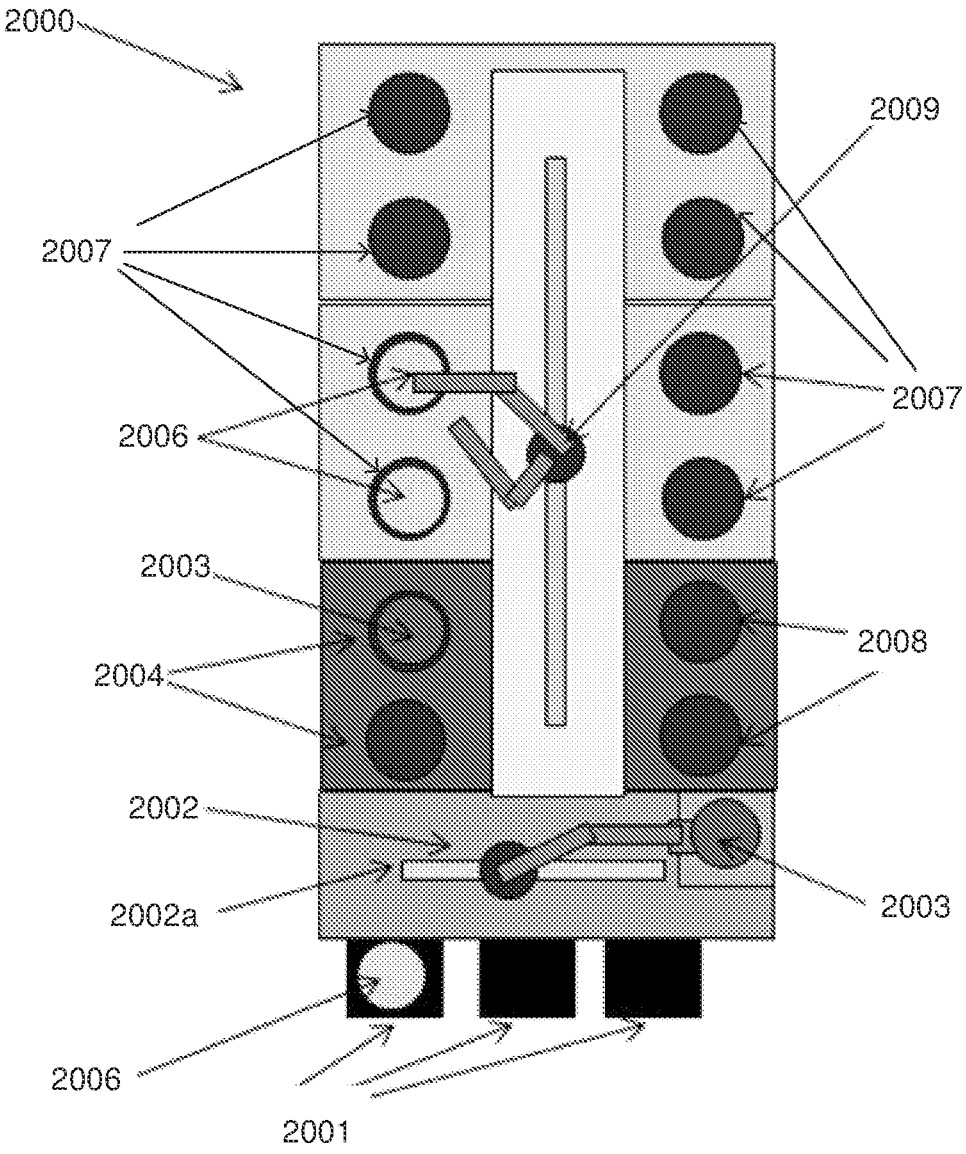

2000
2009
2007
2007
2006
2003
2008
2004
2002
2002a
2003
2006
2001

FIG. 20

MICRO INERT ANODE ARRAY FOR DIE LEVEL ELECTRODEPOSITION THICKNESS DISTRIBUTION CONTROL

INCORPORATION BY REFERENCE

[0001] A PCT Request Form is filed concurrently with this specification as part of the present application. Each application that the present application claims benefit of or priority to as identified in the concurrently filed PCT Request Form is incorporated by reference herein in its entirety and for all purposes.

FIELD

[0002] Implementations herein relate to methods and apparatuses for electroplating metal on a semiconductor wafer. More particularly, the methods and apparatuses described herein relate to controlling current distribution for die layouts when electroplating metal on semiconductor wafers.

BACKGROUND

[0003] In semiconductor device manufacturing, a conductive material, such as copper, is often deposited by electroplating onto a seed layer of metal to fill one or more recessed features on a semiconductor wafer. Electroplating is a method of choice for depositing metal into the vias and trenches of the wafer during damascene processing, and is also used in through-resist plating in wafer level packaging (WIP) applications to form pillars and lines of metal. Another application of electroplating is filling through-silicon vias (TSVs), which are relatively large vertical electrical connections used in 3D integrated circuits and 3D packages.

[0004] In some electroplating substrates, the seed layer is exposed over the entire surface of the substrate prior to electroplating (typically in damascene and TSV processing), and electroplating of metal occurs over the entirety of the substrate. In other electroplating substrates, a portion of the seed layer is covered by a non-conducting mask material, such as by photoresist, while another portion of the seed layer is exposed. In such substrates with a partially masked seed layer, electroplating occurs only over the exposed portions of the seed layer while the covered portions of the seed layer are protected from being plated upon. Electroplating on a substrate having a seed layer that is coated with patterned mask material (e.g., photoresist) is referred to as mask plating and is typically used in WLP applications.

[0005] Fabrication of semiconductor devices commonly involves a series of steps for forming fine line interconnects and other metallic features. For example, in the area of 3D packaging, WLP applications may involve forming a conductive seed layer on the semiconductor substrate, forming a layer of photoresist on the conductive seed layer, and exposing and developing the layer of photoresist to define a pattern therein, where the pattern typically repeats over a certain size scale and shape and may be referred to as a "die." After metallization operations, the semiconductor wafer is typically sliced ("diced") into functionally identical entities (referred to as "die") before undergoing further packaging operations involving other semiconductor wafers and die. However, it will be understood that the die on the semiconductor wafer need not be functionally identical entities.

[0006] Lines, pads, and pillars are typically plated to create bonds between substrates and to create interconnecting electrical connections within and between die of differing functions. It is generally desirable for electroplating to produce acceptable within-die (WID), within-wafer (WIW), and within-feature (WIF) plating non-uniformity.

[0007] The background provided herein is for the purposes of generally presenting the context of the disclosure. Work of the presently named inventors, to the extent that it is described in this background, as well as aspects of the description that may not otherwise qualify as prior art at the time of filing, are neither expressly nor impliedly admitted as prior art against the present disclosure.

SUMMARY

[0008] Provided herein is a method of electroplating metal features on a substrate. The method includes receiving a substrate in an electroplating chamber, where the substrate includes one or more dice having a distribution of patterned features, contacting the substrate with an electrolyte in the electroplating chamber, and electroplating metal on the substrate using a micro inert anode array having a plurality of micro inert anode elements, wherein current is applied to two or more micro inert anode elements to provide a non-uniform current distribution over an area of the substrate. In some implementations, the substrate is a partially fabricated semiconductor substrate.

[0009] In some implementations, the current is applied to two or more micro inert anode elements to provide the non-uniform current distribution that is based at least in part on patterned feature layouts of the one or more dice. In some implementations, the current is applied to two or more micro inert anode elements to provide the non-uniform current distribution that is based at least in part on global within-wafer (WIW) corrections. In some implementations, the current is applied to two or more micro inert anode elements to provide the non-uniform current distribution that is based at least in part on global within-wafer (WIW) corrections. In some implementations, the one or more dice comprise layouts of patterned features, wherein the area over which the non-uniform current distribution is applied includes a distance between repeating layouts of patterned features, and wherein the distance is larger than a pitch defined between micro inert anode elements and larger than a gap size defined between the substrate and the micro inert anode array. In some implementations, a gap size defined between the substrate and the micro inert anode array is equal to or greater than a pitch defined between micro inert anode elements in the micro inert anode array. In some implementations, the gap size is at least three times greater than the pitch defined between micro inert anode elements and at least three times greater than a critical dimension of each micro inert anode element. In some implementations, a gap size defined between the substrate and the micro inert anode array is equal to or less than about 4 mm. In some implementations, a pitch defined between micro inert anode elements in the micro inert anode array is equal to or less than about 500 μm. In some implementations, contacting the substrate with the electrolyte includes cross-flowing the electrolyte laterally across the surface of the substrate. In some implementations, the method further includes identifying patterned feature layouts in the one or more dice in the substrate prior to electroplating metal on the substrate using the micro inert anode array. In some implementations, the

method further includes determining a current distribution on an anode ground plane from a uniform die current distribution through a simulation or calculation to obtain a simulated or calculated current distribution, and assigning current values to each of the micro inert anode elements in the micro inert anode array based on the simulated or calculated current distribution on the anode ground plane. In some implementations, the method further includes rotating the substrate while electroplating metal on the substrate using the micro inert anode array; and changing current applied to the two or more micro inert anode elements to achieve a new current distribution based at least in part on positioning of patterned feature layouts of the one or more dice after rotation. In some implementations, each of the micro inert anode elements are physically isolated from one another, electrically isolated from one another, and independently controllable to receive current from a power source. In some implementations, the metal is electroplated with a substantially uniform thickness in the one or more dice having a distribution of patterned features. In some implementations, the substrate has patterned photoresist over a conductive seed layer, wherein the metal is electroplated in recessed features defined by the patterned photoresist and on exposed portions of the conductive seed layer.

[0010] Also provided herein is an electroplating apparatus that includes a substrate holder configured to hold a partially fabricated semiconductor substrate, where the partially fabricated semiconductor substrate comprises one or more dice having a distribution of patterned features.

[0011] The electroplating apparatus further includes a micro inert anode array proximate the partially fabricated semiconductor substrate, wherein the micro inert anode array includes a plurality of independently controllable micro inert anode elements arranged in an array, and a cross-flow manifold configured to contain an electrolyte flowing between the micro inert anode array and the partially fabricated semiconductor substrate, wherein the cross-flow manifold promotes cross flowing of the electrolyte across the surface of the partially fabricated semiconductor substrate.

[0012] In some implementations, the one or more dice have a non-uniform distribution of patterned features. In some implementations, a gap size defined between the partially fabricated semiconductor substrate and the micro inert anode array is equal to or greater than a pitch defined between micro inert anode elements in the micro inert anode array. In some implementations, the gap size is equal to or less than about 4 mm and wherein the pitch is equal to or less than about 500 μm. In some implementations, the micro inert anode array comprises at least 100 micro inert anode elements. In some implementations, the electroplating apparatus further includes a controller configured with instructions to perform the following operations: apply current to two or more micro inert anode elements in the array to provide a desired current distribution based at least in part on a layout of patterned features in the partially fabricated semiconductor substrate. In some implementations, the controller is further configured with instructions to perform the following operations: rotate the partially fabricated semiconductor substrate while electrolyte is flowing across the surface of the partially fabricated semiconductor substrate, and change current to the two or more micro inert anode elements in the array to provide a new current distribution based at least in part on positioning of the layout of patterned features in the partially fabricated semiconductor substrate after rotation.

[0013] Also provided herein is an electroplating apparatus that includes a substrate load/unload station configured to receive a semiconductor substrate, a substrate pretreatment station configured to pretreat the semiconductor substrate, and one or more electroplating stations configured to plate metal on the semiconductor substrate. Each electroplating station includes a substrate holder configured to hold the semiconductor substrate, a micro inert anode array comprising a plurality of independently controllable micro inert anode elements, where the micro inert anode array is spaced apart from the semiconductor substrate by a gap that is greater than a pitch between the micro inert anode elements, and a plating bath reservoir configured to deliver electrolyte to the gap between the micro inert anode array and the semiconductor substrate. The electroplating apparatus further includes one or more robots configured to transfer the semiconductor substrate between the substrate load/unload station and the substrate pretreatment station and between the substrate pretreatment station and the one or more electroplating stations.

[0014] In some implementations, the substrate pretreatment station comprises one or both of a vacuum backfill station and an acid pre-wetting station. In some implementations, each of the one or more electroplating stations further includes a flow controller configured to control a flow and chemical dosing of the electrolyte delivered to the gap between the micro inert anode array and the semiconductor substrate, a temperature controller configured to control a temperature of the electrolyte in the plating bath reservoir, and a degasser configured to remove dissolved gases from the electrolyte prior to delivery into the gap between the micro inert anode array and the semiconductor substrate. In some implementations, each of the one or more electroplating stations further includes a metal oxide dose control unit configured to dose the electrolyte in the plating bath reservoir with metal oxide to mitigate acidification and metal ion depletion in the electrolyte. In some implementations, each of the one or more electroplating stations further includes a soluble ion redox couple configured regenerate one or more metal ions in the electrolyte and prevent acidification and metal ion depletion in the electrolyte. In some implementations, the electroplating apparatus further includes one or more additional electroplating stations without a micro inert anode array and configured to plate metal on the semiconductor substrate.

[0015] Also provided herein is a method of modeling a current distribution in a micro inert anode array. The method includes receiving a substrate having a die with a non-uniform distribution of features, determining a current distribution on an anode ground plane from a uniform die current distribution in the die of the substrate, and assigning current values to each of a plurality of micro inert anode elements in a micro inert anode array based on the current distribution on the anode ground plane.

[0016] In some implementations, the anode ground plane corresponds to a counter electrode having a continuous conductive surface. In some implementations, the substrate is a partially fabricated semiconductor substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] FIG. **1** illustrates a flow diagram of an example method of electroplating patterned metal features on a substrate.

[0018] FIG. **2** illustrates a flow diagram of an example method of electroplating metal features on a substrate using a micro inert anode array according to some implementations.

[0019] FIG. **3** illustrates a simplified diagram of an example electroplating apparatus including multiple inert anode array plating stations according to some implementations.

[0020] FIG. **4**A illustrates a perspective close-up view of a cross-flow side inlet and surrounding hardware including a high resistance virtual anode (HRVA) of an electroplating apparatus.

[0021] FIG. **4**B illustrates a perspective close-up view of a cross-flow outlet and surrounding hardware including an HRVA of the electroplating apparatus.

[0022] FIG. **4**C illustrates a cross-sectional view of various parts of the electroplating apparatus shown in FIGS. **4**A and **4**B.

[0023] FIG. **4**D illustrates a cross-sectional view of a flow injection manifold relative to a plating cup of the electroplating apparatus.

[0024] FIG. **5**A illustrates a perspective close-up view of a cross-flow side inlet and surrounding hardware including a micro inert anode array of an electroplating apparatus according to some implementations.

[0025] FIG. **5**B illustrates a perspective close-up view of a cross-flow outlet and surrounding hardware including a micro inert anode array of the electroplating apparatus according to some implementations.

[0026] FIG. **5**C illustrates a cross-sectional view of various parts of the electroplating apparatus shown in FIGS. **5**A and **5**B.

[0027] FIG. **5**D illustrates a cross-sectional view of a flow injection manifold relative to a plating cup of the electroplating apparatus according to some implementations.

[0028] FIGS. **6**A and **6**B illustrate schematic diagrams of flow direction of electrolyte and its impact on plating within a patterned feature.

[0029] FIG. **7**A depicts a perspective view of an example schematic micro inert anode array according to some implementations.

[0030] FIG. **7**B depicts a top view of the example schematic micro inert anode array of FIG. **7**A.

[0031] FIG. **8** shows different shapes and arrangements of inert anodes in a micro inert anode array according to some implementations.

[0032] FIG. **9** illustrates a circuit diagram of example micro inert anode array elements with active matrix control circuitry according to some implementations.

[0033] FIG. **10** depicts a top-down view of a schematic illustration of an example micro inert anode array for processing a circular semiconductor substrate according to some implementations.

[0034] FIG. **11**A illustrates a schematic diagram of an example inert anode array electroplating cell in combination with general electroplating cell fluidic and plating controls according to some implementations.

[0035] FIG. **11**B illustrates a close-up view of a schematic of the inert anode array electroplating cell including an inlet port for electrolyte according to some implementations.

[0036] FIG. **11**C illustrates a close-up view of a schematic of the inert anode array electroplating cell including an exit port for electrolyte according to some implementations.

[0037] FIG. **12** illustrates a schematic diagram of an example inert anode array electroplating cell in combination with a metal oxide dose control unit according to some implementations.

[0038] FIG. **13** illustrates a schematic diagram of an example inert anode array electroplating cell in combination with a redox couple according to some implementations.

[0039] FIGS. **14**A-**14**D illustrates a simulation model for determining current distribution in a micro inert anode array in response to identifying a die layout according to some implementations.

[0040] FIGS. **15**N-**15**C depict maps of feature current density distribution for varying anode array element pitches in a micro inert anode array.

[0041] FIG. **16** illustrates a cross-sectional schematic view of an example micro inert anode array positioned relative to a semiconductor substrate according to some implementations.

[0042] FIG. **17**A illustrates an example current distribution on a patterned feature layout of a die using an HRVA.

[0043] FIG. **17**B illustrates an example current distribution on a patterned feature layout of a die surrounded by multiple die using an HRVA.

[0044] FIG. **17**C illustrates an example current distribution of a micro inert anode array on a patterned feature layout of a die at a 1 mm gap according to some implementations.

[0045] FIG. **17**D illustrates an example current distribution of a micro inert anode array on a patterned feature layout of a die at a 4 mm gap according to some implementations.

[0046] FIG. **18** illustrates a graph showing within-die uniformity as a function of a gap between a micro inert anode array and a semiconductor substrate.

[0047] FIG. **19** depicts a simplified view of a multi-tool electroplating apparatus according to some implementations.

[0048] FIG. **20** depicts a simplified view of an example electroplating apparatus with different electroplating cells and modules according to some implementations.

DETAILED DESCRIPTION

[0049] In this application, the terms "semiconductor wafer," "wafer," "substrate," "wafer substrate," and "partially fabricated integrated circuit" are used interchangeably. One of ordinary skill in the art would understand that the term "partially fabricated integrated circuit" can refer to a silicon wafer during any of many stages of integrated circuit fabrication thereon. A wafer or substrate used in the semiconductor device industry typically has a diameter of 200 mm, or 300 mm, or 450 mm. Further, the terms "electrolyte," "plating bath," "bath," and "plating solution" are used interchangeably. The following detailed description assumes the embodiments are implemented on a wafer. However, the embodiments are not so limited. The work piece may be of various shapes, sizes, and materials. In addition to semiconductor wafers, other work pieces that may take advantage of the disclosed embodiments include various articles such as glass panels, printed circuit boards, magnetic recording media, magnetic recording sensors, mirrors, optical elements, micro-mechanical devices and the like. Work pieces

in the disclosed embodiments may include substrates with seed layers and masked surfaces, which can include semiconductor wafers, printed circuit boards, panels, and the like.

[0050] In the following description, numerous specific details are set forth in order to provide a thorough understanding of the presented embodiments. The disclosed embodiments may be practiced without some or all of these specific details. In other instances, well-known process operations have not been described in detail to not unnecessarily obscure the disclosed embodiments. While the disclosed embodiments will be described in conjunction with the specific embodiments, it will be understood that it is not intended to limit the disclosed embodiments.

INTRODUCTION

[0051] Within-wafer (WIW) uniformity is an industrially important metric measuring variations of features over a wafer. WIW uniformity compares the average thickness distribution of multiple die over a substrate and may provide an indication of how the process will be for different die from different location for a set of die coming from the wafer. The WIW distribution can be non-uniform due to a number of factors, including but not limited to: variable flow, non-uniform electric fields, and wafer edge contact uncompensated seed resistance terminal effects. The methods and apparatuses of the present disclosure can improve the WIW uniformity and offer more rapid, less manually intense, and simpler adjustments of hardware to achieve improved WIW results relative to conventionally-employed electroplating apparatuses and methods.

[0052] Within-die (WID) uniformity is a measure of the variable thickness of all the features within the die and can be compared relative to the wafer total feature thickness distribution and relative to other die. For example, small VID variability makes developing overlaying film of subsequent layers less challenging and more reliable, or bonding to pillars and pads of multiple features across die between two different die less challenging and more reliable. Even when the electric and flow fields are uniform over a die, WID non-uniform plating may occur. A thickness distribution of the various features within the die are primarily driven by a variability in exposure of various features and regions of features. This is sometimes referred to as a "feature density distribution" or the "loading effect," and occurs because the electric and mass transfer field resistances around features and regions of features of lower densities are less than for regions of denser features. The apparatuses and methods of the present disclosure can improve the WID uniformity and offer more rapid, less manually intense, and simpler adjustments of hardware to achieve improved WID results relative to conventionally-employed apparatuses and methods.

[0053] Within-feature (WIF) uniformity is a measure of the shape of the top surface of a feature's flatness relative to a base plane and relative to other features. For example, small WIF uniformity makes developing overlaying film of subsequent layers less challenging or more reliable, or bonding individual pillars and pads of two different die less challenging and more reliable. The apparatuses and methods of the present disclosure can improve the WIF uniformity and offer more rapid, less manually intense, and simpler adjustments of hardware to achieve improved WIF results relative to conventionally-employed apparatuses and methods.

[0054] Electroplating through a lithographic mask, or photoresist (PR), is often used to form metal bumps and pillars in advanced semiconductor device fabrication such as in WLP applications. FIG. **1** illustrates a flow diagram of an example method of electroplating patterned metal features on a substrate. A typical process using through-mask electroplating may involve the following process operations.

[0055] First, at block **100**, a substrate (e.g., a semiconductor substrate having, a planar exposed surface) is coated with a thin conductive seed layer material (e.g., Cu). The conductive seed layer may be deposited by any suitable deposition method such as physical vapor deposition (PVD).

[0056] Next, at block **110**, a non-conductive mask layer, such as a photoresist, is deposited over the conductive seed layer. The photoresist may be formed through wet processing methods such as spin coating and allowing solvents to evaporate/dry, or it may be formed through dry methods such as chemical vapor deposition or applying a roll of pre-formed photoresist material over the substrate and applying heat, for example.

[0057] Next, at block **120**, the photoresist may be patterned to define recessed features (e.g., round or polygonal holes). The photoresist may be patterned through exposure to particular irradiation conditions.

[0058] Afterwards, at block **130**, the photoresist is developed. The substrate may be transferred to a photoresist developing apparatus, where the pattern exposed on the substrate is developed. In one example, the photoresist is developed through a wet chemical treatment that involves exposing the substrate to a solution having a dissolution salt. These patterning operations result information of recessed features in the photoresist with portions of the conductive seed layer exposed. The recessed features define selective spaces where metal will be subsequently deposited. The substrate may be a partially fabricated semiconductor substrate having patterned features in one or more dice.

[0059] Next, at block **140**, a descumming operation is optionally performed to remove residual or excess photoresist material left on the substrate. The substrate may be transferred to a plasma etching apparatus to perform descumming. In some embodiments, descumming can provide an additional benefit of creating a more hydrophobic surface improving wettability. In some embodiments, descumming typically involves exposure to an oxygen-containing plasma that acts to remove excess photoresist at the bottom of the recessed features. In alternative embodiments, descumming can be accomplished by applying an aqueous solution containing an oxidizing agent (e.g., ozone) to the surface of the substrate. In some embodiments, a chamber for descumming may be part of a plating chamber or apparatus. In some other embodiments, the chamber for descumming may be a separate tool or separate station from a plating tool. However, integrating the chamber for descumming with the plating chamber or apparatus may reduce capital costs, reduce time between descumming and plating operations, and reduce exposure to ambient conditions.

[0060] Next, at block **150**, metal is electroplated in regions of the substrate defined by the patterned photoresist. This process forms metal features defined according to the patterned photoresist. The substrate may be transferred to a plating station or chamber. Optionally, the substrate may be

treated or may undergo wetting prior to electroplating. In the plating station or chamber, the substrate is cathodically biased and contacted with electroplating solution, Metal is electrodeposited on substrate surfaces defined by the patterned photoresist.

[0061] After that, at block **160**, photoresist may be stripped from the substrate. In some embodiments, the substrate may undergo rinsing, drying, and/or cleaning in a rinse/dry/clean station. The substrate may be transferred to a photoresist stripping station, or to a separate tool or apparatus, where the photoresist is stripped. The photoresist may be stripped using dry plasma etching techniques such as exposing the photoresist to oxygen-containing plasma Or, the photoresist may be stripped using wet etching techniques such as exposing the photoresist to photoresist solvents to dissolve or swell the photoresist. After the photoresist is removed, portions of the conductive seed layer are optionally removed. The substrate may be transferred to a chemical etching apparatus where the conductive seed layer is removed in regions without plating that were previously protected by the patterned photoresist. In some embodiments, the conductive seed layer may be removed by isotropic chemical etching.

[0062] Through-mask electroplating (or, in the case of usage of a photoresist, through-resist electroplating) may involve positioning of the substrate in an electroplating apparatus such that electrical contact is made to the seed layer at the periphery of the substrate. The electroplating apparatus houses an anode and an electrolyte that contains ions of a metal intended to be used for plating. The substrate is cathodically biased and immersed into an electrolyte solution, which provides metal ions that are reduced at the surface of the substrate, as described in the following equation, where, M is a metal (e.g., copper), and n is the number of electrons transferred during the reduction:

$$M^{n+} + ne^- \longrightarrow M^0$$

[0063] Because the conductive seed layer is exposed to the electrolyte solution only at the bottom portions of the recessed features, electrochemical deposition, e.g. as facilitated by a through-mask electroplating process, occurs only within the recessed features, and not on the field, e.g. a top layer of the mask or photoresist exposed to the electrolyte solution. Thus, through-mask electroplating may be used to at least partially fill recesses in the mask with metal. After electroplating, the mask or photoresist may be removed by a conventional stripping method to thus result in the substrate having a number of free-standing metal bumps, pillars, lines, pads, or other metal features.

[0064] It is typically desirable for the rate of deposition within recessed features to be uniform, i.e., at the end of the process each feature has a similar height of metal deposited and is thus co-planar. Co-planarity may be improved with an etch process, such as an electrochemical etching or polishing process, to reduce the height of taller features (e.g., pillars). If the feature within a die are co-planar to each other and to the substrate, then the die will have a good (small) WID distribution value. In some embodiments a chemical mechanical planarization (CMP) process is used to etch back pillars, which may remove the photoresist. An alternative etch process is an electro-oxidative method, which may be used to remove plated metal to improve co-planarity without removing the photoresist. An alternative process to achieve improved uniformity is an electroplating process that electroplates faster in deep features (or deep within features) and comparatively slower in shallow features. This may be accomplished by carefully controlling the deposition conditions and particularly the use of plating additives such as levelers under conditions that limit the levelers' mass transport into the features. Concentration of plating additives may be controlled to improve co-planarity and reduce metal feature height differences within a die or within a wafer. Usage of a certain electroplating bath can result in differential plating rates between features for improving process qualities including WIW uniformity, WID uniformity, and WIF uniformity. As referred to herein, the terms "non-uniformity" and "uniformity" generally refers to observed variation of the height of metal relative to the substrate plated in a target feature on a substrate. Thus, improvement of non-uniformity involves reducing unwanted variation of at least one process quality, e.g. WID. Though it is typically desirable to achieve uniformity of metal feature height in plating, it will be understood that in some cases it may be desirable to plate different feature geometries and heights,

Electroplating with Micro Inert Anode Array

[0065] The present disclosure relates to electroplating metal features on a substrate using a micro inert anode array. Electroplating with a micro inert anode array provides high level of control over the spatial distribution of plating thicknesses. The micro inert anode array can be used to improve plating uniformity on a die level for multiple die layouts on a substrate. The micro inert anode array manipulates or otherwise controls an amount of current going to each of a plurality of micro inert anode array elements in the micro inert anode array. This creates a pattern in current distribution that can be used to modify plating rates by driving more or less current to regions that require more or less current (e.g., due to variability in local feature density). When the micro inert anode array is placed in close proximity to a substrate surface, the electric fields in the electrolyte can be programmed or controlled locally rather than globally as is typical for standard anodes. This control may be based in part on a through-resist pattern of a particular surface layout or die layout. Thus, using the die layout on a substrate, the current distribution in the micro inert anode array can be determined. Additionally, the current distribution in the micro inert anode array may be adjusted in real-time during electroplating. For example, adjustments in current distribution may be made based at least in part on an angular position and rotational path of a rotating substrate. Additionally, as the various features grow within the photoresist cavity, the current applied to the various micro anodes in the array and to the regions of high density versus lower density may be changed over time during the plating process to obtain a more uniform end result. Control over current distribution in the micro inert anode array addresses various plating uniformity challenges such as WID non-uniformity.

[0066] FIG. **2** illustrates a flow diagram of an example method of electroplating metal features on a semiconductor substrate using a micro inert anode array according to some implementations. The operations in a process shown in FIG. **2** may be performed in different orders and/or with different, fewer, or additional operations.

[0067] At block **200**, a semiconductor substrate is loaded. By way of an example as shown in FIG. **3**, the semiconductor substrate may be loaded in a substrate load/unload station **330**. The semiconductor substrate may be received in an electroplating apparatus with one or more plating stations. In some embodiments, the semiconductor substrate may be loaded in one or more pods or front opening unified pods (FOUPs). In some embodiments, the semiconductor substrate may have a conductive seed layer such as a copper seed layer. The conductive seed layer may be disposed on a material layer such as a dielectric layer. A patterned non-conductive mask layer or patterned photoresist may reside on the conductive seed layer. The patterned photoresist may have a plurality of recessed features formed in the photoresist material such that the conductive seed layer is exposed at bottom portions of the recessed features. These recessed features may be referred to as through-resist recessed features. The patterned photoresist may be formed according to the operations described above. The semiconductor substrate may be a partially fabricated semiconductor substrate comprising one or more dice having a distribution of features.

[0068] At block **210**, the substrate type and layouts are identified. The semiconductor substrate typically contains multiple die. Each die may have the same or different layout of features relative to adjacent dice. In some embodiments, each die may have significant variability in feature density, such as dense regions of features and regions of largely isolated features. Some die may have features having a range of different widths. Some die may have features of different depths including deep features and shallow features. This variability in feature density, depth, width, etc. generally leads to variability in metal thickness distribution after electroplating due to variability of ionic resistance and the resulting current distribution during electroplating.

[0069] WLP interconnects, namely solder bumps, pillars typically capped with solder, and/or redistribution lines (RDLs), are typically formed by through-resist plating. However, depending on the die layout and variations across the die, through-resist plating is generally not uniform and conforms to the die design layout. Variations in die design layout may stem from design rules and chip performance. Some die regions may include features (e.g., bumps) tightly packed together (smaller pitch). Some die regions may include smaller diameter features to further increase feature count. In addition, some die regions may include die streets (non-plateable empty spacing between die) that present themselves as lower area density from a plating perspective; hence it is often typical to observe die edge regions plate locally thicker (i.e., "hot areas"). It is desired in the present disclosure to produce a current distribution sufficiently near the substrate to account for die design layout and compensate for feature variations (e.g., variation in local feature density), thereby producing a desired final metallization thickness uniformity at a die level throughout the entire semiconductor substrate. Though the present disclosure is mainly described in context with and may be implemented in through-resist electroplating applications, it will be understood that the present disclosure is not limited to such applications. For instance, the present disclosure may be applied in non-WLP applications such as damascene or TSV feature filling applications.

[0070] At block **220**, the semiconductor substrate may optionally undergo substrate pre-treatment. Pre-treatment of the semiconductor substrate may reduce oxides or remove impurities such as organic impurities. In addition, the pre-treatment may involve vacuum surface pre-wetting. By way of an example shown in FIG. **3**, the semiconductor substrate may be transferred from a substrate load/unload station **330** to a substrate pre-treatment station **310** via robot **350**. In some cases, the substrate pre-treatment station **310** is configured as a vacuum backfill station. In some cases, the substrate pre-treatment station **310** is configured as an acid pre-wetting station.

[0071] At block **230**, the semiconductor substrate is immersed in electrolyte in an anode array plating station. The plating station may also be referred to as an electroplating vessel, electroplating cell, or plating chamber. The plating chamber is configured to contain an electrolyte and one or more anodes while electroplating metal onto the substrate. By way of an example shown in FIG. **3**, the semiconductor substrate may be transferred from the substrate pre-treatment station **310** to the anode array plating station **320***a* via robot **350**. The anode array plating station **320***a* may perform electroplating on the semiconductor substrate using a micro inert anode array as described below. Electroplating operations may be performed in one or more anode array plating stations **320***a*, **320***b*, **320***c*, and **320***d*. It will be understood that any of the one or more anode array plating stations **320***a*, **320***b*, **320***c*, and **320***d* may be replaced by a plating station without a micro inert anode array. In turn, some of the plating stations **320***a*, **320***b*, **320***c*, and **320***d* may include micro inert anode arrays and some of the plating stations **320***a*, **320***b*, **320***c*, and **320***d* may omit micro inert anode arrays.

[0072] The semiconductor substrate is cathodically biased via electrical contacts made to the conductive seed layer, and the substrate surface is immersed in the electrolyte containing ions of the metal to be plated. For example, the electrolyte may contain copper ions from a copper salt such as copper sulfate, copper methane sulfonate, copper pyrophosphate, copper propane sulfonate, etc. The electrolyte may include an acid increasing the electrolyte conductivity. Example acids include but are not limited to sulfuric acid and methane sulfonic acid. In some embodiments, the electrolyte includes plating additives. Plating additives modify the surface reaction kinetics and often are useful in improving the current distribution (feature shape and thickness distribution) relative to that which occurs in their absence (improved relative to the primary or electrolyte-resistance-driven current distribution). In the presence of a mask layer, the ionic current distribution is primarily governed by the distribution of the exposed portions of the conductive seed layer on the substrate surface. As a result of non-uniform ionic current distribution, recessed features will be filled differently.

[0073] In some implementations, the electrolyte includes plating additives such as accelerators, suppressors, and levelers. Other plating additives may include carriers and/or ductilizers. In some embodiments, an accelerator may include an alkane chain with at least one mercapto- and one sulfonic acid group or acid-salt. For example, the accelerator may include mercaptopropane sulfonic acid or mercaptoethane sulfonic acid. In some embodiments, the suppressor may include derivatives of polyethylene- and polypropyleneglycols and oxides. In these or other cases, the suppressor may include at least one material selected from the group consisting of polyethylene oxide, polypropylene oxide,

polyethylene glycol, polypropylene glycol, polyethylene with at least one S- and/or N-containing functional group, and polypropylene oxide with at least one S— and/or N-containing functional group. The composition of additives in the electrolyte may be optimized for use with a micro inert anode array in an electroplating process.

[0074] The plating chamber may be designed with an electrolyte injection flow system designed to produce flow parallel to the semiconductor substrate. The flow of electrolyte across the surface of the semiconductor substrate may occur at high velocities. Further, the electrolyte injection flow system is designed so that the flow of electrolyte is parallel to the micro inert anode array. The micro inert anode array may be positioned in the plating chamber so that there is a thin gap between the micro inert anode array and the semiconductor substrate.

[0075] The plating chamber may include a cross-flow manifold to promote cross-flowing of electrolyte across the substrate surface. The cross-flow manifold may be configured to contain an electrolyte flowing between a micro inert anode array and the substrate surface. The cross-flow manifold may also be referred to as a flow injection manifold. The flow injection manifold may be a cavity with a series of exit holes around its periphery and under a cross-flow confinement ring. The flow injection manifold may serve to create an azimuthally uniform injection of flow into a cross-flow gap. In an alternative embodiment, spatially distributed electrolyte through holes may be placed in the micro inert anode array, allow for the injection of fresh electrolyte to enter a gap from spaces and holes between micro inert anode elements and opposite the gap from the semiconductor substrate, and exiting the gap from the general periphery.

[0076] In semiconductor substrate plating chambers having cross-flow manifolds, plating chambers would historically include an ionically resistive element (instead of the micro inert anode array of this present disclosure), such as a channeled ionically resistive plate (CIRP) or a high resistance virtual anode (HRVA) that is placed in close proximity to the semiconductor substrate. The ionically resistive plate is typically a low porosity plate (less than 5% porosity) made of an electrically insulating material, and pores in the electrically insulating material allow for movement of ions through the porous plate towards the cathodically biased semiconductor substrate. The pores or holes in the ionically resistive element or HRVA would be uniform or regularly distributed and spaced apart. The ionically resistive element can provide an additional resistance on the path of ionic current towards the cathodically biased semiconductor substrate.

[0077] FIG. **4**A illustrates a perspective close-up view of a cross-flow side inlet and surrounding hardware of an electroplating apparatus. FIG. **4**B illustrates a perspective close-up view of a cross-flow outlet and surrounding hardware of the electroplating apparatus. FIG. **4**C illustrates a cross-sectional view of various parts of the electroplating apparatus shown in FIGS. **4**A and **4**B. FIG. **4**D illustrates a cross-sectional view of a flow injection manifold relative to a plating cup of the electroplating apparatus.

[0078] Often (historically in plating chambers having cross-flow manifolds), an electroplating apparatus or electroplating cell includes a cathode chamber and a separate anode chamber. The bottom surface of the cathode chamber may include a membrane frame **474** and membrane **402** (because it is very thin, the membrane is not actually shown, but its location is shown as being located at the lower surface of the membrane frame **474**), that separate the anode chamber from the cathode chamber. The membrane frame **474** is a rigid structural member for holding the membrane **402** that is typically an ion exchange membrane responsible for separating the anode chamber from the cathode chamber.

[0079] A substrate may be positioned in a substrate holder **454**. The substrate holder **454** is often referred to as a cup, cup assembly, or cup and cone assembly, and it may support and feed electrical current to the substrate at its periphery.

[0080] Flow of electrolyte is controlled in the cross-flow manifold or cross-flow manifold region **426**. This cross-flow manifold region **426** may also be referred to as a wafer to HRVA gap or just the wafer gap. Electrolyte flowing in a cross-flow manifold region **426** passes from an inlet cavity **450** (inlet) to an exit port **434** (outlet). The electrolyte enters the cross-flow manifold region **426** from one or more feed channels **458** that terminate into a semi-annular cross-flow injection manifold region **422** of a porous flow distribution plate **442**. Fluid flows through a plurality of distribution of holes **446** in the flow distribution (or showerhead) plate **442**, which are arranged around the periphery of one side of the electroplating cell. Thereafter, the fluid flow turns in a direction parallel to the substrate and passes into the cross-flow manifold region **426** (or cross-flow manifold wafer gap) by impact with and confinement in a channel in the cross-flow manifold region **426** between the cross-flow confinement ring **410** (also known as the top side insert) and the showerhead plate **442**. The cross-flow confinement ring **410** has a set of radially-directed fins or directional fins **466** that aid in directing the fluid flow into and across the cross-flow manifold wafer gap **426** in a straight flowing, parallel trajectory under the substrate. The directional fins **466** are in fluidic communication with the distribution holes **446** of the cross-flow showerhead plate **442**. The directional fins **466** define largely segregated fluid passages under a surface of the cross-flow confinement ring **410** and between adjacent directional fins **466**. As a result, the electrolyte arriving in the cross-flow manifold region **426** via cross-flow initiating structures is directed parallel or substantially parallel to the face of the substrate. On the opposite side of the cross-flow confinement ring **410** is the exhaust port **434** (outlet), where the electrolyte leaves the cross-flow manifold region **426**, where it can be collected, directed, and reclaimed in an outermost peripheral fluid containment region **484** of the electroplating cell formed by the outer containment cup **476** and its top weir surface **482**.

[0081] In FIGS. **4**A-**4**D, an ionically resistive plate or HRVA **406** is positioned between the substrate (working electrode) and an anode (counter electrode). The anode is usually separated from the substrate by the membrane **402**. The cross-flow manifold region **426** is above the HRVA **406** and below the substrate, where the substrate is held by the substrate holder **454**. The HRVA **406** includes openings to allow electrolyte to travel through the HRVA **406** to impinge upon the substrate. Typically, electrolyte can be separated into two different flow paths or streams. One stream flows electrolyte through the openings in the HRVA **406** and into the cross-flow manifold region **426**. The other stream flows electrolyte through the distribution holes **446** from the cross-flow injection manifold **422** and is redirected to flow laterally across the substrate surface in the cross-flow manifold region **426**. In some embodiments, there is no flow through the HRVA hole path.

[0082] The HRVA **406** approximates a nearly constant and uniform ionic current source in the proximity of the substrate (cathode). Normally, the HRVA **406** is placed in close proximity to the substrate. In contrast, an anode in the same close-proximity-location to the substrate would not supply a near constant current, but would present a near-constant potential plane at the anode metal surface, thereby allowing the current to be greatest where the net resistance from the anode plane to the terminus is smaller (e.g., to the edge of the substrate and the short path to the peripheral contact points on the substrate).

[0083] In FIG. **4**D, relevant geometries and heights of certain elements are shown. Distance (a) represents the height of the cross-flow manifold region **426**. This is the distance between the top of the lipseal (dashed line in FIG. **4**D) at its location where it seals the wafer (wafer is not shown in FIG. **4**D) and the plane of the uppermost surface (i.e., the surface closest to the wafer and cup) of the HRVA **406**. In some embodiments, distance (a) is between about 1 mm and about 10 mm. Distance (b) represents the distance between the exposed substrate surface and the bottom-most surface of the substrate holder **454**. In certain embodiments, distance (b) is between about 1 mm and about 4 mm. Distance (c) represents the height of the electrolyte gap between the upper surface of the cross-flow confinement ring **410** and the bottom of the substrate holder **454**. This electrolyte gap (which is typically zero in cases with the cross-flow confinement ring **410**) provides space to allow the substrate holder **454** to rotate during plating and is typically small to prevent electrolyte from leaking. In some cases, attached to the cross-flow confinement ring **410** via a clamping ring is a flow ring (not shown), whose purpose is to seal the electrolyte gap between the cross-flow confinement ring **410** and the bottom surface of the substrate holder **454**. This ensures no leakage of fluid out of the gap except at the exit port **434**. In some embodiments, distance (c) of the gap is about 0.5 mm or less. In some cases the cross-flow confinement ring **410** and substrate holder **454** touch and slide during plating. Distance (d) represents the height of the cross-flow confinement ring **410**. In certain embodiments, distance (d) is between about 1 mm and about 4 mm.

[0084] In the present disclosure, a micro inert anode array resides in the same relative position to the semiconductor substrate, substrate holder **454**, and plating cell; and can be viewed as replacing the ionically resistive element (e.g., HRVA **406**) and current supplying hardware below the HRVA **406**, so that the cross-flow manifold region **426** defines a space/gap between the micro inert anode array and the semiconductor substrate. In other words, the micro inert anode array can be placed in a location proximate to the semiconductor substrate in a plating cell where an HRVA is typically located. Ordinarily, an HRVA or ionically resistive element is employed to provide ionic resistance between the remote anode and the semiconductor substrate, but conductive to fluid electric current by having a series of pores or holes. Further, the HRVA presents a resistance to flow into and through the element, substantially confining fluid flow to remain in the gap between the semiconductor substrate and HRVA and following a direct path between the cross-flow injection manifold and exhaust ports. The HRVA compensates for the terminal effect by creating an ionically resistive region next to the semiconductor substrate that approximates a uniform distribution current source, which facilitates uniform plating from edge-to-center. This improves global control or WIW uniformity for plating metal features. However, because the HRVA has a regular/fixed pattern of holes, the HRVA does not favorably distribute current for die having a non-uniform distribution of features. As a result, the HRVA does not address WID uniformity specific to die layouts. The micro inert anode array of the present disclosure provides a series of independently controllable micro-scale anode electrodes to generate a desired current distribution, where the current distribution to each of the micro-anode electrodes may be determined based at least in part on die layouts and/or wafer level current distribution terminal effect. Thus, the micro inert anode array can address WID uniformity specific to die layouts, and global WIW compensations simultaneously.

[0085] With the micro inert anode array of the present disclosure, the plating cell no longer requires an HRVA, or a separate anode or a separated anode chamber. Conventional plating cells employing HRVAs often included a separated anode chamber underneath the HRVA, where the separated anode chamber would include an anode (e.g. an active copper metal anode) and a membrane. However, because the HRVA is porous, some electrolyte cross-flow would leak down through the holes in the HRVA and bypass the cross-flow channel around. Holes in the HRVA provide a path for some fluid to travel down. Rather than engineering various dams and seals to promote electrolyte cross-flow directly across the surface of the HRVA, the micro inert anode array replaces the HRVA to provide a non-porous block of material(s). Accordingly, the plating cell with the micro inert anode array (replacing a HRVA) is designed without a separate anode or anode chamber and provides a more uniform electrolyte cross-flow across the surface of the micro inert anode array.

[0086] FIG. **5**A illustrates a perspective close-up view of a cross-flow side inlet and surrounding hardware including a micro inert anode array of an electroplating apparatus according to some implementations. FIG. **5**B illustrates a perspective close-up view of a cross-flow outlet and surrounding hardware including a micro inert anode array of the electroplating apparatus according to some implementations. FIG. **5**C illustrates a cross-sectional view of various parts of the electroplating apparatus shown in FIGS. **5**A and **5**B. FIG. **5**D illustrates a cross-sectional view of a flow injection manifold relative to a plating cup of the electroplating apparatus according to some implementations.

[0087] Flow of electrolyte is controlled in the cross-flow manifold or cross-flow manifold region **526**. This cross-flow manifold region **526** may also be referred to as a wafer to HRVA gap or just the wafer gap. Electrolyte flowing in a cross-flow manifold region **526** passes from an inlet cavity **550** (inlet) to an exit port **534** (outlet). The electrolyte enters the cross-flow manifold region **526** from one or more feed channels **558** that terminate into a semi-annular cross-flow injection manifold region **522** of a porous flow distribution plate **542**. Fluid flows through a plurality of distribution of holes **546** in the flow distribution (or showerhead) plate **542**, which are arranged around the periphery of one side of the electroplating cell. Thereafter, the fluid flow turns in a direction parallel to a substrate and passes into the cross-flow manifold region **526** (or cross-flow manifold wafer gap) by impact with and confinement in a channel in the cross-flow manifold region **526** between the cross-flow confinement ring **510** (also known as the top side insert) and the showerhead plate **542**. The cross-flow confinement ring

510 has a set of radially-directed fins or directional fins 566 that aid in directing the fluid flow into and across the cross-flow manifold wafer gap 526 in a straight flowing, parallel trajectory under the substrate. The directional fins 566 are in fluidic communication with the distribution holes 546 of the cross-flow showerhead plate 542. The directional fins 566 define largely segregated fluid passages under a surface of the cross-flow confinement ring 510 and between adjacent directional fins 566. As a result, the electrolyte arriving in the cross-flow manifold region 526 via cross-flow initiating structures is directed parallel or substantially parallel to the face of the substrate. On the opposite side of the cross-flow confinement ring 510 is the exhaust port 534 (outlet), where the electrolyte leaves the cross-flow manifold region 526, where it can be collected, directed, and reclaimed in an outermost peripheral fluid containment region 584 of the electroplating cell formed by the outer containment cup 576 and its top weir surface 582.

[0088] The electrolyte arriving in the cross-flow manifold region 526 via the cross-flow initiating structure opening or inlet 550 is directed parallel or substantially parallel to the face of a substrate. In some cases, the cross-flow manifold region 526 may have a height between about 0.5 mm and about 15 mm, between about 0.5 mm and about 8 mm, or between about 1 mm and about 4 mm. The cross-flow manifold region 526 is defined on its sides by a cross-flow confinement ring 510 which acts to contain the cross flowing electrolyte within the cross-flow manifold region 526. The design of the cross-flow manifold region 526 can achieve a uniform linear flow velocity across the substrate.

[0089] A substrate may be positioned in a substrate holder 554. The substrate holder 554 is often referred to as a cup, cup assembly, or cup and cone assembly, and it may support the substrate at its periphery. The substrate holder 554 having an edge (elastomeric) seal and electrical contact elements configured to make contact to a front side of the substrate, faces a micro inert anode array 506. The substrate holder 554 holds the substrate in a position parallel to and a small distance from a top surface of the micro inert anode array 506. A distance or gap separating the micro inert anode array 506 and the substrate is typically equal to or less than about 4 mm. Electrolyte flows in the gap region between the micro inert anode array 506 and the substrate held by the substrate holder 554. Intense parallel flow inside the gap reduces resistance to mass transfer in the plating process. A cross-flow confinement ring 510 is positioned above the micro inert anode array 506, proximate the periphery of the substrate. The cross-flow confinement ring 510 is ring-shaped and may be azimuthally non-uniform.

[0090] The cross-flow manifold region 526 is above the micro inert anode array 506 and below the substrate. During a plating operation, electrolyte flows into a cross-flow injection manifold 522. From here, the electrolyte passes through distribution holes 546 (which may number more than 100 in certain embodiments) of a cross-flow showerhead plate 542. After leaving the distribution holes 546, the electrolyte's flow direction changes from (a) normal to the substrate to (b) parallel to the substrate. This change in flow direction occurs as the flow impinges upon and is confined by a surface in the cross-flow confinement ring's 510 inlet cavity 550. The electrolyte is delivered directly to the cross-flow manifold region 526 where it enters as a horizontally oriented cross flow below the substrate. On its way to the cross-flow manifold region 526, the electrolyte passes through the cross-flow injection manifold 522 and a cross-flow showerhead plate 542, and is redirected from a vertically upwards flow to a flow parallel to the substrate surface by actions and geometries of the cross-flow confinement ring's 510 inlet cavity 550.

[0091] In some embodiments, there may be one or more feed channels 558 for delivering electrolyte directly to the semi-annular cross-flow injection manifold region 522, where it is then delivered to the cross-flow manifold region 526. These feed channels 558 may exit into the cross-flow manifold region 526 in an azimuthally non-uniform manner (e.g., to improve the distribution of flow out of the flow distribution showerhead plate 542). Specifically, the feed channels 558 enter the cross-flow manifold region 526 at a particular side or azimuthal region (e.g., the inlet side) of the cross-flow manifold region 526. The cross-flow injection manifold 522 may be an azimuthal cavity that may be a dug out channel within a plate that can distribute electrolyte from various located feed channels 558 to various multiple flow distribution holes 546 in the cross-flow distribution plate (showerhead) 542. This cross-flow injection manifold 522 is located along an angular section of the peripheral or edge region of the micro inert anode array 506. Electrolyte flow may flow out of the cross-flow confinement ring exit port 534, sometimes referred to as a cross-flow outlet or side outlet.

[0092] In some embodiments, the direction of the electrolyte coming out of the cross-flow showerhead 542 is further controlled by the cross-flow confinement ring 510. In some embodiments, the cross-flow confinement ring 510 extends over the surface area of the micro inert anode array 506. In some embodiments, the top of the cross-flow confinement ring 510 has an L-shape, as shown in FIGS. 5A-5D. This shape may be selected to match a contour of the bottom surface of the substrate holder 554. In certain embodiments, the cross-flow confinement ring 510 contains a series of flow directing elements such as directional fins or straightening fins 566. The directional fins 566 are in fluidic communication with the distribution holes 546 of the cross-flow showerhead 542. The directional fins 566 define largely segregated fluid passages under a surface of the cross-flow confinement ring 510 and between adjacent directional fins 566. In some instances, the purpose of the directional fins 566 is to redirect and confine flow exiting from the distribution holes 546 from an otherwise radially inward direction to a "left-to-right" flow trajectory (left being an inlet 550 and right being an outlet 534). This helps establish a linear or substantially linear cross flow pattern. In some embodiments, all of the directional fins 566 of the cross-flow confinement ring 510 are parallel to one another.

[0093] Electrolyte flowing in the cross-flow manifold region 526 passes from an inlet cavity 550 (inlet) to a cross-flow confinement ring exit port 534 (outlet). At the outlet side of the cross-flow confinement ring 510, there may be directional fins 566 that are parallel to and align with the directional fins 566 at the inlet side. The cross flow passes through channels created by the directional fins 566 at the outlet 534. The electrolyte may then pass into another region of the plating chamber generally radially outwards and beyond the substrate holder 554 and the cross-flow confinement ring 510, with electrolyte collected and temporarily retained by a weir wall 582 before flowing over the weir wall 582 for collection and recirculation. Electrolyte exiting from the cross-flow manifold region 526 does not pass through

small holes or back through channels analogous to the feed channels **558** at the inlet **550**, but rather passes outward in a generally parallel-to-the-substrate direction as it is accumulated in the aforementioned region.

[0094] In FIG. **5**D, relevant geometries and heights of certain elements are shown. Distance (a) represents the height of the cross-flow manifold region **526**. This is the distance between the top of the lipseal (dashed line in FIG. **5**D) at its location where it seals the wafer (wafer is not shown in FIG. **5**D) and the plane of the uppermost surface (i.e., the surface closest to the wafer and cup) of the micro inert anode array **506**. In some embodiments, distance (a) is between about 1 mm and about 10 mm. Distance (b) represents the distance between the exposed substrate surface and the bottom-most surface of the substrate holder **554**. In certain embodiments, distance (b) is between about 1 mm and about 4 mm. Distance (c) represents the height of the electrolyte gap between the upper surface of the cross-flow confinement ring **510** and the bottom of the substrate holder **554**. This electrolyte gap (which is typically zero in cases with the cross-flow confinement ring **510**) provides space to allow the substrate holder **554** to rotate during plating and is typically small to prevent electrolyte from leaking. In some cases, attached to the cross-flow confinement ring **510** via a clamping ring is a flow ring (not shown), whose purpose is to seal the electrolyte gap between the cross-flow confinement ring **510** and the bottom surface of the substrate holder **554**. This ensures no leakage of fluid out of the gap except at the exit port **534**. In some embodiments, distance (c) of the gap is about 0.5 mm or less. In some cases the cross-flow confinement ring **510** and substrate holder **554** touch and slide during plating. Distance (d) represents the height of the cross-flow confinement ring **510**. In certain embodiments, distance (d) is between about 1 mm and about 4 mm.

[0095] The micro inert anode array **506** includes an array of micro inert anode elements (MIA-elements) disposed on a substrate. Each of the micro inert anode elements may include one or more noble or semi-noble metal layers such as platinum (Pt), iridium (Ir), gold (Au), or niobium (Nb) at the surface of the micro inert anode array **506**. Additionally or alternatively, each of the micro inert anode elements may include a mixed metal oxide electrode ("dimensionally stable anodes") such as titanium oxide (TiO_2), ruthenium oxide (RuO_2), iridium oxide (IrO_2), or platinum oxide (PtO_2) at the surface of the micro inert anode array **506**. Each of the micro inert anode elements can be physically and electrically isolated from one another. A dimension (e.g., width, length, or diameter) of an individual micro inert anode element may be equal to or less than about 5 mm, or more preferably less than about 500 μm in size, for example about 100 μm. Individual micro inert anode elements may be any suitable shape such as circular, rectangular, square, pentagonal, hexagonal, octagonal, or other polygonal geometry. Current may be controlled to each of the individual micro inert anode elements from a common power source such as though a TFT connection architecture. As a result, electrical current across the micro inert anode array **506** may be spatially controlled and varied. By regulating electrical current flow and directing electrical current to various micro inert anode elements, localized current distribution at the die-level may be more precisely controlled. Thus, regardless of irregular patterns in feature size, pitch, shape, etc., more or less current may be targeted for areas higher or lower in localized current density for controlling the plating process across each die of the substrate. For instance, more current may be localized for die patterns higher in density and less current may be localized for die patterns lower in density. Aspects of the micro inert anode array **506** are discussed in more detail below.

[0096] The electroplating apparatus may include various additional elements as needed for a particular application. In some cases, an edge flow element may be provided proximate the periphery of the substrate, within the cross-flow manifold region. The edge flow element may be shaped and positioned to promote a high degree of electrolyte flow (e.g., cross flow) near the edges of the substrate. The edge flow element may be ring-shaped or arc-shaped in certain embodiments, and may be azimuthally uniform, or non-uniform. Edge flow elements are further discussed in U.S. patent application Ser. No. 14/924,124, filed Oct. 27, 2015, and titled "EDGE FLOW ELEMENT FOR ELECTROPLATING APPARATUS," which is herein incorporated by reference in its entirety and for all purposes.

[0097] In some cases, the electroplating apparatus may include a sealing member for temporarily sealing the cross-flow manifold region. The sealing member may be ring-shaped or arc-shaped, and may be positioned proximate the edges of the cross-flow manifold region. A ring-shaped sealing member may seal the entire cross-flow manifold region, while an arc-shaped sealing member may seal a portion of the cross-flow manifold region (in some cases leaving the side outlet open). During electroplating, the sealing member may be repeatedly engaged and disengaged to seal and unseal the cross-flow manifold region. The sealing member may be engaged and disengaged by moving the substrate holder, micro inert anode array, front side insert, or other portion of the electroplating apparatus that engages with the sealing member. In some embodiments, there is a small leakage gap between the bottom surface of the substrate holder and the top surface of an element below the substrate holder. This leakage gap is typically maintained during electroplating to allow the substrate to be rotated freely. A seal may be provided between the bottom of the substrate holder and the top surface of an element below the substrate holder, which can be a cross-flow confinement ring. In some embodiments, the seal is attached (fixedly or releasably) to the substrate holder, e.g., bottom surface of the substrate holder. In some embodiments, the seal is attached (fixedly or releasably) to the cross-flow confinement ring, e.g., top surface of the cross-flow confinement ring. In some embodiments, the seal is a compressible material such as a fluoropolymer elastomer. The seal is configured for w-holly or partially sealing one or more outlets to the cross-flow manifold region other than a side outlet (e.g., exit port), where the seal is positioned at least partially below the substrate holder, and where the seal is either engaged in a sealed state or disengaged in an unsealed state. A controller is configured to cause intermittent switching between the sealed state and the unsealed state during electroplating. In some implementations, the controller is further configured to cause rotation of the substrate while the seal is in the unsealed state. The cross-flow confinement ring is located between the micro inert anode array and the substrate holder, where the leakage gap is between the bottom surface of the substrate holder and the top surface of the cross-flow confinement ring. The cross-flow confinement ring may be positioned peripherally in the cross-flow manifold region.

Sealing members and methods of modulating cross flow are further discussed in the following U.S. Patent Applications, each of which is herein incorporated by reference in its entirety and for all purposes: U.S. patent application Ser. No. 15/225,716, filed Aug. 1, 2016, and titled "DY NAMIC MODULATION OF CROSS FLOW MANIFOLD DURING ELECTROPLATING"; and U.S. patent application Ser. No. 15/161,081, filed May 20, 2016, and titled "DYNAMIC MODULATION OF CROSS FLOW MANIFOLD DURING ELECTROPLATING."

[0098] In various embodiments, one or more electrolyte jets may be provided to deliver additional electrolyte above the micro inert anode array. The electrolyte jet(s) may deliver electrolyte proximate a periphery of the substrate, or at a location that is closer to the center of the substrate, or both. The electrolyte jet(s) may be oriented in any position, and may deliver cross flowing electrolyte. Electrolyte jets are further described in U.S. patent application Ser. No. 15/455,011, filed Mar. 9, 2017, and titled "ELECTROPLATING APPARATUS AND METHODS UTILIZING INDEPENDENT CONTROL OF IMPINGING ELECTROLYTE," which is herein incorporated by reference in its entirety and for all purposes.

[0099] Different flows over the substrate may occur at different times over the course of plating the substrate. For instance, the electroplating apparatus may periodically or intermittently switch between (a) a first flow pattern that delivers cross flowing electrolyte to the substrate surface, e.g., with electrolyte primarily originating from a first side inlet, and (b) a second flow pattern that delivers cross flowing electrolyte to the substrate surface, e.g., with electrolyte primarily originating from a second side inlet. The different flow patterns may be used to achieve different flow fields during the plating process, thereby achieving a desired mass transfer exposure over time that can lead to more uniform plating of metal features. The different flow patterns and directions can be achieved, for example, by rotating the wafer relative to a fixed linear cross flow pattern over the entire plating process.

[0100] FIGS. **6**A and **6**B illustrate schematic diagrams of flow direction of electrolyte and its impact on plating within a patterned feature. If the flow were uniform and the substrate did not rotate, convection inside recessed features defined by a mask (e.g., photoresist) would be uni-directionally biased. In FIGS. **6**A and **6**B, a cross-sectional schematic of a recessed feature within a photoresist is shown, where a bottom of the recessed feature includes exposed portions of a conductive seed layer. The arrows represent a flow field and direction of flow for the electrolyte. When electrolyte flow proceeds from left to right, the flow field generates a clockwise rotation of flow (eddy) inside the recessed feature as shown in FIG. **6**A. When electrolyte flow proceeds from right to left, the flow field generates a counterclockwise rotation of flow inside the recessed feature as shown in FIG. **6**B. Given that deposition of metal can proceed under mass transfer limitations of the depositing metal ion in the electrolyte, a downstream position at a base of the eddy receives a more replenished, higher concentration of metal ion flow than an upstream position at the base of the eddy. This is because electrolyte metal ions are consumed more at the downstream position first and becomes depleted therefore before traveling towards the direction of the upstream position. As shown in FIG. **6**A, deposition occurs at a faster rate at position **2** (downstream position) than at position **1**, and the thickness at position **2** is greater, leading to a non-uniform feature profile. As shown in FIG. **6**B, deposition occurs at a faster rate at position **1** (downstream position) than at position **2**, and the thickness at position **1** is greater, leading to a non-uniform feature profile that is the opposite in direction to FIG. **6**A. If, over the course of plating operations, the direction of flow is both left-to-right and right-to-left for equal durations, then the aforementioned mass transfer bias and undesirable non-uniform feature profile may be avoided. This applies not only in 2-dimensions but also in 3-dimensions. Thus, applying a bi-directional flow only in 2-dimensions (e.g., left-to-right and right-to-left) leaves a bias in a third dimension. Enabling a flow direction into and out of the page, some but not necessarily all of the bias is removed in the third dimension. By continuously changing the direction of flow over time to include equal flow velocity in all directions, a uniform mass transfer exposure can be achieved. One way to enable angular uniform mass transfer exposure is to rotate the substrate at a fixed rotation rate around the linear flow field in the plating gap during an electroplating process. Alternatively, the rotation rate and/or direction can change during the electroplating process. In some embodiments, the rotation speed can change rapidly such as over a time period that is small relative to the duration of the electroplating process, or the rotation speed can change continuously over the entire duration of the electroplating process (e.g., slowly ramped rotation rate). In the present disclosure, the current distribution in the micro inert anode array may dynamically change as the substrate rotates so that the micro anode array's current distribution across its various elements follows the feature and die location requirements and the general rotational path of the substrate.

[0101] FIG. **7**A depicts a perspective view of an example schematic micro inert anode array according to some implementations. FIG. **7**B depicts a top view of the example schematic micro inert anode array of FIG. **7**A. The micro inert anode array **700** may include a substrate **710** having microelectronic embedded elements **720** and electrical wiring **730**. The substrate **710** may include any suitable substrate material such as glass, plastic, ceramic, silicon, or other dielectric material. For example, the substrate **710** can include a dielectric layer such as a polyimide dielectric layer. The microelectronic embedded elements **720** may be inert anodes or dimensionally stable anodes at a surface of the substrate **710**. These inert anodes **720** may also be referred to as micro-anode electrodes, micro inert anode elements (MIA elements), anode elements, or micro-anodes. The inert anodes **720** may be arranged in an array on the substrate **710**. The inert anodes **720** may be physically and electrically isolated from one another. Each of the inert anodes **720** may include a material such as Pt, Ir, Au, Nb, TiO_2, RuO_2, IrO_2, or PtO_2. Current may be delivered to each of the inert anodes **720** via conductive wiring **730** (e.g., copper wiring). A power source (not shown) delivers current to one or more inert anodes **720** through the conductive wiring **730**. As shown in FIGS. **7**A and **7**B, each of the inert anodes **720** may be individually connected to conductive wiring **730** for independent tunable control.

[0102] In some embodiments, the inert anodes **720** may be arranged in an M×N array of elements. For example, the M×N array of elements may be arranged as a square or rectangular pattern. In some other embodiments, the inert anodes **720** may be arranged in alternative arrangements

such as hexagonal or triangular packing arrangements. Size and spacing of inert anodes **720** may be at a sub-mm scale or less than about 1 mm. Spacing between inert anodes **720** may be defined by its pitch, where a pitch of the plurality of inert anodes may be equal to or less than about 1000 μm, equal to or less than about 500 μm, equal to or less than about 300 μm, or between about 100 μm and about 400 μm. The size (e.g., diameter) of each inert anode **720** may be comparable to pitch. In some embodiments, a diameter of an inert anode **720** in the micro inert anode array **700** may be equal to or less than about 800 μm, equal to or less than about 500 μm, equal to or less than about 300 μm, or between about 50 μm and about 200 μm. Essentially, micro-sized inert anodes **720** closely packed together model approximately to an infinite number of very small anodes. This allows for finer or more precise control over current distribution in the micro inert anode array **700**. In some cases, a number of the micro-sized inert anodes **720** may be at least 100, at least 200, at least 500, at least 1000, or at least 2000.

[0103] FIG. **8** shows different shapes and arrangements of inert anodes in a micro inert anode array according to some implementations. Different shapes can include circular, square, hexagonal, or other polygon. Different arrangements can include square or triangular arrangements. In some embodiments, micro inert anode elements **820***a* may be circular and arranged in a square/rectangular arrangement or array. In some embodiments, micro inert anode elements **820***b* may be square and arranged in a square/rectangular arrangement or array. In some embodiments, micro inert anode elements **820***c* may be hexagonal and arranged in a square/rectangular arrangement or array. In some embodiments, micro inert anode elements **820***d* may be hexagonal and arranged in a hexagonal arrangement or array.

[0104] The circuitry for turning on or off or otherwise regulating the current to each of the inert anodes is not shown in FIGS. **7**A, **7**B, and **8**, but is advantageously physically integrated with the micro inert anode array **700**. FIG. **9** illustrates a circuit diagram of example micro inert anode array elements with active matrix control circuitry according to some implementations. In some embodiments, each of the inert anodes **920** of a micro inert anode array **900** is connected in series to a switch device **910** that either connects or isolates a line (e.g., conductive wiring) from a common power source. Optionally, the switch device **910** may be connected in series with or replaced by a current regulator capable of varying the magnitude of the current being delivered to the anode to which it is connected. As shown in FIG. **9**, the switch device **910** is referred to as an "element control circuit" and the inert anode **920** is referred to as a "micro anode." A common power source **930** to some or all of the inert anodes **920** in the micro inert anode array **900** may include an electrical bus (labeled "power buss"). In addition to the switch device **910** or element control circuit, circuitry for monitoring and regulating an amount of current flow to each of the inert anodes **920** may be included.

[0105] The switch device **910** or element control circuit may include one or more of a switching element and a transistor. The element control circuit may be an active matrix element, which may comprise one or more of a transistor, a diode, and a switch (e.g., MEMS or NEMS switch). The element control circuit is coupled to the inert anode **920**. The element control circuit is connected to column lines that connect to a column driver **950** and row lines that connect to a row driver **940**.

[0106] A processor (not shown) may be configured to communicate with an array driver, where the array driver includes a column driver **950** (or column driver circuit) and a row driver **940** (or row driver circuit). The column driver **950** and the row driver **940** provide signals to the array of inert anodes **920**. The row driver **940** and the column driver **950** address the particular inert anode or plurality of inert anodes **920** by an active matrix addressing scheme. The processor may or may not be physically integrated or co-located with the row and column drivers **940**, **950**. The processor and row and column drivers **940**, **950** may be fabricated via one of several common microelectronics production methods or materials sets, including but not limited to thin film transistor (TFT) technology, silicon-based complementary metal oxide semiconductor (CMOS) technology, organic electronics, or other printed electronics fabrication technology. Current delivered to each micro inert anode **920** may be provided continuously or pulsed. The processor and row and column drivers **940**, **950** may be configured to deliver power to all pixels simultaneously, or to a subset of pixels in any instant. In some embodiments, the processor and drivers may be capable of delivering power to a fraction, for example one sixteenth, of the micro inert anode array **900** at any time, and power is delivered to the entire array on a time-averaged basis by sequentially powering different fractions, blocks or sub-arrays in a pulsed mode. In another embodiment, the power to the micro inert anode array **900** may be rastered across the entire array, or the power may be rastered within one or more blocks or sub-arrays. Such pulsed or rastering implementations potentially decrease the implementation cost of the present disclosure, though in most cases as the expense of metal deposition rate.

[0107] Some or all of the components for powering and controlling flow of current to each of the inert anodes, such as the electrical bus and other power/current flow regulating devices may be located at the periphery of the array area or outside the array area FIG. **10** depicts a top-down view of a schematic illustration of an example micro inert anode array for processing a circular semiconductor substrate according to some implementations. In some instances, the manufactured micro inert anode array **1000** is produced in a square or rectangular area as a result, the array area is larger than a circular workpiece or circular substrate. For example, when electroplating on a 300-mm semiconductor substrate, a micro inert anode array **1000** will preferably have a region at least as large as 300 mm in diameter. In some embodiments as shown in FIG. **10**, the micro inert anode array **1000** may be square in shape. Power and control inputs **1030** may be positioned along a periphery of the array area. The power and control inputs **1030**, including the electrical bus and row input control **1040** and column input control **1050**, are positioned in the plane of and at the periphery of the array area outside a central circular region. The peripheral coated area **1010** in FIG. **10** designates the array area for the micro inert anode array **1000**. The central circular region **1020** in FIG. **10** designates the array area for the micro inert anode array **1000** that exposes the 300-nm substrate. In some cases, the peripheral coated area **1010** surrounds the central circular region **1020**. In some cases, the inert anodes outside the central circular region **1020** are not used. In some embodiments, power and connections may generally pass from the

edge to the center of the array. In some other embodiments, power and connections may pass from below a substrate of the micro inert anode array **1000** with connections and bus power made from below the plane of the inert anodes. Regardless, the gap region between exposed inert anodes and the semiconductor substrate being electroplated will comprise an electrolyte containing metal ions or other acids and salts, where the electrolyte is a generally corrosive solution.

[0108] FIG. **11**A illustrates a schematic diagram of an example inert anode array electroplating cell in combination with general electroplating cell fluidic and plating controls according to some implementations. The inert anode array electroplating cell **1110** includes a cup assembly with an elastomeric seal and one or more electrical contact members. The cup assembly serves to hold the substrate at its periphery and provide electrical current to the substrate. The inert anode array electroplating cell **1110** further includes a micro inert anode array adjacent to the substrate, where the micro inert anode array and the substrate is separated by a small gap. A plurality of straightening fins may be positioned around the substrate (not directly under the substrate), where the plurality of straightening fins can have a height defined by the small gap. When electrolyte fluid comes up from an injection manifold, electrolyte fluid turns 90 degrees to provide a lateral flow over the surface of the substrate. This occurs with the assistance of the straightening fins.

[0109] In some embodiments, the inert anode array electroplating cell **1110** is fluidly coupled to a plating solution reservoir **1190** by inlet and outlet plumbing lines to create a circulatory flow loop. An electroplating system **1100** includes the inert anode array electroplating cell **1110** and the plating solution reservoir **1190**. The electroplating system **1100** may further include a recirculation pump **1130**, a flow meter **1134**, a degasser **1136**, cell and reservoir level monitors such as a level sensor **1170**, heat exchangers and/or immersion heaters **1160**, thermocouple **1150**, temperature controller **1180** coupled to the thermocouple **1150** and heat exchangers and/or immersion heaters **1160**, and one or more exhaust ports (e.g., side outlets). In some embodiments, the electroplating system **1100** further includes density, pH, and/or conductivity meters, where such meters may be utilized for bath maintenance **1140**. In addition to the aforementioned hardware components, the electroplating system **1100** may further include controllers such as a flow controller **1132** for modifying and controlling the flow, temperature, chemical dosing of additives, acids, bases, etc. of the electrolyte fluid, and/or a micro inert anode array controller **1120**. A power supply may be electrically coupled to the micro inert anode array controller **1120** for supplying current to the micro inert anode array. A controller may be configured with instructions or programmed to control one or more of the processes described herein. Such processes may be related to flow direction, timing, substrate rotation, substrate and die layout identification, and current distribution control to the micro inert anode array. In some embodiments, an electrochemical metal cation regeneration system is housed within or fluidly coupled to the plating solution reservoir.

[0110] FIGS. **11**B and **11**C illustrate a schematic diagram of an example plating cell including a micro inert anode array according to some implementations. FIGS. **11**B and **11**C depict a plating cell **1110**, with a substrate **1113** positioned in a substrate holder or cup assembly **1112**. The cup assembly **1112** may support the substrate **1113** at its periphery. The cup assembly **1112** may have an edge (elastomeric) seal and electrical contact elements configured to make contact to a front side of the substrate **1113**, where the substrate **1113** faces a micro inert anode array **1116**. The substrate holder **1112** holds the substrate **1113** in a position parallel to and a small distance from a top surface of the micro inert anode array **1116**. A cross-flow manifold region **1114** may be defined by a gap between the top surface of the micro inert anode array **1116** and the substrate **1113**, where electrolyte flows into the gap between the micro inert anode array **1116** and the substrate **1113**.

[0111] The electrolyte travels from an inlet port **1111**, into the cross-flow manifold region **1114**, and out the exit port **1117**. Straightening fins **1115** may redirect the flow of electrolyte coming out of the inlet port **1111** so that flow occurs in a transverse direction parallel or substantially parallel to the surface of the substrate **1113**. In other words, the straightening fins **1115** redirect the flow of electrolyte coming out of the inlet port **1111** so that electrolyte is delivered into the cross-flow manifold region **1114** in a linear manner and at right angles relative to the manifold's are symmetry tangent. In some embodiments, a sealing member (not shown) positioned proximate the edges of the cross-flow manifold region may be employed to seal off the cross-flow manifold region **1114**.

[0112] As in any electrochemical cell, an oxidative electrochemical half-reaction will occur at the micro inert anode elements. In some embodiments, this half-reaction may result in oxygen evolution, where water is broken into hydrogen ions and oxygen gas ($2H_2O \rightarrow O_2+4H^+ +4e^-$). In this embodiment, oxygen gas is generated, and the electrolyte becomes more acidic as hydrogen ions are generated. Metal ions (e.g. copper ions) are consumed from the solution as they are deposited onto the cathode/substrate ($2Cui^{+2}+4e^- \rightarrow 2Cu$). In some embodiments where all substrates are processed from an electrolyte of the nearly the same composition, the depletion of copper ion and decrease in pH resulting from increased hydrogen ions may adversely impact metal plating on the substrate. Bubble generation from oxygen production may also adversely impact metal plating on the substrate. Bubble generation and associated defects from generated oxygen can be mitigated by high flow of a non-oxygen saturated electrolyte near the micro inert anode array, e.g. by using a contactor/membrane degasser in the flow loop that is connected to a vacuum and removes dissolved gases from the solution. The acidification and copper depletion can be mitigated by adjusting the electrolyte concentration. This can be done in one of several approaches, of which two approaches are described below with respect to FIGS. **12** and **13**.

[0113] FIG. **12** illustrates a schematic diagram of an example inert anode array electroplating cell in combination with a metal oxide dose control unit according to some implementations. An electroplating system **1200** includes a plating cell **1210** in fluid communication with a plating solution reservoir **1270**. The plating cell **1210** includes a micro inert anode array **1220** (anode) and a semiconductor substrate or workpiece **1230** (cathode). The semiconductor substrate or workpiece **1230** may include patterned features in one or more dice. The micro inert anode array **1220** may include an array of micro-sized inert anodes configured to provide a desired current distribution over an area of the semiconductor substrate or workpiece **1230**. The micro inert

anode array **1220** and the workpiece **1230** may be separated by a flow gap, where the flow gap may be between about 0.5 mm and about 8 mm, or between about 0.5 mm and about 4 mm. Electrolyte may flow between the workpiece **1230** and the micro inert anode array **1220** in a cross-flow manifold region. The electrolyte may enter the cross-flow manifold region through a cell flow inlet **1212** and exit the cross-flow manifold region through a cell flow outlet **1214**. The plating cell **1210** is fluidly coupled to the plating solution reservoir **1270** by plumbing line to the cell flow inlet **1212** and plumbing lines to the cell flow outlet **1214**, thereby creating a circulatory flow loop. The electrolyte may be recirculated from the plating solution reservoir **1270** to the plating cell **1210** via a recirculation pump **1240**. The electroplating system **1200** may further include controllers such as a controller **1250** for modifying and controlling the flow, temperature, chemical dosing of additives, acids, bases, etc. of the electrolyte fluid, and/or a micro inert anode array controller. A power supply may be electrically coupled to the controller **1250** for supplying current to the micro inert anode array **1220**. The controller **1250** may be configured with instructions or programmed to control one or more of the processes described herein. Such processes may be related to flow direction, timing, substrate rotation, substrate and die layout identification, and current distribution control to the micro inert anode array **1220**.

[0114] As shown in FIG. **12**, oxidative electrochemical half-reactions may result in decreased pH and increased oxygen generation by the breakdown of water ($2H_2O \rightarrow O_2 + 4H^+ + 4e^-$) occurring at the micro inert anode elements of the micro inert anode array **1220**. Concurrently, metal ions (e.g., copper ions) are depleted at the workpiece **1230** by reductive electrochemical half-reactions ($2Cu^{-2} + 4e^- \rightarrow 2Cu$). The acidification and copper depletion may be mitigated by dosing a solution with known concentrations and volumes of electrolyte (preferably of higher copper concentration and lower acid concentration than the plating electrolyte used), and periodically removing excess solution to maintain the overall volume of the system (often referred to as a "bleed and feed" operation). In an alternative embodiment, a material can be added that reacts with the excess acid generated and releases copper ions in the process. In FIG. **12**, solid metal oxide such as copper oxide is dosed as part of an overall plating system bath composition control. A metal oxide dose control unit **1260** is fluidly coupled to the plating solution reservoir **1270**. Using the metal oxide in the stoichiometric ratio associated with the reaction leads to a balanced overall bath composition. For instance, dosing copper oxide reacts with hydrogen ions to produce copper ions and water ($4H^+ + 2CuO \rightarrow 2Cu^{-2} + 2H_2O$). This compensates for copper depletion and acidification in the plating electrolyte. An oxide of the same oxidation state as the metal being plated (Cu^{+2}/CuO, Ni^{+2}/NiO, or Sn^{+2}/SnO) leads to a favorable result because the reaction with the acid generated replaces the metal ion and water consumed and oxygen removed.

[0115] FIG. **13** illustrates a schematic diagram of an example inert anode array electroplating cell in combination with a redox couple according to some implementations, An electroplating system **1300** includes a plating cell **1310** in fluid communication with a plating solution reservoir **1375**. The plating cell **1310** includes a micro inert anode array **1320** (anode) and a semiconductor substrate or workpiece **1330** (cathode). The workpiece **1330** may include patterned features in one or more dice. The micro inert anode array **1320** may include an array of micro-sized inert anodes configured to provide a desired current distribution over an area of the workpiece **1330**. The micro inert anode array **1320** and the workpiece **1330** may be separated by a flow gap, where the flow gap may be between about 0.5 mm and about 8 mm, or between about 0.5 mm and about 4 mm. Electrolyte may flow between the workpiece **1330** and the micro inert anode array **1320** in a cross-flow manifold region. The electrolyte may enter the cross-flow manifold region through a cell flow inlet **1312** and exit the cross-flow manifold region through a cell flow outlet **1314**. The plating cell **1310** is fluidly coupled to the plating solution reservoir **1375** by plumbing line to the cell flow inlet **1312** and plumbing lines to the cell flow outlet **1314**, thereby creating a circulatory flow loop. The electrolyte may be recirculated from the plating solution reservoir **1375** to the plating cell **1310** via a recirculation pump **1340**. The electroplating system **1300** may further include controllers such as a controller **1350** for modifying and controlling the flow, temperature, chemical dosing of additives, acids, bases, etc. of the electrolyte fluid, and/or a micro inert anode array controller. A power supply may be electrically coupled to the controller **1350** for supplying current to the micro inert anode array **1320**. The controller **1350** may be configured with instructions or programmed to control one or more of the processes described herein. Such processes may be related to flow direction, timing, substrate rotation, substrate and die layout identification, and current distribution control to the micro inert anode array **1320**.

[0116] As shown in FIG. **13**, a soluble ion redox couple may be used. For example, ferrous ions (Fe^{+2}) can be oxidized to ferric ions (Fen) at the various micro inert anode electrode surfaces of the micro inert anode array **1320**. In this embodiment, no gas is produced and the electrolyte pH remains unchanged as no oxygen gas or hydrogen ions are generated. However, the concentration of Fe^{+3} ions will increase over time if means to mitigate it are not included. This can be addressed by either dosing a solution with known concentrations ("bleed and feed") as described above, or by driving a reverse electrochemical reaction ($2Fe^{+3} + Cu \rightarrow 2Fe^{+2} + Cu^{+2}$) in an electrochemical cell containing the main plating electrolyte **1375**. This can be done as either part of a recirculation loop as shown in FIG. **13**, or by removing the electrolyte to a separate apparatus and periodically or continuously returning the electrolyte to a main reservoir. As further shown in FIG. **13**, a membrane, such as a cationic membrane **1380**, can optionally be used to separate the active metal anode **1390** ($2Cu \rightarrow Cu^{+2} + 2e^-$) and regenerating anode electrolyte **1395** from a regenerating system cathode **1370** ($2Fe^{+3} + 2e^- \rightarrow 2Fe^{+2}$) and main plating electrolyte **1375**. This can be useful so as to prevent metal particles that may be generated at the soluble metal anode **1390** from reaching the workpiece **1330**, and to avoid organic additive breakdown by exposure of them to the oxidizing surface of the active metal anode **1390**.

[0117] Returning to FIG. **2**, at block **240**, the anodes in the micro inert anode array are energized based at least in part on identified substrate type and layouts. A controller including one or more processors may regulate and direct current to various micro inert anode elements of the micro inert anode array. Each of the micro inert anode elements may be independently controllable and tunable. As such, the micro inert anode elements may be referred to as independently

controllable micro inert anode elements. The micro inert anode array coupled with its drive circuitry provides a finely spatially resolved tunable array of current sources. The semiconductor substrate may have die layouts having a non-uniform distribution of features. However, it will be understood that in some embodiments, the semiconductor substrate may have die layouts having a uniform distribution of features. In some cases, the semiconductor substrate may have multiple die, where each die has a pattern of features (e.g., region of isolated features and a region of dense features). The feature patterns on each die may exhibit varying density, varying feature sizes, shapes, and depths, and the patterns appearing on one die may vary from those on adjacent dice. The micro inert anode array placed in proximity to the semiconductor substrate can produce a current distribution such as a non-uniform current distribution over an area of the semiconductor substrate. Current may be applied to at least two or more micro inert anode elements to generate the desired current distribution. In some cases, the micro inert anode array can produce a current distribution corresponding to the die layouts having a distribution of features. Accordingly, when electrolyte flows laterally in contact with the substrate and the micro inert anode array, the electric fields can be controlled to match a die pattern. More or less current is provided to regions that require more or less current (e.g., due to variability in local feature density), which provides a more uniform plating thickness distribution than would be otherwise possible. Quite simply, electroplating metal features on the semiconductor substrate occurs using a micro inert anode array where the current is spatially controlled and varied improves the uniformity of plating distribution relative to having a single anode far away (e.g., more than about 8 mm away) from the substrate surface or relative to a HRVA having a uniform current distribution resistance pattern. As a result, metal is plated with a substantially uniform thickness in one or more dice having a distribution of features.

[0118] Control of wafer-level current distribution can also be achieved, for example, by modifying the current from center-to-edge radially, compensating for the terminal effect or compensating for impact of a non-uniform photoresist thickness profiles. The current distribution can also be controlled to compensate for missing patterned areas, which may also be referred to as "missing die" areas, for example between die streets or edge-of-wafer missing die and feature regions. A particular advantage of being able to control the current to avoid "missing die" areas is that it eliminates the need of filling that space with a "dummy" die to avoid local current loading. Elimination of such dummy edge dice reduces the photolithographic processing (to generate such a die), eliminates the potential for sealing failures at the edge of the wafer in the missing die region, reduces the material consumption, and reduces the possibility of tin and tin-silver lipseal plating in the area Thus, in some cases, the current applied to the inert anodes of the micro inert anode array may provide a current distribution based on a non-uniform distribution of features in one or more dice. Alternatively or additionally, the current applied to the inert anodes of the micro inert anode array may provide a current distribution based on global within-wafer corrections.

[0119] High-resolution die level current distribution control may be achieved for die patterns by controlling or determining at least (a) the pitch (distance) between micro inert anode elements, and (b) the gap between the semiconductor substrate and the micro inert anode array. Smaller micro inert anode element sizes and spacing can be used, but doing so may come with a tradeoff of increased design, manufacturing, and current distribution control complexity, and the need for small gaps between the micro inert anode array and the substrate. Gaps may be equal to or smaller than about four times the micro inert anode element feature size so as to lead to improved results relative to using a larger feature. By way of an example, for current control on a 0.25 mm scale, micro inert anode element may have a size (e.g., diameter) and pitch of about 50 μm, and a gap between the micro inert anode array and the semiconductor substrate may be about 00 μm.

[0120] Though the present disclosure is mainly described in context with and may be implemented in through-resist electroplating applications, it will be understood that the present disclosure is not limited to such applications. In some implementations, the present disclosure may be applied in non-WLP applications such as damascene applications or TSV applications. Damascene and TSV processes involve plating that occurs over the entire seeded and exposed surface of the substrate (no masking, but with recess metallized surfaces), and the feature patterns can still have variability in feature density that may be addressed with a micro inert anode array of the present disclosure. More particularly, the micro inert anode array and current distribution control in the micro inert anode array may be applied in plating metal in damascene and TSV applications or similar applications where local control of the macroscopic current distribution is beneficial. Furthermore, by varying the amount of current as a function of radial position and programming a wafer level anode array current source optimized profile, one can compensate for the effects of a thin seed layer (the so-called "terminal effect") with this new hardware and process. The process can by quite dynamic for damascene and TSV plating applications (it is usually less so for through-resist applications, where most of the surface around the plated features remain at their original thickness covered by the photoresist coating). As metal is plated over the general surface, there is a reduction in the resistance of the base layer (seed plus plated field film) over time, and thereby a reduction in the magnitude of the terminal effect correction is required.

[0121] Therefore, a process with both changing currents with time to compensate for the changing terminal effects, overlaid with a process that is correcting for the local (e.g., die level) feature density effects, is envisioned. Typically, the difference in the current applied at the center versus the wafer edge will decrease over time; when the base metal layer becomes sufficiently thick (theoretically when it is infinitely thick) no correction is required and the micro inert anode array will apply a generally uniform center to edge current (with within-die variation still applied for within-die controlled behavior).

[0122] FIGS. **14**A-**14**D illustrates a simulation model for determining current distribution in a micro inert anode array in response to identifying a die layout according to some implementations. A controller including one or more processors may be configured with instructions or programmed to determine or identify die layout(s) in a substrate. Identifying the die layout(s) in the substrate may be obtained with the assistance of a camera or other spatial characterization instrument, or may be known a-priori and provided to the controller separately. In FIG. **14**A, a die **1410** (e.g., "model

die") may have dimensions of 28 mm long by 4 mm wide, containing a total of 1974 features each 100 μm in size. The features are arranged on the die **1410** in at least two regions: (1) a first region having 150 μm pitch (tight pitch, high density) and (2) a second region having 500 μm pitch (low pitch, low density). The blacked-out regions correspond to the first region and the dotted regions correspond to the second region. After determining the die layout in the substrate, a computer model can be used to determine the plated current distribution from a micro inert anode array. The computer model may be capable of modeling expected trends in behavior based on various physical configurations of the micro inert anode array and spacing (gap size) to the substrate. To develop such a computer model, simulations may be performed. In each simulation, a unique applied current and a resulting current distribution over all of the array is imposed on each of the micro inert anode elements, driving a distribution of current over the substrate. Variables that are controlled for each simulation include: (a) the pitch (distance) between the micro inert anode elements, and (b) the gap between the micro inert anode array and the substrate surface. As shown in FIGS. **14**A-**14**D, the micro inert anode elements are arranged as an array in a rectangular pattern. A size of each of the micro inert anode elements may be half the pitch spacing (e.g., a 1 mm pitch anode has a 0.5 mm diameter micro inert anode element).

[0123] Techniques and procedures may be used to approximate an optimal result for each configuration. For example, a first model is run with each of the features of the die having an identical current (i.e., a 0% non-uniformity or ideally flat current density distribution) with a counter electrode being a continuous conductive surface at the target gap position. Such a counter electrode is equivalent to a micro inert anode array having an infinite number of very small inert anode elements. The counter electrode may be an anode ground plane **1420** as shown in FIG. **14**B. From there, the current distribution on the anode ground plane **1420** from the first simulation is used to assign a corresponding current of equal magnitude to each of the micro inert anode element **1430** in a second simulation in FIG. **14**C. To calculate a second simulation ("results" simulation), an average value of the current in the area of the micro inert anode element **1430** from the first simulation is assigned as the current value of each individual micro inert anode element **1430**, and the potential of all of the die feature surfaces may be set to ground potential Because of the finite number of micro inert anode elements **1430**, and the fact that there are dead zones between elements which cannot supply current in the same distribution as in the simulated anode ground plane **1420**, the results of the second simulation have a finite non-uniformity and non-identical current for each feature. Depending on the particular configurations of the micro inert anode array and gap, an improved and more uniform die current distribution may be achieved by a using an altered microarray applied current distribution (i.e., different than that predicted by the simulation) to the micro inert anode elements. Overall, an optimized model may be achieved in a two-step procedure: the first step obtains an optimal current distribution by setting the die features to equal current density, where an anode ground plane **1420** is set to ground potential to simulate a continuous conductive surface so that current density can be extracted from the anode ground plane **1420**; the second step obtains a model for the micro inert anode array, where each of the micro inert anode elements **1430** are treated as current sources in a grid surrounded by an insulator, and each micro inert anode element **1430** is assigned a current density calculated from an optimal current density taken from the anode ground plane **1420**. Finally, a process that combines this two-step simulation process, used as program a first micro anode array test-current distribution, followed by analysis of the wafer results, and then one or more subsequent test runs with relatively minor modifications to the distribution pattern targeted to achieve an optimal current distribution, is envisioned. This results in a non-uniform plating distribution **1440** shown in FIG. **14**D, which approximates the on-wafer plating performance.

[0124] An alternative procedure to determine the optimal micro inert anode element current distribution omits the initial simulation, and instead directly calculates a "results" simulation with a uniform current assigned to each micro inert anode element. Based on the result of this simulation, the current assigned to each micro inert array element is perturbed (e.g. increased in regions where the current density on the substrate is low) and the simulation is re-run. This procedure is then repeated until the current density on the substrate meets a minimum result, or a desired uniformity specification.

[0125] The model of the present disclosure can be constructed by first approximating the geometry of the substrate and the volume between the substrate and the micro inert anode array. An example of such a model can be seen in FIG. **14**A. The model may be simplified by considering only a single die or repeat unit, approximating uniform areas of small features as uniform areas of larger features while maintaining the same open area, or approximating round, oblong, or otherwise complex feature shapes as squares. The latter two approximations can be checked for accuracy against a more detailed model or empirical data for accuracy before use. Surface resistances may be approximated by assigning the plating surface a resistance or by assigning the modeled feature a resistivity, the value of which can be derived from experiment or calculated from other known values. Mass transport of the metal ions may be represented in the model fully, or approximated by a calculation of the diffusion boundary layer thickness and the additional resistance this imposes, or omitted entirely in cases where it is not a concern.

[0126] Boundary conditions are then determined, and the Laplace equation is solved for this geometry to determine the current and potential within the domain. To determine the current that each electrode in the micro inert anode array should produce, the boundary conditions imposed can be as follows: first, the plating surface (in each feature) is assigned the same current density at all points; second, the surface bearing the inert anode array is treated as a continuous conductive grounded surface. Additional boundary conditions representing symmetry planes or periodicity (e.g. due to adjacent dice) are set as appropriate for the geometry. The solution to this model gives an "ideal" current distribution, which if imposed at the inert anode array should give a near-0% non-uniformity. This result for the example die is shown in FIG. **14**B. During electroplating, each inert anode can be assigned a current based on its location in this ideal current distribution as demonstrated in FIG. **14**C.

[0127] The results can additionally be verified and the actual non-uniformity predicted by setting the boundary conditions of the same model such that the plating surface in

each feature is a continuous conductive grounded surface and the inert anodes each have a current density dictated by the previously calculated ideal current distribution. The solution to this model, as illustrated in FIG. **14**D for the example die, approximates the actual on-wafer performance expected.

[0128] FIGS. **15**A-**15**C depict maps of feature current density distribution for varying anode array element pitches in a micro inert anode array. The results show that when using micro inert anode elements whose critical dimensions are smaller than the anode to wafer gap, one can more effectively direct current to the desired regions of a die layout. In contrast, when using larger micro inert anode elements, the potential and current will distribute in an unfavorable manner in the gap with imaging associated with each individual anode element. Each bar is a gradient map in greyscale representing the local current distribution on the modeled die for a particular condition. In FIG. **15**A, the micro inert anode array has a small pitch of 1 mm between adjacent micro inert anode elements **1510***a* The gap size between the micro inert anode array and the wafer is 1 mm. In FIG. **15**B, the micro inert anode array has a larger pitch of 4 mm between adjacent micro inert anode elements **1510***b*. The gap size between the micro inert anode array and the wafer is 1 mm. In FIG. **15**C, the micro inert anode array also has a larger pitch of 4 mm between adjacent micro inert anode elements **1510***c* but uses constant current, which approximates the situation of using a uniform 4 mm pitch HRVA. The gap between the substrate and micro inert anode array is the same at 1 mm. As shown in FIGS. **15**A-**15**C, decreased pitch can more effectively direct current to the desired regions of the die layout, and a more uniform constant current (rather than a spatially tuned current) fails to direct current to desired regions of the die layout.

[0129] Comparing the two 4 mm pitch cases between FIGS. **15**B and **15**C, for gaps less than about 4 mm, the variable distributed micro inert anode array currents can show a significantly tighter current distribution than the constant current case. In some cases, the die features are separated at a distance larger than the gap (4 mm pitch>2 mm gap), and a region of high current corresponding to the location of the individual micro inert anode element is seen. At smaller pitches for these same smaller gaps, the current distribution is more spatially uniform. Generally, in order to achieve the optimal plated die distributions, the micro inert anode array pitch should be smaller than the array-to-substrate gap, or the relationship P/G<1, where P is the pitch and G is the gap. Therefore, the uniformity of plating thicknesses in non-uniform die patterns improve with smaller gaps as long as the micro inert anode element size and pitch are less than the gap size.

[0130] In the range of gaps greater than about 5 mm but less than a distance where a continuous anode source reaches an asymptote of non-uniformity, the non-uniformity of all the micro inert anode array cases have a higher non-uniformity than this value, and a single anode far away would be superior to a micro inert anode array at theses gap sizes. However, below about 5 mm gap, all of the anode pitch cases shown have a lower non-uniformity than this baseline case, with a value of about 4%, or more than 3 times better for the smallest gap and smallest pitch (1 mm gap/pitch). As before, the 4 mm pitch case has an uptick in non-uniformity at the 1 mm gap case, because the gap is smaller than the pitch and the individual micro inert anode elements create a concentration of current around their projected position on the die layout. For a gap below about 1 mm (P/G=1), no further improvement in non-uniformity is obtained. For better non-uniformity, a smaller gap in combination with a smaller pitch is required. There are practical limitation and tradeoffs to consider for each case between using a smaller gap and smaller pitch: the smaller the pitch, the more expensive the array and the more complex the control of the parabolically larger number of micro inert anode elements. Smaller gaps are mechanically more difficult to set and maintain coplanarity, particularly when combined with rotation, and fluid flow through the gap and large system pressures to enable minimal mass transfer plating resistances can become increasingly problematic.

[0131] FIG. **16** illustrates a cross-sectional schematic view of an example micro inert anode array positioned relative to a semiconductor substrate according to some implementations. The micro inert anode array **1620** includes a plurality of micro inert anode elements **1625**. The semiconductor substrate **1630** may be a partially fabricated semiconductor substrate having a pattern of features **1660**. The pattern of features **1660** may be non-uniformly distributed in one or more dice. The pattern of features **1660** may be disposed on a conductive seed layer **1640** of the semiconductor substrate **1630**. Metal-containing electrolyte may flow between the semiconductor substrate **1630** and the micro inert anode array **1620** in an electroplating cell.

[0132] A pitch between adjacent micro inert anode elements **1625** may be defined by p. Each of the micro inert anode elements may have a critical dimension (e.g., diameter) defined by d. A gap size between the semiconductor substrate **1630** and the micro inert anode array **1620** may be defined by g. A distance between repeating substrate patterns in the pattern of features **1660** may be defined by L. Current is applied to the micro inert anode elements **1625** in the micro inert anode array **1620** to provide a particular current distribution over an area of the semiconductor substrate **1630** having the pattern of features **1660**. The area may include an area of repeating layouts of patterned features or repeating substrate patterns, where the repeating substrate patterns may be separated by the distance L. For effective current distribution control, dimensions p (pitch), g (gap size), d (critical dimension), and L (distance between repeating substrate patterns) are optimized. Generally speaking, for effective current distribution control to target variable current to different regions of the semiconductor substrate **1630**, p is configured to be less than L, p is configured to be less than g, and d is configured to be less than L In some embodiments, g is also configured to be less than L. Accordingly, for the ability to effectively target variable currents into regions of different pattern density, dimensionless ratios of g/L and p/L, and d/L are each less than 1. To further effectively use the micro inert anode elements **1625** for enhanced current control, p is configured to be at least three times less than g, and d is configured to be at least three times less than g. In other words, dimensionless ratios of p/g and d/g are less than ⅓. At such dimensions, this level of current distribution control prevents images and discrete anodes.

[0133] The previously described procedure with respect to FIGS. **15**A-**15**C was used to simulate the performance of a micro inert anode array on a simple die pattern. Another example die pattern consists of 200 μm features in a square

frame pattern on a 15 mm×15 mm die. The results of this simulation can be found in FIGS. **17**A-I **7**D and FIG. **18**.

[0134] FIG. **17**A illustrates an example current distribution on a patterned feature layout of a die using an HRVA. While only a single die is pictured, the simulation is designed to emulate a repeating array of such dice. With a uniform current source, the features tend to be plated thicker at the sides of the die relative to the corners of the die. This is due at least in part to a lower local open area or lower feature density loading at the sides. As shown in FIG. **17**B with a repeating array of such dice, features are more closely concentrated at the corners of each die than at the sides of each die. Since the HRVA facilitates a uniform current density across the repeating array of dice, less plating occurs at the corners than at the sides due to the non-uniform distribution of features.

[0135] FIG. **17**C illustrates an example current distribution of a micro inert anode array on a patterned feature layout of a die at a 1 mm gap according to some implementations. FIG. **17**D illustrates an example current distribution of a micro inert anode array on a patterned feature layout of a die at a 4 mm gap according to some implementations. The within-die (WID) non-uniformity of the die with a micro inert anode array at a 4 mm gap is similar to the WID non-uniformity when plating using an HRVA (substantially uniform current source). Here, the 4 mm gap between the micro inert anode array and the die is large enough to allow the current to redistribute freely over the 10 mm-wide die, so that the micro inert anode array cannot be used to effectively control the current density at the plating surface. However, as the micro inert anode array is moved closer to the die, the ability to control the current density at the plating surface improves, and more current can be directed to the corners of the die to reduce VID non-uniformity. As shown in FIG. **17**C, the features tend to be plated substantially uniformly at the sides of the die and at the corners of the die. In FIG. **17**D, the features tend to be plated thicker at the sides of the die relative to the corners of the die. These simulations indicate that the distance over which the current can be effectively redirected within the die is related to the gap size between the micro inert anode array and the die.

[0136] FIG. **18** illustrates a graph showing within-die uniformity as a function of a gap between a micro inert anode array and a semiconductor substrate. At a 4 mm gap size between the micro inert anode array and a semiconductor substrate having one or more dice such as described in FIGS. **17**A-**17**D, the WID non-uniformity is approximately 3%. The WID non-uniformity at such a gap is similar to the WID non-uniformity when plating with an HRVA. At a 1 mm gap size between the micro inert anode array and a semiconductor substrate having one or more dice such as described in FIGS. **17**A-**17**D, the WID non-uniformity is approximately 1%. The WID non-uniformity is reduced to approximately ¼ of the prior value. At a gap size greater than 6 mm, there is little change in WID non-uniformity. At a gap size greater than 8 mm (not shown in FIG. **8**), there is essentially no change in WID non-uniformity. At a gap size smaller than 4 mm, the WID non-uniformity decreases relatively quickly with gap size. Simulations with other die layouts confirm the following observation: if there is some characteristic distance for feature heights that contribute to WID non-uniformity, gap size has little to no effect on WID non-uniformity when the gap size is equal to or larger than the characteristic distance. When the gap size is between 0.5 and 1 times this characteristic distance for feature heights, then the gap size has a weak effect on VID non-uniformity. When the gap size is less than 0.5 times this characteristic distance for feature heights, then the gap size has a strong effect on VID non-uniformity. In some embodiments, this characteristic distance between feature heights can be a distance between the maximum and minimum heights on the die, which is approximately half the die width. In some embodiments, this characteristic distance between feature heights can constitute a length of the variance of pattern densities. In FIGS. **17**A-**17**D, the characteristic distance or half the die width is approximately 7-8 mm. Accordingly, the gap size can be configured to be less than 0.5 times this characteristic distance (i.e., less than 4 mm) to have a strong effect on VID non-uniformity, Note that because the micro inert anode array is a discrete array of anodes, current control is not possible at a size scale smaller than the pitch of the micro inert anode elements. Therefore, the pitch of the micro inert anode elements imposes a lower limit on the effects of the gap size on the WID non-uniformity. Going to a smaller gap that is lower than this limit will not yield further improvements in WID non-uniformity.

[0137] In the present disclosure, a desired current distribution can be programmed to be applied using a driver system (e.g., array driver) and computer programming software implemented on a controller. Even if processing different substrates with different die layouts, no physical change in plating tool hardware is required. This is in contrast with attempting to achieve the desired current distribution using a HRVA with a spatial arrangement of holes, or varying local resistivity, because the HRVA would have to be switched out for a different physical part with a different design suited for the new feature pattern, for processing different substrates with different die layouts. The relative orientation of the substrate to the array can be determined and maintained throughout the electroplating process. If the substrate is placed in a substrate holder such as a cup, the position of the substrate relative to the array can be made with a precision generally better than the gap size, such as to a precision of about 20% or even about 5% of the gap size. Therefore, hardware suitable for reproducibly placing the substrate inside those tolerances may be employed, or alternatively, hardware capable of determining the position of each substrate placed into the plating cell to those tolerances may be used.

[0138] Returning to FIG. **2**, at block **250**, electrolyte is flowed laterally across a substrate surface and the semiconductor substrate is rotated while the micro inert anode array is energized to achieve a desired spatial and temporal current distribution pattern. As discussed above, substrate rotation may be employed to achieve time average directional flow uniformity, and as a result WIF uniformity and avoid unevenly-shaped features. For instance, in FIGS. **6**A and **6**B, if flow fields occur in one direction, then non-uniform feature profiles in recessed features are produced. Even if flow fields occur in multiple directions, non-uniform feature profiles in recessed features can still result. Having the flow field change during the electroplating process can reduce the non-uniformity of feature profiles, but some non-uniformity may still be evident. One technique for achieving improved uniformity within features is to have the flow entering the gap between the semiconductor substrate and the micro inert anode array on one side and rotating the semiconductor substrate. Thus, in the present disclosure, the electrolyte may

be provided in the plating chamber such that it flows laterally substantially parallel to the plating face of the semiconductor substrate. In such embodiments, the electrolyte flows substantially in one direction entering and exiting the plating chamber at azimuthally opposite positions proximate the perimeter of the chamber. As the electrolyte flows laterally, the semiconductor substrate is rotated. However, it will be understood that alternative techniques may be employed for achieving improved uniformity within features, such as enabling the flow entering the gap between the semiconductor substrate and micro inert anode array come from a set of or continuously different directions.

[0139] If the semiconductor substrate is rotated, the applied current to each of the micro inert anode elements in the array may follow the locations of the die features. In other words, the current distribution in the micro inert anode array can dynamically change according to the position of die features in a semiconductor substrate even as the semiconductor substrate is rotated. The array-imposed current pattern can follow a time-variable distribution of the optimized target distribution, with the rotation of the semiconductor substrate around a mechanical rotation center. Because the rotation center may move (i.e. the concentricity of the rotation of the micro inert anode array to the wafer center may not be perfect), the magnitude and direction of the non-concentricity relative to the rotation center can be determined, and the programmed time-varying array current distribution may be modified over time. By way of an example, prior to starting the electroplating process, the relative center position of the semiconductor substrate to the micro inert anode array can be determined and the non-concentricity magnitude and direction can also be determined. The semiconductor substrate is indexed, and rotation of the semiconductor substrate is started and followed by a computer program or controller. The semiconductor substrate is immersed into the plating solution and the plating solution fills the gap between the semiconductor substrate and the micro inert anode array. The computer program or controller is configured to turn on power at the power source knowing where the semiconductor substrate and die feature positions are at that point in time. At a set time later (e.g., after 10 ms), the semiconductor substrate shall have rotated a known amount, and the center position of the semiconductor substrate will have shifted by a known amount, allowing the controller to calculate the new die feature location relative to the micro inert anode array. The controller can also calculate a new optimal micro inert anode element current distribution, decreasing or increasing the various element applied current depending on the calculated requirements, and modifying the current distribution to the new current distribution. This process is repeated as the semiconductor substrate rotates and plating occurs during the entire electroplating process until the target time and/or target film thickness is achieved.

[0140] In some embodiments, the semiconductor substrate may be rotated according to a time base edge shielding, or "smart" spin technique. Such techniques are further discussed in U.S. Pat. No. 9,260,793 to Mayer et al., filed Sep. 11, 2014, and titled "ELECTROPLATING APPARATUS FOR TAILORED UNIFORMITY PROFILE," which is herein incorporated by reference in its entirety and for all purposes. Because die layouts at the edge of a semiconductor substrate may not be uniform and because some portions of the die may have "missing dice," at certain azimuthal locations, the semiconductor substrate may be slowed down or sped up over a shielded or missing region of an HRVA, depending on the die layout or die pattern. This process is sometimes referred to as the "smart spin" technique. As the semiconductor substrate is rotated, a portion of the semiconductor substrate (e.g., missing die) may be encountered that needs to get less current or no current in such spaces. The substrate rotation may initially be slow but then quickly sped up upon encountering the portion of the semiconductor substrate that requires less or no current. Accordingly, the rotation of the semiconductor substrate may be dynamically changed in response to encountering certain die patterns during rotation. Implementations of the "smart spin" technique can be extended to micro inert anode array plating methods and apparatuses, by having certain peripheral regions of the micro inert anode array missing active anode elements, or having them blocked or otherwise shielded. However, because micro inert anode array elements can be turned off and/or modulated in current intensity, it will be understood that in some instances, substrate rotation according to "smart" spin techniques may be unnecessary. Specifically, the micro inert anode array may be programmed so that missing die regions are programmed to not have inert anodes supplying current to those regions. As rotation occurs, the pattern of low current in the missing die traces the angular rotation of the part. This technique has the advantage over the shielding and rotation speed modulation ("smart spin") technique in that an inherent time-based flow direction bias associated with dwelling in one region and angular orientation and the related feature shape irregularities that can occur can be avoided.

[0141] The features being plated may be started at a substantially deep photoresist depth. For example, a 20 μm diameter feature may be 20 μm or 40 μm deep. The mass transfer and ionic (ohmic) resistance to plating inside a deep feature can be significant relative to a resistance governing the distribution of current to an array of plated metal features. So as metal features are plated on the semiconductor substrate, if the anode source position and source distribution remains unchanged, the current distribution across the micro inert anode array will also change, due to the reduction in the series resistance from the resistance of mass transfer and electrical (ionic) resistance. Larger or smaller features and features in high versus lower densities, will experience a different relative change of these resistance. Therefore, an optimal applied micro inert anode array current distribution for a feature in a 20 μm deep condition is not likely to be the optimal applied micro inert anode array current distribution when the features are 10 μm or 5 μm deep. Therefore, during the plating process, changing parameters to maintain an instantaneously optimal profile such as changing the micro inert anode array programmed/applied current distribution, or changing the array-to-substrate gap, can be used to obtain a desired time-integrated plating non-uniformity result.

[0142] At block **260**, the semiconductor substrate may undergo substrate post-treatment. In some embodiments, the substrate post-treatment can include rinsing, drying, and/or cleaning operations in a rinse/dry/clean station. In some embodiments, the substrate post-treatment can include etching in an etching module. Etches may be performed to selectively remove photoresist, or etches may be used to selectively remove patterned features or non-patterned features. Removal of patterned features may only remove

portions of the patterned features to achieve coplanarity. Thus, the process may include both plating and etching operations.

Electroplating Systems

[0143] The methods described herein may be performed by any suitable system/apparatus. A suitable apparatus includes hardware for accomplishing the process operations and a system controller having instructions for controlling process operations in accordance with the present embodiments. For example, in some embodiments, the hardware may include one or more process stations included in a process tool.

[0144] FIG. **19** depicts a simplified view of a multi-tool electroplating apparatus according to some implementations. The electrodeposition apparatus **1900** can include three separate electroplating modules **1902**, **1904**, and **1906**. The electrodeposition apparatus **1900** can also include three separate modules **1912**, **1914**, and **1916** configured for various process operations. For example, in some embodiments, one or more of modules **1912**, **1914**, and **1916** may be a spin rinse drying (SR-D) module. In other embodiments, one or more of the modules **1912**, **1914**, and **1916** may be post-electrofill modules (PEMs), each configured to perform a function, such as edge bevel removal, backside etching, and acid cleaning of substrates after they have been processed by one of the electroplating modules **1902**, **1904**, and **1906**.

[0145] The electrodeposition apparatus **1900** includes a central electrodeposition chamber **1924**. The central electrodeposition chamber **1924** is a chamber that holds the chemical solution used as the electroplating solution in the electroplating modules **1902**, **1904**, and **1906**. The electrodeposition apparatus **1900** also includes a dosing system **1926** that may store and deliver additives for the electroplating solution. A chemical dilution module **1922** may store and mix chemicals to be used as an etchant. A filtration and pumping unit **1928** may filter the electroplating solution for the central electrodeposition chamber **1924** and pump it to the electroplating modules.

[0146] A system controller **1930** provides electronic and interface controls required to operate the electrodeposition apparatus **1900**. The system controller **1930** (which may include one or more physical or logical controllers) controls some or all of the properties of the electroplating apparatus **1900**.

[0147] Signals for monitoring the process may be provided by analog and/or digital input connections of the system controller **1930** from various process tool sensors. The signals for controlling the process may be output on the analog and digital output connections of the process tool. Non-limiting examples of process tool sensors that may be monitored include mass flow controllers, pressure sensors (such as manometers), thermocouples, optical position sensors, etc. Appropriately programmed feedback and control algorithms may be used with data from these sensors to maintain process conditions.

[0148] A hand-off tool **1940** may select a substrate from a substrate cassette such as the cassette **1942** or the cassette **1944**. The cassettes **1942** or **1944** may be front opening unified pods (FOUPs). A FOUP is an enclosure designed to hold substrates securely and safely in a controlled environment and to allow the substrates to be removed for processing or measurement by tools equipped with appropriate load ports and robotic handling systems. The hand-off tool **1940** may hold the substrate using a vacuum attachment or some other attaching mechanism.

[0149] The hand-off tool **1940** may interface with a wafer handling station **1932**, the cassettes **1942** or **1944**, a transfer station **1950**, or an aligner **1948**. From the transfer station **1950**, a hand-off tool **1946** may gain access to the substrate. The transfer station **1950** may be a slot or a position from and to which hand-off tools **1940** and **1946** may pass substrates without going through the aligner **1948**. In some embodiments, however, to ensure that a substrate is properly aligned on the hand-off tool **1946** for precision delivery to an electroplating module, the hand-off tool **1946** may align the substrate with an aligner **1948**. The hand-off tool **1946** may also deliver a substrate to one of the electroplating modules **1902**, **1904**, or **1906** or to one of the three separate modules **1912**, **1914**, and **1916** configured for various process operations.

[0150] An example of a process operation according to the methods described above may proceed as follows: (1) receiving a substrate in an electroplating module, where the substrate includes one or more dice having a non-uniform distribution of features; (2) contacting the substrate with an electrolyte in the electroplating module; and (3) electroplating metal on the substrate using a micro inert anode array having a plurality of micro inert anode elements, where current is applied to one or more micro inert anode elements to achieve a current distribution based at least in part on feature layouts of the one or more dice. In some embodiments, a gap size defined between the substrate and the micro inert anode array is equal to or greater than a pitch defined between micro inert anode elements in the array. In some embodiments, contacting the substrate with the electrolyte includes cross-flowing the electrolyte laterally across the surface of the substrate.

[0151] An apparatus configured to allow efficient cycling of substrates through sequential plating, rinsing, drying, and PEM process operations may be useful for implementations for use in a manufacturing environment. To accomplish this, the module **1912** can be configured as a spin rinse dryer and an edge bevel removal chamber. With such a module **1912**, the substrate would only need to be transported between the electroplating module **1904** and the module **1912** for the copper plating and EBR operations. In some embodiments the methods described herein will be implemented in a system which comprises an electroplating apparatus and a stepper.

[0152] FIG. **20** depicts a simplified view of an example electroplating apparatus with different electroplating cells and modules according to some implementations. An alternative embodiment of an electrodeposition apparatus **2000** is schematically illustrated in FIG. **20**. In this embodiment, the electrodeposition apparatus **2000** has a set of electroplating cells **2007**, each containing an electroplating bath, in a paired or multiple "duet" configuration. In addition to electroplating per se, the electrodeposition apparatus **2000** may perform a variety of other electroplating related processes and sub-steps, such as spin-rinsing, spin-drying, metal and silicon wet etching, electroless deposition, pre-wetting and pre-chemical treating, reducing, annealing, electro-etching and/or electropolishing, photoresist stripping, and surface pre-activation with a pre-accelerator solution, for example. The electrodeposition apparatus **2000** is shown schematically looking top down in FIG. **20**, and only a single level

or "floor" is revealed in the figure, but it is to be readily understood by one having ordinary skill in the art that such an apparatus, e.g., the Lam Sabre™ 3D tool, can have two or more levels "stacked" on top of each other, each potentially having identical or different types of processing stations.

[0153] Referring once again to FIG. **20**, the substrates **2006** that are to be electroplated are generally fed to the electrodeposition apparatus **2000** through a front end loading FOUP **2001** and, in this example, are brought from the FOUP to the main substrate processing area of the electrodeposition apparatus **2000** via a front-end robot **2002** that can retract and move a substrate **2006** driven by a spindle **2003** in multiple dimensions from one station to another of the accessible stations-two front-end accessible stations **2004** and also two front-end accessible stations **2008** are shown in this example. The front-end accessible stations **2004** and **2008** may include, for example, pre-treatment stations, and spin rinse drying (SRD) stations. Lateral movement from side-to-side of the front-end robot **2002** is accomplished utilizing robot track **2002***a*. Each of the substrates **2006** may be held by a cup/cone assembly (not shown) driven by a spindle **2003** connected to a motor (not shown), and the motor may be attached to a mounting bracket **2009**. Also shown in this example are the four "duets" of electroplating cells **2007**, for a total of eight electroplating cells **2007**. A system controller (not shown) may be coupled to the electrodeposition apparatus **2000** to control some or all of the properties of the electrodeposition apparatus **2000**. The system controller may be programmed or otherwise configured to execute instructions according to processes described earlier herein.

[0154] In some implementations, a controller is part of a system, which may be part of the above-described examples. Such systems can comprise semiconductor processing equipment, including a processing tool or tools, chamber or chambers, a platform or platforms for processing, and/or specific processing components (a wafer pedestal, a gas flow system, etc.). These systems may be integrated with electronics for controlling their operation before, during, and after processing of a semiconductor wafer or substrate. The electronics may be referred to as the "controller," which may control various components or subparts of the system or systems. The controller, depending on the processing requirements and/or the type of system, may be programmed to control any of the processes disclosed herein, including the delivery of processing gases, temperature settings (e.g., heating and/or cooling), pressure settings, vacuum settings, power settings, radio frequency (RF) generator settings, RF matching circuit settings, frequency settings, flow rate settings, fluid delivery settings, positional and operation settings, wafer transfers into and out of a tool and other transfer tools and/or load locks connected to or interfaced with a specific system.

[0155] Broadly speaking, the controller may be defined as electronics having various integrated circuits, logic, memory, and/or software that receive instructions, issue instructions, control operation, enable cleaning operations, enable endpoint measurements, and the like. The integrated circuits may include chips in the form of firmware that store program instructions, digital signal processors (DSPs), chips defined as application specific integrated circuits (ASICs), and/or one or more microprocessors, or microcontrollers that execute program instructions (e.g., software). Program instructions may be instructions communicated to the controller in the form of various individual settings (or program files), defining operational parameters for carrying out a particular process on or for a semiconductor wafer or to a system. The operational parameters may, in some embodiments, be part of a recipe defined by process engineers to accomplish one or more processing steps during the fabrication of one or more layers, materials, metals, oxides, silicon, silicon dioxide, surfaces, circuits, and/or dice of a wafer.

[0156] The controller, in some implementations, may be a part of or coupled to a computer that is integrated with, coupled to the system, otherwise networked to the system, or a combination thereof. For example, the controller may be in the "cloud" or all or a part of a fab host computer system, which can allow for remote access of the wafer processing. The computer may enable remote access to the system to monitor current progress of fabrication operations, examine a history of past fabrication operations, examine trends or performance metrics from a plurality of fabrication operations, to change parameters of current processing, to set processing steps to follow a current processing, or to start a new process. In some examples, a remote computer (e.g. a server) can provide process recipes to a system over a network, which may include a local network or the Internet. The remote computer may include a user interface that enables entry or programming of parameters and/or settings, which are then communicated to the system from the remote computer. In some examples, the controller receives instructions in the form of data, which specify parameters for each of the processing steps to be performed during one or more operations. It should be understood that the parameters may be specific to the type of process to be performed and the type of tool that the controller is configured to interface with or control, Thus as described above, the controller may be distributed, such as by comprising one or more discrete controllers that are networked together and working towards a common purpose, such as the processes and controls described herein. An example of a distributed controller for such purposes would be one or more integrated circuits on a chamber in communication with one or more integrated circuits located remotely (such as at the platform level or as part of a remote computer) that combine to control a process on the chamber.

[0157] Without limitation, example systems may include a plasma etch chamber or module, a deposition chamber or module, a spin-rinse chamber or module, a metal plating chamber or module, a clean chamber or module, a bevel edge etch chamber or module, a physical vapor deposition (PVD) chamber or module, a chemical vapor deposition (CVD) chamber or module, an atomic layer deposition (ALD) chamber or module, an atomic layer etch (ALE) chamber or module, an ion implantation chamber or module, a track chamber or module, and any other semiconductor processing systems that may be associated or used in the fabrication and/or manufacturing of semiconductor wafers.

[0158] In the foregoing description, numerous specific details are set forth to provide a thorough understanding of the presented embodiments. The disclosed embodiments may be practiced without some or all of these specific details. In other instances, well-known process operations have not been described in detail to not unnecessarily obscure the disclosed embodiments. While the disclosed embodiments are described in conjunction with the specific

embodiments, it will be understood that it is not intended to limit the disclosed embodiments.

[0159] Although the foregoing embodiments have been described in some detail for purposes of clarity of understanding, it will be apparent that certain changes and modifications may be practiced within the scope of the appended claims. It should be noted that there are many alternative ways of implementing the processes, systems, and apparatus of the present embodiments. Accordingly, the present embodiments are to be considered as illustrative and not restrictive, and the embodiments are not to be limited to the details given herein.

What is claimed is:

1. A method of electroplating metal features on a substrate, the method comprising:

receiving a substrate in an electroplating chamber, wherein the substrate includes one or more dice having a distribution of patterned features;

contacting the substrate with an electrolyte in the electroplating chamber; and

electroplating metal on the substrate using a micro inert anode array having a plurality of micro inert anode elements, wherein current is applied to two or more micro inert anode elements to provide a non-uniform current distribution over an area of the substrate.

2. The method of claim **1**, wherein the current is applied to two or more micro inert anode elements to provide the non-uniform current distribution that is based at least in part on patterned feature layouts of the one or more dice.

3. The method of claim **1**, wherein the current is applied to two or more micro inert anode elements to provide the non-uniform current distribution that is based at least in part on global within-wafer (WW) corrections.

4. The method of claim **1**, wherein the one or more dice comprise layouts of patterned features, wherein the area over which the non-uniform current distribution is applied includes a distance between repeating layouts of patterned features, and wherein the distance is larger than a pitch defined between micro inert anode elements and larger than a gap size defined between the substrate and the micro inert anode array.

5. The method of claim **1**, wherein a gap size defined between the substrate and the micro inert anode array is equal to or greater than a pitch defined between micro inert anode elements in the micro inert anode array.

6. The method of claim **5**, wherein the gap size is at least three times greater than the pitch defined between micro inert anode elements and at least three times greater than a critical dimension of each micro inert anode element.

7. The method of claim **1**, wherein a gap size defined between the substrate and the micro inert anode array is equal to or less than about 4 mm.

8. The method of claim **1**, wherein a pitch defined between micro inert anode elements in the micro inert anode array is equal to or less than about 500 urn.

9. The method of claim **1**, wherein contacting the substrate with the electrolyte includes cross-flowing the electrolyte laterally across the surface of the substrate.

10. The method of claim **1**, further comprising:

identifying patterned feature layouts in the one or more dice in the substrate prior to electroplating metal on the substrate using the micro inert anode array.

11. The method of claim **1**, further comprising:

determining a current distribution on an anode ground plane from a uniform die current distribution through a simulation or calculation to obtain a simulated or calculated current distribution; and

assigning current values to each of the micro inert anode elements in the micro inert anode array based on the simulated or calculated current distribution on the anode ground plane.

12. The method of claim **1**, further comprising:

rotating the substrate while electroplating metal on the substrate using the micro inert anode array; and

changing current applied to the two or more micro inert anode elements to achieve a new current distribution based at least in part on positioning of patterned feature layouts of the one or more dice after rotation.

13. The method of claim **1**, wherein each of the micro inert anode elements are physically isolated from one another, electrically isolated from one another, and independently controllable to receive current from a power source.

14. The method of claim **1**, wherein the metal is electroplated with a substantially uniform thickness in the one or more dice having a distribution of patterned features.

15. The method of claim **1**, wherein the substrate has patterned photoresist over a conductive seed layer, wherein the metal is electroplated in recessed features defined by the patterned photoresist and on exposed portions of the conductive seed layer.

16. An electroplating apparatus comprising:

a substrate holder configured to hold a partially fabricated semiconductor substrate, wherein the partially fabricated semiconductor substrate comprises one or more dice having a distribution of patterned features;

a micro inert anode array proximate the partially fabricated semiconductor substrate, wherein the micro inert anode array includes a plurality of independently controllable micro inert anode elements arranged in an array; and

a cross-flow manifold configured to contain an electrolyte flowing between the micro inert anode array and the partially fabricated semiconductor substrate, wherein the cross-flow manifold promotes cross flowing of the electrolyte across the surface of the partially fabricated semiconductor substrate.

17. The electroplating apparatus of claim **16**, wherein the one or more dice have a non-uniform distribution of patterned features.

18. The electroplating apparatus of claim **16**, wherein a gap size defined between the partially fabricated semiconductor substrate and the micro inert anode array is equal to or greater than a pitch defined between micro inert anode elements in the micro inert anode array.

19. The electroplating apparatus of claim **18**, wherein the gap size is equal to or less than about 4 mm and wherein the pitch is equal to or less than about 500 μm.

20. The electroplating apparatus of claim **16**, wherein the micro inert anode array comprises at least 100 micro inert anode elements.

21. The electroplating apparatus of claim **16**, further comprising:

a controller configured with instructions to perform the following operations:

apply current to two or more micro inert anode elements in the array to provide a desired current

distribution based at least in part on a layout of patterned features in the partially fabricated semiconductor substrate.

22. The electroplating apparatus of claim **21**, wherein the controller is further configured with instructions to perform the following operations:

rotate the partially fabricated semiconductor substrate while electrolyte is flowing across the surface of the partially fabricated semiconductor substrate; and

change current to the two or more micro inert anode elements in the array to provide a new current distribution based at least in part on positioning of the layout of patterned features in the partially fabricated semiconductor substrate after rotation.

23. An electroplating apparatus comprising:

a substrate load/unload station configured to receive a semiconductor substrate;

a substrate pretreatment station configured to pretreat the semiconductor substrate;

one or more electroplating stations configured to plate metal on the semiconductor substrate, each electroplating station comprising:

a substrate holder configured to hold the semiconductor substrate:

a micro inert anode array comprising a plurality of independently controllable micro inert anode elements, wherein the micro inert anode array is spaced apart from the semiconductor substrate by a gap that is greater than a pitch between the micro inert anode elements; and

a plating bath reservoir configured to deliver electrolyte to the gap between the micro inert anode array and the semiconductor substrate; and

one or more robots configured to transfer the semiconductor substrate between the substrate load/unload station and the substrate pretreatment station and between the substrate pretreatment station and the one or more electroplating stations.

24. The electroplating apparatus of claim **23**, wherein the substrate pretreatment station comprises one or both of a vacuum backfill station and an acid pre-wetting station.

25. The electroplating apparatus of claim **23**, wherein each of the one or more electroplating stations further comprises:

a flow controller conficured to control a flow and chemical dosing of the electrolyte delivered to the gap between the micro inert anode array and the semiconductor substrate;

a temperature controller configured to control a temperature of the electrolyte in the plating bath reservoir; and

a degasser configured to remove dissolved gases from the electrolyte prior to delivery into the gap between the micro inert anode array and the semiconductor substrate.

26. The electroplating apparatus of claim **25**, wherein each of the one or more electroplating stations further comprises:

a metal oxide dose control unit configured to dose the electrolyte in the plating bath reservoir with metal oxide to mitigate acidification and metal ion depletion in the electrolyte.

27. The electroplating apparatus of claim **25**, wherein each of the one or more electroplating stations further comprises:

a soluble ion redox couple configured regenerate one or more metal ions in the electrolyte and prevent acidification and metal ion depletion in the electrolyte.

28. The electroplating apparatus of claim **23**, further comprising:

one or more additional electroplating stations without a micro inert anode array and configured to plate metal on the semiconductor substrate.

29. A method of modeling a current distribution in a micro inert anode array, the method comprising:

receiving a substrate having a die with a non-uniform distribution of features;

determining a current distribution on an anode ground plane from a uniform die current distribution in the die of the substrate; and

assigning current values to each of a plurality of micro inert anode elements in a micro inert anode array based on the current distribution on the anode ground plane.

30. The method of claim **29**, wherein the anode ground plane corresponds to a counter electrode having a continuous conductive surface.

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