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[Continued on next page]

(54) Title: COMBINING DATA FROM MULTIPLE IMAGE SENSORS

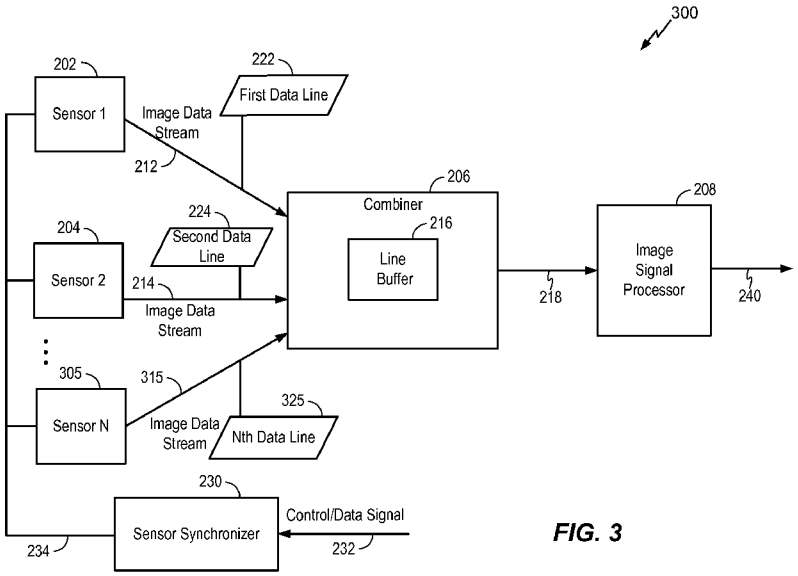

FIG. 3

(57) Abstract: A method of combining data from multiple sensors is disclosed. The method includes providing a common control signal to multiple image sensors to be synchronized. The method further includes receiving a first data line from a first image sensor of the multiple image sensors, receiving a second data line from a second image sensor of the multiple image sensors, and combining the first data line and the second data line to generate a synchronized data line.

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COMBINING DATA FROM MULTIPLE IMAGE SENSORS

Priority Claim

[0001] This application claims the benefit of, and incorporates by reference, each of U.S. Provisional Application No. 61/320,940 filed April 5, 2010, U.S. Provisional Application No. 61/324,259 filed April 14, 2010, U.S. Provisional Application No. 61/359,312 filed June 28, 2010, and U.S. Provisional Application No. 61/412,755, filed November 11, 2010.

Field

[0002] The present disclosure is generally related to combining data from multiple image sensors.

Description of Related Art

[0003] Advances in technology have resulted in smaller and more powerful computing devices. For example, there currently exist a variety of portable personal computing devices, including wireless computing devices, such as portable wireless telephones, personal digital assistants (PDAs), and paging devices that are small, lightweight, and easily carried by users. More specifically, portable wireless telephones, such as cellular telephones and internet protocol (IP) telephones, can communicate voice and data packets over wireless networks. Further, many such wireless telephones include other types of devices that are incorporated therein. For example, a wireless telephone can also include a digital still camera and a digital video camera. Also, such wireless telephones can process executable instructions, including software applications, such as a web browser application, that can be used to access the Internet.

[0004] In addition, wireless devices may execute three dimensional (3D) applications. In 3D applications, typically at least two image sensors are used to capture depth information from a scene. Frame data from two image sensors is combined and processed to infer distance information and used to construct a 3D representation. Combining image data from each of the sensors typically involves performing frame synchronization and line synchronization, which may result in synchronization and alignment challenges. In addition, filtering of image data from multiple sensors and interleaving such image data may be further complicated when source sensors provide

data at different frequencies or phases. It would be advantageous to effectively synchronize data from multiple sensors and efficiently process the data to reduce overall image processing system cost and complexity.

Summary

[0005] In multiple camera array applications, image data from each of the multiple sensors is to be synchronized at a line level and processed. An image processing system to combine data from multiple sensors is disclosed where image data from a first image sensor and a second image sensor is synchronized and processed. Synchronized data lines are generated by synchronizing and combining first data from a first data stream generated by the first image sensor with second data from a second data stream generated by the second image sensor. The image signal processor is configured to process the synchronized data lines received from a combiner and to output the processed frame to a display.

[0006] In a particular embodiment, a method is disclosed. The method includes providing a common control signal to multiple image sensors to be synchronized. The method further includes receiving a first data line from a first image sensor of the multiple image sensors, receiving a second data line from a second image sensor of the multiple image sensors, and combining the first data line and the second data line to generate a synchronized data line.

[0007] In another particular embodiment, an apparatus is disclosed. The apparatus includes a first input configured to receive a first data line from a first image sensor of multiple image sensors to be synchronized via a common control signal. The apparatus further includes a second input configured to receive a second data line from a second image sensor of the multiple image sensors, and a combiner coupled to the first input and to the second input, wherein the combiner is configured to combine the first data line and the second data line to generate a synchronized data line.

[0008] In another particular embodiment, a method is disclosed. The method includes providing a common control signal to multiple image sensors. Each of the multiple image sensors is responsive to the common control signal to generate image data. The method further includes receiving synchronized data output from each of the multiple

image sensors, combining the synchronized data output from each of the multiple image sensors to generate a synchronized data line, and providing the synchronized data line to an image processor via a single camera input of the image processor.

[0009] In another particular embodiment, an apparatus is disclosed. The apparatus includes a sensor synchronizer configured to provide a common control signal to multiple image sensors. Each of the multiple image sensors is responsive to the common control signal to generate image data. The apparatus further includes a combiner configured to combine synchronized data output received from each of the multiple image sensors to generate a synchronized data line to be provided to an image processor via a single camera input of the image processor.

[0010] In another particular embodiment, a method is disclosed. The method includes providing a common control signal to multiple image sensors. Each of the multiple image sensors is responsive to the common control signal to generate image data. The method further includes receiving synchronized data output from each of the multiple image sensors.

[0011] In another particular embodiment, a method is disclosed. The method includes receiving a common control signal at multiple image sensors. Each of the multiple image sensors is responsive to the common control signal to generate image data. The method further includes generating synchronized data output from each of the multiple image sensors.

[0012] In another particular embodiment, an apparatus is disclosed. The apparatus includes a sensor synchronizer configured to provide a common control signal to multiple image sensors to cause the multiple image sensors to generate image data. The apparatus further includes a sensor data interface configured to receive synchronized data output from each of the multiple image sensors.

[0013] In another particular embodiment, a method is disclosed. The method includes receiving lines of image data at an image processor having an input for a single camera. Each line of the image data includes first line data from a first image captured by a first camera and second line data from a second image captured by a second camera. The method further includes generating an output frame having a first section corresponding

to line data of the first image and having a second section corresponding to line data of the second image. The first section and the second section are configured to be used to generate a three-dimensional (3D) image format or a 3D video format.

[0014] In another particular embodiment, an apparatus is disclosed. The apparatus includes an image processor having an input for a single camera. The image processor is configured to receive lines of image data via the input. Each line of the image data includes first line data from a first image captured by a first camera and second line data from a second image captured by a second camera. The image processor is configured to generate an output frame having a first section corresponding to line data of the first image and having a second section corresponding to line data of the second image. The first section and the second section are configured to be used to generate a three-dimensional (3D) image format or a 3D video format

[0015] In a particular embodiment, a method of combining data from multiple sensors into a frame is disclosed. The method includes receiving a first data stream from a first image sensor, receiving a second data stream a second image sensor, and combining data from the first data stream and from the second data stream to generate a frame. The method further includes processing the frame at an image signal processor to generate a processed frame and outputting the processed frame for display. Each of the first image sensor and the second image sensor is directly responsive to the image signal processor.

[0016] In another particular embodiment, an apparatus is disclosed. The apparatus includes a first image sensor configured to generate a first data stream, a second image sensor configured to generate a second data stream, and a combiner configured to combine first data from the first data stream and second data from the second data stream to generate a frame. The apparatus further includes an image signal processor configured to process the frame and to output a processed frame to a display. Each of the first image sensor and the second image sensor is directly responsive to the image signal processor.

[0017] In another particular embodiment, a method is disclosed. The method includes receiving first image data of an image from a first image sensor, receiving second image data of an image from a second image sensor, and synchronizing line by line exposure

of the first image sensor and the second image sensor during image data acquisition. The first image sensor and the second image sensor are independent of each other. The synchronizing may be line by line and may be frame by frame.

[0018] In another particular embodiment, an apparatus is disclosed. The apparatus includes a memory buffer. The memory buffer includes a section to align incoming streams in a deterministic order through the streaming of each frame and a programmable gap section between streams.

[0019] In another particular embodiment, a method is disclosed. The method includes receiving rows of image data at an image processor having an input for a single camera. Each row of the image data includes data from a row of a first image captured by a first camera and data from a row of a second image captured by a second camera. The method also includes generating an output having a three dimensional (3D) image format or a 3D video format. The output corresponds to the first image and the second image.

[0020] In another particular embodiment, an apparatus is disclosed. The apparatus includes an image processor having an input for a single camera. The apparatus also includes a combiner configured to send rows of image data to the image processor. Each row of the image data includes first data from a row of a first image captured by a first camera and second data from a row of a second image captured by a second camera. The image processor is configured to generate an output having either a three dimensional (3D) image format or a 3D video format. The output corresponds to the first image and the second image.

[0021] One particular advantage provided by at least one of the disclosed embodiments is that a single image signal processor may be used to synchronize and control image data from multiple image sensors. Another particular advantage is that having gaps between streams offers the flexibility of processing the combined stream in an image signal processor as a single frame, and avoids contamination of streams by subsequent block-based processing (i.e., if the gap is equal with the biggest block-based processing contamination of streams is avoided).

[0022] Other aspects, advantages, and features of the present disclosure will become apparent after review of the entire application, including the following sections: Brief Description of the Drawings, Detailed Description, and the Claims.

Brief Description of the Drawings

[0023] FIG. 1 is a block diagram of a particular illustrative embodiment of an image processing system to combine data from multiple image sensors;

[0024] FIG. 2 is a block diagram of a second illustrative embodiment of an image processing system to combine data from multiple image sensors;

[0025] FIG. 3 is a block diagram of a third illustrative embodiment of an image processing system to combine data from multiple image sensors;

[0026] FIG. 4 is a block diagram of a particular illustrative embodiment of a selected portion of the image processing system of FIG. 2, where a first image sensor and a second image sensor receive common control data;

[0027] FIG. 5 is a block diagram of a fourth illustrative embodiment of an image processing system to combine data from multiple image sensors;

[0028] FIG. 6 is a diagrammatic representation of a first embodiment of a first data stream at an output of a first image sensor and a second data stream at an output of a second image sensor being combined to form a synchronized data line;

[0029] FIG. 7 is a diagrammatic representation of a second embodiment of a first data stream at an output of a first image sensor and a second data stream at an output of a second image sensor being combined to form a synchronized data line;

[0030] FIG. 8 is a diagrammatic representation of a first embodiment of phase diagram illustrating a two line phase difference between a first data stream from a first sensor and a second data stream from a second sensor;

[0031] FIG. 9 is a diagrammatic representation of a second embodiment of phase diagram illustrating a one line phase difference between a first data stream from a first sensor and a second data stream from a second sensor;

[0032] FIG. 10 is a diagrammatic representation illustrating pixel data of each of a plurality of sensors and illustrating synchronized data lines;

[0033] FIG. 11 is a timing diagram illustrating frame valid and line valid signal timing for multiple sensors;

[0034] FIG. 12 is a diagrammatic representation of a third embodiment of phase diagram illustrating a three line phase difference between a first data stream from a first sensor and a second data stream from a second sensor;

[0035] FIG. 13 is a block diagram of a particular illustrative embodiment of an image processing system to combine data from multiple image sensors to produce a three dimensional image format;

[0036] FIG. 14 is a diagrammatic representation illustrating various embodiments of mobile devices having image processing systems to combine data from multiple image sensors;

[0037] FIG. 15 is a diagrammatic representation illustrating an example of images that are captured by an array of cameras including overlap between images;

[0038] FIG. 16 is a diagrammatic representation illustrating an example of images that are captured by an array of cameras including overlap between images where each image may have its own shifting component and rotation component;

[0039] FIG. 17 is a block diagram illustrating a particular embodiment of an array of cameras and electrical connections associated with the array of cameras;

[0040] FIG. 18 is a block diagram of a first particular illustrative embodiment of a camera array processing system;

[0041] FIG. 19 is a block diagram of a first particular illustrative embodiment of a camera array processing system;

[0042] FIG. 20 is a diagrammatic representation illustrating a camera system that includes a main lens and multiple cameras arranged in an array;

[0043] FIG. 21 is a diagrammatic representation illustrating a multiple camera module in an automobile;

[0044] FIG. 22 is a flow diagram of a particular illustrative embodiment of a method of combining data from multiple sensors into a synchronized data line;

[0045] FIG. 23 is a flow diagram of a particular illustrative embodiment of a method of providing a common control signal to multiple image sensors and providing a synchronized data line to an image processor via a single camera input of the image processor;

[0046] FIG. 24 is a flow diagram of a particular illustrative embodiment of a method of providing a common control signal to multiple image sensors and receiving synchronized data output from each of the multiple image sensors;

[0047] FIG. 25 is a flow diagram of a particular illustrative embodiment of a method of receiving a common control signal at multiple image sensors and generating synchronized data output from each of the multiple image sensors;

[0048] FIG. 26 is a flow diagram of a particular illustrative embodiment of a method of combining data from multiple sensors at an image signal processor having an input for a single camera;

[0049] FIG. 27 is a flow diagram of a particular illustrative embodiment of a method of combining data from multiple sensors into a frame;

[0050] FIG. 28 is a flow diagram of a particular illustrative embodiment of a method of synchronizing line by line exposure of a first image sensor and a second image sensor;

[0051] FIG. 29 is a flow diagram of a first illustrative embodiment of a method of combining data from multiple sensors to generate three dimensional image data;

[0052] FIG. 30 is a flow diagram of a second illustrative embodiment of a method of combining data from multiple sensors to generate three dimensional image data;

[0053] FIG. 31 is a flow diagram of a particular illustrative embodiment of a method of synchronizing line by line exposure of a first image sensor and a second image sensor;

[0054] FIG. 32 is a flow diagram of a particular illustrative embodiment of a method of combining data from multiple sensors to generate three dimensional image data from a synchronized data line;

[0055] FIG. 33 is a block diagram of a particular illustrative embodiment of an image processing system to combine data from multiple image sensors;

[0056] FIG. 34 is a block diagram of a first illustrative embodiment of a wireless device including an image processing system to combine data from multiple image sensors; and

[0057] FIG. 35 is a block diagram of a second illustrative embodiment of a wireless device including an image processing system to combine data from multiple image sensors.

I. Detailed Description

[0058] Referring to FIG. 1, a particular illustrative embodiment of an image processing system to combine data from multiple sensors is depicted and generally designated 100. The image processing system 100 includes a multiple camera module 102, a sensor module 104, and a single camera chip module 106. In a particular embodiment, the sensor module 104 may include a plurality of sensors, such as sensors 202 and 204 of FIG. 2 and FIG. 3, where each of the plurality of sensors is configured to generate a data stream that includes data lines of an image. The single camera module 106 may include an image processor having a single camera input, such as image processor 208 of FIG. 2 and FIG. 3. Combining line-by-line image data of the image data streams of multiple sensors into synchronized data lines 108 enables the image processor to perform formatting for multi-camera processing even though the image processor has a single camera input. As a result, the system 100 may be implemented at a reduced cost as compared to a system that uses a separate processor for each camera or that uses a processor having multiple camera inputs.

[0059] Referring to FIG. 2, a particular illustrative embodiment of an image processing system to combine data from multiple sensors is depicted and generally designated 200. The image processing system 200 includes a first sensor 202 and a second sensor 204. The image processing system 200 further includes a combiner 206, an image signal

processor or video front end 208, and a sensor synchronizer 230. The image signal processor 208 may be coupled to a display device (not shown). The combiner 206 includes one or more line buffers 216. The image processing system 200 may be integrated in at least one semiconductor die.

[0060] The first sensor 202 is configured to generate a first data stream, illustrated as a first image data stream 212. The first image data stream 212 includes a first data line 222. The second sensor 204 is configured to generate a second data stream, illustrated as a second image data stream 214. The second image data stream 214 includes a second data line 224. The first and second sensors 202, 204 may be substantially similar image sensors that are independent of each other and that receive a common control signal 234 from the sensor synchronizer 230. The sensor synchronizer 230 is configured to receive a control/data signal 232 and to output the common control signal 234 to the first and second sensors 202, 204, enabling the first and second sensors 202, 204 to generate closely aligned data streams 212, 214. For example, the data streams 212, 214 may have substantially the same timing characteristics, such as frequency and phase. In a particular embodiment, the control/data signal 232 may be received from the image signal processor 208.

[0061] The combiner 206 is responsive to the first image data stream 212 and the second image data stream 214. The combiner 206 is configured to combine data from the first image data stream 212 and data from the second image data stream 214 within the line buffer 216. In a particular embodiment, the line buffer 216 is configured to align first data, such as the first data line 222 from the first sensor 202, and second data, such as the second data line 224 from the second sensor 204. In a particular embodiment, the combiner 206 is responsive to data stored within the line buffer 216 and provides line data 218 to the image signal processor 208. In a particular embodiment, the line data 218 may include a plurality of rows, where each row is a combination of corresponding rows from each sensor 202, 204, such as described with respect to FIG. 6.

[0062] The image signal processor 208 is configured to process the line data 218 and to generate processed line data 240. In a particular embodiment, the processed line data 240 may be provided as processed frame data. While two sensors have been shown, it

should be understood that other embodiments may include more than two sensors. For example, FIG. 3 depicts an embodiment 300 that includes more than two sensors. An Nth sensor 305 is configured to generate an Nth data stream, illustrated as an Nth image data stream 315. The Nth image data stream 315 includes an Nth data line 325. The Nth sensor 305 may be substantially similar to the first and second image sensors 202, 204 and may receive the common control signal 234 from the sensor synchronizer 230, enabling the first, second, and Nth sensors 202, 204, 305 to generate closely aligned data streams 212, 214, 315. For example, the data streams 212, 214, 315 may have substantially the same timing characteristics, such as frequency and phase. The combiner 206 is responsive to the first image data stream 212, the second image data stream 214, and the Nth image data stream 315. The combiner 206 is configured to combine data from the first image data stream 212, the second image data stream 214, and the Nth image data stream 315 within the line buffer 216.

[0063] Because data received from commonly controlled, similar sensors (e.g., 202, 204 of FIG. 2, or 202, 204, 305 of FIG. 3) has substantially the same frequency and phase, synchronization between data streams received at the combiner 206 may occur within a single image line of image data. In a particular embodiment, the line buffer 216 may be dimensioned for a worst case of misalignment (i.e., if the synchronization misalignment is three lines then the line buffer 212 should be sized to buffer at least six lines). As a result, the combined data may be efficiently processed using a single image signal processor. Thus, overall image system cost and complexity may be reduced compared to multiple processor systems (e.g., a processor assigned to each sensor).

[0064] Referring to FIG. 4, a particular illustrative embodiment of a selected portion 400 of the image processing system 200 of FIG. 2 is depicted. The portion 400 of the image processing system includes the first sensor 202, the second sensor 204, and the sensor synchronizer 230. In a particular embodiment, the first sensor 202 and the second sensor 204 are identical sensors or nearly identical sensors that receive the same start-up or reset signals and the same clock input from the sensor synchronizer 230. For example, the first sensor 202 and the second sensor 204 may each receive common control data/signals from the sensor synchronizer 230. In a particular embodiment, the control data/signals may include a control clock signal 404, a control data signal 406, a camera clock signal 408, and a camera reset signal 410. The control data/signals 404-

410 may be formed and transmitted via an interface compliant with a two wire inter-chip communication protocol, such as an Inter-Integrated Circuit (I2C) multi-master serial computer bus. Alternatively, the control data/signals 404-410 may be formed and transmitted according to an interface compliant with a specification of a serial interface between a digital camera module and mobile phone engine, such as a Camera Serial Interface (CSI), an interface between a peripheral device (camera) and a host processor (baseband, application engine) such as a Camera Serial Interface 2 (CSI-2), a parallel interface between a digital camera module and a mobile phone engine such as a Camera Parallel Interface (CPI), or other control interfaces.

[0065] The first sensor 202 may be configured to send first timing data 420 and first sensor image data 422 to the combiner 206 as illustrated in the system of FIG. 2 or FIG. 5. Similarly, the second sensor 204 may be configured to send second timing data 430 and second sensor image data 432 to the combiner 206 of FIG. 2 or FIG 5.

[0066] During operation, the first sensor 202 and the second sensor 204 each operate in identical or nearly identical conditions from a timing standpoint. For example, the first and second sensors 202, 204 each receive the same control clock signal 404, the same control data signal 406, the same camera clock signal 408, and the same camera reset signal 410. Because the first and second sensors 202, 204 are identical or nearly identical, they operate substantially similarly under the same timing conditions. For example, data output from the first sensor 202 has substantially the same frequency and phase as data output from the second sensor 204. To illustrate, a phase difference between data output from the first sensor 202 and the second sensor 204 may be less than a single horizontal line of phase difference, enabling a single image signal processor to be used to synchronize and control image data from the two image sensors 202, 204.

[0067] Referring to FIG. 5, a block diagram of a particular illustrative embodiment of an image processing system to combine data from multiple sensors is depicted and generally designated 500. The system 500 includes the first image sensor 202, the second image sensor 204, the combiner 206, the sensor synchronizer 230, and the image signal processor 208. The system 500 further includes a register interface 510 and a clock management device 512. In a particular embodiment, the register interface 510

may be within the sensor synchronizer 230. Alternatively, the register interface 510 may be a standalone module. In a particular embodiment, the system 500 may further include a thin output formatter 506 (shown in shadow) and a transport packer and formatter 508 (shown in shadow).

[0068] In a particular embodiment, the combiner 206 is configured to receive the first timing data 420 and the first sensor image data 422 from the first sensor 202. The combiner 206 is also configured to receive the second timing data 430 and the second sensor image data 432 from the second sensor 204. The combiner 206 is further configured to receive a clock signal 526 from the clock management device 512. The combiner 206 uses the first timing data 420, the first sensor image data 422, the second timing data 430, and the second sensor image data 432 to generate a synchronized data line which is provided to the image signal processor 208. The image signal processor 208 processes the synchronized data line to create processed data line data. The processed data line data may be provided to another component, such as to a display device. Thus, image data from multiple sensors may be combined, processed and rendered for display at a display device.

[0069] In a particular embodiment, the first timing data 420 may be associated with a first pixel clock, the first sensor image data 422 may be associated with a first pixel size, the second timing data 430 may be associated with a second pixel clock, and the second sensor image data 432 may be associated with a second pixel size. When the combiner 406 combines the first timing data 420, the first sensor image data 422, the second timing data 430, and the second sensor image data 432 to generate the synchronized data line, a first line of the first image data and a corresponding line of the second image data are combined into a single image line. In a particular embodiment, the size of the single image line may be substantially double that of the first line of the first image data or the corresponding line of the second image data (e.g., double that of the first pixel size or the second pixel size), and the rate of pixel clock of the combined single image line may be substantially double the rate of the first pixel clock or the second pixel clock (e.g., may have a clock frequency that is double the first pixel clock frequency or the second pixel clock frequency). The generated synchronized data line is sent to the image signal processor 208 via a combiner timing data signal 528 and a combiner image data signal 530.

[0070] In a particular embodiment, the synchronized data line that is generated by the combiner 206 may be provided to the thin output formatter 506 to create formatted data which is provided to the transport packer and formatter 508 prior to being provided to the image signal processor 208.

[0071] In a particular embodiment, the thin output formatter 506 receives the combiner timing data signal 528 and the combiner image data signal 530 to create formatted data. The formatted data may include output formatter timing data signal 536, output formatter image data signal 538, output formatter stats data signal 540, output formatter start data signal 542, and output formatter valid data signal 544. In a particular embodiment, the transport packer and formatter 508 receives the formatted data 536-544 from the thin output formatter 506 and generates a transport data stream including a transport timing data signal 546 and a transport image data signal 548.

[0072] In a particular embodiment, the register interface 510 may be coupled to the image signal processor 208 and coupled to the clock management device 512. In a particular embodiment, the register interface 510 may receive a clock signal 527 from the clock management device 512 and may be coupled to a register bus 572. The clock management device 512 is configured to receive the second timing data signal 430 and to output the clock signal 526. In a particular embodiment, the clock signal 526 is substantially double the frequency of the second timing data signal 430 to enable the combiner 206 to maintain a frame processing rate while combining concurrent data from multiple sensors.

[0073] Because data output from commonly controlled, similar sensors has substantially the same frequency and phase, synchronization between data streams may occur within a single image line of image data. Thus, the combined data may be efficiently processed using a single image signal processor having access to the single line of image data.

[0074] Referring to FIG. 6, a diagrammatic representation of a particular embodiment of a first data stream at an output of a first image sensor and a second data stream at an output of a second image sensor being combined to form a synchronized data line is depicted and generally designated 600. A first sensor, such as the first sensor 202 of FIG. 2, generates a first data stream 602 that corresponds to first image data of an

image. A second sensor, such as the second sensor 204 of FIG. 2, generates a second data stream 604 that corresponds to second image data of the image. Data from the first data stream 602 and data from the second data stream 604 are combined to form a data out data stream 606.

[0075] In a particular embodiment, the first data stream 602 includes data associated with a first line of the first image data of the image and the second data stream 604 includes data associated with a corresponding line of the second image data of the image. The first data stream 602 includes line data 610 having a first line index value, line data 612 having a second line index value, line data 614 having a third line index value, and line data 616 having a fourth line index value. The second data stream 604 includes corresponding line data to that of the first data stream, including corresponding line data 620 having the first line index value, corresponding line data 622 having the second line index value, corresponding line data 624 having the third line index value, and corresponding line data 626 having the fourth line index value.

[0076] The data out data stream 606 includes a combination of the first line of the first image data of the image and the corresponding line of the second image data of the image. As illustrated, the first data stream 602 and the second data stream 604 are interleaved to form the data out data stream 606. For example, the data out data stream 606 includes combined line data 630 having the first line index value, combined line data 632 having the second line index value, and combined line data 634 having the third line index value. The combined line data 630 includes the line data 610 and the corresponding line data 620. The combined line data 632 includes the line data 612 and the corresponding line data 622. The combined line data 634 includes the line data 614 and the corresponding line data 624. Each combined line 630-634 may be generated by combining corresponding lines within a line buffer, such as the line buffer 216 of FIG. 2.

[0077] In a particular embodiment, the data from the first data stream 602 is combined with the data from the second data stream 604 to generate a plurality of synchronized data lines that form a frame 660. The frame 660 may include a plurality of rows 642, where each row corresponds to a line index value and stores a synchronized data line that includes a line of the first image data having the line index value and a

corresponding line of the second image data having the line index value. For example, a first row of the frame 660 may include the combined line data 630, a second row of the frame 660 may include the combined line data 632, a third row of the frame 660 may include the combined line data 634, etc. Each synchronized image data line forms part of the frame 660 such that the data in the frame 660 is aligned.

[0078] The frame 660 is depicted with an order of the rows 642 matching a read order of the image data from the image sensors (i.e. combined data from the top line of the image sensors (line index 1) is in a top line of the frame 660 and combined data from a next line of the image sensors (line index 2) is in a next line of the frame 660. Alternatively, in other embodiments the rows of the frame 660 may not match a read order of the image data and may instead correspond to any other order of the image data. For example, a top row of the frame 660 may to line index 2 while a next row of the frame 660 may correspond to line index 1. The frame 660 may be programmable such that each of the rows 642 can be programmed to correspond to any of the line index values of the image data.

[0079] In a particular embodiment, the first line 610 of the first image data is associated with a first pixel size (e.g., a number of pixels per line) and a first pixel clock, and the corresponding line 620 of the second image data is associated with a second pixel size and a second pixel clock. The first sensor and the second sensor generating the data streams 602, 604 are configured to receive a common clock signal and a common reset signal. When the first line 610 of the first image data and the corresponding line 620 of the second image data are combined into a single image line, the size of the single image line is substantially double that of the first line 610 of the first image data or the corresponding line 620 of the second image data, and the pixel clock signal of the combined single image line (e.g., a third pixel clock signal) has a clock rate that is substantially double that of the first pixel clock signal or the second pixel clock signal. For example, the combined line data 630 may have an image size that is substantially double that of the line data 610 or double that of the corresponding line data 620. Similarly, the pixel clock frequency of the combined line data 630 may have a frequency that is substantially double that of the first pixel clock signal associated with the line data 610 or double that of the second pixel clock signal associated with the corresponding line data 620, such that the pixel clock frequency of the combined line

data 630 may be associated with the third pixel clock signal having substantially double the frequency of that of the first pixel clock or the second pixel clock.

[0080] Alternatively, in an implementation where line data three image sensors having equal line sizes are combined, a synchronized line size may be substantially three times the sensor line size and a pixel clock rate may be substantially three times a pixel clock rate of the individual sensors. In a general case of an arbitrary number of sensors that may have unequal sizes, a synchronized line size can be set as greater than or equal to a sum of the line sizes that are combined, and a pixel clock rate can be set so that the output line bandwidth is equal to or greater than the sum of the input bandwidth.

[0081] The frame 660 may be processed at an image signal processor, such as the image signal processor 208 of FIG. 2, to generate a processed frame 650. The processed frame 650 includes a first section 652 including first image data from a first image sensor, such as the sensor 202 of FIG. 2, a second section 654 including second image data from a second image sensor, such as the sensor 204 of FIG. 2, and a gap section 656. The gap section 656 may include non-image data disposed between the first section 652 and the second section 654.

[0082] In a particular embodiment, the first section 652 includes a line of the first image data and the second section 654 includes a corresponding line of the second image data. In a particular embodiment, the gap section 656 may be used for edge filtering and may include a black gap that is approximately five pixels in width. As a further example, the gap section 656 may be added between lines and have a size equal to the size of an interpolation kernel or a size of a largest two-dimensional filter applied to the frame 650 by the image signal processor.

[0083] In a particular illustrative embodiment, statistics for automatic exposure, automatic focus, and automatic white balance may be collected from either the first section 652 or the second section 654, either of which may be a full image from one of the respective sensors. Therefore, the statistics for automatic exposure, automatic focus, and automatic white balance may be collected from half of the final image (e.g., the first section 652) and may be applied to both sensors since both sensors are receiving substantially identical timing information. As such, data output from multiple sensors

has substantially the same frequency and phase such that synchronization may occur within one image line of image data of the image.

[0084] The frame 650 may be stored in a memory that is integrated in at least one semiconductor die. The frame 650 may be stored in memory that is incorporated into a consumer electronic device, such as a set top box, a music player, a video player, an entertainment unit, a navigation device, a communications device, a personal digital assistant (PDA), a fixed location data unit, and a computer. The electronic devices may utilize image processing methods, including 3D applications that process image data from multiple sensors.

[0085] Referring to FIG. 7, a diagrammatic representation of a second embodiment of a first data stream at an output of a first image sensor and a second data stream at an output of a second image sensor being combined to form a synchronized data line is depicted and generally designated as 700. A first sensor, such as the first image sensor 202 of FIG. 2, generates a first data stream 702 that corresponds to first image data of an image. A second sensor, such as the second image sensor 204 of FIG. 2, generates a second data stream 704 that corresponds to second image data of the image. Data from the first data stream 702 and data from the second data stream 704 are combined to form a data out data stream 706.

[0086] In a particular embodiment, the first data stream 702 includes data associated with a first line of the first image data of the image and the second data stream 704 includes data associated with a corresponding line of the second image data of the image. The first data stream 702 includes line data 710 having a first line index value, line data 712 having a second line index value, line data 714 having a third line index value, and line data 716 having a fourth line index value. The second data stream 704 includes corresponding line data to that of the first data stream, including corresponding line data 720 having the first line index value, corresponding line data 722 having the second line index value, corresponding line data 724 having the third line index value, and corresponding line data 726 having the fourth line index value.

[0087] The data out data stream 706 includes a combination of the first line of the first image data of the image and the corresponding line of the second image data of the image. As illustrated, the first data stream 702 and the second data stream 704 are

interleaved with a gap section 708 to form the data out data stream 706. For example, the illustrated portion of the data out data stream 706 includes combined line data 730 having the first line index value, combined line data 732 having the second line index value, and combined line data 734 having the third line index value. The combined line data 730 includes the line data 710 separated from the corresponding line data 720 by the gap section 708. The combined line data 732 includes the line data 712 separated from the corresponding line data 722 by the gap section 708. The combined line data 734 includes the line data 714 separated from the corresponding line data 724 by the gap section 708. Each combined line 730-734 may be generated by combining corresponding lines with the gap section 708 between the corresponding lines within a line buffer, such as the line buffer 216 of FIG. 2.

[0088] In a particular embodiment, the data from the first data stream 702 is combined with the data from the second data stream 704 to generate a plurality of synchronized data lines that form a frame 740. The frame 740 may include a plurality of rows 742, where each row corresponds to a line index value and stores a line of the first image data having the line index value and stores a corresponding line of the second image data having the line index value. For example, a first row of the frame 740 may include the combined line data 730, a second row of the frame 740 may include the combined line data 732, a third row of the frame 740 may include the combined line data 734, etc. such that the data in the frame 740 is aligned.

[0089] In a particular embodiment, the first line 710 of the first image data is associated with a first pixel size (e.g., a number of pixels per line) and a first pixel clock, and the corresponding line 720 of the second image data is associated with a second pixel size and a second pixel clock. The first sensor and the second sensor generating the data streams 702, 704 are configured to receive a common clock signal and a common reset signal. When the first line 710 of the first image data and the corresponding line 720 of the second image data are combined into a single image line, the size of the single image line is approximately double that of the first line 710 of the first image data or the corresponding line 720 of the second image data. Further, the pixel clock signal of the combined single image line (e.g., a third pixel clock signal) has a clock rate that is approximately double that of the first pixel clock signal or the second pixel clock signal. For example, the combined line data 730 may have an image size that is approximately

double that of the line data 710 or double that of the corresponding line data 720. Similarly, the pixel clock frequency of the combined line data 730 may have a frequency that is approximately double that of the first pixel clock signal associated with the line data 710 or double that of the second pixel clock signal associated with the corresponding line data 720, such that the pixel clock frequency of the combined line data 730 may be associated with the third pixel clock signal having approximately double the frequency of that of the first pixel clock or the second pixel clock.

[0090] Each gap section 708 may include non-image data. In a particular embodiment, the non-image data area in the frame 740 formed by the gap sections 708 may be used for edge filtering. The gap section 708 may include a black gap that is approximately five pixels in width. In other embodiments, each gap section 708 has a size equal to the size of an interpolation kernel or a size of a largest two-dimensional filter applied to the frame 740 by an image processor, such as the image processor 208 of FIG. 2. The frame 740 may be processed by the image processor to generate a 3D image.

[0091] Referring to FIG. 8, a diagrammatic representation of a first embodiment of a phase diagram illustrating a two line phase difference between a first data stream from a first sensor and a second data stream from a second sensor is depicted and generally designated 800. A first sensor, such as the first sensor 202 of FIG. 2, generates a first data stream that includes first sensor first line data 802, first sensor second line data 804, and first sensor third line data 806. A second sensor, such as the second sensor 204 of FIG. 2, generates a second data stream that includes second sensor first line data 812, second sensor second line data 814, and second sensor third line data 816. Data from the first data stream and data from the second data stream are combined to form a combined line 820. In the particular embodiment illustrated in FIG. 8, first, second and third line data is illustrated. Alternatively, any number of line data may be generated (e.g., 720 lines as illustrated in FIGs. 6 and 7).

[0092] In the particular embodiment of FIG. 8, there is a two line phase difference between data of the first data stream and data of the second data stream. For example, the first sensor first line data 802 may be received by a combiner such as combiner 216 of FIG. 2 during a first line phase, the first sensor second line data 804 may be received during a second line phase, and the first sensor third line data 806 and the second sensor

first line data 812 may be received during a third line phase. As such, there is a two line phase difference between the first sensor first line data 802 and the second sensor first line data 812.

[0093] The combined line 820 includes a combination of the first line of the first image data of the image and the corresponding line of the second image data of the image. As illustrated, the first data stream and the second data stream are interleaved to form the combined line 820. For example, the combined line 820 includes combined line data 822 having the first sensor first line data 802 and the second sensor first line data 812, combined line data 824 having the first sensor second line data 804 and the second sensor second line data 814, and combined line data 826 having the first sensor third line data 806 and the second sensor third line data 816. Each combined line 822-826 may be generated by combining corresponding lines within a line buffer, such as the line buffer 216 of FIG. 2. The line buffer may be configured to buffer at least a portion of a next data line (e.g. the first sensor second line data 804) that is received from the first image sensor before a synchronized data line (e.g. the combined line data 822) is generated. As such, data output from multiple sensors having a two line phase difference may be combined such that synchronization may occur within one image line of image data of the image.

[0094] Referring to FIG. 9, a diagrammatic representation of a first embodiment of a phase diagram illustrating a one line phase difference between a first data stream from a first sensor and a second data stream from a second sensor is depicted and generally designated 900. A first sensor, such as the first sensor 202 of FIG. 2, generates a first data stream that includes first sensor first line data 902, first sensor second line data 904, first sensor third line data 906, and first sensor fourth line data 908. A second sensor, such as the second sensor 204 of FIG. 2, generates a second data stream that includes second sensor first line data 912, second sensor second line data 914, second sensor third line data 916, and second sensor fourth line data 918. Data from the first data stream and data from the second data stream are combined to form a combined line 920. In the particular embodiment illustrated in FIG. 9, first, second, third, and fourth line data is illustrated. Alternatively, any number of line data may be generated (e.g., 720 lines as illustrated in FIGs. 6 and 7).

[0095] In the particular embodiment of FIG. 9, there is a one line phase difference between data of the first data stream and data of the second data stream. For example, the first sensor first line data 902 may be received by a combiner such as combiner 216 of FIG. 2 during a first line phase, and the first sensor second line data 904 and the second sensor first line data 912 may be received during a second line phase. As such, there is a one line phase difference between the first sensor first line data 902 and the second sensor first line data 912.

[0096] The combined line 920 includes a combination of the first line of the first image data of the image and the corresponding line of the second image data of the image. As illustrated, the first data stream and the second data stream are interleaved to form the combined line 920. For example, the combined line 920 includes combined line data 922 having the first sensor first line data 902 and the second sensor first line data 912, combined line data 924 having the first sensor second line data 904 and the second sensor second line data 914, combined line data 926 having the first sensor third line data 906 and the second sensor third line data 916, and combined line data 928 having the first sensor fourth line data 908 and the second sensor fourth line data 918. Each combined line 922-926 may be generated by combining corresponding lines within a line buffer, such as the line buffer 216 of FIG. 2. As such, data output from multiple sensors having a one line phase difference may be combined such that synchronization may occur within one image line of image data of the image.

[0097] Referring to FIG. 10, a diagrammatic representation illustrating red-green-blue (RGB) data for each of a plurality of sensors and illustrating synchronized data lines is depicted and generally designated 1000. In the embodiment illustrated in FIG. 10, a first sensor, such as the first sensor 202 of FIG. 3, generates a first data stream that includes first sensor first line data 1002, first sensor second line data 1004, and first sensor third line data 1006. A second sensor, such as the second sensor 204 of FIG. 3, generates a second data stream that includes second sensor first line data 1012, second sensor second line data 1014, and second sensor third line data 1016. A third sensor, such as the Nth sensor 305 of FIG. 3, generates a third data stream that includes third sensor first line data 1022, third sensor second line data 1024, and third sensor third line data 1026. Data from the first data stream, data from the second data stream, and data from the third data stream are combined to form a combined line 1020.

[0098] As an illustrative example, each of the first line data 1002, 1012, 1022 includes alternating red and green pixel values, each of the second line data 1004, 1014, 1024 includes alternating green and blue pixel values, and each of the third line data 1006, 1016, 1026 includes alternating red and green pixel values according to a Bayer filter pattern.

[0099] As illustrated, the first data stream, the second data stream, and the third data stream are interleaved to form a combined line data stream 1020. For example, the combined line data stream 1020 includes combined line data 1040 having the first sensor first line data 1002, the second sensor first line data 1012, and the third sensor first line data 1002, combined line data 1050 having the first sensor second line data 1004, the second sensor second line data 1014, and the third sensor second line data 1024, and combined line data 1060 having the first sensor third line data 1006, the second sensor third line data 1016, and the third sensor third line data 1026. Each combined line 1040-1060 may be generated by combining corresponding lines within a line buffer, such as the line buffer 216 of FIG. 3. Each combined line 1040-1060 may include raw pixel (e.g., R, G, and B) values read from its respective sensor line data to be demosaiced at an image signal processor, such as the image signal processor 208 of FIG. 3. As such, data output from multiple sensors may be combined such that synchronization may occur within one image line of image data of the image.

[00100] Although FIG. 10 illustrates raw pixel values as including RGB data according to a Bayer filter pattern, in other embodiments the line data from the sensors may not include Bayer RGB pixel values. For example, the sensors may instead provide: luma, blue-difference chroma, red-difference chroma (YCbCr) values; cyan, yellow, green, and magenta (CYGM) values; red, green, blue, and emerald (RGBE) values; red, green, blue, and white (RGBW) values; or any other type of values, as illustrative, non-limiting examples. Alternatively, or in addition, one or more of the sensors may implement panchromatic cells, microlenses over groups of photoreceptors, vertical color filters, or any other sensor technology capable of line-by-line readout of raw image data.

[00101] Referring to FIG. 11, a particular embodiment of a timing diagram illustrating signal timing associated with an apparatus having multiple sensors is

depicted and generally designated 1100. The signals include a frame valid (FV) signal 1102 and a line valid (LV) signal 1104 of a first sensor, an FV 1106 and an LV 1108 of a second sensor, and an FV 1110 and an LV 1112 of a third sensor. In a particular embodiment, the first sensor, the second sensor, and a third sensor may be the first, second, and third sensors 202, 204, 305 of FIG. 3. A combined frame valid signal 1114 is also illustrated in conjunction with a combined line valid/data signal 1116 and a line load (LL) signal 1118.

[00102] In a particular embodiment, the signals 1114-1118 correspond to signaling related to one or more synchronized data lines of a frame, such as the frame 660 of FIG. 6 generated by a combiner, and the signals 1102-1112 correspond to signaling received at the combiner. As illustrated, a first line data 1120, a second line data 1122, and a third line data 1124 are received from the first sensor, a first line data 1130, a second line data 1132, and a third line data 1134 are received from the second sensor, and a first line data 1140, a second line data 1142, and a third line data 1144 are received from the third sensor.

[00103] The first line data 1130 is received from the second sensor prior to the first line data 1120 and the first line data 1140. A phase difference between receipt of the first line data 1130 and the second line data 1120 is illustrated as a first phase difference 1180. The first line data 1120 of the first sensor is received prior to the first line data 1140 of the third sensor, illustrated as a second phase difference 1182. The line data from each of the sensors may follow a rising edge of a corresponding frame valid signal, indicating that data received via an image data line is valid line data from each particular sensor. As illustrated, the combined frame valid line 1114 remains low, indicating non-valid data, until after each of the first line data 1120, 1130, and 1140 have been received, such as at the combiner 206 of FIG. 2. After each of the first lines 1120, 1130, and 1140 has been received, the combined frame valid signal 1114 rises to indicate valid data on the line valid signal 1116. A first synchronized data line 1150 is generated in conjunction with a valid signal being asserted on the LL line 1118. After generation of the first synchronized line data 1150, the combined frame valid signal 1114 remains in a valid state while the LL signal 1118 returns to a non-valid state, after which the LL signal 1118 returns to a valid state upon generation of a second

synchronized data line 1160, which is followed by generation of a third synchronized data line 1170.

[00104] Referring to FIG. 12, a diagrammatic representation of a first embodiment of a phase diagram illustrating a three line phase difference between a first data stream from a first sensor, a second data stream from a second sensor, and a third data stream from a third sensor is depicted and generally designated 1200. A first sensor, such as the first sensor 202 of FIG. 3, generates a first data stream that includes first sensor first line data 1202, first sensor second line data 1204, first sensor third line data 1206, and first sensor fourth line data 1208. A second sensor, such as the second sensor 204 of FIG. 3, generates a second data stream that includes second sensor first line data 1212, second sensor second line data 1214, second sensor third line data 1216, and second sensor fourth line data 1218. A third sensor, such as the Nth sensor 305 of FIG. 3, generates a third data stream that includes third sensor first line data 1222, third sensor second line data 1224, third sensor third line data 1226, and third sensor fourth line data 1228. Data from the first data stream, data from the second data stream, and data from the third data stream are combined to form a combined line 1220. In the particular embodiment illustrated in FIG. 12, first, second, third, and fourth line data is illustrated. Alternatively, any number of line data may be generated (e.g., 720 lines as illustrated in FIGs. 6 and 7).

[00105] In a particular embodiment, there is a three line phase difference between data of the first data stream, data of the second data stream, and data from the third data stream. For example, the third sensor first line data 1222 may be received by a combiner such as combiner 216 of FIG. 2 during a first line phase, the first sensor first line data 1202 and the third sensor second line data 1224 may be received during a second line phase, the first sensor second line data 1204 and the third sensor third line data 1226 may be received during a third line phase, and the first sensor third line data 1206, the second sensor first line data 1212, and the third sensor fourth line data 1228 may be received during a fourth line phase. As such, there is a three line phase difference between the first sensor first line data 1202, the second sensor first line data 1212, and the third sensor first line data 1222.

[00106] The combined line 1220 includes a combination of the first line of the first image data of the image and the corresponding line of the second image data and the third image data of the image. As illustrated, the first data stream, the second data stream, and the third data stream are interleaved to form the combined line 1220. For example, the combined line 1220 includes combined line data 1232 having the first sensor first line data 1202, the second sensor first line data 1212, and the third sensor first line data 1222, combined line data 1234 having the first sensor second line data 1204, the second sensor second line data 1214, and the third sensor second line data 1224, and combined line data 1236 having the first sensor third line data 1206, the second sensor third line data 1216, and the third sensor third line data 1226. Each combined line 1232-1236 may be generated by combining corresponding lines within a line buffer, such as the line buffer 216 of FIG. 3. As such, data output from multiple sensors having a three line phase difference may be combined such that synchronization may occur within one image line of image data of the image.

[00107] Referring to FIG. 13, a particular illustrative embodiment of an image processing system to combine data from multiple sensors to generate 3D data is depicted and generally designated 1300. The image processing system 1300 includes a first image sensor 1302 and a second image sensor 1304. The image processing system 1300 further includes a combiner 1306 and an image processor 1308. The image processor 1308 is coupled to a display device 1310. The combiner 1306 includes at least one line buffer 1312. The image processing system 1300 may be integrated in at least one semiconductor die.

[00108] The first image sensor 1302 is configured to generate a first data stream, illustrated as a first image data stream 1314, and the second image sensor 1304 is configured to generate a second data stream, illustrated as a second image data stream 1316. In a particular embodiment, the first image data stream 1314 may be asynchronous to the second image data stream 1316. The first and second image sensors 1302, 1304 may be substantially similar image sensors that are independent of each other and that may receive a common control signal from a processor (e.g., the combiner 1306 or the image processor 1308) to generate closely aligned image data streams 1314, 1316. For example, the image data streams 1314, 1316 may have substantially the same timing characteristics, such as frequency and phase. Because the

common control signal may be generated by the processor, such as via the signal synchronizer 230 of FIG. 2, each of the image sensors 1302, 1304 may be directly responsive to, and controlled by, the single processor. While two image sensors 1302, 1304 have been shown, it should be understood that more than two image sensors may be used with the image processing system 1300.

[00109] The combiner 1306 is responsive to the first image data stream 1314 and the second image data stream 1316. The combiner 1306 is configured to combine data from the first image data stream 1314 and data from the second image data stream 1316 within the line buffer 1312. In a particular embodiment, the line buffer 1312 is configured to align first data from the first image sensor 1302 and second data from the second image sensor 1304. In a particular embodiment, the combiner 1306 is responsive to data stored within the line buffer 1312 and provides frame data 1318 to the image processor 1308. In a particular embodiment, the frame data 1318 may include a plurality of rows of image data, where each row is a combination of corresponding rows from each sensor 1302, 1304, such as described with respect to FIG. 3.

[00110] The image processor 1308 is configured to process the frame data 1318 and to output processed frame data 1320 to the display device 1310. The processed frame data 1320 may have a 3D image format or a 3D video format.

[00111] The display device 1310 renders and displays image data in response to receiving the processed frame data 1320. Thus, image data from multiple image sensors may be combined, processed and then rendered for display at the display device 1310. In a particular embodiment, the display device 1310 may be decoupled from the image processor 1308 to not be directly responsive to the image processor 1308. For example, the display device 1310 may be a separate device from the image processor 1308.

[00112] Because data received from the commonly controlled, similar image sensors 1302, 1304 may have substantially the same frequency and phase, synchronization between the data streams 1314, 1316 may occur within a single image line of image data. In a particular embodiment, the line buffer 1312 may be dimensioned for a worst case of misalignment (e.g., if the synchronization misalignment is three lines, then the line buffer 1312 should be sized to store at least six lines). As a result, the combined

data may be efficiently processed using a single image processor 1308. Thus, overall image system cost and complexity may be reduced compared to multiple processor systems (e.g., a processor assigned to each sensor).

[00113] Embodiments may be configured to provide 3D/stereoscopic images and/or video data. For example, in one such embodiment, the first image sensor 1302 and the second image sensor 1304 may be positioned side by side so as to provide left/right (stereoscopic) images. The signal provided by the combiner 1306 is received and may be processed by the image processor 1308 to produce 3D images. A user command may allow the image processor 1308 to receive and process data from only a single sensor (i.e., the first image sensor 1302 or the second image sensor 1304) to produce two dimensional (2D) images in lieu of producing 3D images.

[00114] An image processor having an input for a single camera, such as image processor 1308, is able to process data that can be used for 3D processing by using combined data from two cameras provided by the combiner 1306. The image processor 1308 may receive image data from the combiner 1306 or from a memory that stores image data from the combiner 1306. In one such embodiment, the image processor 1308 processes received image data as 2D image/video data so that subsequent processing by the image processor 1308 provides a 3D stereoscopic image/video stream based on the processed data from the image processor 1308. Alternatively, the image processor 1308 may be configured to directly provide a 3D stereoscopic image/video stream based on received image data. In one embodiment, a 3D capture system comprises the combiner 1306 implemented as a first integrated circuit and the image processor 1308 implemented as a second integrated circuit. The first and second integrated circuits may be connected, for example, by one or more of a serial, parallel, or I2C bus.

[00115] Combining the image data stream 1314, 1316 to generate the frame data 1318 enables the image processor 1308 to perform formatting for multi-camera 3D processing even though the image processor 1308 has a single camera input. As a result, the system 1300 may be implemented at a reduced cost as compared to a system that use a separate processor for each camera or that uses a processor having multiple camera inputs.

[00116] Referring to FIG. 14, a diagrammatic representation illustrating various embodiments of mobile devices having image processing systems to combine data from multiple image sensors is depicted and generally designated 1400. In the particular embodiment illustrated at 1402, the mobile device includes an image processing system having an array of two adjacent cameras. In the particular embodiment illustrated at 1404, the mobile device includes an image processing system having an array of three cameras arranged in an in-line configuration. Alternatively, any number of cameras may be arranged in an in-line configuration. In the particular embodiment illustrated at 1406, the mobile device includes an image processing system having a three-by-three array of cameras. In the particular embodiment illustrated at 1408, the mobile device includes an image processing system having a five-by-five array of cameras. Alternatively, any number of cameras may be arranged in a two-dimensional array.

[00117] Referring to FIG. 15, an example of an array of images that are captured by multiple cameras or image sensors is illustrated and generally designated 1500. As illustrated in FIG. 15, an image captured by one camera may overlap with images captured by other neighboring cameras. Image overlap may be useful in combining the images captured by each of the cameras into a single image. In the particular embodiment illustrated in FIG. 15, the array 1500 corresponds to a four-by-four array of cameras or image sensors. Alternatively, any number of cameras may be arranged in a two-dimensional array (e.g., a five-by-five array as illustrated in FIGs. 18 and 19).

[00118] Each camera captures a single camera image of the array 1500. In the embodiment illustrated in FIG. 15, the array 1500 is a four-by-four array. As such, the array 1500 includes a first row 1502, a second row 1504, a third row 1506, and a fourth row 1508. Further, the array 1500 includes a first column 1510, a second column 1512, a third column 1514, and a fourth column 1516. As an illustrative example, a single camera image 1518 may be captured by a camera corresponding to the first row 1502 and the fourth column 1516. The single camera image 1518 may overlap with camera images captured by other cameras of neighboring cells. In the case of the camera corresponding to the first row 1502 and the fourth column 1516, a camera of a neighboring cell may include a camera corresponding to the first row 1502 and the third column 1514, a camera corresponding to the second row 1504 and the third column 1514, or a camera corresponding to the second row 1504 and the fourth column 1516.

For example, a single camera image overlap 1520 may be associated with the single camera image 1508 captured by a camera corresponding to the first row 1502 and the fourth column 1516. FIG. 15 illustrates a theoretical case of absolute alignment of each camera of each of the rows 1502-1508 and each camera of each of the columns 1510-1516. As such, the image overlap with an image captured by a camera corresponding to a neighboring row (e.g., the second row 1504) may be the same as the image overlap with an image captured by a camera corresponding to a neighboring column (e.g., the third column 1514).

[00119] An individual image may be captured with a particular horizontal resolution ("H-res"). To illustrate, a horizontal resolution 1522 may be associated with the single camera image 1518 captured by the camera corresponding to the first row 1502 and the fourth column 1516. FIG. 15 illustrates a theoretical case of image overlap where each camera has the same horizontal resolution 1522. As such, an overall horizontal resolution 1524 (i.e., a number of pixels in each of the rows 1502-1508) may be calculated based on a combination of the horizontal resolution 1522 of an individual camera and a number of cells in a row ("n"). In the case of the four-by-four array 1500 of FIG. 15, there are four cells in each row (i.e., a cell associated with each of the columns 1510-1516). The overall horizontal resolution 1524 may account for image overlap. For example, the overall horizontal resolution 1524 may be calculated as H_res*n – overlap*(n-2), where overlap indicates a number of overlapping pixels of adjacent images. A similar calculation may be performed to determine an overall vertical resolution.

[00120] FIG. 15 illustrates a theoretical case of absolute alignment of each camera with the same image overlap. The image overlap between images captured by the individual cameras may allow each of the individual images to be "stitched together" into a single image.

[00121] Referring to FIG. 16, an example of an array of images that are captured by multiple cameras or image sensors is illustrated and generally designated 1600. As illustrated in FIG. 16, an image captured by one camera may overlap with images captured by other neighboring cameras. Image overlap may be useful in combining the images captured by each of the cameras into a single image. In the particular

embodiment illustrated in FIG. 16, the array 1600 corresponds to a four-by-four array of cameras or image sensors. Alternatively, any number of cameras may be arranged in a two-dimensional array. FIG. 16 illustrates that, due to mechanical constraints, it may not be feasible to achieve absolute alignment of cameras in a row or column (as illustrated in FIG. 15).

[00122] Each image of the array 1600 may have its own rotation 1602, shift 1604, and tilt (not shown). One or more positioning tolerances 1606 may be associated with each image. The positioning tolerances 1606 may include a rotation tolerance, a shift tolerance, a tilt tolerance, or a combination thereof. Image overlap may be useful in combining the images captured by each of the cameras into a single image. FIG. 16 illustrates that the image overlap that is used in combining the images may account for the rotation 1602, shift 1604, and tilt of each image that results from mechanical constraints associating with building a device. Once the device is built, the image overlap may be known and stable. As such, the image overlap may be quantified and may be corrected in a later stage.

[00123] Referring to FIG. 17, a particular embodiment of an array of cameras and electrical connections associated with the array is illustrated and generally designated 1700. FIG. 17 illustrates that each camera of the array 1700 has a first type of interface (i.e., a data interface 1702) and a second type of interface (i.e., a control interface 1704). In the embodiment illustrated in FIG. 17, the array 1700 includes a three-by-three array of cameras. Alternatively, the array 1700 may include cameras arranged in a four-by-four array (e.g., the arrays 1500, 1600 of FIGs. 15 and 16) or any other number of cameras arranged in a two-dimensional array.

[00124] The data interface 1702 may include a serial data bus (e.g., a Mobile Industry Processor Interface or a Standard Mobile Imaging Architecture interface). The data interface 1702 in FIG. 17 is associated with a first row 1706 of the array 1700, a second row 1708 of the array 1700, and a third row 1710 of the array 1700. Lines associated with the data interface 1702 may be used to collect data from cameras in each of the rows 1706-1710 to be processed in parallel. As an illustrative example, for a resolution up to five megapixels (mpix) and ten frames per second, four wires may be needed (e.g., differential data and clock).

[00125] In the illustrative three-by-three array 1700 of FIG. 17, each of the rows 1706-1710 includes a camera in a first column 1712 of the array 1700, a camera in a second column 1714 of the array 1700, and a camera in a third column 1716 of the array 1700. Thus, the data interface 1702 may be used to collect data from nine cameras to be processed in parallel.

[00126] The control interface 1704 may include lines that are used to synchronize all cameras in the array 1700. For example, control interface lines may be associated with clock, reset, and I2C communication. In the illustrative three-by-three array 1700 of FIG. 17, the control interface 1704 may be used to synchronize the nine cameras of the array 1700.

[00127] Referring to FIG. 18, a particular embodiment of a camera array processing system is illustrated and generally designated 1800. All cameras in an array 1802 may be responsive to common control signals, aligned, and processed prior to the resulting image data being combined into a final image. In the embodiment illustrated in FIG. 18, the array 1802 includes a five-by-five array of cameras. Alternatively, the array 1802 may include any other number of cameras arranged in a two-dimensional array (e.g., the three-by-three array 1700 of FIG. 17).

[00128] All cameras in the array 1802 may be synchronized using a method of concurrent image sensor support using a single ISP pipeline. Further, each row of cameras may be aligned using an alignment method. That is, one row of images may be collected, aligned in the same order and sent for processing as a single line with a size n*line, where n is the number of cameras in a row and line is the horizontal size (i.e., "H_res" as described in FIG. 15) of one camera. The five-by-five array 1802 illustrated in FIG. 18 includes a first row 1804, a second row 1806, a third row 1808, a fourth row 1810, and a fifth row 1812. Further, the five-by-five array 1802 includes a first column 1814, a second column 1816, a third column 1818, a fourth column 1820, and a fifth column 1822. Each of the rows 1804-1812 may be processed in parallel for color at a VFE component, and each of the rows 1804-1812 may be processed at a graphics processor or graphics processing unit (GPU) component to align and rectify each individual image in a row. After rectification and alignment, GPU processing may be performed to combine all of the rows 1804-1812 together, resulting in a final image.

[00129] The first row 1804 may be associated with a first alignment block 1824, the second row 1806 may be associated with a second alignment block 1826, the third row 1808 may be associated with a third alignment block 1828, the fourth row 1810 may be associated with a fourth alignment block 1830, and the fifth row 1812 may be associated with a fifth alignment block 1832. To illustrate, the first alignment block 1824 may be adapted to collect image data lines from each camera in the first row 1804 (i.e., five cameras in the five columns 1814-1822 of the array 1802). The first alignment block 1824 may be adapted to align the image data lines in the same order and send the image data lines for processing as a single line. The first alignment block 1824 may be adapted to send the image data lines for processing as a single line to a first VFE component 1834 to be processed for color such as described with respect to the combiner of 206 of FIGs. 2, 3, and 5. A size of the single line may be determined based on the number of cameras (i.e., five cameras) and the horizontal size (i.e., "H_res" as described in FIG. 15) of each camera in the first row 1804.

[00130] The second alignment block 1826 may be adapted to collect images from each camera in the second row 1806, to align the images in a same order, and to send the images for processing as a single line to a second VFE component 1836. The third alignment block 1828 may be adapted to collect an image data line from each camera in the third row 1808, to align the image data lines in a same order, and to send the image data lines for processing as a single line to a third VFE component 1838. The fourth alignment block 1830 may be adapted to collect image data lines from each camera in the fourth row 1810, to align the image data lines in a same order, and to send the image data lines for processing as a single line to a fourth VFE component 1840. The fifth alignment block 1832 may be adapted to collect image data lines from each camera in the fifth row 1812, to align the image data lines in a same order, and to send the image data lines for processing as a single line to a fifth VFE component 1842.

[00131] A control synchronization block 1844 may be used to synchronize each of the cameras of the array 1802 (i.e., twenty five cameras in the case of the illustrative five-by-five array 1802 of FIG. 18) in a manner similar to the sensor synchronizer 230. In a particular embodiment, the control synchronization block 1834 may implement the control interface 1704 of FIG. 17. The control synchronization block 1844 may be communicatively coupled to each of the cameras of the array 1802 and to each of the

VFE components 1834-1842. Synchronization of all cameras in the array 1802 may allow for usage of a rolling shutter on a high resolution. As all cameras may be read out at the same time, the rolling shutter effect may be diminished (with the size of the array). For example, in the five-by-five array 1802 of FIG. 18, synchronization of the twenty five cameras may diminish the rolling shutter effect associated with a Complementary Metal Oxide Semiconductor (CMOS) camera.

[00132] The first VFE component 1834 may be communicatively coupled to a first GPU component 1846 to align and rectify each individual image in the first row 1804 (i.e., five images captured by the cameras in the five columns 1814-1822). The second VFE component 1836 may be communicatively coupled to a second GPU component 1848 to align and rectify each individual image in the second row 1806. The third VFE component 1838 may be communicatively coupled to a third GPU component 1850 to align and rectify each individual image in the third row 1808. The fourth VFE component 1840 may be communicatively coupled to a fourth GPU component 1852 to align and rectify each individual image in the fourth row 1810. The fifth VFE component 1842 may be communicatively coupled to a fifth GPU component 1854 to align and rectify each individual image in the fifth row 1812. Each of the GPU components 1846-1854 may be communicatively coupled to a GPU processing component 1856 that is adapted to combine all of the rows 1804-1812 together, resulting in a final image.

[00133] In the embodiment illustrated in FIG. 18, each of the alignment blocks 1824-1832 is associated with its own VFE component and its own GPU rectification and alignment component. Thus, FIG. 18 illustrates that each of the rows 1804-1812 may be processed in parallel for color using separate VFE components, and each of the rows 1804-1812 may be processed using separate GPU components to align and rectify each individual image in a particular row. Alternatively, each of the alignment blocks 1824-1832 may be associated with a single VFE component and a single GPU rectification and alignment component (see FIG. 19).

[00134] Referring to FIG. 19, a particular embodiment of a camera array processing system is illustrated and generally designated 1900. All cameras in an array 1902 may be synchronized, aligned, and processed prior to being combined into a final image. In

the embodiment illustrated in FIG. 19, the array 1902 includes a five-by-five array of cameras. Alternatively, the array 1902 may include any other number of cameras arranged in a two-dimensional array. FIG. 19 illustrates that a single VFE component and a single GPU rectification and alignment component may be used to process all rows of the array 1902, rather than the multiple VFE and GPU rectification and alignment components illustrated in FIG. 18.

[00135] The five-by-five array 1902 illustrated in FIG. 19 includes a first row 1904, a second row 1906, a third row 1908, a fourth row 1910, and a fifth row 1912. Further, the five-by-five array 1902 includes a first column 1914, a second column 1916, a third column 1918, a fourth column 1920, and a fifth column 1922. The first row 1904 may be associated with a first alignment block 1924, the second row 1906 may be associated with a second alignment block 1926, the third row 1908 may be associated with a third alignment block 1928, the fourth row 1910 may be associated with a fourth alignment block 1930, and the fifth row 1912 may be associated with a fifth alignment block 1932. To illustrate, the first alignment block 1924 may be adapted to collect image data lines from each camera in the first row 1904 (i.e., five cameras in the five columns 1914-1922 of the array 1902).

[00136] The first alignment block 1924 may be adapted to align the image data lines in a same order and send the image data lines for processing as a single line. The second alignment block 1926 may be adapted to collect image data lines from each camera in the second row 1906, to align the image data lines in a same order, and to send the image data lines for processing as a single line. The third alignment block 1928 may be adapted to collect image data lines from each camera in the third row 1908, to align the image data lines in a same order, and to send the image data lines for processing as a single line. The fourth alignment block 1930 may be adapted to collect image data lines from each camera in the fourth row 1910, to align the image data lines in a same order, and to send the image data lines for processing as a single line. The fifth alignment block 1932 may be adapted to collect image data lines from each camera in the fifth row 1912, to align the image data lines in a same order, and to send the image data lines for processing as a single line.

[00137] In the embodiment illustrated in FIG. 19, each of the alignment blocks 1924-1932 may be adapted to send its images for processing to a single VFE component 1934 to be processed for color. The single VFE component 1934 may process each of the five lines that are sent from the five alignment blocks 1924-1932. As noted above, the size of a single line from a particular alignment block may be determined based on a number of cameras in a particular row (i.e., five cameras) and a horizontal size (i.e., "H_res" as described in FIG. 15) of each camera in the particular row. As such, the size of the multiple lines processed by the single VFE component 1934 of FIG. 19 may be five times the size of a single line processed by one of the VFE components 1834-1842 of FIG. 18.

[00138] A control synchronization block 1936 may be used to synchronize each of the cameras of the array 1902 such as providing common control signals to cameras in one or more rows 1904-1912. The control synchronization block 1936 may be communicatively coupled to each of the cameras of the array 1902 and to the single VFE components 1934. Synchronization of all cameras in the array 1902 may allow for usage of a rolling shutter on a high resolution. As all cameras may be read out at the same time, a rolling shutter effect may be diminished (with the size of the array). For example, in the five-by-five array 1902 of FIG. 19, synchronization of the twenty five cameras may diminish a rolling shutter effect associated with a CMOS camera.

[00139] The single VFE component 1934 may be communicatively coupled to a single GPU component 1938 to align and rectify each individual image in each of the rows 1904-1912. As such, the single GPU component 1938 of FIG. 19 may align and rectify twenty five images compared to the five images processed by each of the GPU alignment and rectification components 1846-1854 of FIG. 18. The single GPU component 1938 may be communicatively coupled to a GPU processing component 1940 that is adapted to combine all of the rows 1904-1912 together, resulting in a final image.

[00140] FIG. 20 illustrates a high-resolution digital camera system 2000 that includes a main lens 2002 configured to focus incoming light 2004 and multiple cameras arranged in an array 2006. A high-resolution image can be generated as a composite (or "mosaic") image by combining images captured at each of the cameras in the array

2006. For example, each of the cameras of the array 2006 may be a CMOS-type camera or a Charge Coupled Device (CCD) type camera. The main lens 2002 may focus a captured scene to a plane 2008 (referred to as a "focus plane" of the main lens 2002 or an "object plane" of cameras in the array 2006), and each camera in the array 2006 may capture a portion of the total image. Each camera of the array 2006 has a field of view that partially overlaps its neighbors' fields of view at the plane 2008. This overlap may enable images taken from neighboring cameras in the array 2006 to be aligned on a row-by-row basis and "stitched" together during subsequent processing and may provide tolerance for non-ideal position and alignment of cameras within the array (such as described with respect to FIG. 16).

[00141] A composite image can be generated by aligning image data from the cameras of the array 2006 on a row-by-row basis. For example, the array 2006 of FIG. 20 includes a three-by-three array with three rows. Each camera within a particular row of the array 2006 (an "array row") may include an image sensor that has light detectors arranged in columns and rows ("sensor columns" and "sensor rows"). The cameras within an array row may be positioned so that sensor rows are substantially aligned. To illustrate, a first sensor row of each camera in an array row is substantially aligned with the first sensor row of every other camera in the same array row.

[00142] During image capture, the first sensor row of image data is read from each camera in an array row and provided to image processing circuitry (such as described with respect to FIGs. 17-19). The image data from the first sensor row is merged according to the position of each camera in the array row. The merged image data is processed as if it were a single row of image data from a larger camera. The second, third, and subsequent image sensor rows are read, merged, and provided to the image processing circuitry to be processed as rows of the composite image. Each array row may be processed in parallel with the other array rows.

[00143] The arrangement of FIG. 20 may provide an inexpensive alternative to high-resolution cameras. For example, a 100 megapixel (mpix) camera can be built using an array of twenty 5 mpix CMOS cameras behind a main lens. Because image capture can be performed using multiple CMOS cameras with each camera capturing a portion of

the image, "rolling shutter" artifacts may be reduced as compared to a single 100 mpix CMOS camera capturing the entire image.

[00144] Referring to FIG. 21, a particular embodiment of an implementation of a multi-camera module is depicted and generally designated 2100. The system 2100 illustrates a multiple camera module, such as a multiple camera module as illustrated in FIGs. 1-5, mounted on an automobile. The multiple camera module may be configured to generate synchronized line data frames for formatting as three dimensional image or video data, such as described with respect to FIGs. 6-7. By mounting the multiple camera module to a rear portion of the automobile, a three dimensional view may be obtained to provide an operator of the automobile with depth perception on an internal display (not shown) while backing the automobile. It will be understood that the multiple camera module may be mounted to any type of vehicle, without limitation to automobiles.

[00145] Referring to FIG. 22, a flow diagram of a particular illustrative embodiment of a method of combining data from multiple sensors into a synchronized data line depicted and generally designated 2200. As an illustrative example, the method 2200 may be performed by the system of FIG. 2, the system of FIG 3, the system of FIG. 5, or any combination thereof

[00146] A common control signal may be provided to multiple image sensors to be synchronized, at 2202. For example, the common control signal may include a common clock signal and a common reset signal, such as the common control signals 404-410 depicted in FIG. 4.

[00147] A first data line from a first image sensor of the multiple image sensors may be received, at 2204. A second data line from a second image sensor of the multiple image sensors may be received, at 2206. For example, the first sensor and the second sensor may be the sensors 202, 204 of FIG. 2.

[00148] The first data line and the second data line may be combined line to generate a synchronized data line, at 2208. For example, the method 2200 may include interleaving a first data stream received from the first image sensor and a second data stream received from the second image sensor on a line by line basis. The synchronized

data line may be formed as described with respect to the combiner 406 of combining the first sensor image data 422 and the second sensor image data 432 illustrated in FIG. 5.

[00149] The synchronized data line may form part of a frame, such as the frame 660 of FIG. 6. The frame can include a first section (e.g. the first section 652) including first image data from the first image sensor, a second section (e.g. the second section 654) including second image data from the second image sensor, and a gap section (e.g. the gap section 656) including non-image data disposed between the first section and the second section. In other embodiments, the frame may not include a gap section between the first section and the second section.

[00150] Receiving the first data line may be completed before receiving the second data line is completed, and the synchronized data line may be generated after receiving the second data line is completed. As an example, the combined data line 822 of FIG. 8 is generated after the second sensor first line data 812 has been received.

[00151] In an embodiment having more than two image sensors, a third data line may be received from a third image sensor of the multiple image sensors, such as illustrated in FIG. 11. The third data line can be combined with the first data line and the second data line to generate the synchronized data line, such as the first synchronized data line 1150 of FIG. 11.

[00152] Referring to FIG. 23, a flow diagram of a particular illustrative embodiment of a method of providing a common control signal to multiple image sensors and providing a synchronized data line to an image processor via a single camera input of the image processor is depicted and generally designated 2300. The method 2300 may be performed at one or more of the systems of FIGs. 2, 3, and 5, as illustrative, non-limiting examples.

[00153] A common control signal may be provided to multiple image sensors, at 2302. Each of the multiple image sensors may be responsive to the common control signal to generate image data. For example, the common control signal may be provided by a sensor synchronizer that is coupled to each of the multiple image sensors, such as the sensor synchronizer 230 of FIG. 2. To illustrate, the sensor synchronizer may be coupled to each of the multiple image sensors via an inter-integrated circuit

(I2C) control interface, via an interface compliant with a camera serial interface (CSI) specification, or via an interface compliant with a camera parallel interface (CPI) specification.

[00154] Synchronized data output from each of the multiple image sensors may be received, at 2304. A first data line may be received from a first image sensor of the multiple image sensors and a second data line may be received from a second image sensor of the multiple image sensors. Receiving the first data line may be completed before receiving the second data line is completed, and a synchronized data line may be generated after receiving the second data line is completed, such as the combined data line 822 that is generated after the second sensor first line data 812 has been received in FIG. 8.

[00155] The synchronized data output from each of the multiple image sensors may be combined to generate a synchronized data line, at 2306. For example, the combiner 206 of FIG. 2 may interleaving a first data stream received from the first image sensor 202 and a second data stream received from the second image sensor 204 on a line by line basis.

[00156] The synchronized data line may be provided to an image processor via a single camera input of the image processor, at 2308. The synchronized data line may form part of a frame that has a multiple rows, such as the frame 660 of FIG. 6. For example, the frame may include a first section including first image data from the first image sensor, a second section including second image data from the second image sensor, and a gap section between the first and second sections.

[00157] Referring to FIG. 24, a flow diagram of a particular illustrative embodiment of a method of providing a common control signal to multiple image sensors and receiving synchronized data output from each of the multiple image sensors is depicted and generally designated 2400.

[00158] A common control signal to multiple image sensors may be provided, at 2402. Each of the multiple image sensors is responsive to the common control signal to generate image data. For example, the common control signal may provided by a sensor synchronizer that is coupled to each of the multiple image sensors, such as the

sensor synchronizer 230 of any of FIGs. 2-5, the control synchronization block 1844 of FIG. 18, the control synchronization block 1936 of FIG. 19, or any combination thereof.

[00159] Synchronized data output from each of the multiple image sensors may be received, at 2404. The synchronized data output may include first data lines received from a first image sensor and second data lines received from a second image sensor. A phase offset between each received data line from the first image sensor and each corresponding data line from the second image sensor may be substantially constant, such as the one-line phase difference of FIG. 9, the two-line phase difference of FIG. 8, or the 3-line phase difference of FIG. 12, as illustrative, non-limiting examples.

[00160] Referring to FIG. 25, a flow diagram of a particular illustrative embodiment of a method of receiving a common control signal at multiple image sensors and generating synchronized data output from each of the multiple image sensors is depicted and generally designated 2500.

[00161] A common control signal may be received at multiple image sensors, at 2502. Each of the multiple image sensors is responsive to the common control signal to generate image data. For example, the common control signal may received from a sensor synchronizer that is coupled to each of the multiple image sensors, such as the sensor synchronizer 230 of any of FIGs. 2-5, the control synchronization block 1844 of FIG. 18, the control synchronization block 1936 of FIG. 19, or any combination thereof.

[00162] Synchronized data output from each of the multiple image sensors may be generated, at 2504. The synchronized data output may include first data lines received from a first image sensor and second data lines received from a second image sensor. A phase offset between each received data line from the first image sensor and each corresponding data line from the second image sensor may be substantially constant, such as the one-line phase difference of FIG. 9, the two-line phase difference of FIG. 8, or the 3-line phase difference of FIG. 12, as illustrative, non-limiting examples.

[00163] Referring to FIG. 26, a flow diagram of a particular illustrative embodiment of a method of combining data from multiple sensors at an image signal processor having an input for a single camera is depicted and generally designated 2600.

[00164] Lines of image data may be received at an image processor having an input for a single camera, at 2602. Each line of the image data may include first line data from a first image captured by a first camera and second line data from a second image captured by a second camera. As an illustrative, non-limiting example, the image processor may include the image signal processor 208 of FIGs. 2-3 or FIG. 5, the image processor 1308 of FIG. 13, the VFEs 1834-1842 of FIG. 18, the VFEs 1934-1942 of FIG. 19, or any combination thereof.

[00165] The lines of image data may be received at the image processor from a combiner that is coupled to the first camera and to the second camera. Line by line readout of first image data from the first camera and second image data from the second camera may be synchronized, using the combiner, to generate each line of the image data. For example, the combiner may be the combiner 206 of FIGs. 2-3 or FIG. 5, the combiner 1306 of FIG. 13, the data alignment blocks 1824-1832 of FIG. 18, the data alignment blocks 1924-1932 of FIG. 19, or any combination thereof.

[00166] An output frame having a first section corresponding to line data of the first image and having a second section corresponding to line data of the second image may be generated, at 2604. The first section and the second section may be configured to be used to generate a three-dimensional (3D) image format or a 3D video format.

[00167] In a particular embodiment, the output frame is processed to generate 3D image data, and the 3D image data is sent to a display device. In another embodiment, the output frame is processed to generate 3D video data, and the 3D video data is sent to a display device, such as the display device 1310 of FIG. 13. To illustrate, the display device may be a component of at least one of a communication device, a camera, a personal digital assistant, and a computer.

[00168] Referring to FIG. 27, a flow diagram of an illustrative embodiment of a method of combining data from multiple sensors into a frame is depicted and generally designated 2700. As an illustrative example, the method 2700 may be performed by the system of FIG. 2, the system of FIG. 5, or any combination thereof.

[00169] A first data stream may be received from a first image sensor, such as the first sensor 202 of FIG. 2, at 2702. The first data stream, such as the first image data

stream 212 of FIG. 2, the first data stream 602 of FIG. 6, or the timing data signal 420 and the image data signal 422 of FIG. 5, may correspond to first image data of an image. A second data stream may be received from a second image sensor, such as the second sensor 204 of FIG. 2, at 2704. The second data stream, such as the second image data stream 214 of FIG. 2, the second data stream 604 of FIG. 6, or the timing signal data 430 and the image data signal 432 of FIG. 5, may correspond to second image data of the image.

[00170] Data from the first data stream and data from the second data stream may be combined, at 2706. For example, a combiner, such as the combiner 206 of FIG. 2 or the combiner 206 of FIG. 5, may combine the first image data from the first data stream and the second image data from the second data stream and generate a resulting frame. To illustrate, the first data stream may include data associated with a first line of the first image data including line data having a first line index value, line data having a second line index value, etc. The second data stream may include line data that corresponds to that of the first data stream, including corresponding line data having a first line index value, and corresponding line data having a second line index value, etc. The line data from the first data stream having the first line index value and the line data from the second data stream having the corresponding first line index value may be appended to each other, or combined, to form a single image line. The process may be repeated for each line index value to generate the resulting frame, such as the frame 660 of FIG. 6. In a particular embodiment, the frame may include a plurality of rows, where each row corresponds to a line index value and stores a line of the first image data having the line index value and stores a corresponding line of the second image data having the line index value. In a particular embodiment, when the first line of the first image data and the corresponding line of the second image data are combined into a single image line, the size of the single image line is substantially double that of the first line of the first image data or the corresponding line of the second image data.

[00171] The frame may be processed at an image signal processor to generate a processed frame, at 2708. In a particular embodiment, the image signal processor may be the image signal processor 208 of FIG. 2 or the image signal processor 208 of FIG. 5, and the processed frame may be the processed frame 240 of FIG. 2 or the processed frame 650 of FIG. 6. In a particular embodiment, the processed frame may include a

first section including first image data from the first image sensor, such as the first section 652, a second section including second image data from the second image sensor, such as the second section 654, and a gap section, such as the gap section 656 of FIG. 6. The gap section may include non-image data disposed between the first section and the second section. In a particular embodiment, the first section may include a line of the first image data and the second section may include a corresponding line of the second image data.

[00172] The processed frame may be output to be displayed at a display device, at 2710. In a particular embodiment, the first image sensor and the second image sensor are each directly responsive to the image signal processor, and the display device may be decoupled from the image signal processor.

[00173] Referring to FIG. 28, a flow diagram of an illustrative embodiment of a method of synchronizing a first image sensor and a second image sensor is depicted and generally designated 2800. As an illustrative example, the method 2800 may be performed at the system 200 of FIG. 2, the system 600 of FIG. 5, or any combination thereof.

[00174] First image data of an image may be received from a first image sensor, at 2802. In a particular embodiment, the first image sensor may be the first sensor 202 of FIG. 2. A first data stream associated with the first image data may be received from the first image sensor, at 2804. In a particular embodiment, the first data stream may be generated by the image sensor and may be the first image data stream 212 of FIG. 2, the first data stream 602 of FIG. 6, or the timing data signal 420 and the image data signal 422 of FIG. 5.

[00175] Second image data of the image may be received from a second image sensor, at 2806. In a particular embodiment, the second image sensor may be the second sensor 204 of FIG. 2. A second data stream associated with the second image data may be received from the second image sensor, at 2808. In a particular embodiment, the second data stream may be generated by the image sensor and may be the second image data stream 214 of FIG. 2, the second data stream 604 of FIG. 6, or the timing data signal 430 and the image data signal 432 of FIG. 5.

[00176] Line by line exposure of the first image sensor and the second image sensor during image data acquisition may be synchronized, at 2810. In a particular embodiment, the synchronization may occur during image data acquisition of an image at a host including a combiner, such as the combiner 206 of FIG. 2 or the combiner 206 of FIG. 5. In a particular embodiment, the first image sensor and the second image sensor are independent of each other. For example, the first and second sensors 202, 204 of FIG. 2 are directly responsive to the image signal processor 208 via the control signal 232 to have similar timing characteristics while remaining independent of each other. The first data stream and the second data stream may be interleaved, at 2812. In a particular embodiment, the first data stream and the second data stream may be interleaved on a line by line basis. For example, line data from the first data stream having a first line index value and line data from the second data stream having a corresponding first line index value may be appended to each other to form an interleaved single image line.

[00177] Thus, the combined data may be efficiently processed using a single image signal processor. Thus, overall image system cost and complexity may be reduced compared to multiple processor systems in which a processor is assigned to each sensor.

[00178] Referring to FIG. 29, a flow diagram of a first illustrative embodiment of a method of combining data from multiple image sensors to generate 3D image data is depicted and generally designated 2900. As an illustrative example, the method 2900 may be performed by the system of FIG. 13.

[00179] The method includes synchronizing line by line readout of first image data from a first camera and a second camera to generate rows of image data, at 2902. The first image data from the first camera may be the image data stream 1314 from the first image sensor 1302 of FIG. 1 and the second image data may be the image data stream 1316 from the second image sensor 1304 of FIG. 13.

[00180] The method includes receiving rows of the image data at an image processor having an input for a single camera, at 2904. Each row of the image data includes data from a row of a first image captured by the first camera and data from a row of a second image captured by the second camera. The rows of image data may be the data out stream 706 depicted in FIG. 7.

[00181] The method includes generating, with the image processor, an output having one of a 3D image format and a 3D video format, at 2906. The output corresponds to the first image and the second image. The output is sent to a display device (e.g., the display device 1310 of FIG. 13), at 2908.

[00182] Referring to FIG. 30, a flow diagram of an illustrative embodiment of a method of combining data from multiple sensors into a frame is depicted and generally designated 3000. As an illustrative example, the method 3000 may be performed by the system of FIG. 13.

[00183] A first data stream is received from a first image sensor, such as the first image sensor 1302 of FIG. 13, at 3002. The first data stream, such as the first image data stream 1314 of FIG. 13 or the first data stream 702 of FIG. 7 may correspond to first image data of a first image. A second data stream may be received from a second image sensor, such as the second image sensor 1304 of FIG. 13, at 3004. The second data stream, such as the second image data stream 1316 of FIG. 13, the second data stream 704 of FIG. 7 may correspond to second image data of a second image. The first image and the second image may be images of a scene. The first image and the second image of the scene may be taken at substantially the same time, or may be taken at different times. The first image may be taken from a different vantage point than the second image so that depth information can be determined from the first image and the second image of the scene.

[00184] Data from the first data stream and data from the second data stream is combined, at 3006. For example, a combiner, such as the combiner 1306 of FIG. 13 may combine the first image data from the first data stream and the second image data from the second data stream and generate a resulting frame. To illustrate, the first data stream may include data associated with a first line of the first image data including line data having a first line index value, line data having a second line index value, etc. The second data stream may include line data that corresponds to that of the first data stream, including corresponding line data having a first line index value, and corresponding line data having a second line index value, etc. The line data from the first data stream having the first line index value and the line data from the second data stream having the corresponding first line index value may be appended to each other,

or combined, to form a single image line. The process may be repeated for each line index value to generate the resulting frame, such as the frame 740 of FIG. 7. In a particular embodiment, the frame may include a plurality of rows, where each row corresponds to a line index value and stores a line of the first image data having the line index value and stores a corresponding line of the second image data having the line index value. In a particular embodiment, when the first line of the first image data and the corresponding line of the second image data are combined into a single image line, the size of the single image line is substantially double that of the first line of the first image data or the corresponding line of the second image data.

[00185] The frame is received as rows of image data via an input for a single camera, at 3008. In a particular embodiment, the input for the single camera may be the input of an image processor, such as the image processor 1308 of FIG. 13. The frame may be frame 740 of FIG. 7.

[00186] An output is generated from the frame, at 3010. The output has one of a 3D image format and a 3D video format. The output corresponds to the first image and the second image. The output may be the processed frame data 1320 of FIG. 13. The output is sent to a display device, at 3012. In a particular embodiment, the display device may be the display device 1310 of FIG. 13.

[00187] Referring to FIG. 31, a flow diagram of an illustrative embodiment of a method of synchronizing a first image sensor and a second image sensor is depicted and generally designated 3100. As an illustrative example, the method 3100 may be performed by the system 1300 of FIG. 13.

[00188] First image data of an image may be received from a first image sensor, at 3102. In a particular embodiment, the first image sensor may be the first image sensor 1302 of FIG. 13. A first data stream associated with the first image data may be received from the first image sensor, at 3104. In a particular embodiment, the first data stream may be generated by the image sensor and may be the first image data stream 1314 of FIG. 13 or the first data stream 702 of FIG. 7.

[00189] Second image data of the image may be received from a second image sensor, at 3106. In a particular embodiment, the second image sensor may be the

second image sensor 1304 of FIG. 13. A second data stream associated with the second image data may be received from the second image sensor, at 3108. In a particular embodiment, the second data stream may be generated by the image sensor and may be the second image data stream 1316 of FIG. 13 or the second data stream 704 of FIG. 7.

[00190] Line by line exposure of the first image sensor and the second image sensor during image data acquisition may be synchronized, at 3110. In a particular embodiment, the synchronization may occur during image data acquisition of an image at a host including a combiner, such as the combiner 1306 of FIG. 13. In a particular embodiment, the first image sensor and the second image sensor are independent of each other. For example, the first and second image sensors 1302, 1304 of FIG. 13 may be directly responsive to the image processor 1308 via a control signal to have similar timing characteristics while remaining independent of each other. In another embodiment, the first and second image sensors 1302, 1304 are directly responsive to the combiner 1306 via a control signal to have similar timing characteristics while remaining independent of each other. The first data stream and the second data stream may be interleaved, at 3112. In a particular embodiment, the first data stream and the second data stream may be interleaved on a line by line basis. For example, line data from the first data stream having a first line index value and line data from the second data stream having a corresponding first line index value may be appended to each other to form an interleaved single image line.

[00191] Thus, the combined data may be efficiently processed using a single image processor. Thus, overall image system cost and complexity may be reduced compared to multiple processor systems in which a processor is assigned to each sensor.

[00192] Referring to FIG. 32, a flow diagram of an illustrative embodiment of a method of generating a 3D image with an image processor is depicted and generally designated as 3200. The image processor may be the image processor 1308 of FIG. 13. The method 3200 may be used when the image processor treats a frame received from a combiner (e.g., the combiner 1306 of FIG. 1), a frame from a memory, or when a user chooses to alter a displayed 3D image using a zoom feature or a pan feature of a device displaying the 3D image.

[00193] The image processor rectifies a first image and a second image based on parameters of a calibration matrix, at 3202. The calibration matrix may provide adjustments for relative positions of a first image sensor and a second image sensor that capture the first image and the second image. The relative positions of the two cameras may be selected to ensure minimal scene distortion and eye strain. The calibration matrix may be determined during a manufacturing process for a device that takes the 3D image where the positions of the first image sensor and the second image sensor are fixed relative to each other. The calibration may be stored in a memory of the device. For a device that takes the 3D image where the positions of the first image sensor, the second image sensor, or both are adjustable, a processor of the device may be used to run a calibration routine to determine the calibration matrix and store the calibration matrix in the memory. The calibration routine may require the first image sensor and the second image sensor to be focused on a particular calibration scene positioned a set distance from the image sensors. The calibration routine may be performed after position adjustment of the image sensors relative to each other.

[00194] The image processor detects keypoints in the first image, at 3204. The image processor may detect distinctive (high frequency) points in the first image. The image processor block matches between local image patches in the first image and the second image to compute disparities for each detected keypoint in the first image, at 3206. A reliability estimator may be produced for every keypoint to insure that erroneous matches are discarded. The image processor determines a convergence adjustment based on a disparity range determined from the computed disparities, at 3208. The convergence adjustment takes scene depth and display geometry into consideration.

[00195] The image processor selectively shifts at least one of the first image and the second image based on the convergence adjustment when the convergence adjustment is within capabilities of a display device that will display the 3D image to generate output, at 3210. The image processor uses the first image with disparity adjusted to match a majority of the scene when the convergence adjustment is not within the capabilities of the display device to generate the output, at 3212. The image processor crops the output based on one or more display characteristics of the display device, at 3214.

[00196] FIG. 33 is a block diagram of a particular embodiment of an image processing system 3300 to combine data from multiple image sensors. The image processing system 3300 may include an image sensor device 3302 that is coupled to a first lens 3304, coupled to a second lens 3306, and coupled to an application processor chipset of a portable multimedia device 3308. The image sensor device 3302 may include a combiner 3310 and an image processor 3312 that receives input for a single camera. The image processor 3312 may receive the single camera input from the combiner 3310 or from a memory device 3314 of the application processor chipset of the portable multimedia device 3308. The combiner 3310 may combine data from a first data stream and from a second data stream to generate a frame, such as by implementing the system 1300 of FIG. 13, by operating in accordance with any of the embodiments of FIGs. 29-31, or any combination thereof.

[00197] The combiner 3310 is coupled to receive image data from a first sensor 3316 via a first analog-to-digital convertor 3318. The combiner 3310 is coupled to receive image data from a second sensor 3320 via a second analog-to-digital convertor 3322. The combiner 3310 or the image processor 3312 may control the first sensor 3316 and the second sensor 3320, which may be otherwise independent of each other. In a particular embodiment, the image processor 3312 may control the first sensor 3316 and the second sensor 3320 via a sensor synchronizer 3330 (shown in shadow).

[00198] In a particular embodiment, an integrated circuit that includes image processing circuitry, such as the combiner 3310, is configured to generate a frame. The image processing circuitry is configured to receive a first data stream from a first image sensor, such as the first sensor 3316, to receive a second data stream from a second image sensor, such as the second sensor 3320, and to combine data from the first data stream and from the second data stream to generate the frame. For example, the first data stream 702 and the second data stream 704 of FIG. 7 may be combined by the combiner 3310 to form the frame 740 of FIG. 7.

[00199] Output from the combiner 3310 may be sent to a memory device 3314 of the application processor chipset of the portable multimedia device 3308, to an image processor 3312, or both. The image processor 3312 may be configured to perform additional image processing operations, such as one or more operations performed by an

image processing system. The image processor 3312 may receive a frame from the combiner 3310 or from the memory device 3314. The image processor 3312 may produce processed image data such as a processed frame having a 3D image format or a 3D video format. In an embodiment, an average time for producing processed image data is about 20 milliseconds. The image processor 3312 may provide the processed image data to the application processor chipset of the portable multimedia device 3308 for further processing, transmission, storage, display to a display device 3324, or any combination thereof.

[00200] Referring to FIG. 34, a block diagram of a particular illustrative embodiment of an electronic device, such as a wireless phone, including a frame generator module, as described herein, is depicted and generally designated 3400. The device 3400 includes a processor 3410 coupled to a memory 3432. The processor includes or is coupled to a controller 3464. Alternatively, the electronic device may be a set top box, a music player, a video player, an entertainment unit, a navigation device, a communications device, a personal digital assistant (PDA), a camera, a fixed location data unit, or a computer.

[00201] FIG. 34 also shows a display controller 3426 that is coupled to the processor 3410 and to a display 3428. A coder/decoder (CODEC) 3434 can also be coupled to the processor 3410. A speaker 3439 and a microphone 3438 can be coupled to the CODEC 3434. A camera controller 3470 can also be coupled to the processor 3410. A first camera 3472 and a second camera 3473 can be coupled to the camera controller 3470.

[00202] FIG. 34 also indicates that a wireless interface 3440 can be coupled to the processor 3410 and to a wireless antenna 3442. In a particular embodiment, the processor 3410, the display controller 3426, the memory 3432, the CODEC 3434, the wireless interface 3440, and the controller 3464 are included in a system-in-package or system-on-chip 3422. In a particular embodiment, an input device 3430 and a power supply 3444 are coupled to the on-chip system 3422. Moreover, in a particular embodiment, as illustrated in FIG. 34, the display 3428, the input device 3430, the speaker 3439, the microphone 3438, the wireless antenna 3442, and the power supply 3444 are external to the on-chip system 3422. However, each can be coupled to a component of the on-chip system 3422, such as an interface or a controller.

[00203] In a particular embodiment, the processor 3410 executes processor-readable program instructions from a processor-readable medium, such as program instructions 3482 stored at the memory 3432. For example, the memory 3432 may be readable by the processor 3410 and the instructions 3482 may be operational instructions that are executable by the processor 3410 to perform the method 2200 of FIG. 22. For example, the instructions 3482 may include instructions that are executable by the processor 3410 to receive a first data stream from a first image sensor, such as the camera 3473 to receive a second data stream from a second image sensor, such as the camera 3472, and to combine data from the first data stream and from the second data stream to generate a frame. For example, the first image sensor may be the first sensor 202 of FIG. 2 and the second image sensor may be the second sensor 204 of FIG. 2. The instructions 3482 may further include instructions that are executable by the processor 3410 to process the frame at the processor 3410 or at an image signal processor (not shown) to generate a processed frame. The instructions 3482 may further include instructions that are executable by the processor 3410 to output the processed frame to be displayed at the display device 3428 or stored at the memory 3432 as image data 3480.

[00204] Referring to FIG. 35, a block diagram of a particular illustrative embodiment of an electronic device, such as a mobile phone, is depicted and generally designated 3500. The device 3500 includes a processor 3502 coupled to a memory 3504. The processor 3502 includes or is coupled to an image processor 3506. The image processor 3506 may receive a single camera input and may output 3D data 3590. The 3D data 3590 may be in 3D image format or 3D video format. Alternatively, the electronic device 3500 may be a set top box, a music player, a video player, an entertainment unit, a navigation device, a communications device, a personal digital assistant (PDA), a camera, a fixed location data unit, a computer, or combinations thereof.

[00205] FIG. 35 also shows a display controller 3508 that is coupled to the processor 3502 and to a display 3510. A coder/decoder (CODEC) 3512 can also be coupled to the processor 3502. A speaker 3514 and a microphone 3516 can be coupled to the CODEC 3512. A camera controller 3518 can also be coupled to the processor 3502. The camera controller 3518 may include a combiner 3520. The combiner 3520 may provide image data to the image processor 3506. As illustrative examples, the combiner 3520 may be the combiner 1306 of FIG. 13, or other hardware circuitry or processor configured to

combine data from multiple cameras as illustrated with respect to FIG. 7. A first camera 3522 and a second camera 3524 can be coupled to the camera controller 3518.

[00206] FIG. 35 also indicates that a wireless interface 3526 can be coupled to the processor 3502 and to a wireless antenna 3528. In a particular embodiment, the processor 3502, the display controller 3508, the memory 3504, the CODEC 3512, the camera controller 3518, and the wireless interface 3526 are included in a system-in-package or system-on-chip 3530. In a particular embodiment, an input device 3532 and a power supply 3534 are coupled to the on-chip system 3530. Moreover, in a particular embodiment, as illustrated in FIG. 35, the display 3510, the input device 3532, the speaker 3514, the microphone 3516, the wireless antenna 3528, and the power supply 3534 are external to the on-chip system 3530. However, each can be coupled to a component of the on-chip system 3530, such as an interface or a controller.

[00207] In a particular embodiment, the processor 3502 executes processor-readable program instructions from a processor-readable medium, such as program instructions 3536 stored at the memory 3504. For example, the memory 3504 may be readable by the processor 3502 and the instructions 3536 may be operational instructions that are executable by the processor 3502 to perform the method 2500 of FIG. 25. For example, the instructions 3536 may include instructions that are executable by the processor 3502 to receive a first data stream from a first image sensor, such as the camera 3522, to receive a second data stream from a second image sensor, such as the camera 3524, and to combine data from the first data stream and from the second data stream using the combiner 3520 of the camera controller 3518 to generate a frame. For example, the first image sensor may be the first image sensor 1302 of FIG. 13, and the second image sensor may be the second image sensor 1304 of FIG. 13. The instructions 3536 may further include instructions that are executable by the processor 3502 to process the frame at the image processor 3506 to generate a processed frame. The instructions 3536 may further include instructions that are executable by the processor 3502 to output the processed frame as 3D data to the display controller 3508 for display at the display device 3510 or to store the processed frame at the memory 3504 as image data 3538.

[00208] Those of skill would further appreciate that the various illustrative logical blocks, configurations, modules, circuits, and algorithm steps described in connection

with the embodiments disclosed herein may be implemented as electronic hardware, computer software executed by a processor, or combinations of both. Various illustrative components, blocks, configurations, modules, circuits, and steps have been described above generally in terms of their functionality. Whether such functionality is implemented as hardware or software executed by a processor depends upon the particular application and design constraints imposed on the overall system. Skilled artisans may implement the described functionality in varying ways for each particular application, but such implementation decisions should not be interpreted as causing a departure from the scope of the present disclosure.

[00209] The methods of FIGs. 22-32 may be performed by executing program code that may be stored in memory in the form of computer readable instructions. In that case, a processor, such as a digital signal processor (DSP) an image signal processor (ISP), or other processor, may execute instructions stored in memory in order to carry out one or more of the image processing methods. In some cases, the methods may be executed by a DSP or ISP that invokes various hardware components to accelerate the image processing. In other cases, the units described herein may be implemented as, or methods may be performed by, a microprocessor, one or more application specific integrated circuits (ASICs), one or more field programmable gate arrays (FPGAs), or any combination thereof.

[00210] The steps of a method or algorithm described in connection with the embodiments disclosed herein may be embodied directly in hardware, in a software module executed by a processor, or in a combination of the two. A software module may reside in random access memory (RAM), flash memory, read-only memory (ROM), programmable read-only memory (PROM), erasable programmable read-only memory (EPROM), electrically erasable programmable read-only memory (EEPROM), registers, hard disk, a removable disk, a compact disc read-only memory (CD-ROM), or any other form of non-transitory computer readable storage medium known in the art. An exemplary storage medium is coupled to the processor such that the processor can read information from, and write information to, the storage medium. In the alternative, the storage medium may be integral to the processor. The processor and the storage medium may reside in an application-specific integrated circuit (ASIC). The ASIC may reside in a computing device or a user terminal. In the alternative, the processor and the

storage medium may reside as discrete components in a computing device or user terminal.

[00211] The previous description of the disclosed embodiments is provided to enable a person skilled in the art to make or use the disclosed embodiments. Various modifications to these embodiments will be readily apparent to those skilled in the art, and the principles defined herein may be applied to other embodiments without departing from the scope of the disclosure. Thus, the present disclosure is not intended to be limited to the embodiments shown herein but is to be accorded the widest scope possible consistent with the principles and novel features as defined by the following claims.

WHAT IS CLAIMED IS:

1. A method comprising:

providing a common control signal to multiple image sensors to be synchronized;

receiving a first data line from a first image sensor of the multiple image sensors;

receiving a second data line from a second image sensor of the multiple image sensors; and

combining the first data line and the second data line to generate a synchronized data line.

2. The method of claim 1, wherein the synchronized data line forms part of a frame, wherein the frame comprises:

a first section including first image data from the first image sensor; and

a second section including second image data from the second image sensor.

3. The method of claim 2, wherein the frame further comprises a gap section comprising non-image data disposed between the first section and the second section.

4. The method of claim 2, wherein the frame has a plurality of rows, wherein each row corresponds to a line index value and stores a line of the first image data having the line index value and stores a corresponding line of the second image data having the line index value.

5. The method of claim 1, wherein the common control signal comprises a common clock signal and a common reset signal.

6. The method of claim 1, wherein the first data line is associated with a first pixel size and a first pixel clock, wherein the second data line is associated with a second pixel size and a second pixel clock, and wherein the synchronized data line has a size substantially double that of the first data line or the second data line and is associated

with a pixel clock having a rate that is substantially double a rate of the first pixel clock or the second pixel clock.

7. The method of claim 1, further comprising interleaving a first data stream received from the first image sensor and a second data stream received from the second image sensor on a line by line basis, wherein the first data stream includes the first data line, wherein the second data stream includes the second data line, and wherein combining the first data line and the second data line is performed during the interleaving of the first and second data streams.

8. The method of claim 1, further comprising receiving a third data line from a third image sensor of the multiple image sensors, wherein the third data line is combined with the first data line and the second data line to generate the synchronized data line.

9. The method of claim 1, wherein receiving the first data line is completed before receiving the second data line is completed, and wherein the synchronized data line is generated after receiving the second data line is completed.

10. A device comprising:

a first input configured to receive a first data line from a first image sensor of multiple image sensors to be synchronized via a common control signal;

a second input configured to receive a second data line from a second image sensor of the multiple image sensors; and

a combiner coupled to the first input and to the second input, wherein the combiner is configured to combine the first data line and the second data line to generate a synchronized data line.

11. The device of claim 10, wherein the synchronized data line forms part of a frame, wherein the frame comprises:

a first section including first image data from the first image sensor; and

a second section including second image data from the second image sensor.

12. The device of claim 11, wherein the frame further comprises a gap section comprising non-image data disposed between the first section and the second section.

13. The device of claim 11, wherein the frame has a plurality of rows, wherein each row corresponds to a line index value and stores a line of the first image data having the line index value and stores a corresponding line of the second image data having the line index value.

14. The device of claim 10, wherein the common control signal comprises a common clock signal and a common reset signal.

15. The device of claim 10, wherein the first data line is associated with a first pixel size and a first pixel clock, wherein the second data line is associated with a second pixel size and a second pixel clock, and wherein the synchronized data line has a size substantially double that of the first data line or the second data line and is associated with a pixel clock having a rate that is substantially double a rate of the first pixel clock or the second pixel clock.

16. The device of claim 10, wherein the combiner is configured to interleave a first data stream received from the first image sensor and a second data stream received from the second image sensor on a line by line basis, wherein the first data stream includes the first data line, wherein the second data stream includes the second data line, and wherein the combiner is configured to combine the first data line and the second data line while interleaving the first and second data streams.

17. The device of claim 10, further comprising a third input coupled to the combiner and configured to receive a third data line from a third image sensor of the multiple image sensors, wherein the combiner is further configured to combine the third data line with the first data line and the second data line to generate the synchronized data line.

18. The device of claim 10, wherein combiner comprises a buffer and wherein the combiner is configured to buffer least a portion of a next data line that is received from the first image sensor or from the second image sensor before the synchronized data line is generated.

19. The device of claim 10, wherein the first input, the second input, and the combiner are integrated in a portable electronic device.

20. The device of claim 10, wherein the first input, the second input, and the combiner are integrated in a camera module configured to be coupled to a processor of a portable electronic device.

21. A device comprising:

means for receiving a first data line from a first image sensor of multiple image sensors to be synchronized via a common control signal;

means for receiving a second data line from a second image sensor of the multiple image sensors; and

means for combining the first data line and the second data line to generate a synchronized data line.

22. The device of claim 21, further comprising means for buffering at least a portion of a next data line that is received from the first image sensor or from the second image sensor before the synchronized data line is generated.

23. A device comprising:

a first image sensor and a second image sensor configured to be synchronized via a common control signal; and

a combiner coupled to receive a first data line of the first image sensor and a second data line from a second image sensor, wherein the combiner is configured to combine the first data line and the second data line to generate a synchronized data line.

24. The device of claim 23, further comprising:

an image signal processor coupled process the synchronized data line; and

a display device configured to display processed image data.

25. A non-transitory computer readable-medium comprising instructions, which when executed by a processor cause the processor to:

provide a common control signal to multiple image sensors to be synchronized;

receive a first data line from a first image sensor of the multiple image sensors;

receive a second data line from a second image sensor of the multiple image sensors; and

combine the first data line and the second data line to generate a synchronized data line.

26. The non-transitory computer readable-medium of claim 23, wherein the synchronized data line forms part of a frame, and wherein the frame comprises:

a first section including first image data from the first image sensor; and

a second section including second image data from the second image sensor.

27. The non- transitory computer readable-medium of claim 23, wherein the frame further comprises a gap section comprising non-image data disposed between the first section and the second section.

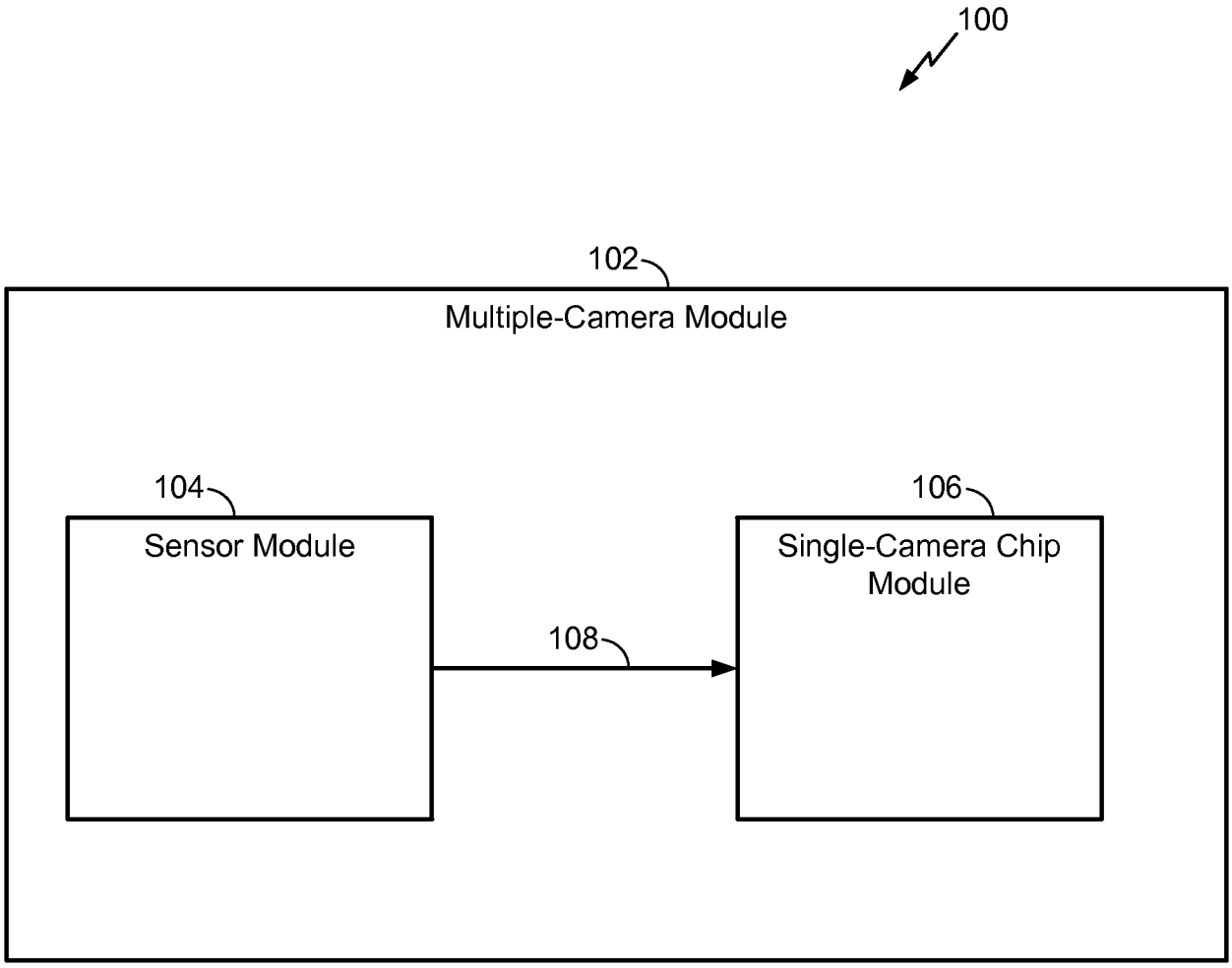
100
102
Multiple-Camera Module
104
Sensor Module
106
Single-Camera Chip Module
108

FIG. 1

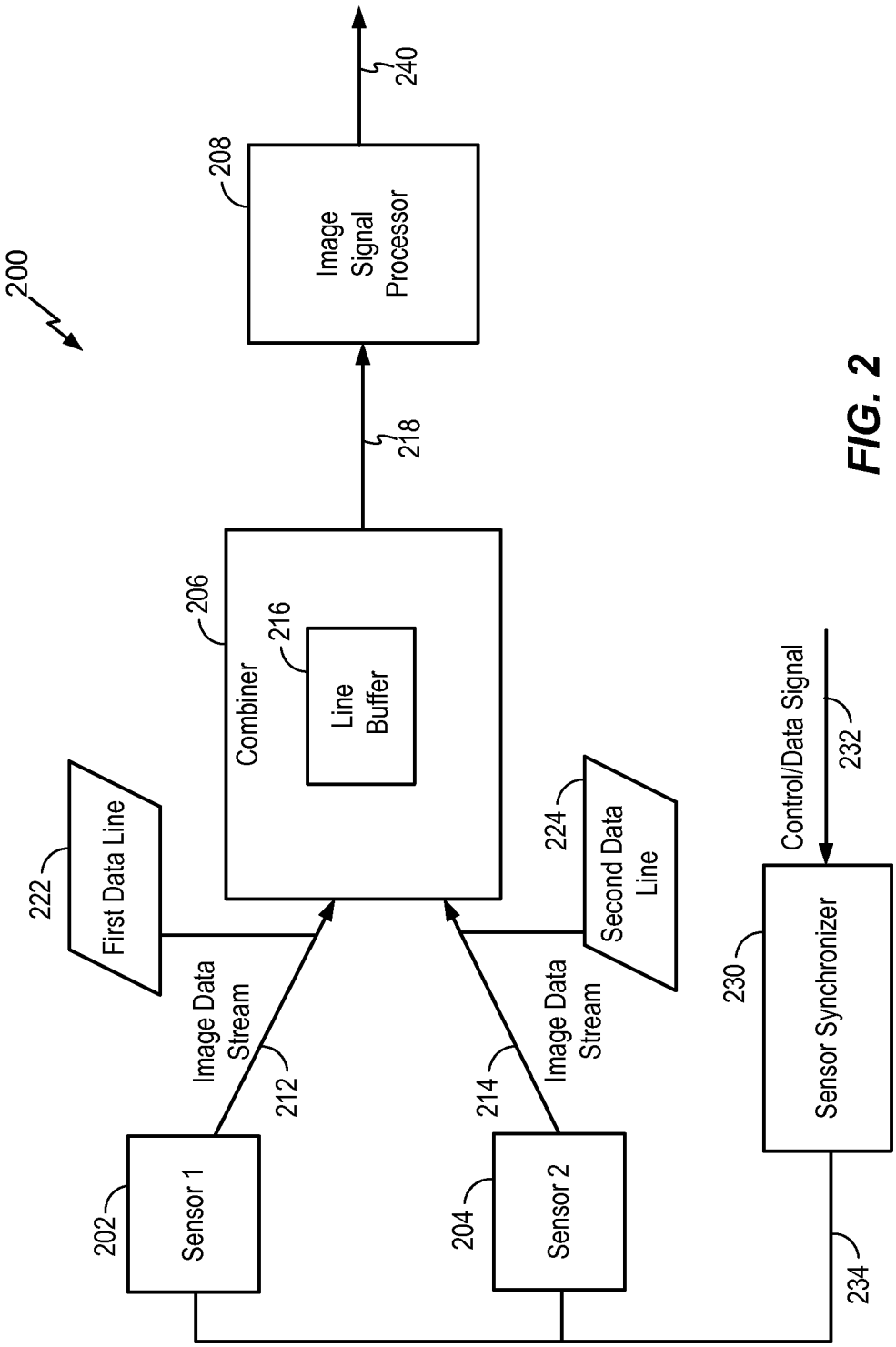
200
Sensor 1
202
Sensor 2
204
First Data Line
222
Second Data Line
224
Image Data Stream
212
Image Data Stream
214
Combiner
206
Line Buffer
216
218
Image Signal Processor
208
240
Sensor Synchronizer
230
Control/Data Signal
232
234

FIG. 2

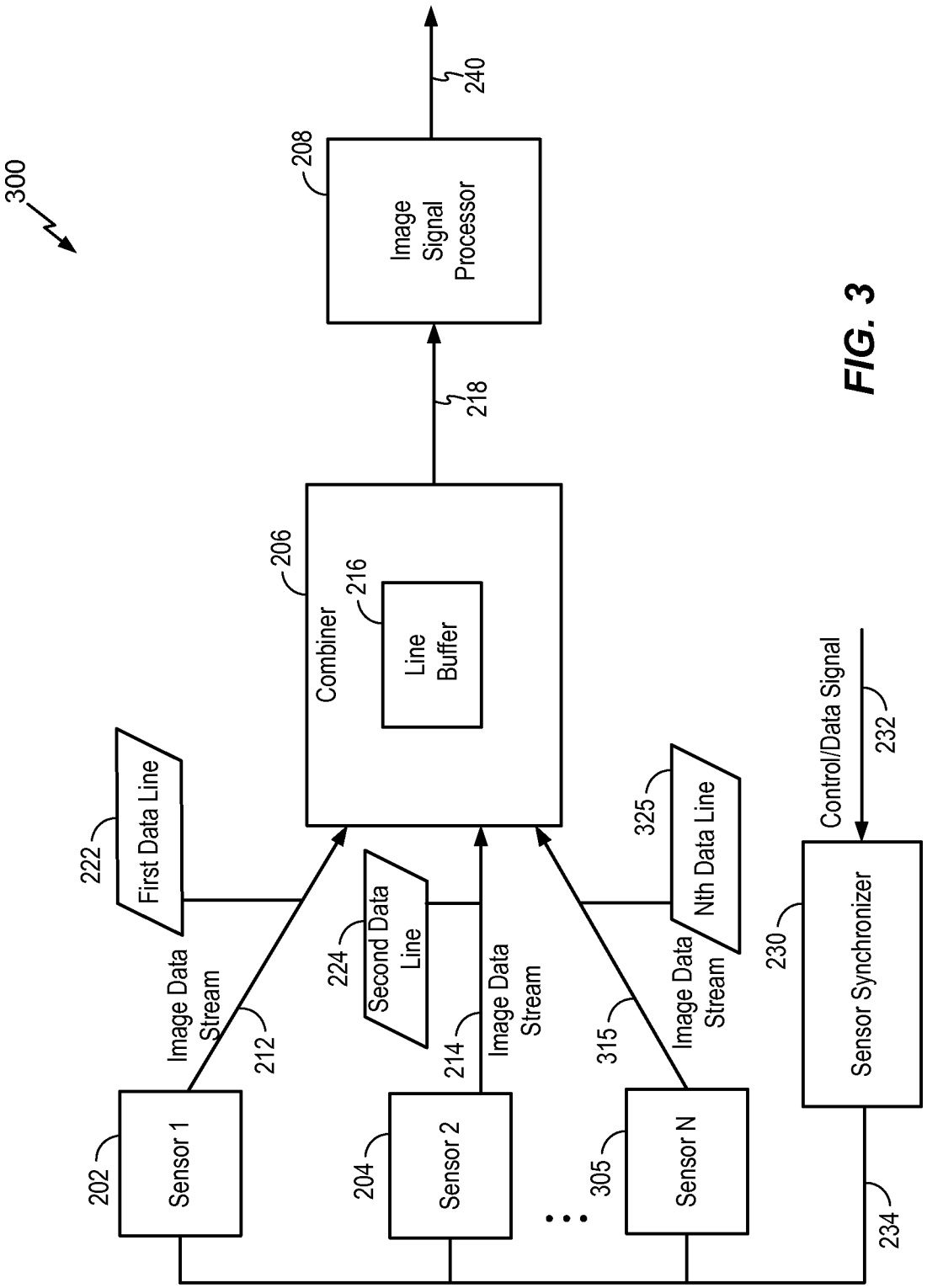
300
Image Signal Processor
208
240
218
Combiner
206
Line Buffer
216
First Data Line
222
Second Data Line
224
Nth Data Line
325
Image Data Stream
212
214
315
Sensor 1
202
Sensor 2
204
Sensor N
305
Sensor Synchronizer
230
Control/Data Signal
232
234

FIG. 3

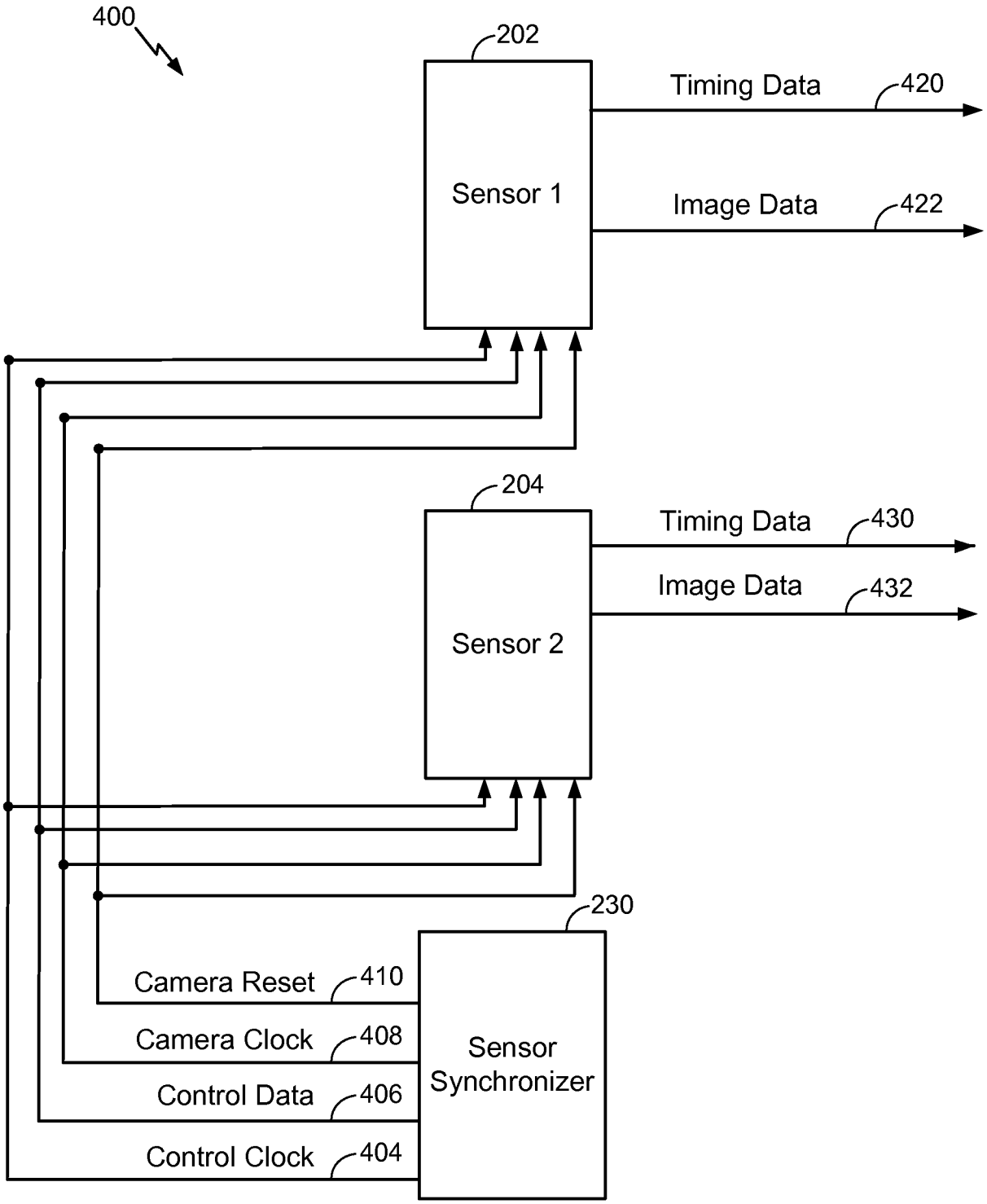
400
202
Sensor 1
Timing Data
420
Image Data
422
204
Sensor 2
Timing Data
430
Image Data
432
230
Sensor Synchronizer
Camera Reset
410
Camera Clock
408
Control Data
406
Control Clock
404

FIG. 4

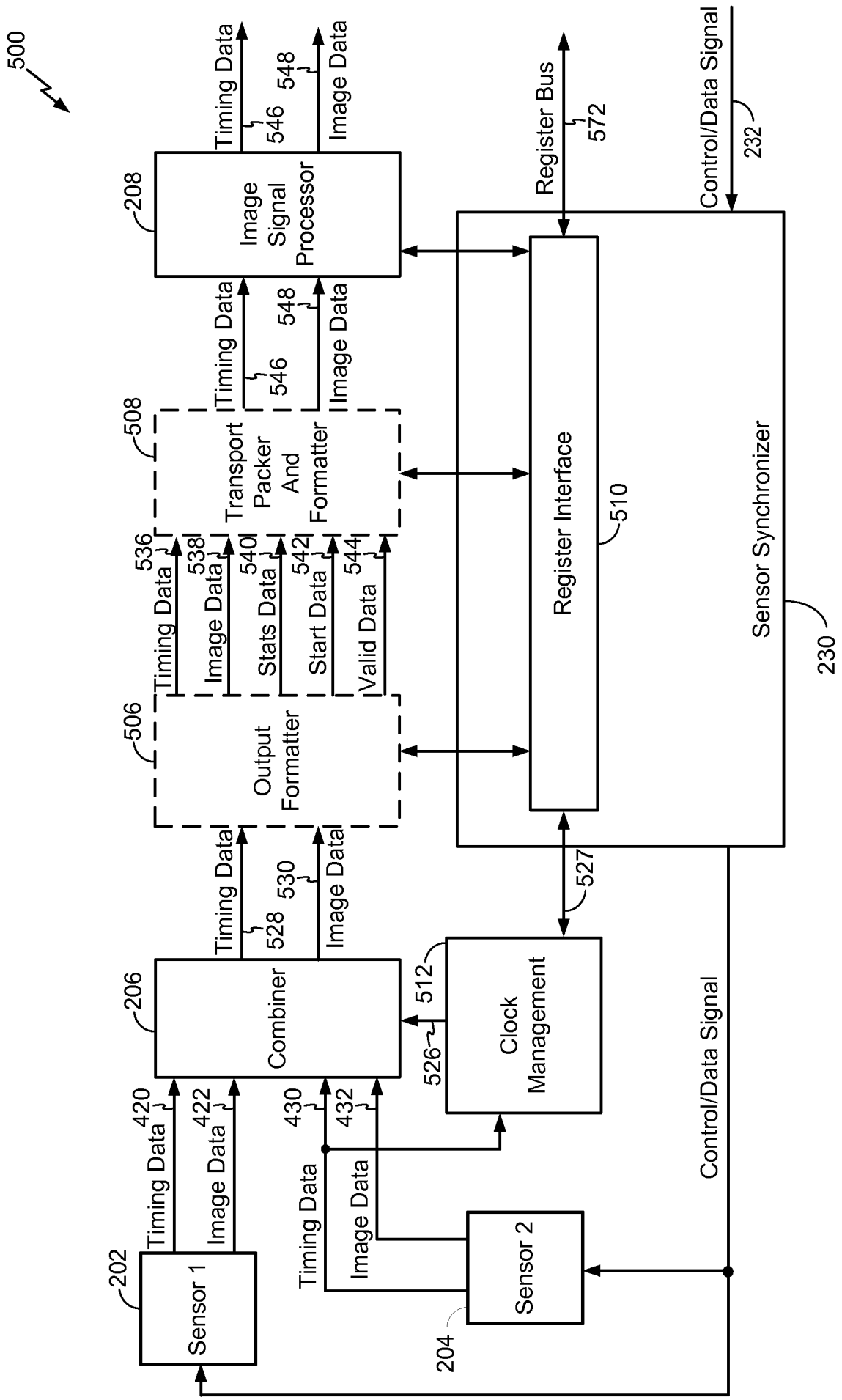
500
Sensor 1
202
Sensor 2
204
Combiner
206
Output Formatter
506
Transport Packer And Formatter
508
Image Signal Processor
208
Clock Management
512
526
527
Register Interface
510
Sensor Synchronizer
230
Control/Data Signal
232
Register Bus
572
Timing Data
420
Image Data
422
430
432
528
530
536
538
540
542
544
546
548
Stats Data
Start Data
Valid Data

FIG. 5

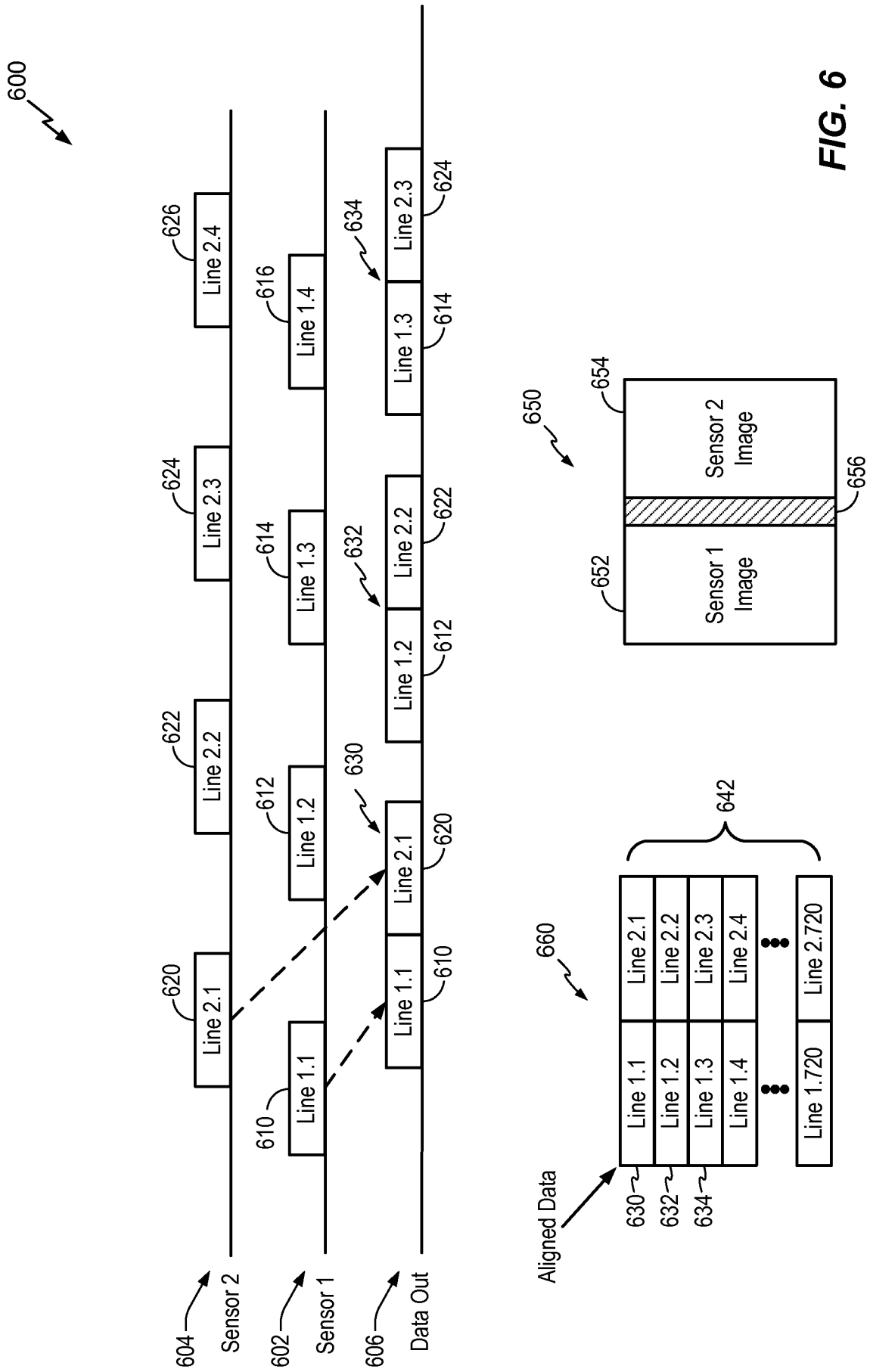
600
604
Sensor 2
602
Sensor 1
606
Data Out
620
Line 2.1
622
Line 2.2
624
Line 2.3
626
Line 2.4
610
Line 1.1
612
Line 1.2
614
Line 1.3
616
Line 1.4
630
Line 2.1
632
Line 2.2
634
Line 2.3
Line 1.1
Line 1.2
Line 1.3
Line 1.4
610
612
614
620
622
624
650
652
Sensor 1 Image
654
Sensor 2 Image
656
660
Aligned Data
630
632
634
642
Line 2.1
Line 2.2
Line 2.3
Line 2.4
Line 2.720
Line 1.1
Line 1.2
Line 1.3
Line 1.4
Line 1.720

FIG. 6

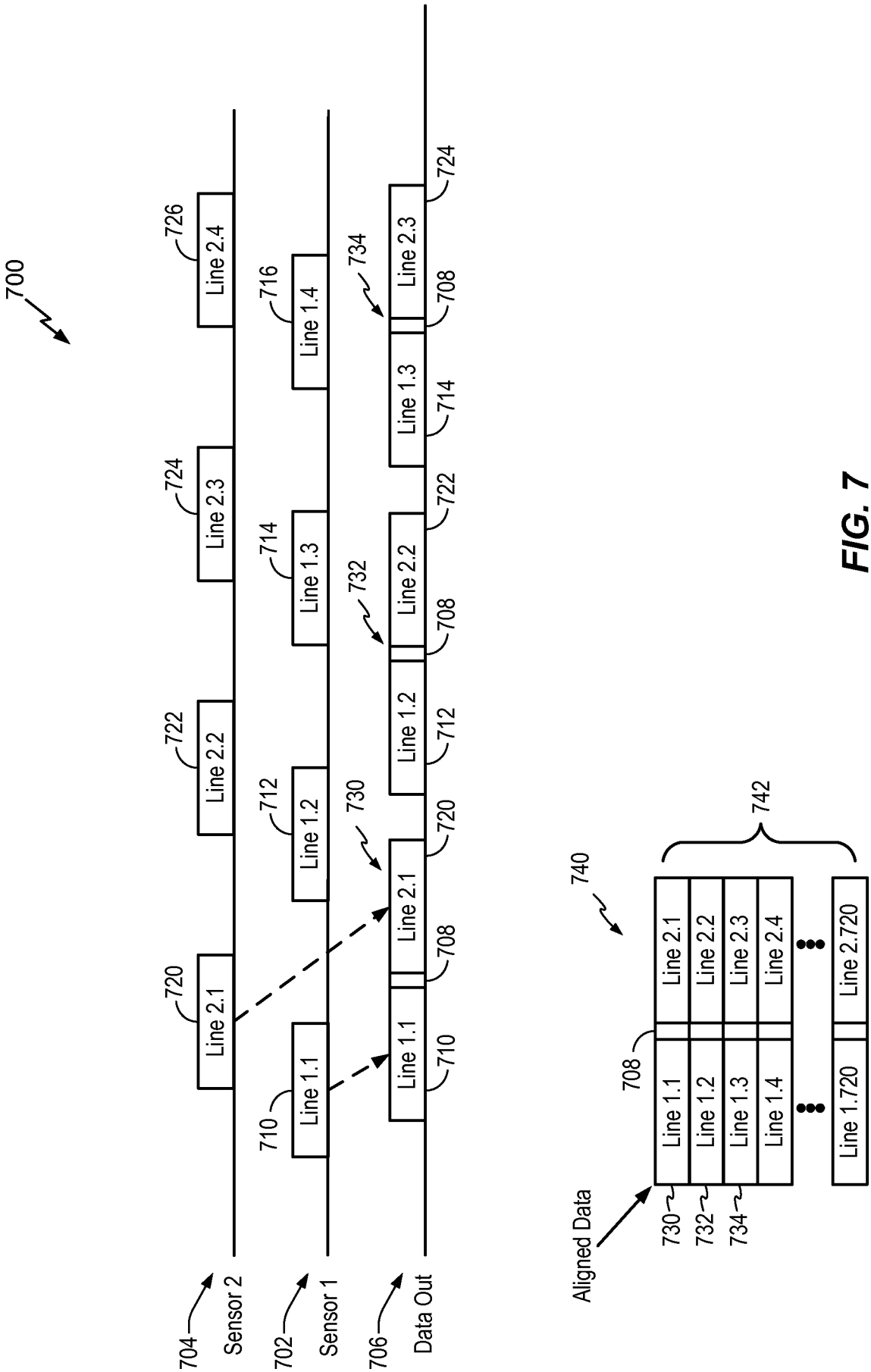
700
Sensor 2
704
Sensor 1
702
Data Out
706
Line 2.1
720
Line 2.2
722
Line 2.3
724
Line 2.4
726
Line 1.1
710
Line 1.2
712
Line 1.3
714
Line 1.4
716
730
732
734
708
Aligned Data
740
742
Line 2.720
Line 1.720

FIG. 7

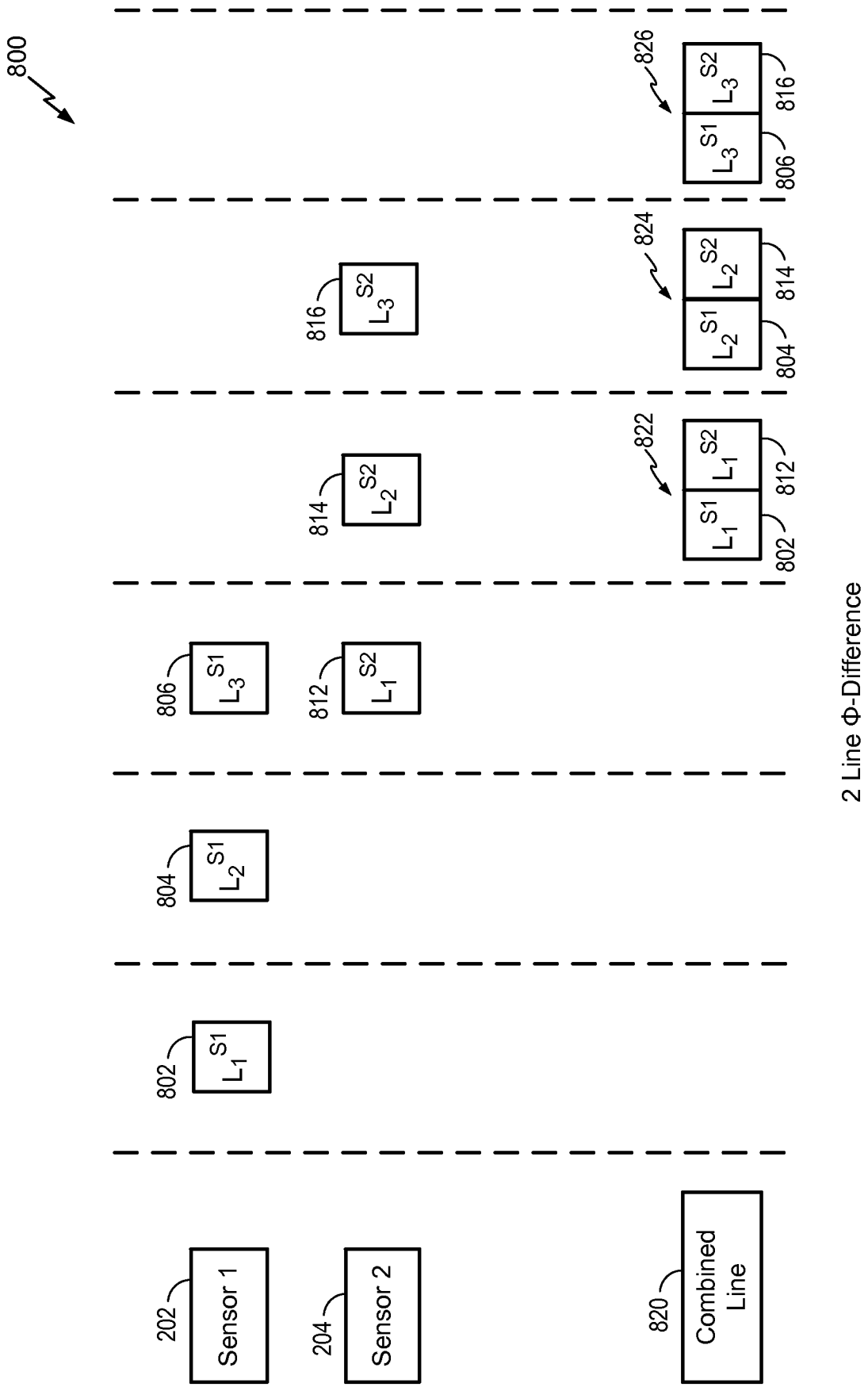
800
826
S2
L3
S1
L3
816
806
824
S2
L2
S1
L2
814
804
822
S2
L1
S1
L1
812
802
816
S2
L3
814
S2
L2
806
S1
L3
812
S2
L1
804
S1
L2
802
S1
L1
202
Sensor 1
204
Sensor 2
820
Combined Line
2 Line Φ-Difference

FIG. 8

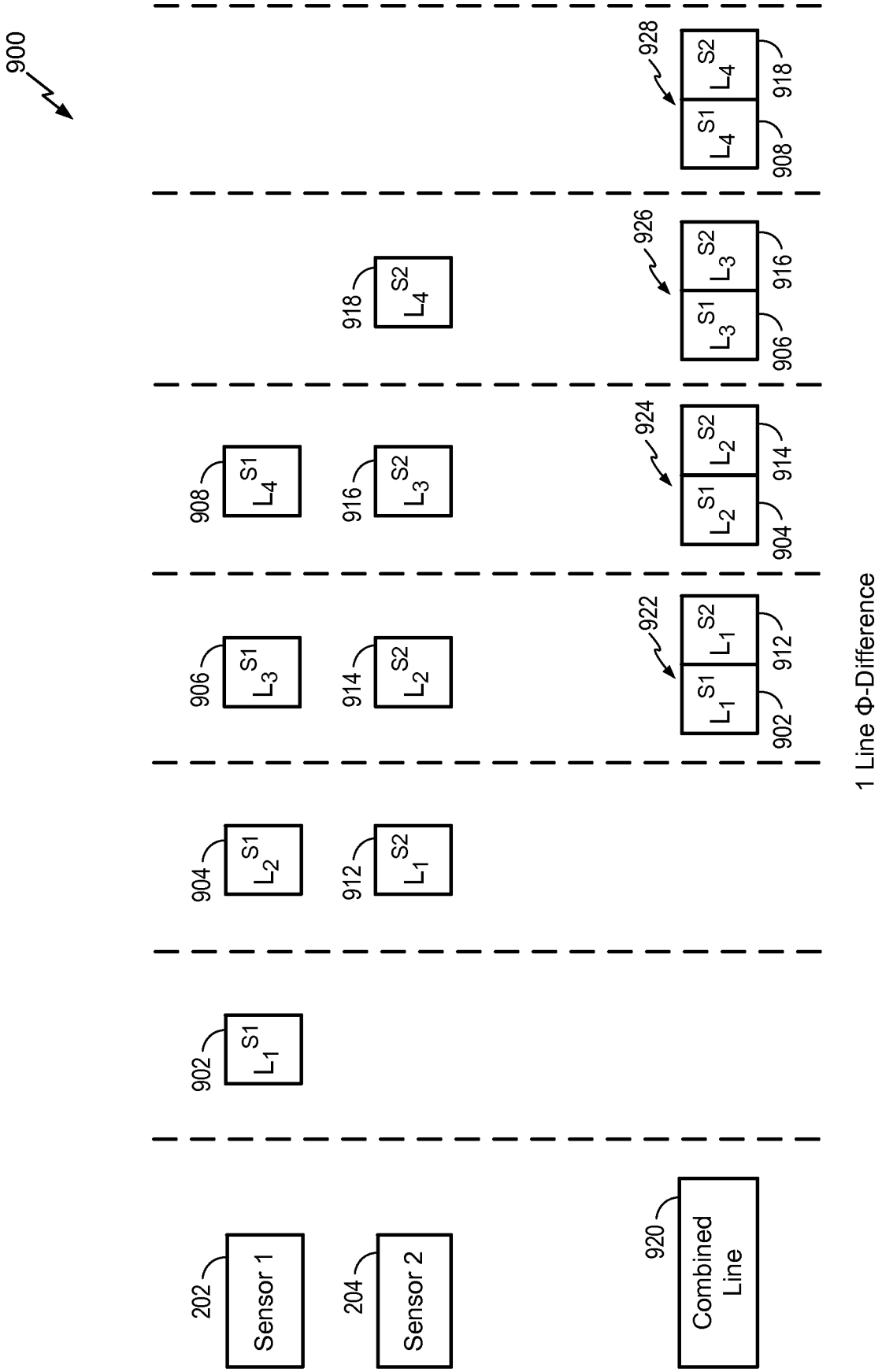
900
202
Sensor 1
204
Sensor 2
920
Combined Line
902
S1 L1
904
S1 L2
906
S1 L3
908
S1 L4
912
S2 L1
914
S2 L2
916
S2 L3
918
S2 L4
922
S1 L1
S2 L1
902
912
924
S1 L2
S2 L2
904
914
926
S1 L3
S2 L3
906
916
928
S1 L4
S2 L4
908
918
1 Line Φ-Difference

FIG. 9

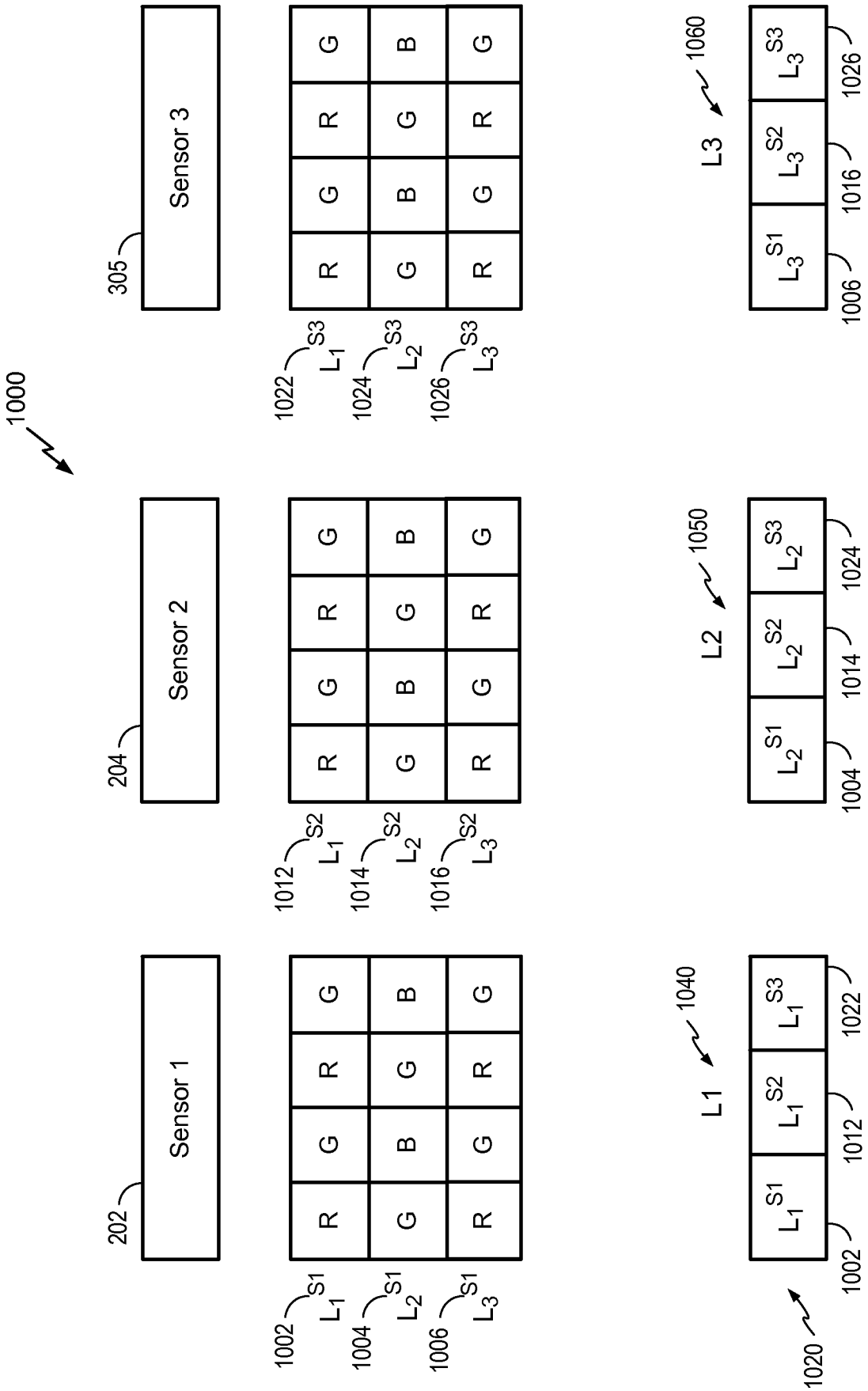
1000
202
Sensor 1
204
Sensor 2
305
Sensor 3
1002 S1 L1
1004 S1 L2
1006 S1 L3
1012 S2 L1
1014 S2 L2
1016 S2 L3
1022 S3 L1
1024 S3 L2
1026 S3 L3
R G R G
G B G B
R G R G
1020
L1
1040
L2
1050
L3
1060
1002 S1 L1 1012 S2 L1 1022 S3 L1
1004 S1 L2 1014 S2 L2 1024 S3 L2
1006 S1 L3 1016 S2 L3 1026 S3 L3

FIG. 10

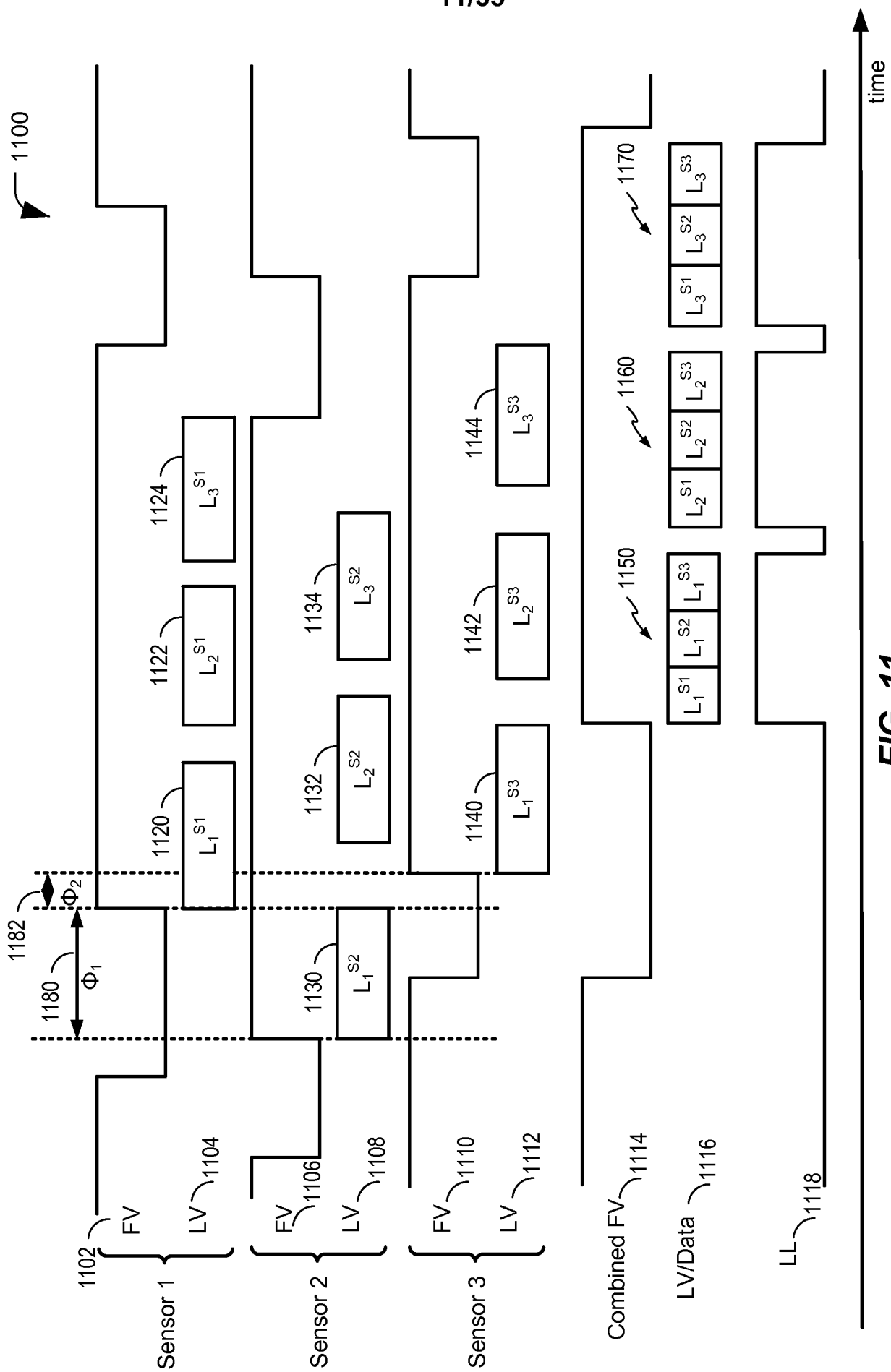
1100
1102
FV
LV
1104
Sensor 1
FV
1106
LV
1108
Sensor 2
FV
1110
LV
1112
Sensor 3
Combined FV
1114
LV/Data
1116
LL
1118
1120
L_1^{S1}
1122
L_2^{S1}
1124
L_3^{S1}
1130
L_1^{S2}
1132
L_2^{S2}
1134
L_3^{S2}
1140
L_1^{S3}
1142
L_2^{S3}
1144
L_3^{S3}
1150
L_1^{S1} L_1^{S2} L_1^{S3}
1160
L_2^{S1} L_2^{S2} L_2^{S3}
1170
L_3^{S1} L_3^{S2} L_3^{S3}
1180
Φ_1
1182
Φ_2
time

FIG. 11

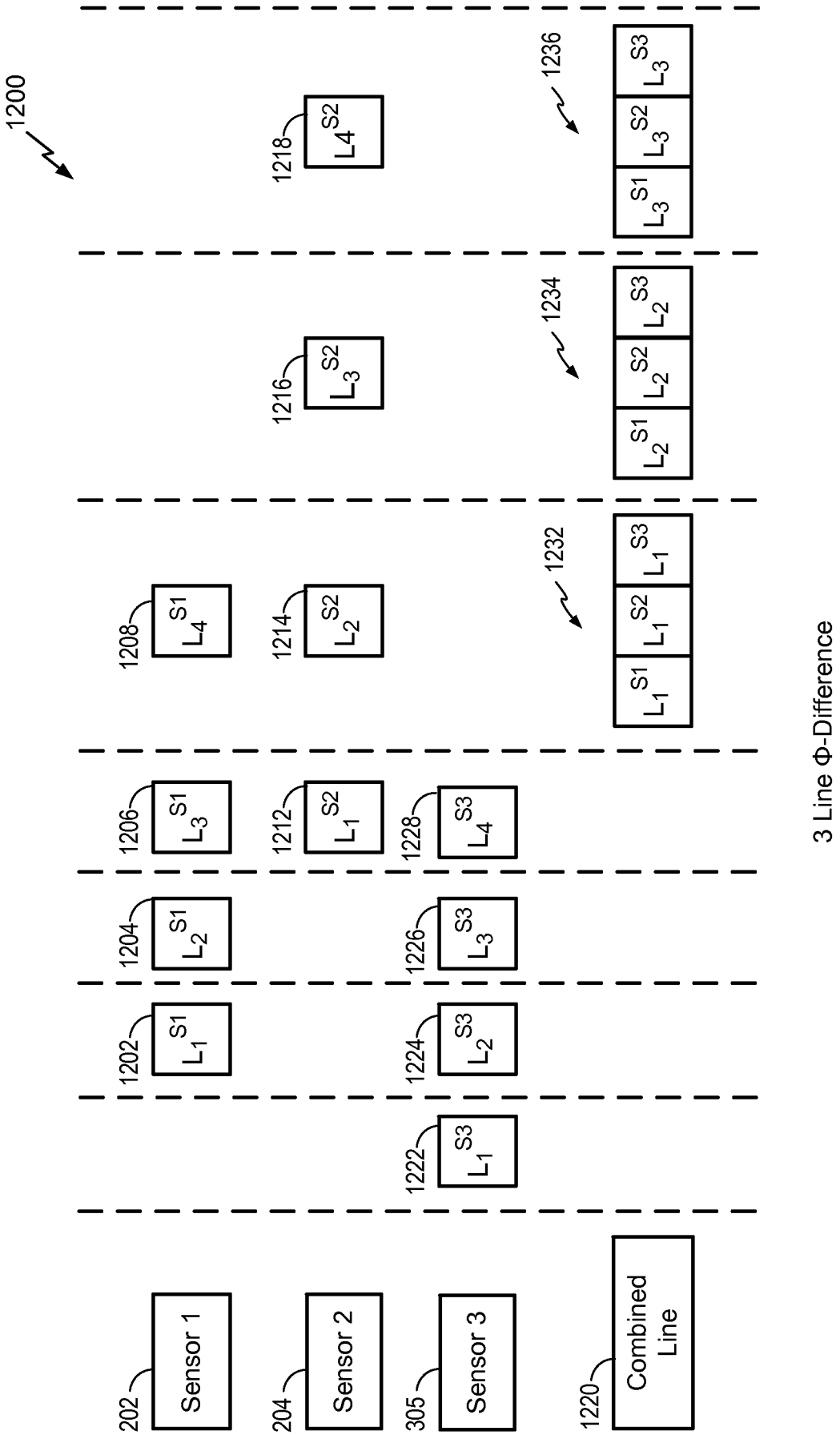
1200
202
Sensor 1
204
Sensor 2
305
Sensor 3
1220
Combined Line
1202
S1 L1
1204
S1 L2
1206
S1 L3
1208
S1 L4
1222
S3 L1
1224
S3 L2
1226
S3 L3
1228
S3 L4
1212
S2 L1
1214
S2 L2
1216
S2 L3
1218
S2 L4
1232
S1 L1 S2 L1 S3 L1
1234
S1 L2 S2 L2 S3 L2
1236
S1 L3 S2 L3 S3 L3
3 Line Φ-Difference

FIG. 12

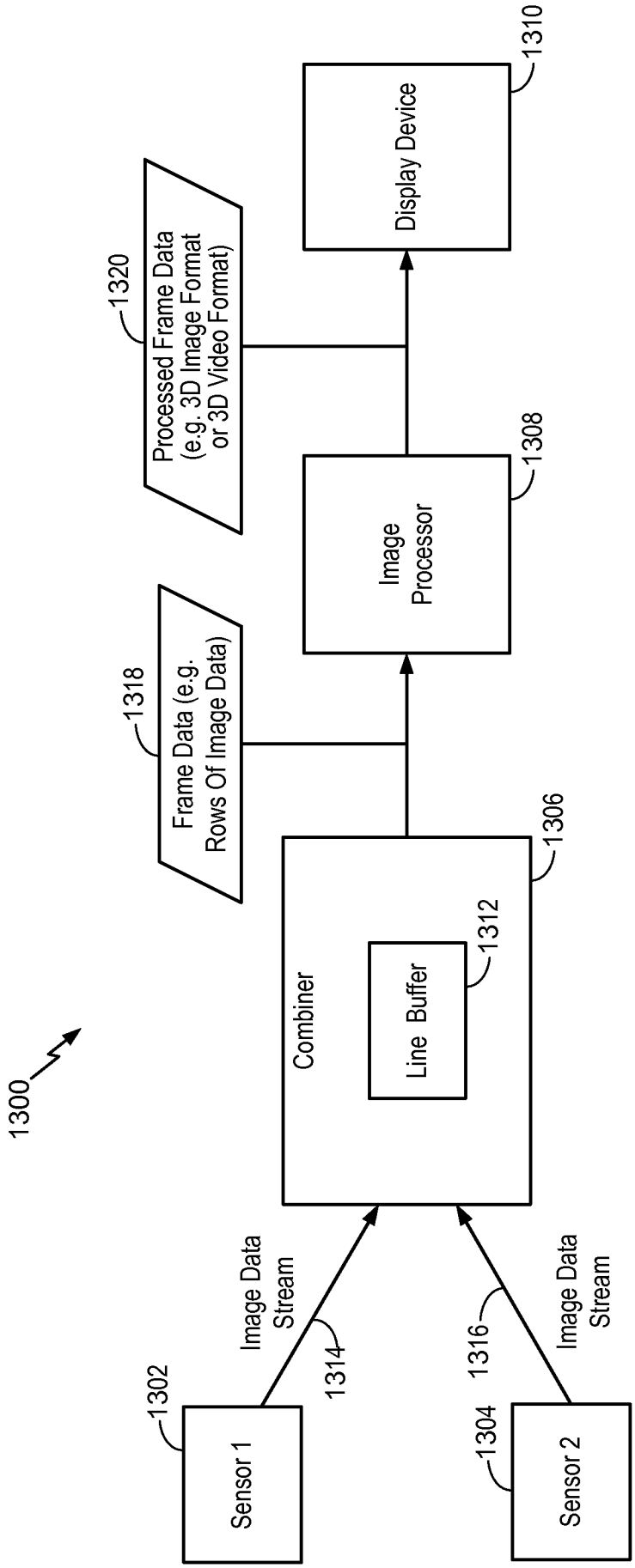
1300
Sensor 1
1302
Image Data Stream
1314
Sensor 2
1304
1316
Image Data Stream
Combiner
Line Buffer
1312
1306
Frame Data (e.g. Rows Of Image Data)
1318
Image Processor
1308
Processed Frame Data (e.g. 3D Image Format or 3D Video Format)
1320
Display Device
1310

FIG. 13

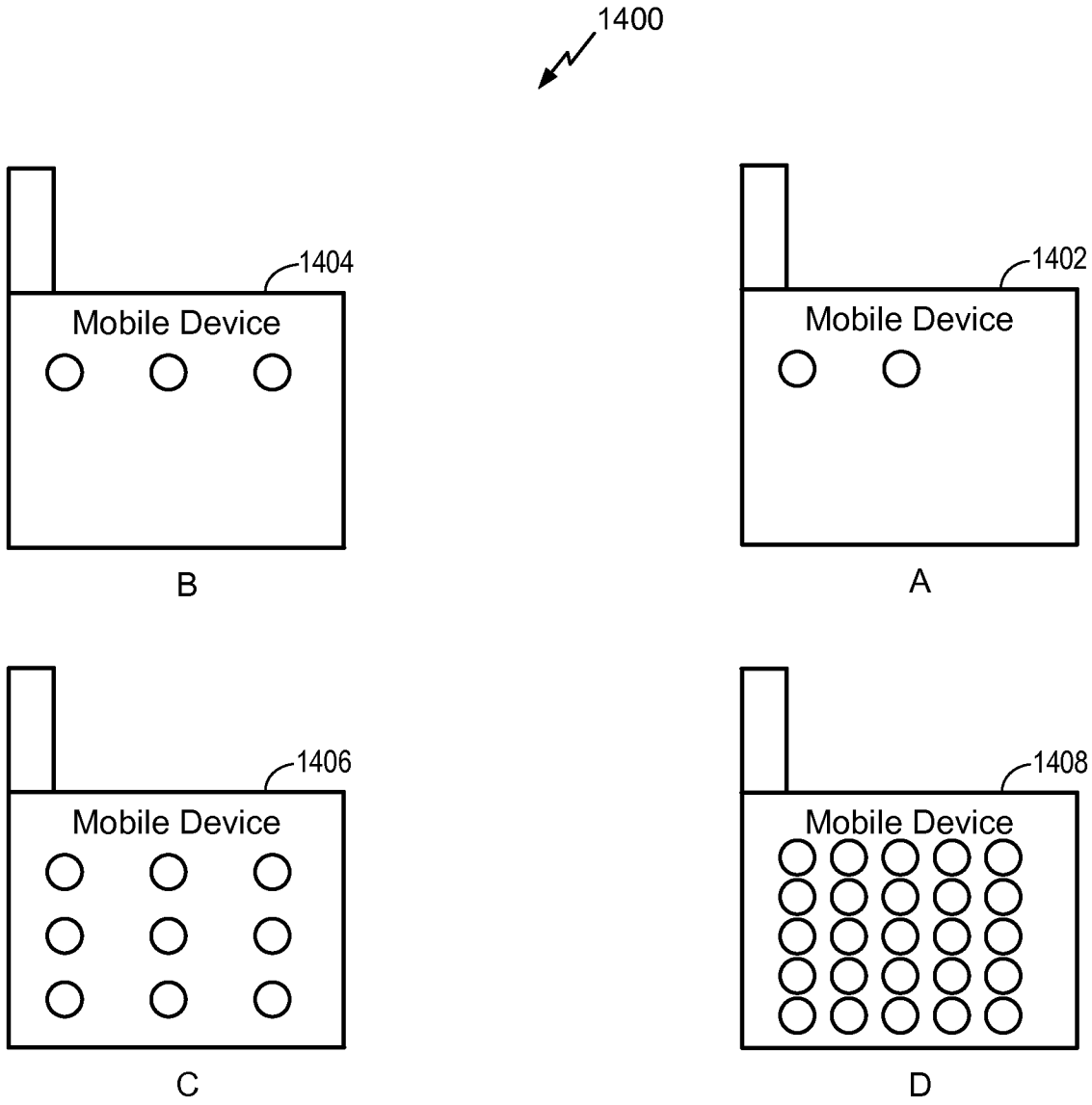
1400
1404
Mobile Device
B
1402
Mobile Device
A
1406
Mobile Device
C
1408
Mobile Device
D

FIG. 14

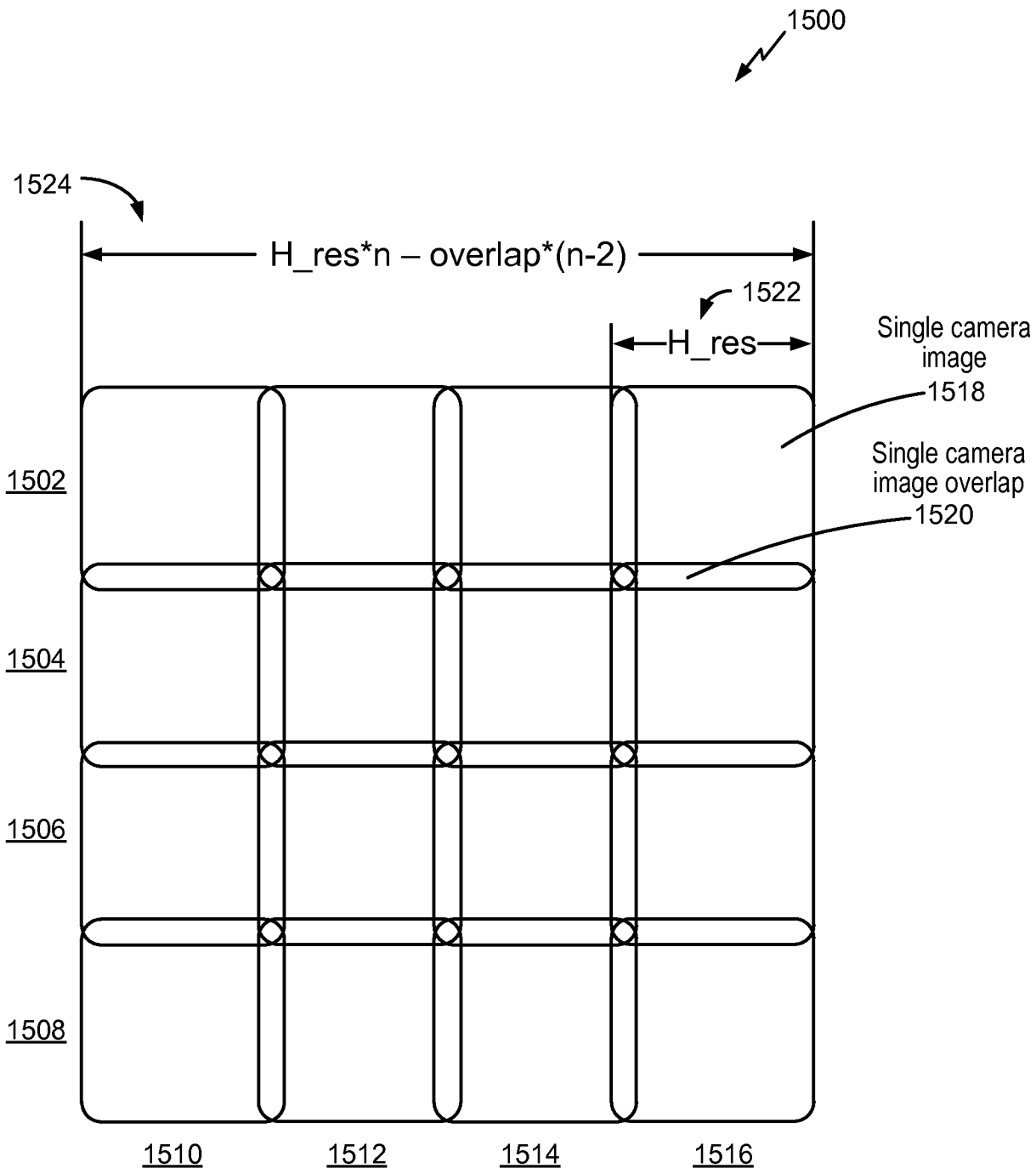
1500
1524
H_res*n – overlap*(n-2)
1522
H_res
Single camera image
1518
Single camera image overlap
1520
1502
1504
1506
1508
1510
1512
1514
1516

FIG. 15

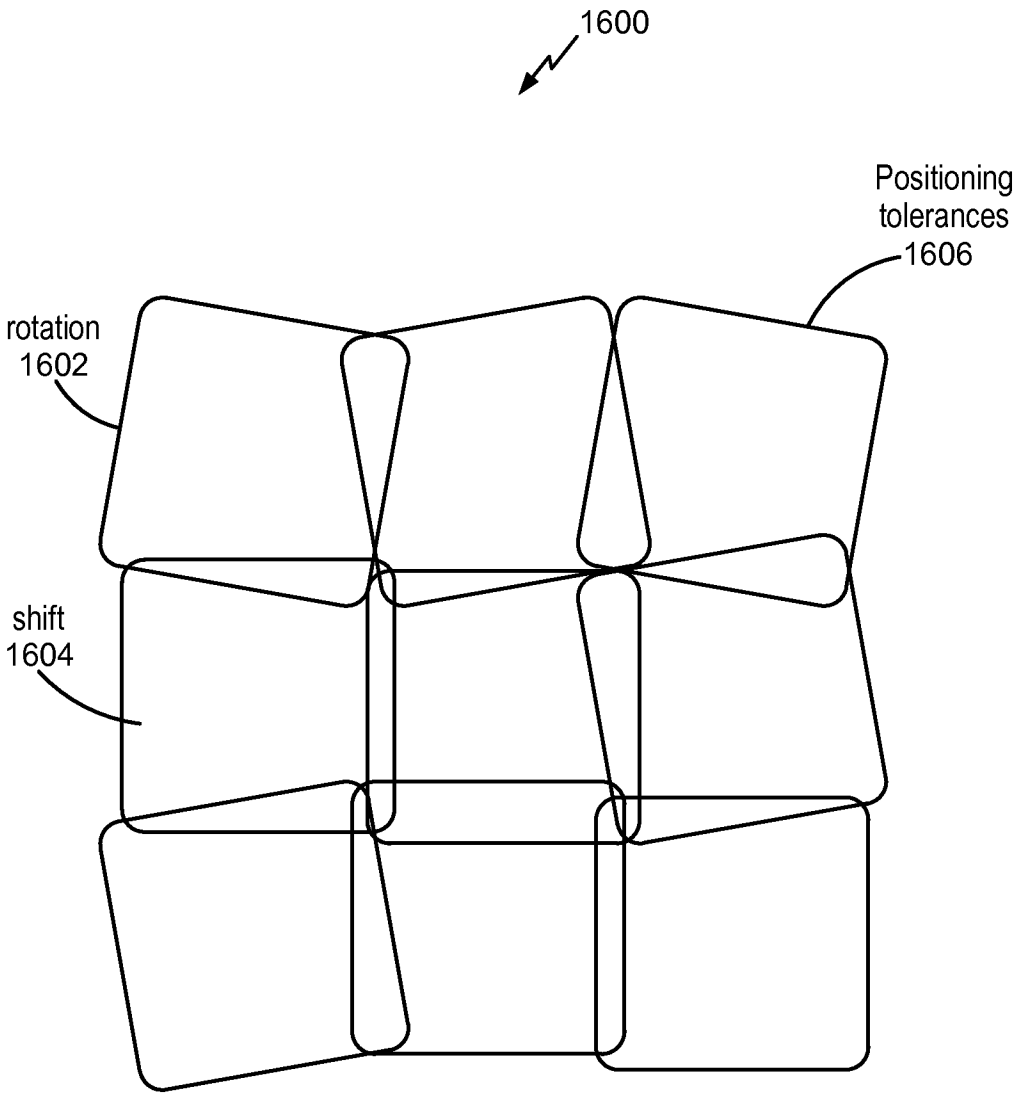
1600
Positioning tolerances 1606
rotation 1602
shift 1604

FIG. 16

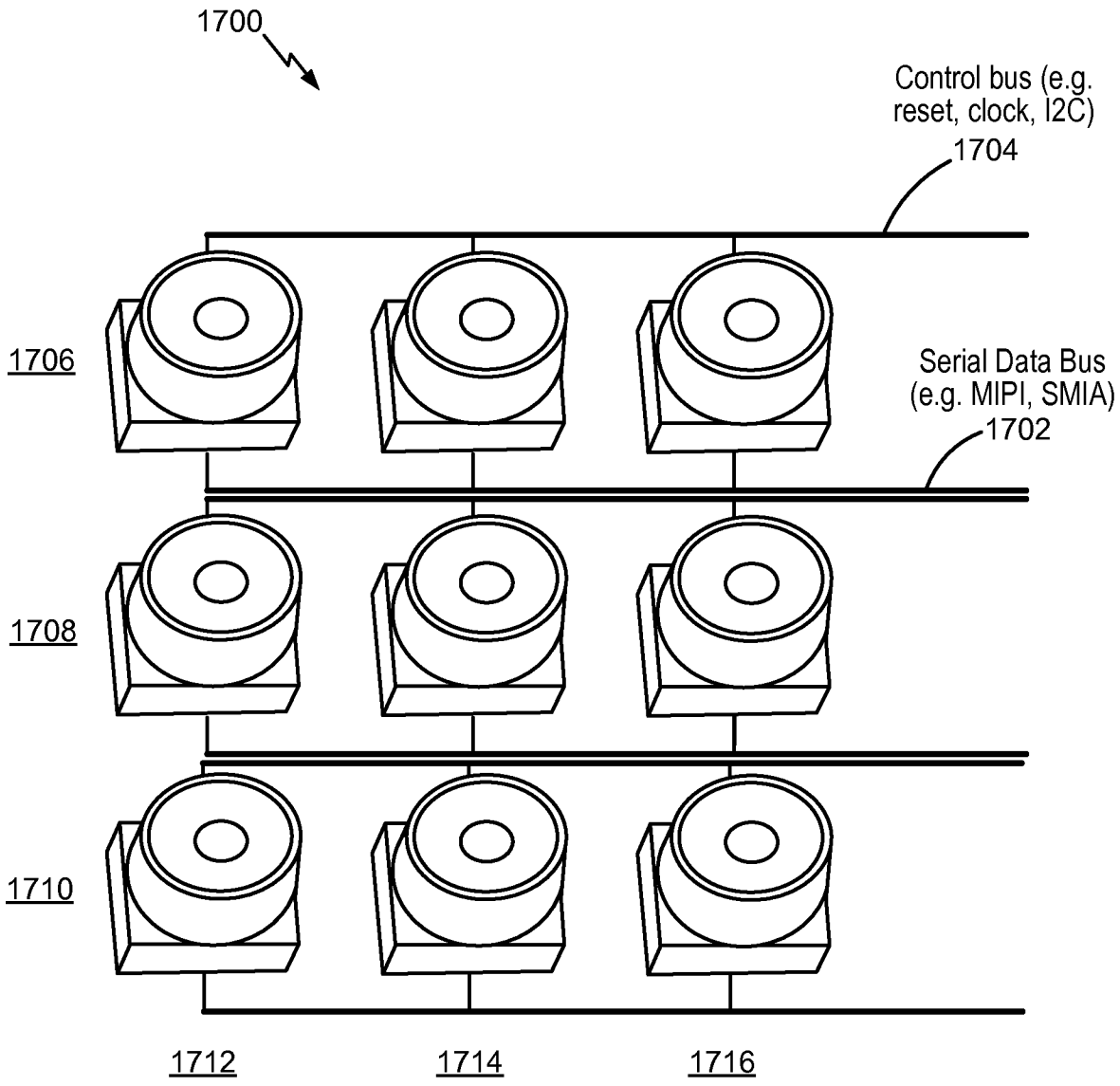
1700
Control bus (e.g. reset, clock, I2C)
1704
1706
Serial Data Bus (e.g. MIPI, SMIA)
1702
1708
1710
1712
1714
1716

FIG. 17

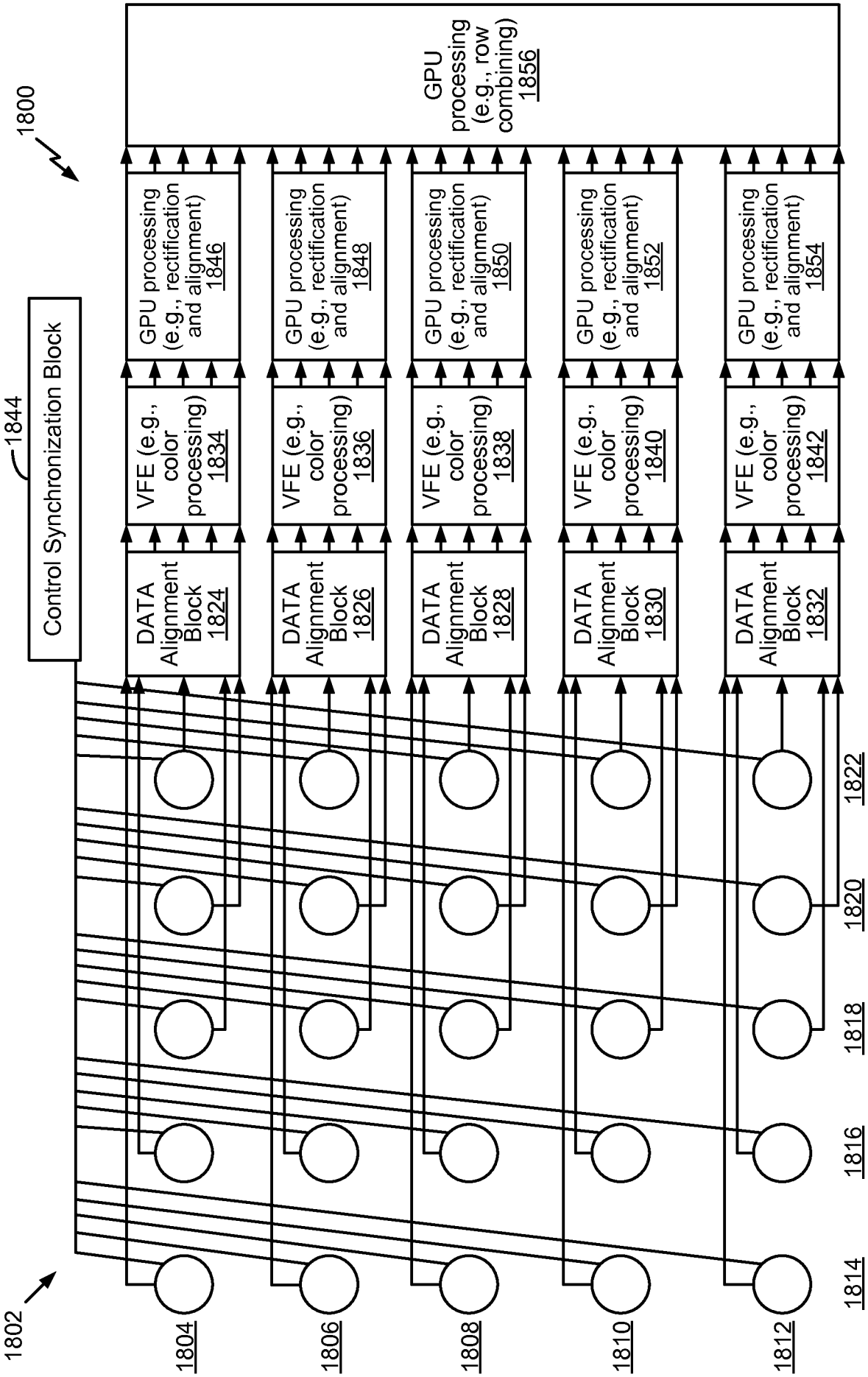
1800
GPU processing (e.g., row combining) 1856
GPU processing (e.g., rectification and alignment) 1846
GPU processing (e.g., rectification and alignment) 1848
GPU processing (e.g., rectification and alignment) 1850
GPU processing (e.g., rectification and alignment) 1852
GPU processing (e.g., rectification and alignment) 1854
1844
Control Synchronization Block
VFE (e.g., color processing) 1834
VFE (e.g., color processing) 1836
VFE (e.g., color processing) 1838
VFE (e.g., color processing) 1840
VFE (e.g., color processing) 1842
DATA Alignment Block 1824
DATA Alignment Block 1826
DATA Alignment Block 1828
DATA Alignment Block 1830
DATA Alignment Block 1832
1822
1820
1818
1816
1814
1802
1804
1806
1808
1810
1812

FIG. 18

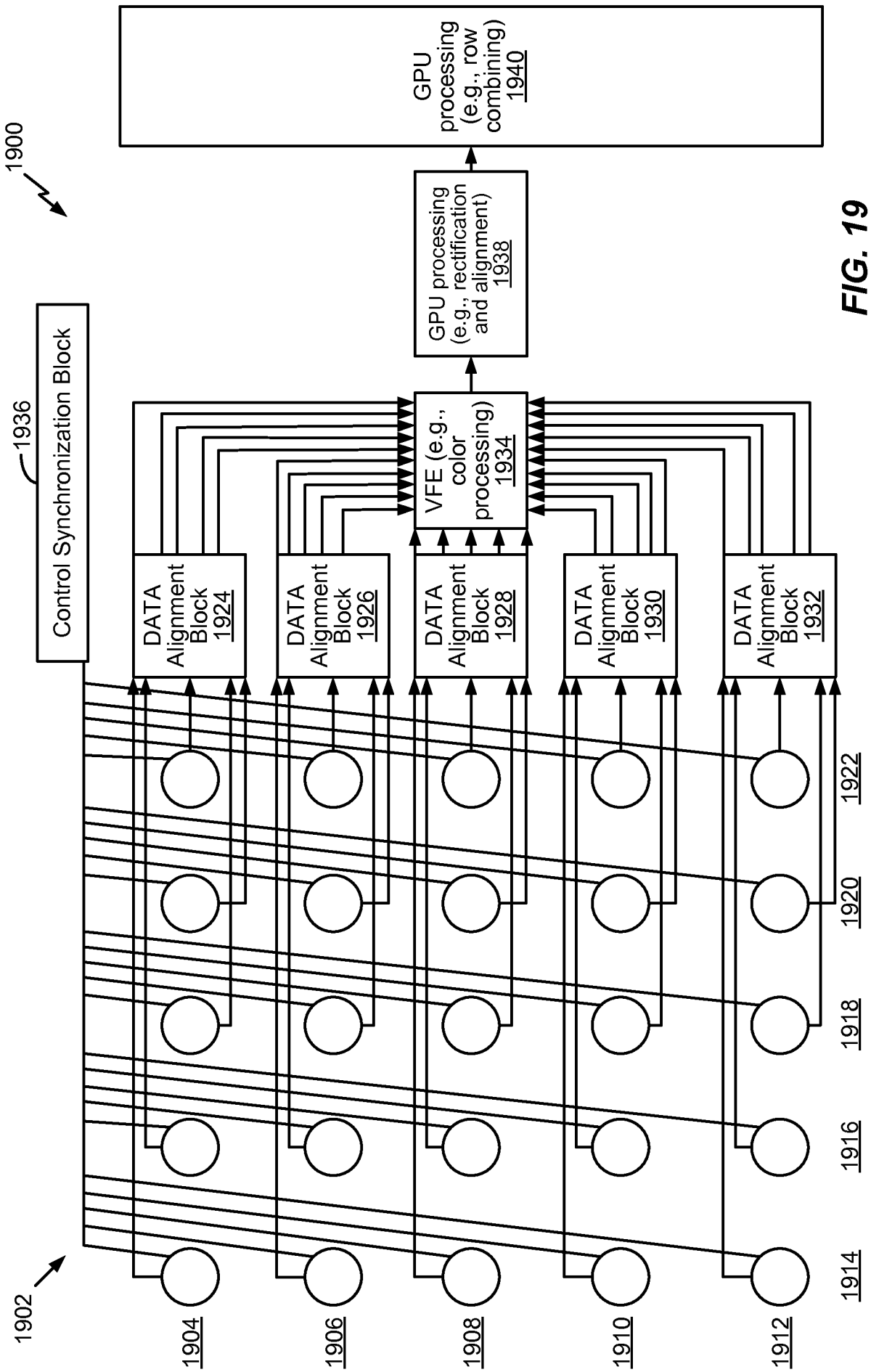
1900
GPU processing (e.g., row combining) 1940
GPU processing (e.g., rectification and alignment) 1938
VFE (e.g., color processing) 1934
Control Synchronization Block
1936
DATA Alignment Block 1924
DATA Alignment Block 1926
DATA Alignment Block 1928
DATA Alignment Block 1930
DATA Alignment Block 1932
1922
1920
1918
1916
1914
1902
1904
1906
1908
1910
1912

FIG. 19

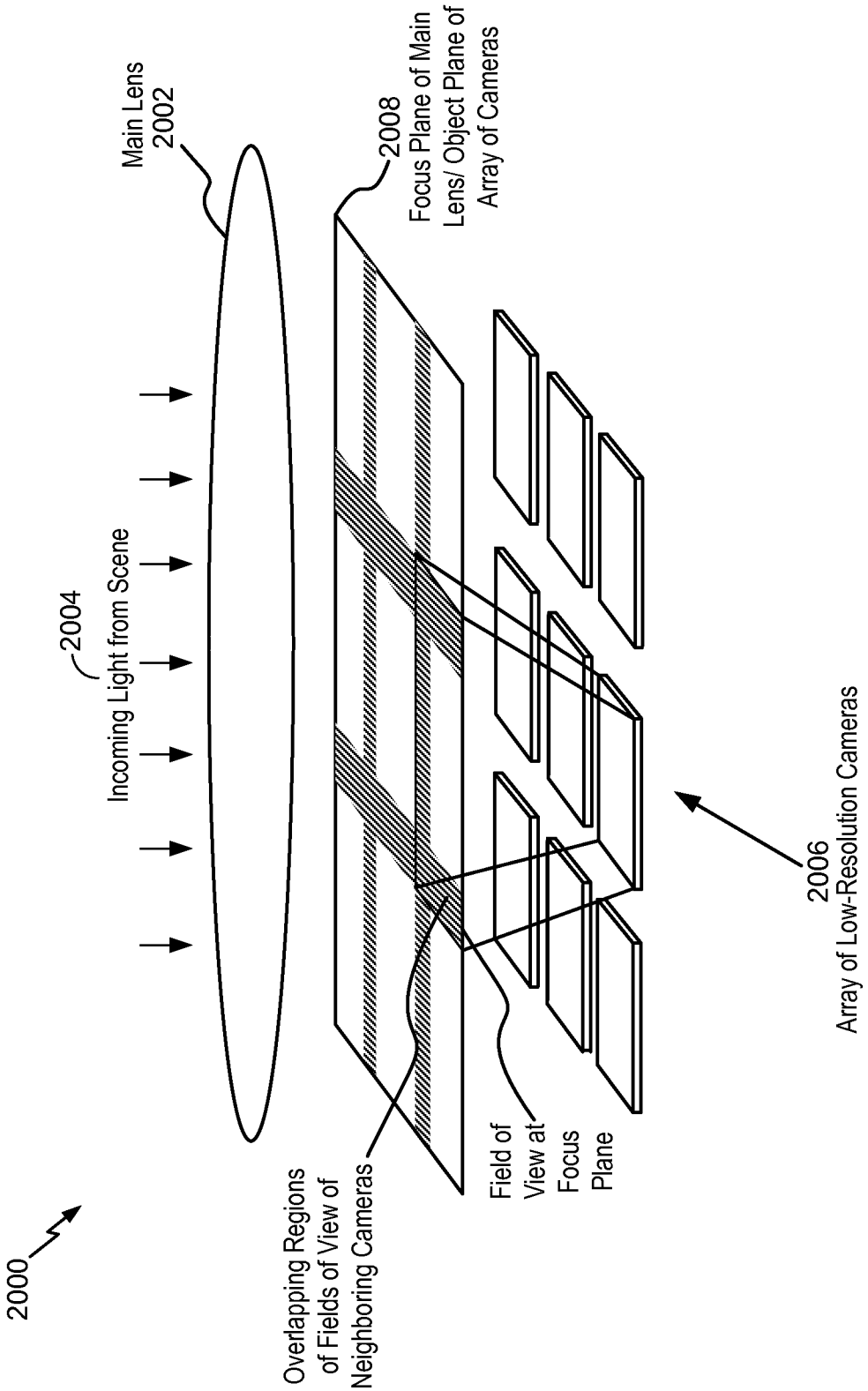
2000
2004
Incoming Light from Scene
Main Lens
2002
2008
Focus Plane of Main
Lens/ Object Plane of
Array of Cameras
Overlapping Regions
of Fields of View of
Neighboring Cameras
Field of
View at
Focus
Plane
2006
Array of Low-Resolution Cameras

FIG. 20

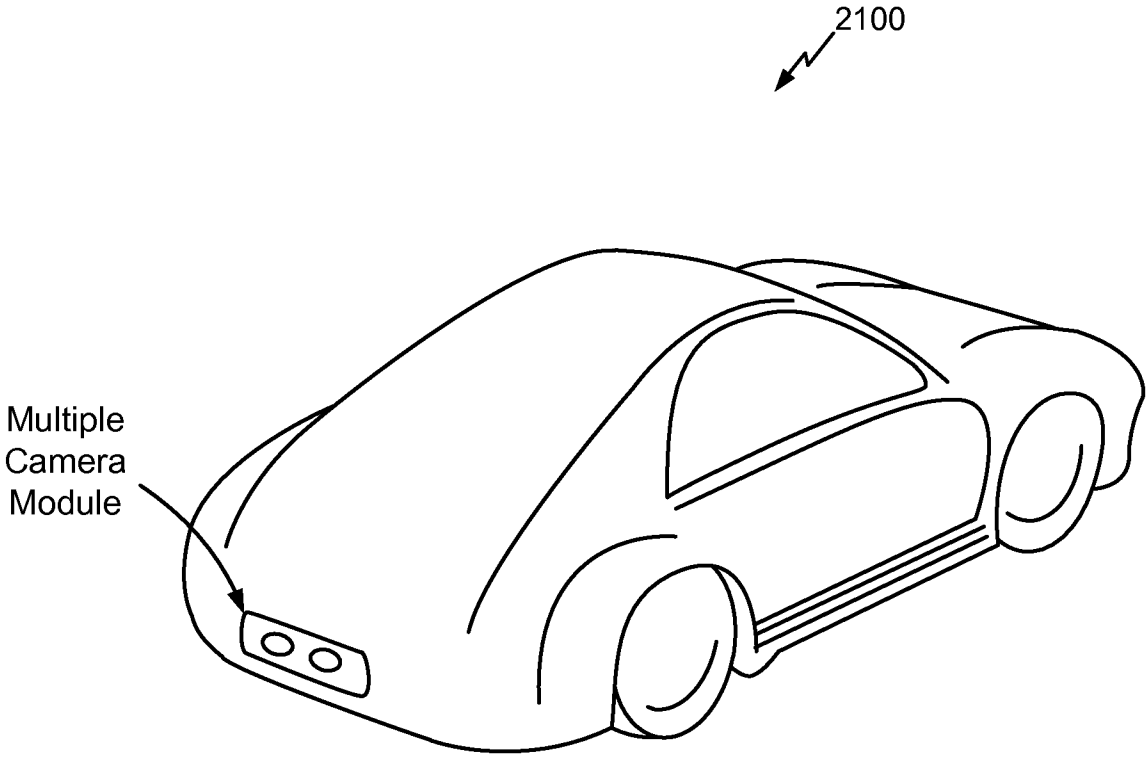

FIG. 21

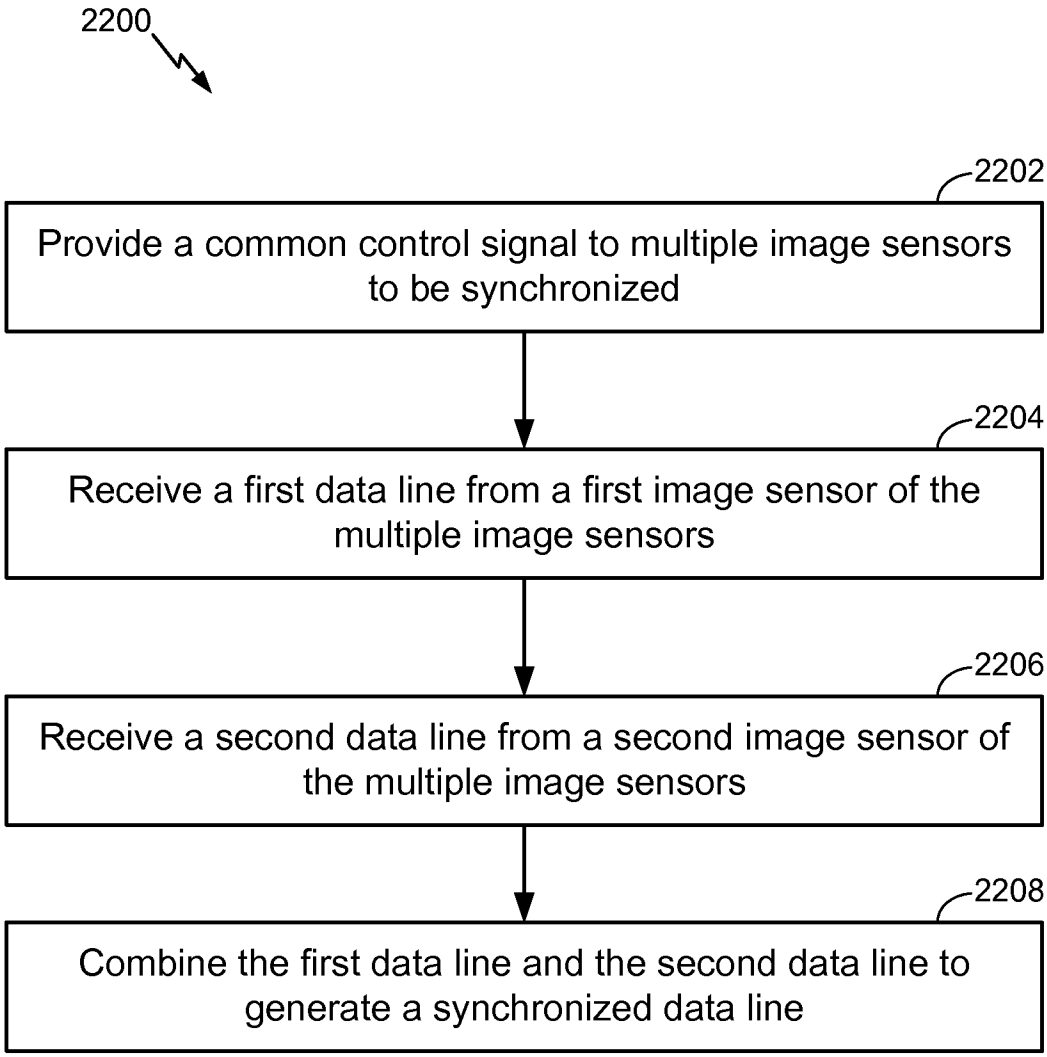
2200
2202
Provide a common control signal to multiple image sensors to be synchronized
2204
Receive a first data line from a first image sensor of the multiple image sensors
2206
Receive a second data line from a second image sensor of the multiple image sensors
2208
Combine the first data line and the second data line to generate a synchronized data line

FIG. 22

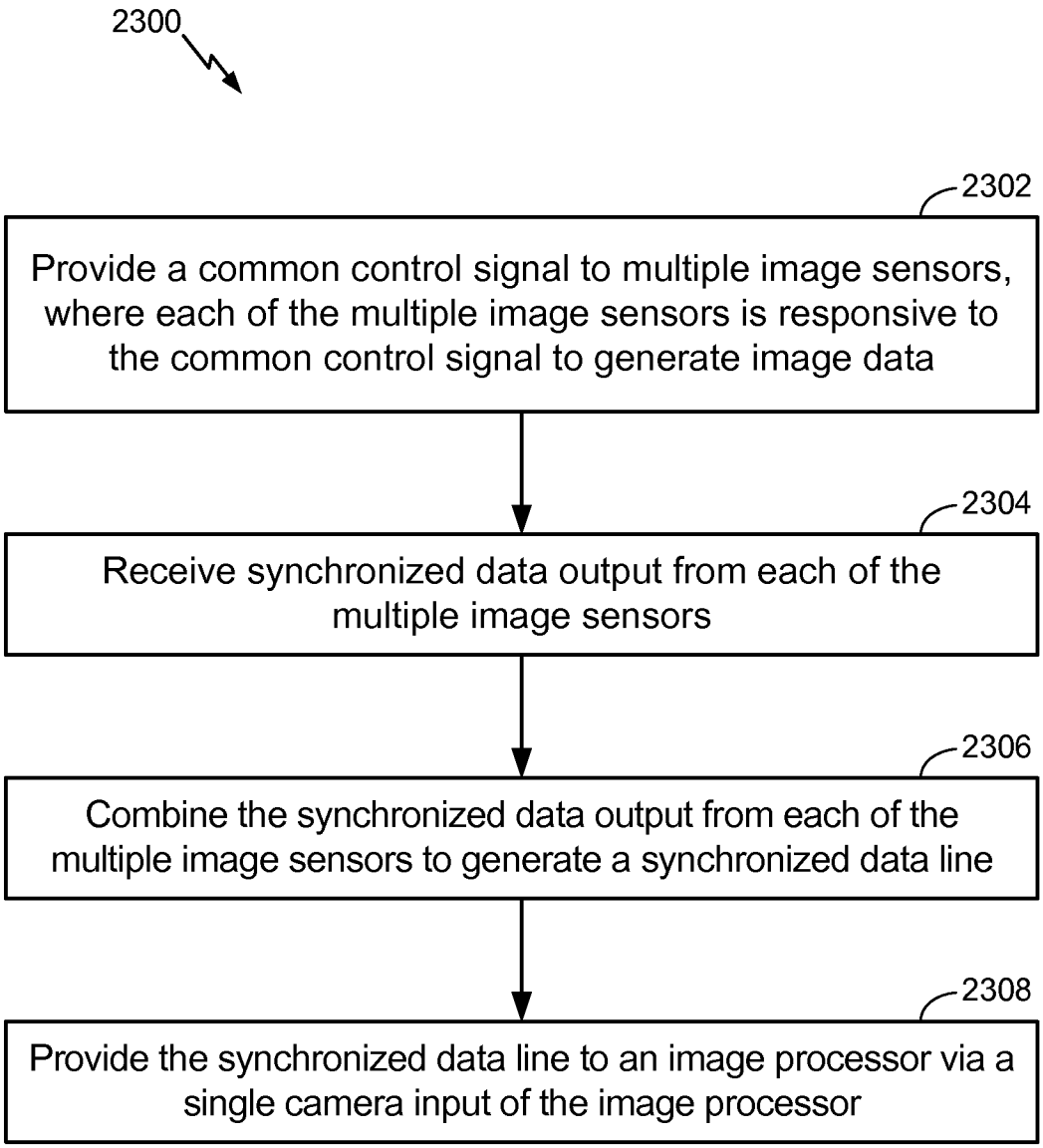
2300
2302
Provide a common control signal to multiple image sensors, where each of the multiple image sensors is responsive to the common control signal to generate image data
2304
Receive synchronized data output from each of the multiple image sensors
2306
Combine the synchronized data output from each of the multiple image sensors to generate a synchronized data line
2308
Provide the synchronized data line to an image processor via a single camera input of the image processor

FIG. 23

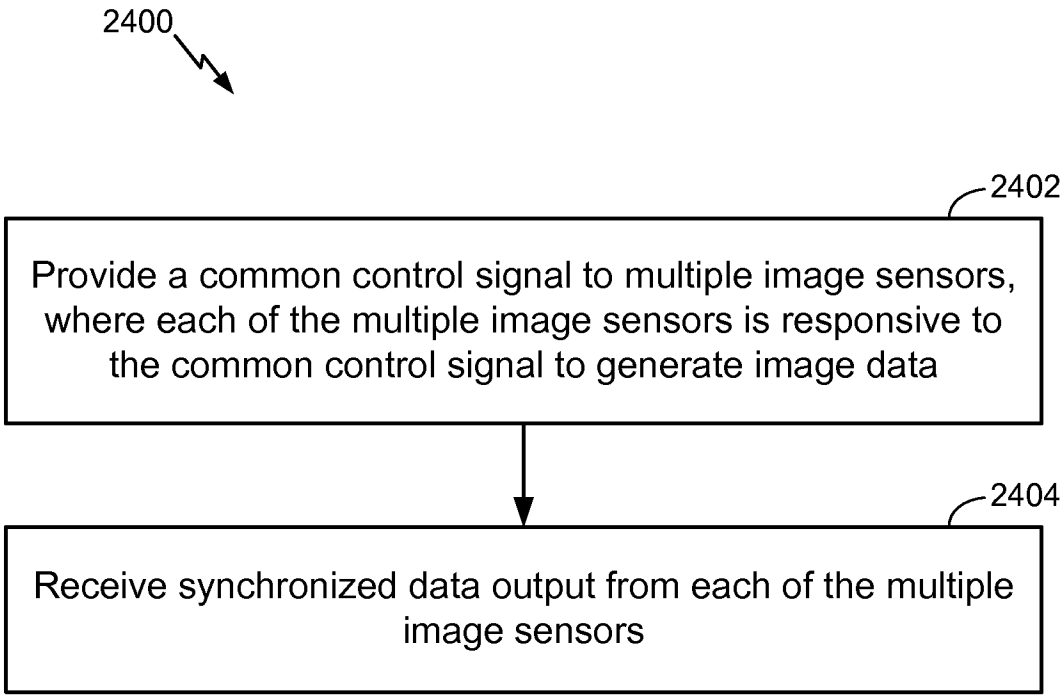
2400
2402
Provide a common control signal to multiple image sensors, where each of the multiple image sensors is responsive to the common control signal to generate image data
2404
Receive synchronized data output from each of the multiple image sensors

FIG. 24

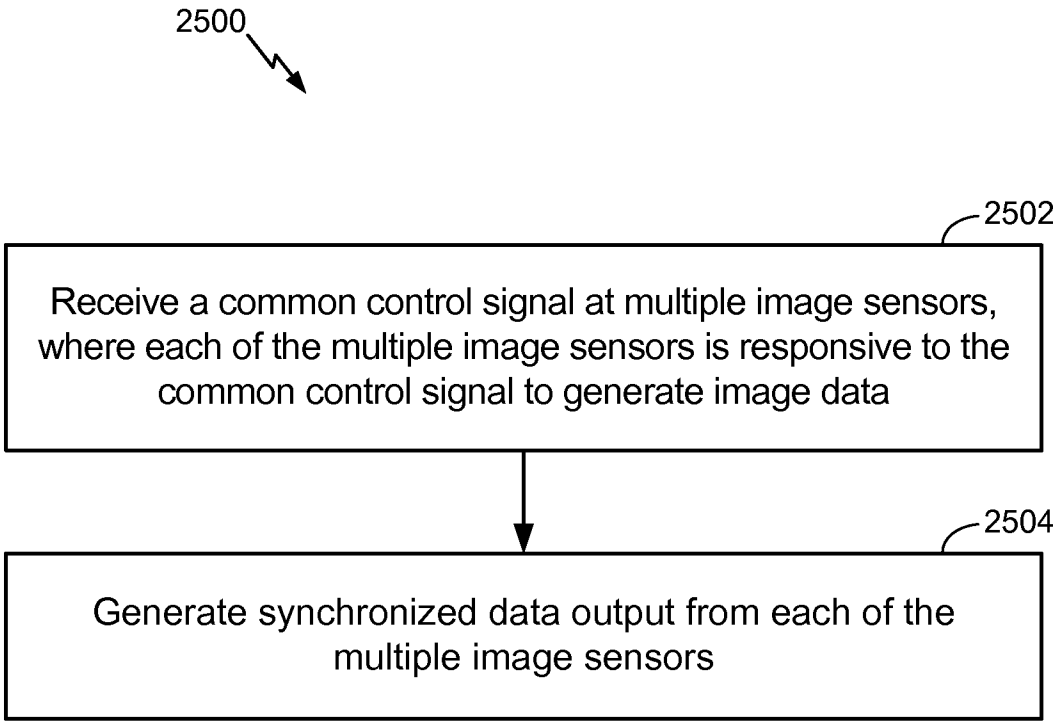
2500
2502
Receive a common control signal at multiple image sensors, where each of the multiple image sensors is responsive to the common control signal to generate image data
2504
Generate synchronized data output from each of the multiple image sensors

FIG. 25

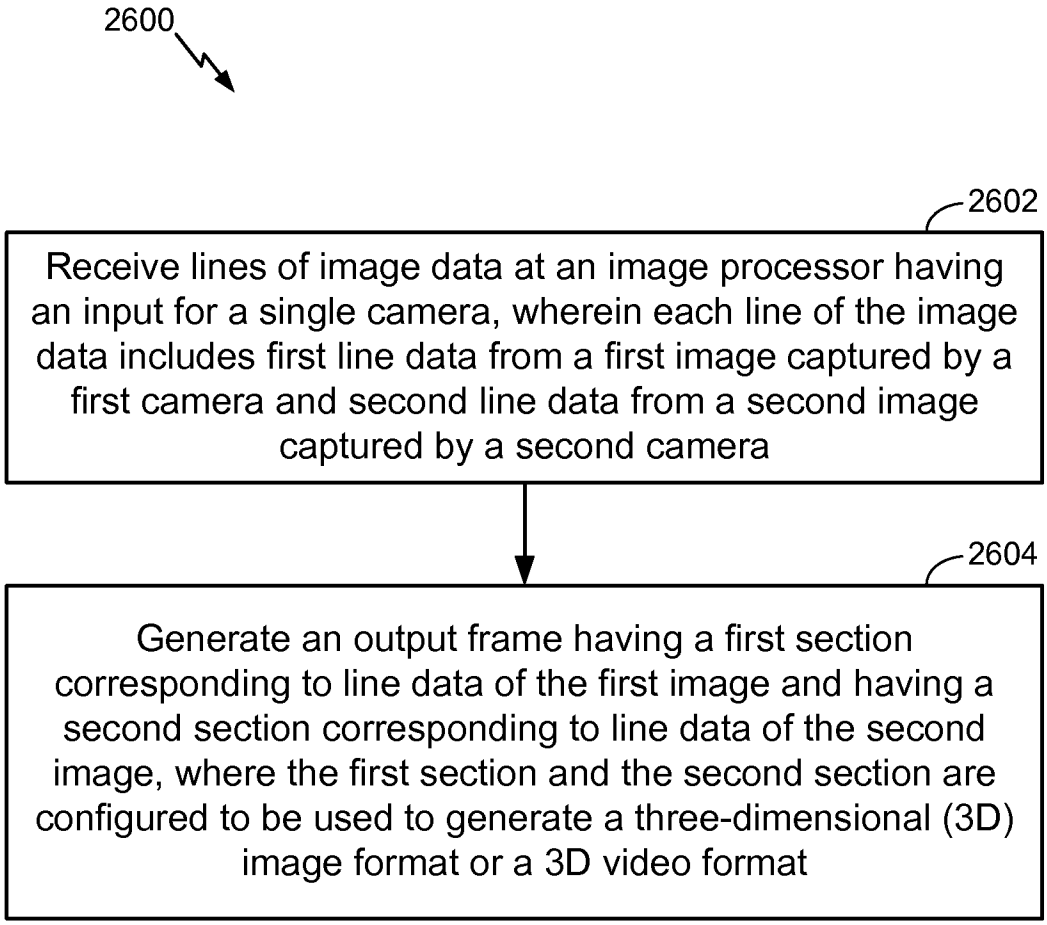
2600
2602
Receive lines of image data at an image processor having an input for a single camera, wherein each line of the image data includes first line data from a first image captured by a first camera and second line data from a second image captured by a second camera
2604
Generate an output frame having a first section corresponding to line data of the first image and having a second section corresponding to line data of the second image, where the first section and the second section are configured to be used to generate a three-dimensional (3D) image format or a 3D video format

FIG. 26

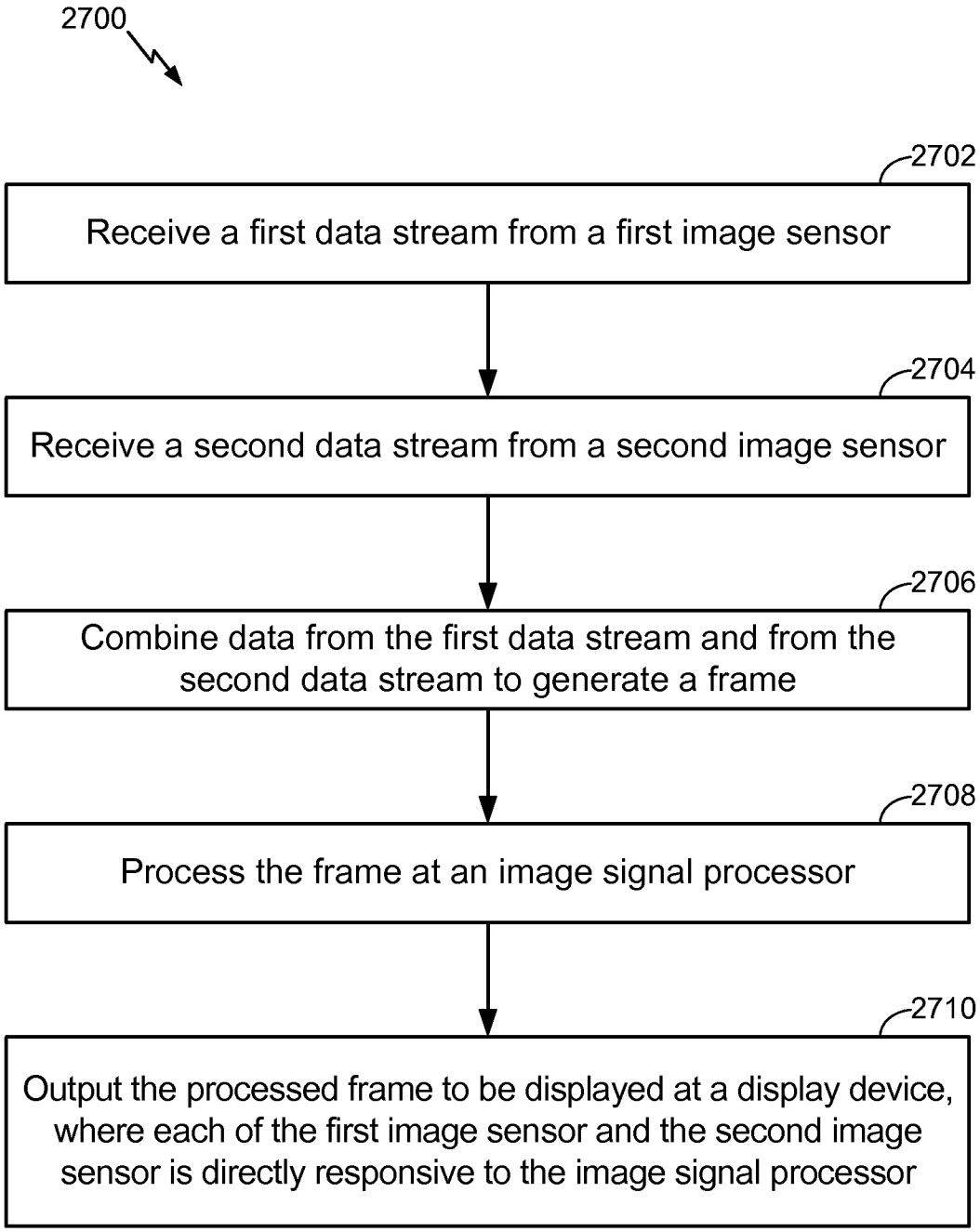
2700
2702
Receive a first data stream from a first image sensor
2704
Receive a second data stream from a second image sensor
2706
Combine data from the first data stream and from the second data stream to generate a frame
2708
Process the frame at an image signal processor
2710
Output the processed frame to be displayed at a display device, where each of the first image sensor and the second image sensor is directly responsive to the image signal processor

FIG. 27

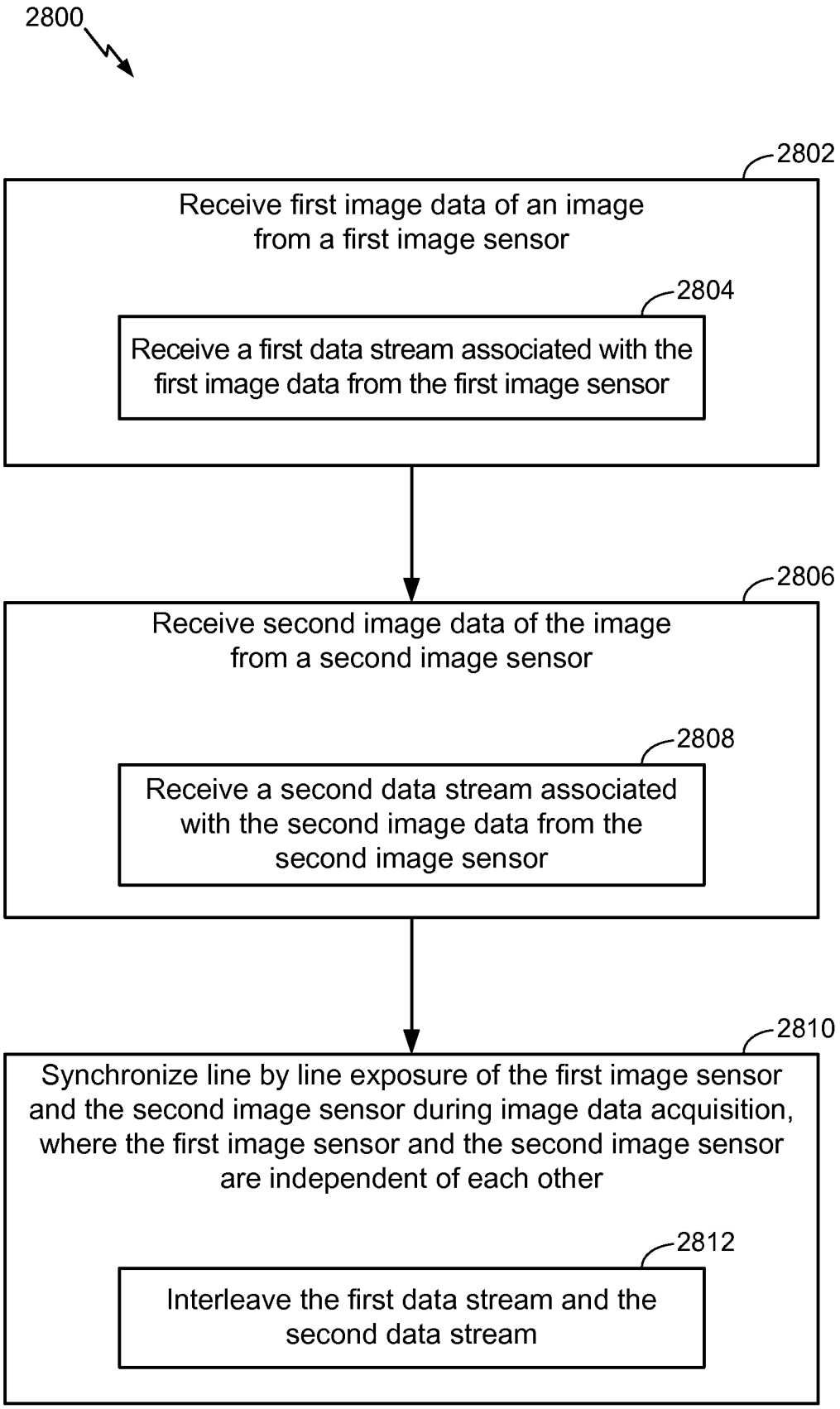
2800
2802
Receive first image data of an image from a first image sensor
2804
Receive a first data stream associated with the first image data from the first image sensor
2806
Receive second image data of the image from a second image sensor
2808
Receive a second data stream associated with the second image data from the second image sensor
2810
Synchronize line by line exposure of the first image sensor and the second image sensor during image data acquisition, where the first image sensor and the second image sensor are independent of each other
2812
Interleave the first data stream and the second data stream

FIG. 28

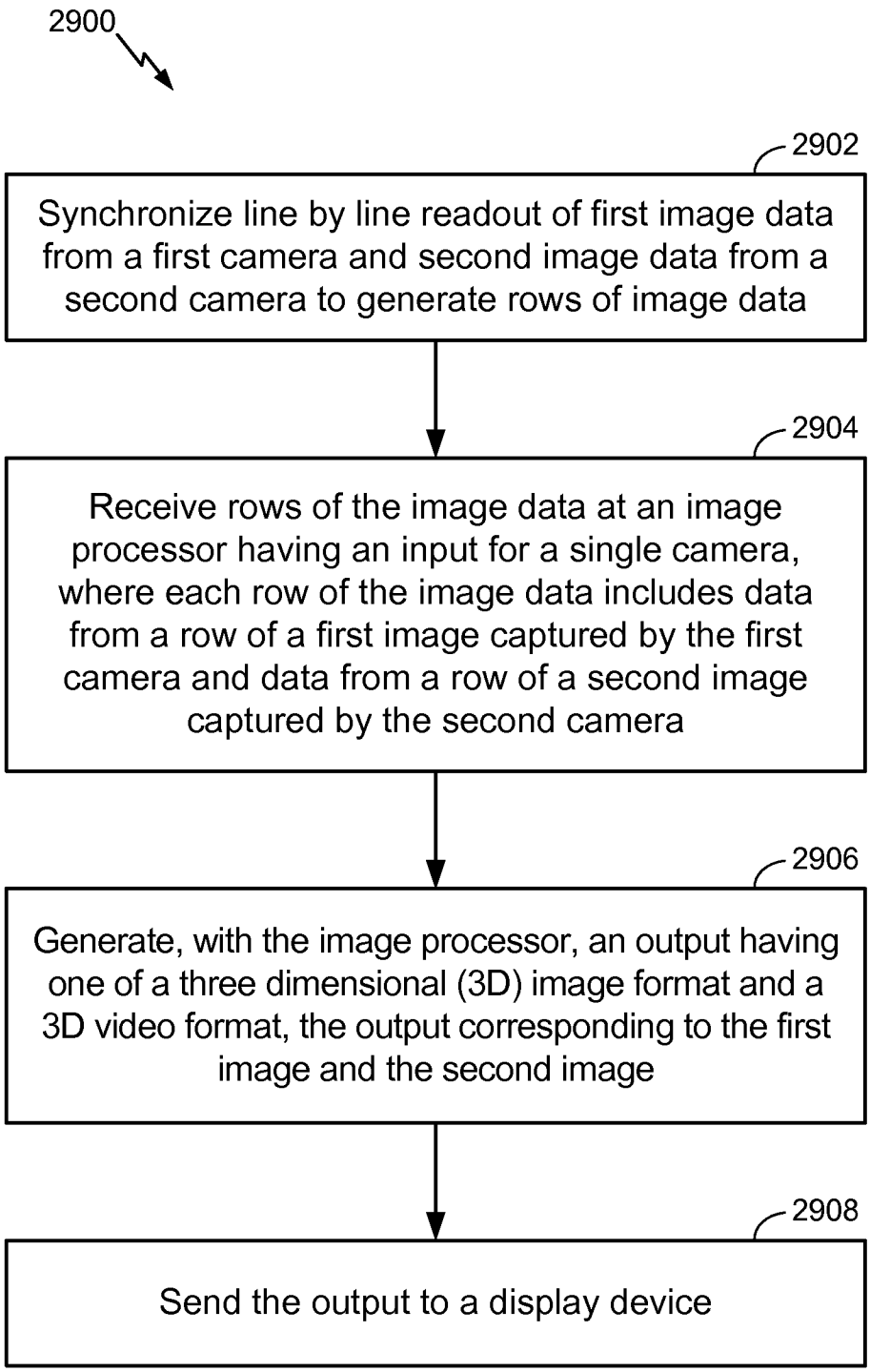
2900
2902
Synchronize line by line readout of first image data from a first camera and second image data from a second camera to generate rows of image data
2904
Receive rows of the image data at an image processor having an input for a single camera, where each row of the image data includes data from a row of a first image captured by the first camera and data from a row of a second image captured by the second camera
2906
Generate, with the image processor, an output having one of a three dimensional (3D) image format and a 3D video format, the output corresponding to the first image and the second image
2908
Send the output to a display device

FIG. 29

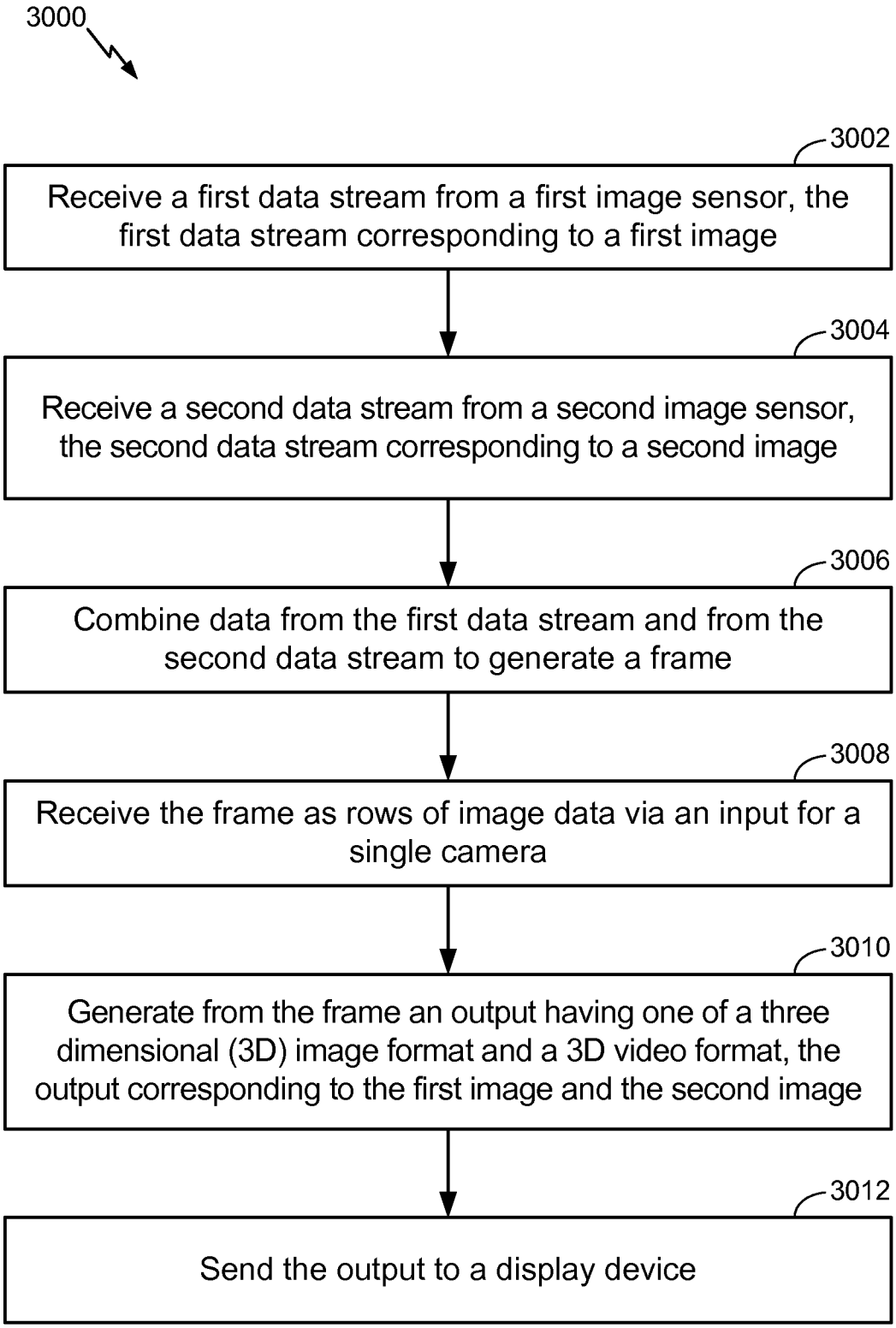
3000
3002
Receive a first data stream from a first image sensor, the first data stream corresponding to a first image
3004
Receive a second data stream from a second image sensor, the second data stream corresponding to a second image
3006
Combine data from the first data stream and from the second data stream to generate a frame
3008
Receive the frame as rows of image data via an input for a single camera
3010
Generate from the frame an output having one of a three dimensional (3D) image format and a 3D video format, the output corresponding to the first image and the second image
3012
Send the output to a display device

FIG. 30

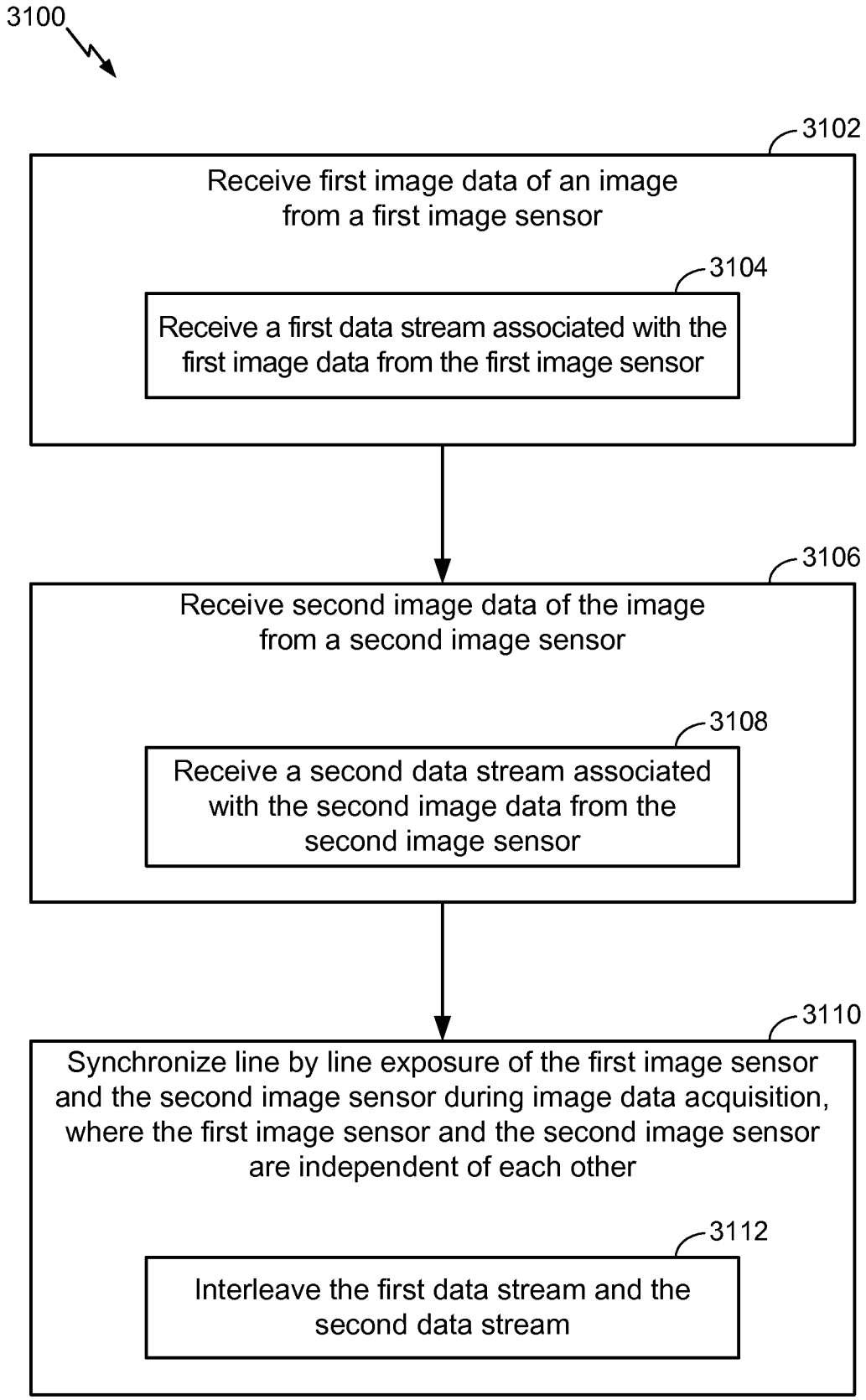
3100
3102
Receive first image data of an image from a first image sensor
3104
Receive a first data stream associated with the first image data from the first image sensor
3106
Receive second image data of the image from a second image sensor
3108
Receive a second data stream associated with the second image data from the second image sensor
3110
Synchronize line by line exposure of the first image sensor and the second image sensor during image data acquisition, where the first image sensor and the second image sensor are independent of each other
3112
Interleave the first data stream and the second data stream

FIG. 31

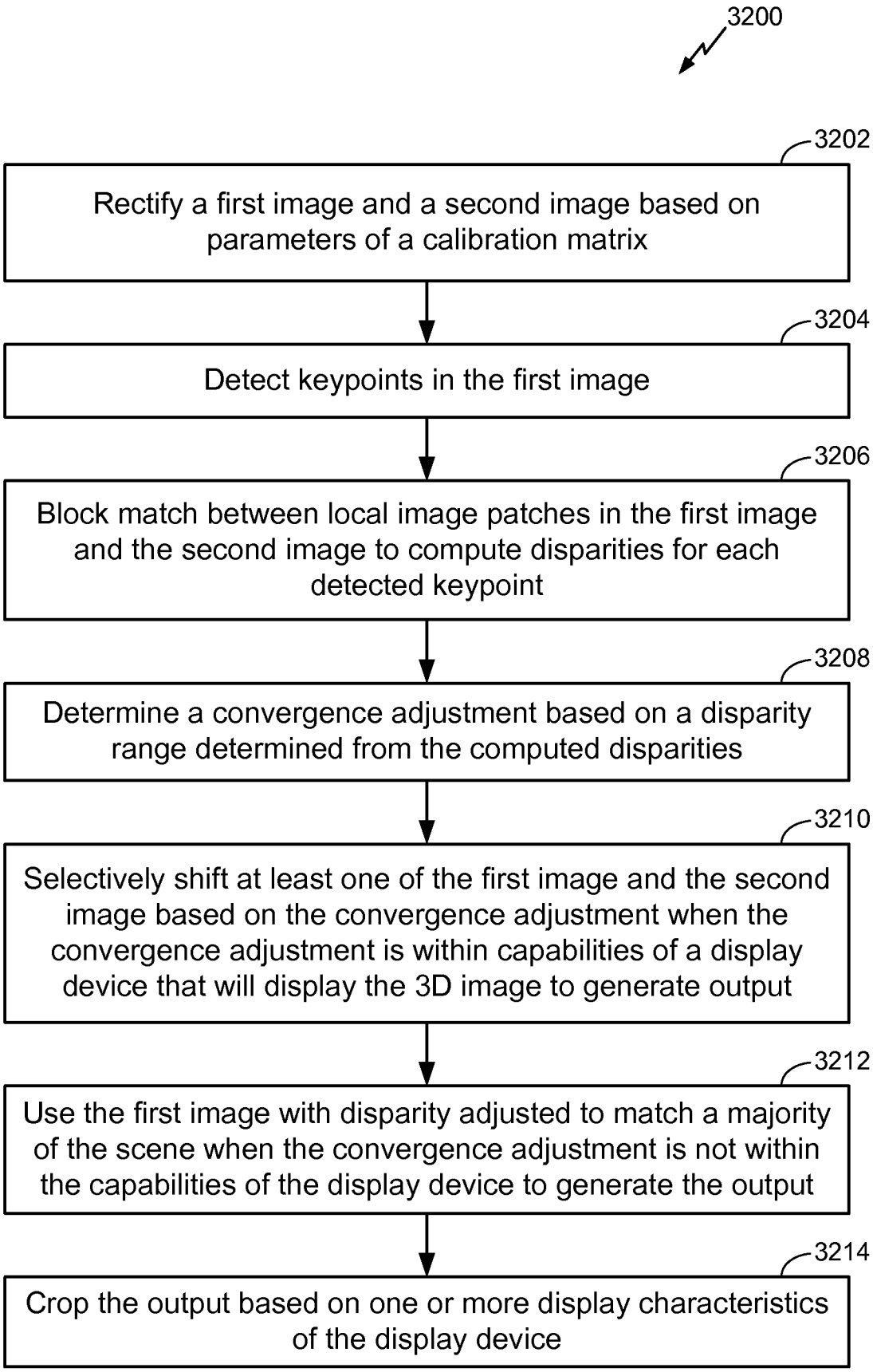
3200
3202
Rectify a first image and a second image based on parameters of a calibration matrix
3204
Detect keypoints in the first image
3206
Block match between local image patches in the first image and the second image to compute disparities for each detected keypoint
3208
Determine a convergence adjustment based on a disparity range determined from the computed disparities
3210
Selectively shift at least one of the first image and the second image based on the convergence adjustment when the convergence adjustment is within capabilities of a display device that will display the 3D image to generate output
3212
Use the first image with disparity adjusted to match a majority of the scene when the convergence adjustment is not within the capabilities of the display device to generate the output
3214
Crop the output based on one or more display characteristics of the display device

FIG. 32

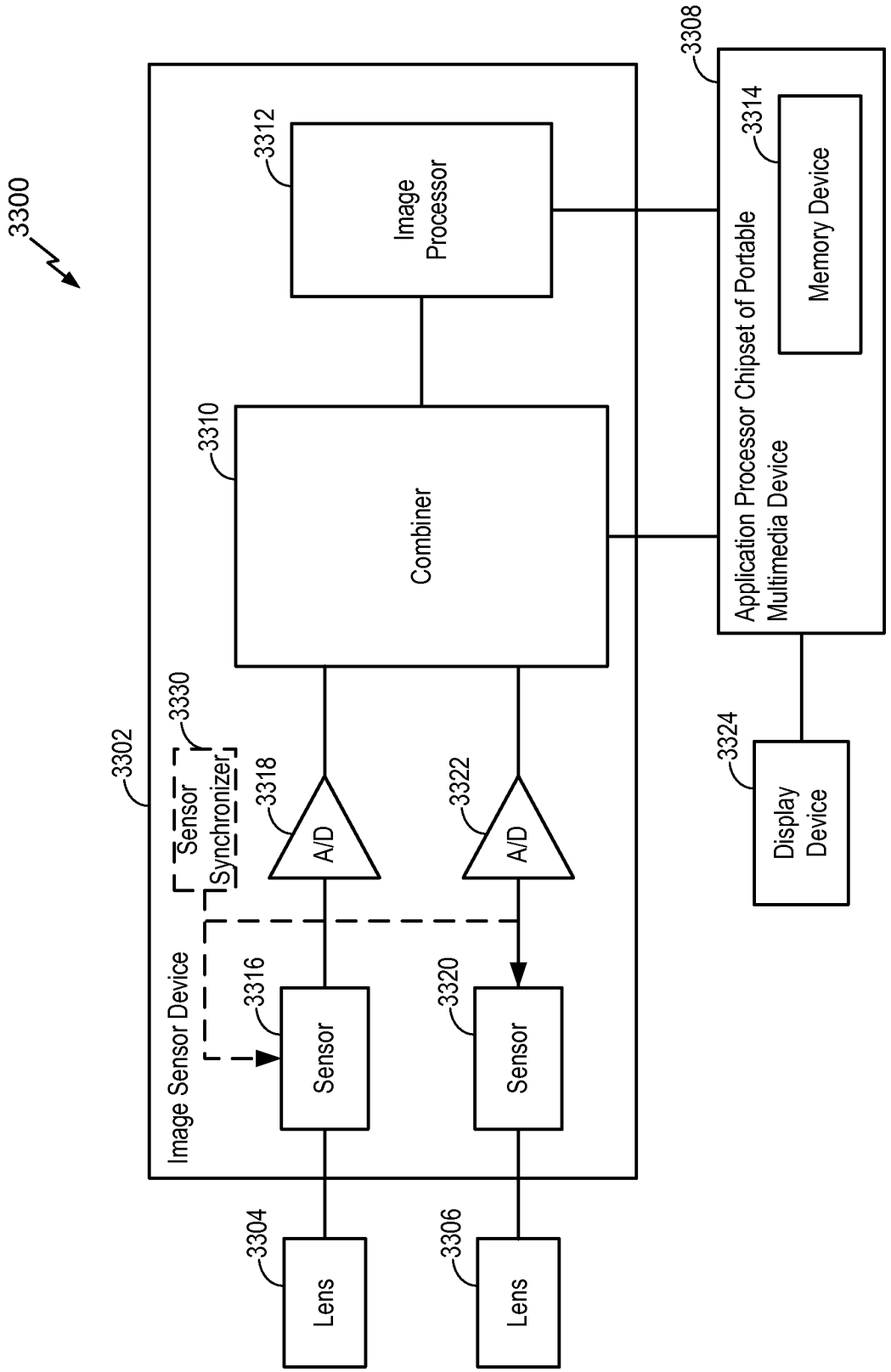
3300
3302
Image Sensor Device
3330
Sensor Synchronizer
3304
Lens
3306
Lens
3316
Sensor
3320
Sensor
3318
A/D
3322
A/D
3310
Combiner
3312
Image Processor
3308
Application Processor Chipset of Portable Multimedia Device
3314
Memory Device
3324
Display Device

FIG. 33

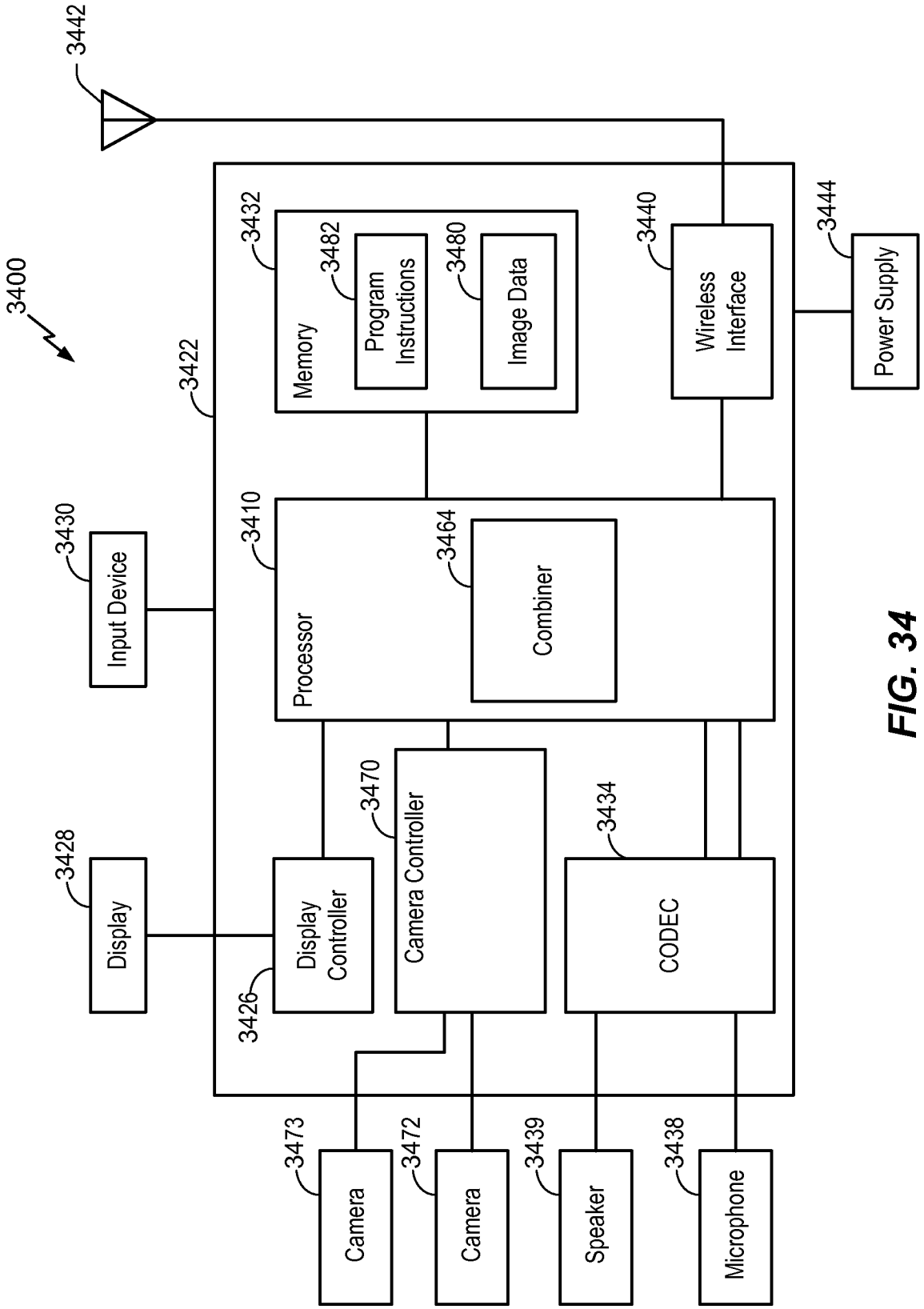
3400
3442
3422
3432
Memory
3482
Program Instructions
3480
Image Data
3440
Wireless Interface
3444
Power Supply
3430
Input Device
3410
Processor
3464
Combiner
3428
Display
3426
Display Controller
3470
Camera Controller
3434
CODEC
3473
Camera
3472
Camera
3439
Speaker
3438
Microphone

FIG. 34

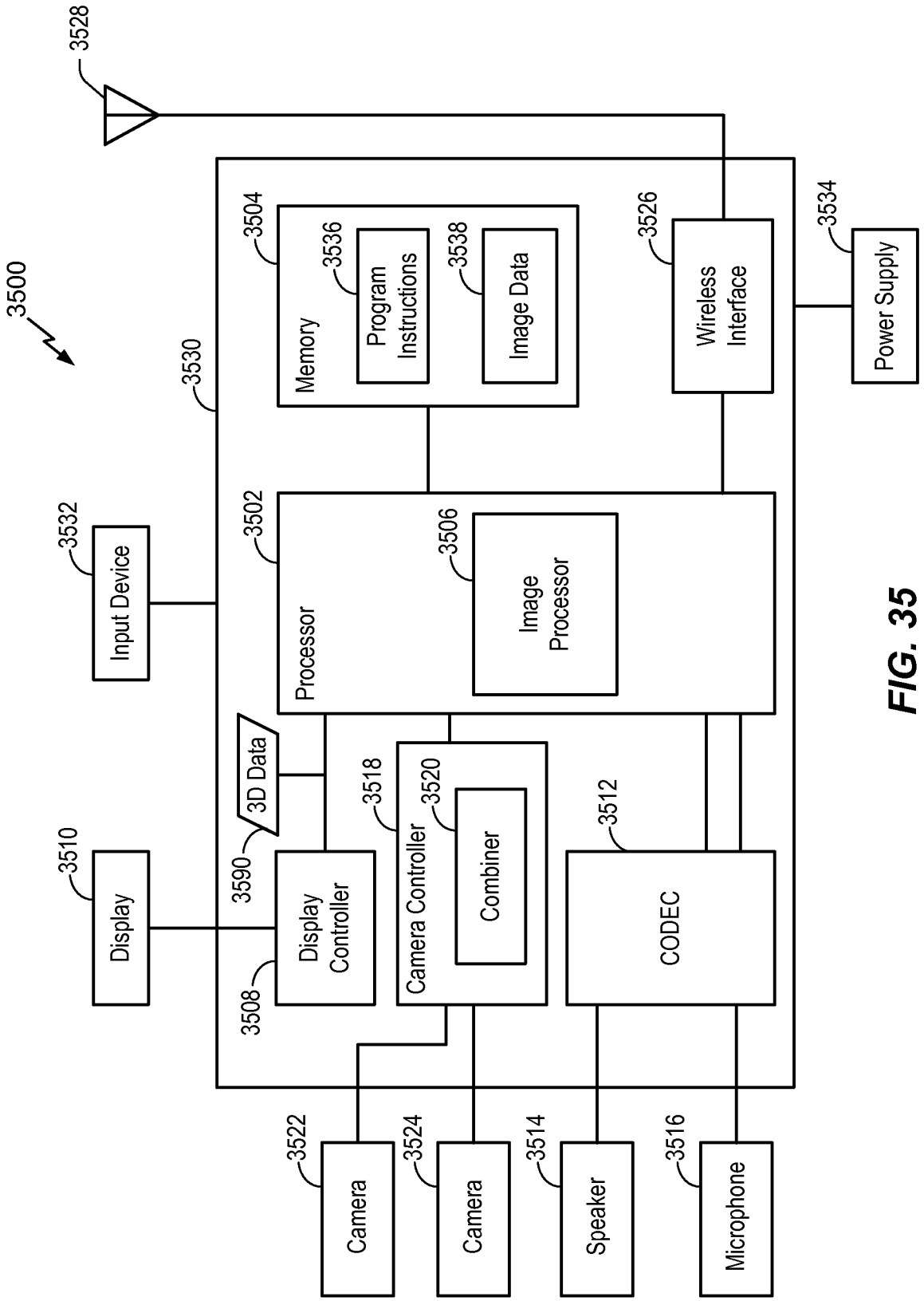
3500
3528
3530
3504
Memory
3536
Program Instructions
3538
Image Data
3526
Wireless Interface
3534
Power Supply
3532
Input Device
3502
Processor
3506
Image Processor
3510
Display
3590
3D Data
3508
Display Controller
3518
Camera Controller
3520
Combiner
3512
CODEC
3522
Camera
3524
Camera
3514
Speaker
3516
Microphone

FIG. 35

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2011/031282

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04N5/232 H04N13/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04N H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	GB 2 355 612 A (TRICORDER TECHNOLOGY PLC [GB]) 25 April 2001 (2001-04-25)	1,2,4,5, 7,8,10, 11,13, 14,16-26
Y	page 1, paragraph 24 - page 2, line 16; figures 1,2 page 4, line 18 - page 5, line 16 page 7 - page 8	3,9,12, 27

Y	US 2002/122585 A1 (SWIFT DAVID C [US] ET AL) 5 September 2002 (2002-09-05) paragraph [0062]; figure 14	3,12,27

Y	US 7 577 881 B1 (SHRIDHAR AVADHANI [US] ET AL) 18 August 2009 (2009-08-18) figure 4a	9

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
23 June 2011	04/07/2011

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Ogor, Mariëlle

1

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INTERNATIONAL SEARCH REPORT

International application No
PCT/US2011/031282

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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X	US 2005/077450 A1 (BAER RICHARD L [US]) 14 April 2005 (2005-04-14) paragraphs [0013], [0014], [0017], [0018], [0025]; figure 1 -----	1,2,4, 6-8,10, 11,13, 15-18, 21-26
X	WO 01/48537 A2 (VREX INC [US]; TSERKOVNYUK WALTER V [US]; DIVELBISS ADAM W [US]) 5 July 2001 (2001-07-05) page 2, lines 4-24; figure 1 page 7, lines 1-10 -----	1,2,4,8, 10,11, 13,17, 20,21, 23-26
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A	EP 1 906 677 A1 (SONY CORP [JP]; SANYO ELECTRIC CO [JP]; OLYMPUS IMAGING CORP [JP]; SHA) 2 April 2008 (2008-04-02) paragraph [0050]; figure 7 -----	3,12,27

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