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(54) Title: SUPER JUNCTION TRENCH POWER MOSFET DEVICES

(57) Abstract: In a super junction trench power MOSFET (metal oxide semiconductor field effect transistor) device, a column of p-type dopant in the super junction is separated from a first column of n-type dopant by a first column of oxide and from a second column of n-type dopant by a second column of oxide. In an n-channel device, a gate element for the FET is advantageously situated over the column of p-type dopant; and in a p-channel device, a gate element for the FET is advantageously situated over the column of n-type dopant.

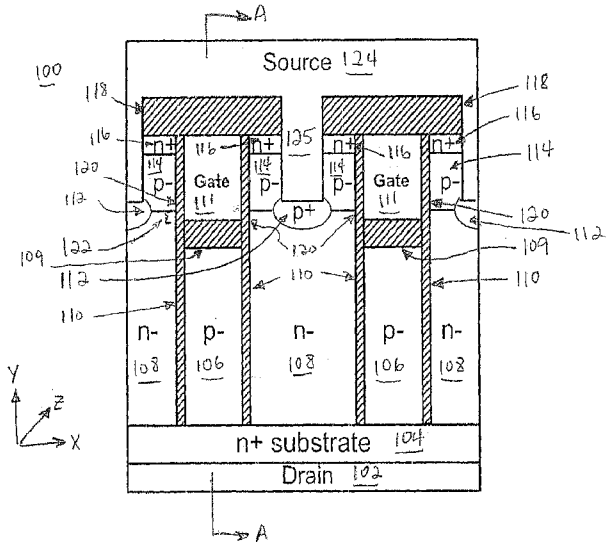

Figure 1

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SUPER JUNCTION TRENCH POWER MOSFET DEVICES

CROSS-REFERENCE

This application is related to the co-pending U.S. Patent Application with Serial No. 12/549,190, filed August 27, 2009, by Gao et al., and entitled "Super Junction Trench Power MOSFET Device Fabrication," assigned to the assignee of the present application.

FIELD

Embodiments in accordance with the present writing generally pertain to semiconductor devices.

BACKGROUND

To conserve power, it is important to reduce power losses in transistors that are used, for example, in direct current (DC) to DC converters. In a metal oxide semiconductor field effect transistor (MOSFET) device, and in particular in the class of MOSFETs known as power MOSFETs, power losses can be reduced by reducing the device's on-resistance (Rdson).

Breakdown voltage provides an indication of a device's ability to withstand breakdown under reverse voltage conditions. Because breakdown voltage is inversely related to Rdson, it is adversely affected when Rdson is reduced. To address this problem, super junction (SJ) power MOSFETs, which include alternating p-type and n-type regions below the active regions of the device, were introduced. The alternating p-type and n-type regions in a SJ power MOSFET are ideally in charge balance ($Q_p = Q_n$) so that those regions deplete one another

under a reverse voltage condition, thereby enabling the device to better withstand breakdown.

SUMMARY

Even though conventional SJ power MOSFETs provide advantages such as the one described above, there is room for improvement. For example, in conventional SJ trench power MOSFET devices, the p-type columns and n-type columns that form the super junction may diffuse into one another when they are heated during fabrication; this diffusion will reduce the breakdown voltage. Also, the p-type columns are floating so that carriers in those columns cannot be removed rapidly, and thus conventional SJ trench power MOSFET devices are generally considered to be unsuitable for use in high speed circuits. Furthermore, the density of the active devices is limited in conventional SJ trench power MOSFET devices by the placement of each trench gate; for example, in a conventional n-channel device, the trench gate is placed between two p-type columns (that is, the gate is placed over an n-type column).

In one embodiment according to the invention, an SJ trench power MOSFET device includes a super junction that includes alternating columns of p-type dopant and n-type dopant. For example, the super junction includes a column of p-type dopant that, on one side, is separated from a first column of n-type dopant by a first column (or layer) of oxide and, on its other side, is separated from a second column of n-type dopant by a second column (or layer) of oxide. The oxide layers keep the adjacent n-type and p-type columns from diffusing into one another when the device is heated during fabrication. Hence, the oxide layers can prevent breakdown voltage from being adversely affected by the fabrication process.

In another embodiment, in an n-channel device, a p-type column in the super junction is picked up and shorted to a source, so that the carriers in the p-

type column can be swept away rapidly when the resultant body diode is switched from on to off; in a p-channel device, an n-type column in the super junction is picked up and shorted to a source to similar advantage. Accordingly, a SJ trench power MOSFET device with this feature is better suited for use in high speed circuits.

In another embodiment, in an n-channel device, gate elements (e.g., trench gates) for the FETs are situated over columns of p-type dopant in the super junction instead of over columns of n-type dopant. By aligning the trench gates with the p-type columns, the widths of the n-type columns can be reduced. In a p-channel device, gate elements for the FETs are situated over columns of n-type dopant in the super junction instead of over columns of p-type dopant so that the widths of the p-type columns can be reduced. Accordingly, the trench gates can be placed closer together, increasing the cell density, which also has the effect of further reducing the on-resistance (Rdson) of the SJ trench power MOSFET device.

In yet another embodiment, an SJ trench power MOSFET device incorporates each of the features just described.

These and other objects and advantages of the present invention will be recognized by one skilled in the art after having read the following detailed description, which are illustrated in the various drawing figures.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of this specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. Like numbers denote like elements throughout the drawings and specification.

Figures 1 and 2 are cross-sectional views showing elements of semiconductor devices according to embodiments of the present invention.

Figures 3A, 3B, and 3C illustrate a flowchart of a process that is used in the fabrication of a semiconductor device according to embodiments of the present invention.

Figures 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, and 25 are cross-sectional views showing selected stages in the fabrication of a semiconductor device according to embodiments of the present invention.

Figure 26 is a cross-sectional view showing elements of a semiconductor device according to another embodiment of the present invention.

DETAILED DESCRIPTION

In the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be recognized by one skilled in the art that the present invention may be practiced without these specific details or with equivalents thereof. In other instances, well-known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the present invention.

Some portions of the detailed descriptions that follow are presented in terms of procedures, logic blocks, processing, and other symbolic representations of operations for fabricating semiconductor devices. These descriptions and representations are the means used by those skilled in the art of semiconductor device fabrication to most effectively convey the substance of their work to others skilled in the art. In the present application, a procedure, logic block, process, or the like, is conceived to be a self-consistent sequence of steps or instructions leading to a desired result. The steps are those requiring physical manipulations of physical quantities. It should be borne in mind, however, that all of these and similar terms are to be associated with the appropriate physical quantities and are merely convenient labels applied to these quantities. Unless specifically stated otherwise as apparent from the following discussions, it is appreciated that throughout the present application, discussions utilizing terms such as "forming," "performing," "producing," "depositing," "etching" or the like, refer to actions and processes (e.g., flowchart 300 of Figures 3A, 3B, and 3C) of semiconductor device fabrication.

The figures are not drawn to scale, and only portions of the structures, as

well as the various layers that form those structures, may be shown in the figures. Furthermore, fabrication processes and steps may be performed along with the processes and steps discussed herein; that is, there may be a number of process steps before, in between and/or after the steps shown and described herein. Importantly, embodiments in accordance with the present invention can be implemented in conjunction with these other (perhaps conventional) processes and steps without significantly perturbing them. Generally speaking, embodiments in accordance with the present invention can replace portions of a conventional process without significantly affecting peripheral processes and steps.

As used herein, the letter "n" refers to an n-type dopant and the letter "p" refers to a p-type dopant. A plus sign "+" or a minus sign "-" is used to represent, respectively, a relatively high or relatively low concentration of the dopant.

The term "channel" is used herein in the accepted manner. That is, current moves within a FET in a channel, from the source connection to the drain connection. A channel can be made of either n-type or p-type semiconductor material; accordingly, a FET is specified as either an n-channel or p-channel device. Figures 1-25 are discussed in the context of an n-channel device, specifically an n-channel super junction MOSFET; however, embodiments according to the present invention are not so limited. That is, the features described herein can be utilized in a p-channel device as shown in Figure 26, described further below. The discussion of Figures 1-25 can be readily mapped to a p-channel device by substituting n-type dopant and materials for corresponding p-type dopant and materials, and vice versa.

Figure 1 is a cross-sectional view showing elements of a semiconductor device 100 (e.g., an n-channel SJ trench power MOSFET device) according to an embodiment of the present invention. The device 100 includes a drain electrode 102 on the bottom surface of an n+ drain layer or substrate 104. Alternating p- drift regions or p-type columns 106 and n- drift regions or n-type columns 108 are located above the substrate 104. The alternating p-type (p-) columns 106 and n-type (n-) columns 108 form what is known as a super junction. Significantly, the columns 106 of p-type dopant are separated from the adjacent columns 108 of n-type dopant by isolation layers or columns 110 (e.g., a layer/column of dielectric or oxide). The isolation layers 110 keep the n-type and p-type columns 106 and 108 from diffusing into one another when the structure is heated during fabrication, as described below. Hence, the isolation layers 110 can prevent breakdown voltage from being adversely affected by the fabrication process.

Also of significance, in the example of Figure 1, each p-type column 106 is located under a respective polysilicon (poly) trench gate 111 (gate poly 111). Generally speaking, each trench gate 111 is aligned between adjacent isolation layers 110 and above a corresponding p-type column 106. More specifically, each trench gate 111 is aligned along the longitudinal axis of a corresponding p-type column 106 (given the orientation of Figure 1, the longitudinal axis is a vertical line within a p-type column) – in one embodiment, the longitudinal axis of a trench gate 111 coincides with the longitudinal axis of a p-type column 106 such that the trench gate is centered over the p-type column. In the Figure 1 embodiment, the p-type columns 106 are separated from the trench gates 111 by a respective isolation layer 109, which may be formed of a material that is different from the material used for the isolation layers 110.

By aligning the trench gates 111 with the p-type columns 106, the width of the n-type columns 108 can be reduced. Accordingly, the trench gates can be placed closer together, increasing the cell density, which also has the effect of further reducing the on-resistance (Rdson) of the device 100. In one embodiment, the pitch between adjacent trench gates is approximately 1.2 microns, as opposed to five microns in conventional devices.

Another advantage associated with the structure in Figure 1 is that the gate-to-drain charge (Qgd) is reduced because the amount of overlap 122 between a trench gate 111 and an adjacent n-type column 108 is small. In one embodiment, the amount of overlap 122 is approximately 0.1 microns.

In the Figure 1 embodiment, a trench 125 is formed between adjacent trench gates 111, above the n-type columns 108. More specifically, each trench 125 is aligned along the longitudinal axis of a corresponding n-type column 108 – in one embodiment, the longitudinal axis of a trench 125 coincides with the longitudinal axis of an n-type column 108 such that the trench is centered over the n-type column. The trench 125 is filled with a source metal 124.

A p+ region (p-type contact region 112) separates the source metal 124 in each trench 125 from a corresponding n-type column 108. A p- region (p-type body region 114) is situated on each side of each trench 125, between the trench and a trench gate 111 and also between the source metal 124 and an n-type column 108. Also, n+ regions (n-type source regions 116) are situated on opposite sides of each trench 125 as shown in Figure 1.

The p-type (p-) body regions 114 and n-type (n+) source regions 116 are separated from a respective trench gate 111 by another isolation layer 120 (e.g., a gate oxide). As will be seen, the isolation layers 110 and 120 are formed at different points in the fabrication process and so may not be aligned as shown in Figure 1. Also, the isolation layers 110 and 120 may be made using different materials. Nevertheless, the isolation layers 110 and 120 provide a nearly continuous boundary in the y-direction of Figure 1, and in that sense can be characterized as single columns of isolation material.

An insulating layer 118 can be formed over each n-type source region 116 and each trench gate 111. The source metal layer 124 is formed over the insulating layer 118 and, as mentioned above, extends into the trenches 125.

According to an embodiment of the invention, the p-type columns 106 are picked up and electrically shorted to the source metal layer 124. One way to accomplish this is shown in Figure 2, which is a cross-sectional view of the device 100 along the cut line A-A of Figure 1; that is, the view presented in Figure 2 is in the third dimension (z) orthogonal to the two dimensions (x and y) shown in Figure 1.

In the Figure 2 embodiment, a trench 225 is formed to connect a corresponding p-type column 106 to the source metal layer 124. The trench 225 is filled with metal, and the metal in the trench 225 is separated from the trench gate 111 by the n-type column 108, a poly region 211, and isolation layers 120, as shown in the figure. By shorting the p-type columns 106 to the source metal layer 124, the carriers in the p-type columns can be swept away rapidly when the

resultant body diodes are switched from on to off. Accordingly, the device 100 is better suited for use in high speed circuits.

Figures 3A, 3B, and 3C illustrate a flowchart 300 of one embodiment of a process that is used in the fabrication of semiconductor devices such as the devices of Figures 1 and 2. Although specific steps are disclosed in Figures 3A-3C, such steps are exemplary. That is, embodiments according to the present invention are well suited to performing various other steps or variations of the steps recited in Figures 3A-3C. Figures 3A, 3B, and 3C are discussed in conjunction with Figures 4 through 25, which are cross-sectional views showing selected stages in the fabrication of a semiconductor device according to an embodiment of the present invention.

In block 302 of Figure 3A, an epitaxial layer 402 (Figure 4) of p- dopant is grown over an n+ substrate 104. The substrate 104 may include a drain electrode layer 102 (Figure 1).

In block 304, a first dielectric layer 502 is deposited over the epitaxial layer 402, and a layer 504 of photoresist (PR) is deposited over the dielectric layer (Figure 5). The dielectric layer 502 may be, for example, a thermal oxide or an oxide deposited via sub-atmospheric pressure chemical vapor deposition (SACVD).

In block 306, a first mask (not shown) is formed, and exposed portions of the photoresist layer 504 and dielectric layer 502 are etched away as shown in Figure 6. The remaining portions of the dielectric layer 502 correspond to the isolation layers 109 of Figure 1.

In block 308, portions of the p-type epitaxial layer 402 are also etched away, forming the p-type columns 106 as shown in Figure 7. The etch of the epitaxial layer 402 may extend to a relatively slight extent into the substrate 104. The etching material applied in block 308 may be different from that used in block 306. In block 310, the remaining photoresist layer 504 is removed (Figure 8).

In block 312 of Figure 3A, a second dielectric layer 902 (Figure 9) is grown or deposited over the exposed surfaces of the isolation layers 109 and the p-type columns 106. In particular, the dielectric layer 902 is formed on opposite sides of the p-type columns 106 as well as over the isolation layers 109, in effect forming layers or columns of dielectric material on either side of the p-type columns. The material used for the second dielectric layer 902 may be different from that used for the isolation layers 109. Also, the second dielectric layer 902 may be relatively thin (on the order of 300-500 Angstroms) in comparison to the thickness of the isolation layers 109.

In block 314 of Figure 3A, the portion of the dielectric layer 902 (Figure 9) that is adjacent to the substrate 104 is removed as shown in Figure 10, a process that may be referred to as bottom oxide breakthrough. The portions of the dielectric layer 902 on either side of the p-type columns 106 are not removed; those portions correspond to the isolation layers 110 of Figure 1. The portions of the dielectric layer 902 that are over the isolation layers 109 may also be removed in part or in entirety as part of the bottom oxide breakthrough process. In other words, after bottom oxide breakthrough, the substrate 104 is exposed as shown in Figure 10, while the isolation layers 109 may consist of either only the material deposited as part of the first dielectric layer 502 (Figure 5) or a

combination of the materials included in the first dielectric layer 502 and the second dielectric layer 902. Also in block 314, after bottom oxide breakthrough, an epitaxial layer 1002 of n- dopant is grown over the substrate 104 and around the structures comprising the p-type columns 106 and isolation layers 109 and 110.

In block 316 of Figure 3A, a layer of photoresist is applied and then selectively removed to form a mask 1102 as shown in Figure 11. The mask 1102 will be used to form a termination trench 1202 in the n-type epitaxial layer 1002 as shown in Figure 12. The termination trench 1202 may extend into the substrate 104. The mask 1102 can then be removed, also as shown in Figure 12.

In block 318 of Figure 3A, a third dielectric layer 1302 is grown or deposited (e.g., using SACVD) inside the termination trench 1202 and over the n-type epitaxial layer 1002 as shown in Figure 13. The material used for the third dielectric layer 1302 may be different from the material(s) used for the isolation layers 109 and 110. The third dielectric layer 1302 can then be cured or annealed using a densification process. Importantly, the isolation layers 110 prevent or limit the diffusion of the p-type columns 106 and the n-type epitaxial layer 1002 into one another during the densification process and at any other time in the fabrication process during which the structure may be heated.

In block 320 of Figure 3A, the dielectric layer 1302 is etched back such that the level of dielectric in the termination trench 1202 is essentially level with the upper surface of the n-type epitaxial layer 1002 as shown in Figure 14.

In block 322 of Figure 3B, a layer of photoresist is applied and then selectively removed to form a mask 1502 as shown in Figure 15. The openings 1504 in the mask coincide with the locations of the p-type columns 106. The widths of the openings 1504 (measured in the x-direction of Figure 15) may be less than the widths of the p-type columns 106 in order to avoid issues with the alignment of the openings and the p-type columns. In other words, as will be seen, the mask 1502 will be used to form trenches over the p-type columns 106, and ideally those trenches will not extend beyond the outer edges of the p-type columns.

In block 324 of Figure 3B, with reference to Figures 15 and 16, the portions of the n-type epitaxial layer 1002 underlying the openings 1504 are etched away, forming trenches 1602 that extend to the isolation layers 109. The portions of the epitaxial layer 1002 that are not etched away correspond to the n-type columns 108 of Figure 1. The mask 1502 can then be removed.

In block 326 of Figure 3B, a gate oxide layer 1702 (Figure 17) is grown over the exposed surfaces of the isolation layers 109 and n-type columns 108, including the sides and bottoms of the trenches 1602. The material used for the gate oxide layer 1702 may be different from the material(s) included in the first dielectric layer 502 (Figure 5) and the second dielectric layer 902 (Figure 9). The isolation layers 109 of Figure 1 may include the gate oxide layer 1702 as well as material(s) from the first dielectric layer 502 and the second dielectric layer 902 – in other words, although depicted in the figures as a single homogeneous layer, in actual practice the isolation layers 109 may include different isolation materials. Furthermore, depending on the widths of the trenches 1602, the portions of the gate oxide layer 1702 that line those trenches may coincide with

the isolation layers 110, forming essentially continuous columns of isolation material in the vertical (y-direction) of Figure 17.

In block 328 of Figure 3B, a polysilicon (poly) layer 1802 is deposited over the gate oxide layer 1702 and into the trenches 1602 as shown in Figure 18.

In block 330 of Figure 3B, a chemical-mechanical planarization or polishing (CMP) process can be used to remove some of the poly layer 1802 (Figure 18), down to the gate oxide layer 1702. An etch back process can then be used to remove more of the poly layer 1802, to form recessed elements as shown in Figure 19. These recessed elements correspond to the trench gates 111 of Figure 1.

In block 332 of Figure 3B, with reference also to Figure 20, a blanket p-dopant is implanted into the device 100 – that is, into the n-type columns 108 – to form the p-type (p-) body regions 114 of Figure 1. The p-type body regions 114 are shallower in depth (in the y-direction of Figure 20) than the trench gates 111.

In block 334 of Figure 3B, a source mask 2102 is formed over the termination trench 1202 and the adjacent regions as shown in Figure 21, and n+ dopant is then implanted into the p-type body regions 114 to form the n-type (n+) source regions 116 of Figure 1. In this manner, trench gates are formed over the p-type columns 106 instead of over the n-type columns 108. By forming the trench gates over the p-type columns 106, the gates can be placed closer together, increasing the cell density, which also has the effect of reducing Rdson. After the n-type source implant, the mask 2102 can be removed.

In block 336 of Figure 3B, a layer of low temperature oxide (LTO) followed by a layer of borophosphosilicate glass (BPSG) are deposited – these layers are identified as layer 2202 in Figure 22. (For clarity, not all of the gate oxide regions 1702 are identified in Figures 22 and 23.)

In block 338 of Figure 3B, a layer of photoresist is applied over the layer 2202 and then selectively removed to form a mask 2302 with openings 2304 that coincide with the n-type columns 108, as shown in Figure 23. The materials underneath the openings 2304 – the portions of the layer 2202, the gate oxide 1702, the n+ source regions 116, and portions of the p-type body regions 114 that are underneath those openings – can then be etched away to form the insulating layers 118 of Figure 1, and also to form the trenches 125 that expose the n+ source regions 116, p-type body regions 114, and gate pickup regions. The insulating layers 118 of Figure 1 include both the remaining portions of the layer 2202 and the remaining horizontal (x-direction) portions of the gate oxide layer 1702; the y-direction (vertical) portions of gate oxide layer 1702 coincide with the isolation layers 120 of Figure 1. At the bottom of each trench 125, p+ dopant is then implanted to form the p-type (p+) contact regions 112 of Figure 1.

In a similar manner, in block 340 of Figure 3C, a mask 2402 can be formed in the z-direction of Figure 23 with openings 2404 that coincide with the p-type columns 106, as shown in Figure 24. The materials underneath the openings 2404 – the portions of the layer 2202, the trench gates 111, and the isolation layers 109 that are underneath those openings – can then be etched away to form the isolated poly region 211 and the trenches 225 that expose the p-type columns 106 and the poly region 211. The p-type column contact trench 225 is isolated from the gate poly 111 by an oxidation layer (gate oxide) 120, an

n-type column 108, and another oxidation layer 120, and the trench 225 is also isolated by an oxidation layer 120.

In block 342 of Figure 3C, with reference also to Figures 23, 24, and 25, the mask(s) 2302 and 2402 are removed, and a metal is deposited into the trenches 2304 and 2404 and over the insulating layer 118. A layer of photoresist is applied over the metal and then selectively removed to form a mask (not shown) with openings, and the metal under the openings is etched away to form the source metal layer 124 of Figures 1 and 2, and to form a gate bus (not shown). Accordingly, both the p-type columns 106 and the n-type columns 108 are electrically connected to the source metal layer 124 as shown in Figures 1 and 2. Consequently, the carriers in the p-type columns 106 can be swept away rapidly when the resultant body diode is switched from on to off.

In block 344 of Figure 3C, a passivation layer is optionally deposited. A mask can then be applied to etch the passivation layer to define gate and source pads.

As mentioned above, features described herein are applicable also to p-channel SJ trench power MOSFET devices. Figure 26 is a cross-sectional view showing elements of a p-channel SJ trench power MOSFET device 2600 according to an embodiment of the present invention. The device 2600 includes a drain electrode (not shown) on the bottom surface of a p+ drain layer or substrate 2604. Alternating p- drift regions or p-type columns 2606 and n- drift regions or n-type columns 2608 are located above the substrate 2604 to form a super junction. The columns 2606 of p-type dopant are separated from the adjacent columns 2608 of n-type dopant by isolation layers or columns 110 to

keep the n-type and p-type columns from diffusing into one another when the structure is heated during fabrication.

In the Figure 26 embodiment, each n-type column 2608 is located under a respective polysilicon trench gate 111. The n-type columns 2608 are separated from the trench gates 111 by a respective isolation layer 109. By aligning the trench gates 111 with the n-type columns 2608, the width of the p-type columns 2606 can be reduced so that the trench gates can be placed closer together.

A trench 125 is formed between adjacent trench gates 111, above the p-type columns 2606. The trench 125 is filled with a source metal 124. An n+ region (n-contact region 2612) separates the source metal 124 in each trench 125 from a corresponding p-type column 2606. An n- region (n-body region 2614) is situated on each side of each trench 125, between the trench and a trench gate 111 and also between the source metal 124 and a p-type column 2606. Also, p+ regions (p-source regions 2616) are situated on opposite sides of each trench 125. The n-type body regions 2614 and p-type source regions 2616 are separated from a respective trench gate 111 by another isolation layer 120 (e.g., a gate oxide). An insulating layer 118 can be formed over each p-type source region 2616 and each trench gate 111. The source metal layer 124 is formed over the insulating layer 118 and, as mentioned above, extends into the trenches 125.

According to an embodiment of the invention, the n-type columns 2608 are picked up and electrically shorted to the source metal layer 124, in a manner similar to that shown in Figure 2.

In summary, embodiments of SJ trench power MOSFET devices, and embodiments of methods for fabricating such devices, are described. The features described herein can be used in low voltage devices as well as high voltage devices such as 1000-volt power MOSFETs as an alternative to split-gate, dual-trench and other conventional high voltage super junction devices.

Broadly, this writing has disclosed the following. In a super junction trench power MOSFET (metal oxide semiconductor field effect transistor) device, a column of p-type dopant in the super junction is separated from a first column of n-type dopant by a first column of oxide and from a second column of n-type dopant by a second column of oxide. In an n-channel device, a gate element for the FET is advantageously situated over the column of p-type dopant; and in a p-channel device, a gate element for the FET is advantageously situated over the column of n-type dopant.

Broadly, this writing discloses the following. In a super junction trench power MOSFET (metal oxide semiconductor field effect transistor) device, a column of p-type dopant in the super junction is separated from a first column of n-type dopant by a first column of oxide and from a second column of n-type dopant by a second column of oxide. In an n-channel device, a gate element for the FET is advantageously situated over the column of p-type dopant; and in a p-channel device, a gate element for the FET is advantageously situated over the column of n-type dopant.

The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms

disclosed, and many modifications and variations are possible in light of the above teaching. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the claims appended hereto and their equivalents. It is understood that any and all elements and steps presented here are preferably included. Any of these elements and steps may be omitted or replaced as is obvious to those skilled in the art.

As short summaries, this writing has disclosed at least the following broad concepts.

Concept 1. A super junction trench power metal oxide semiconductor field effect transistor (MOSFET) device having a channel of first type dopant, said device comprising:

a first column comprising insulating material that separates a column of second type dopant from a first column of said first type dopant;

a second column comprising insulating material that separates said column of said second type dopant from a second column of said first type dopant; and

a gate element for a field effect transistor, wherein said gate element is aligned between said first column of insulating material and said second column of insulating material.

Concept 2. The super junction trench power MOSFET device of Concept 1 further comprising an isolation layer that separates said gate element from said column of said second type dopant.

Concept 3. The super junction trench power MOSFET device of Concept 1 wherein if said first type dopant comprises n-type dopant then said second type dopant comprises p-type dopant, and wherein if said first type dopant comprises p-type dopant then said second type dopant comprises n-type dopant.

Concept 4. The super junction trench power MOSFET device of Concept 1 further comprising a layer of source metal that is electrically shorted to said column of said second type dopant.

Concept 5. The super junction trench power MOSFET device of Concept 4 further comprising a trench formed between said gate element and an adjacent gate element, wherein said source metal fills said trench.

Concept 6. The super junction trench power MOSFET device of Concept 5 further comprising a body region of said second type dopant and a source region of said first type dopant disposed between said gate element and said trench.

Concept 7. The super junction trench power MOSFET device of Concept 5 wherein said trench is aligned with the longitudinal axis of said first column of said first type dopant.

Concept 8. The super junction trench power MOSFET device of Concept 7 wherein said trench is separated from said first column of said first type dopant by a region of said second type dopant.

Concept 9. A semiconductor device having a channel of first type dopant, said device comprising:

a substrate of said first type dopant;

a super junction structure coupled to said substrate and comprising a columnar region of second type dopant disposed between a columnar first region of said first type dopant and a columnar second region of said first type dopant, wherein said region of said second type dopant is separated from said first region of said first type dopant by a first isolation layer and from said second region of said first type dopant by a second isolation layer; and

a field effect transistor coupled to said super junction structure and comprising a gate element, wherein said gate element is aligned with the longitudinal axis of said region of said second type dopant.

Concept 10. The semiconductor device of Concept 9 further comprising an oxide layer that separates said gate element from said region of said second type dopant.

Concept 11. The semiconductor device of Concept 9 further comprising a layer of source metal that is electrically shorted to said region of said second type dopant.

Concept 12. The semiconductor device of Concept 11 further comprising a trench formed between said gate element and an adjacent gate element, wherein said source metal fills said trench.

Concept 13. The semiconductor device of Concept 12 further comprising a body region of said second type dopant and a source region of said first type dopant disposed between said gate element and said trench.

Concept 14. The semiconductor device of Concept 12 wherein said trench is aligned with the longitudinal axis of said first region of said first type dopant.

Concept 15. A semiconductor device having a channel of first type dopant, comprising:

a substrate of said first type dopant;

a super junction structure coupled to said substrate and comprising a region of second type dopant disposed between a first region of said first type dopant and a second region of said first type dopant, wherein said region of said second type dopant and said first and second regions of said first type dopant each have a first dimension greater than a second dimension, said first dimension measured in a first direction and said second dimension measured in a second direction that is orthogonal to said first direction;

a field effect transistor comprising a gate element, wherein said region of said second type dopant lies between said gate element and said substrate in said first direction; and

a layer of source metal that is electrically shorted to said region of said second type dopant in a third direction that is orthogonal to both said first direction and said second direction.

Concept 16. The semiconductor device of Concept 15 wherein said region of said second type dopant is separated from said first region of said first type dopant by a first isolation layer and from said second region of said first type dopant by a second isolation layer.

Concept 17. The semiconductor device of Concept 15 further comprising an oxide layer that separates said gate element from said region of said second type dopant.

Concept 18. The semiconductor device of Concept 15 further comprising a trench formed between said gate element and an adjacent gate element, wherein said source metal fills said trench.

Concept 19. The semiconductor device of Concept 18 further comprising a body region of said second type dopant and a source region of said first type dopant disposed between said gate element and said trench.

Concept 20. The semiconductor device of Concept 18 wherein said first region of said first type dopant lies between said trench and said substrate in said first direction.

CLAIMS

What is claimed is:

1. A super junction trench power metal oxide semiconductor field effect transistor (MOSFET) device having a channel of first type dopant, said device comprising:

a first column comprising insulating material that separates a column of second type dopant from a first column of said first type dopant;

a second column comprising insulating material that separates said column of said second type dopant from a second column of said first type dopant; and

a gate element for a field effect transistor, wherein said gate element is aligned between said first column of insulating material and said second column of insulating material.

2. The super junction trench power MOSFET device of Claim 1 further comprising an isolation layer that separates said gate element from said column of said second type dopant.

3. The super junction trench power MOSFET device of Claim 1 wherein if said first type dopant comprises n-type dopant then said second type dopant comprises p-type dopant, and wherein if said first type dopant comprises p-type dopant then said second type dopant comprises n-type dopant.

4. The super junction trench power MOSFET device of Claim 1 further comprising a layer of source metal that is electrically shorted to said column of said second type dopant.

5. The super junction trench power MOSFET device of Claim 4 further comprising a trench formed between said gate element and an adjacent gate element, wherein said source metal fills said trench.

6. The super junction trench power MOSFET device of Claim 5 further comprising a body region of said second type dopant and a source region of said first type dopant disposed between said gate element and said trench.

7. The super junction trench power MOSFET device of Claim 5 wherein said trench is aligned with the longitudinal axis of said first column of said first type dopant.

8. The super junction trench power MOSFET device of Claim 7 wherein said trench is separated from said first column of said first type dopant by a region of said second type dopant.

9. A semiconductor device having a channel of first type dopant, said device comprising:

a substrate of said first type dopant;

a super junction structure coupled to said substrate and comprising a columnar region of second type dopant disposed between a columnar first region of said first type dopant and a columnar second region of said first type dopant, wherein said region of said second type dopant is separated from said first region of said first type dopant by a first isolation layer and from said second region of said first type dopant by a second isolation layer; and

a field effect transistor coupled to said super junction structure and comprising a gate element, wherein said gate element is aligned with the longitudinal axis of said region of said second type dopant.

10. The semiconductor device of Claim 9 further comprising an oxide layer that separates said gate element from said region of said second type dopant.

11. The semiconductor device of Claim 9 further comprising a layer of source metal that is electrically shorted to said region of said second type dopant.

12. The semiconductor device of Claim 11 further comprising a trench formed between said gate element and an adjacent gate element, wherein said source metal fills said trench.

13. The semiconductor device of Claim 12 further comprising a body region of said second type dopant and a source region of said first type dopant disposed between said gate element and said trench.

14. The semiconductor device of Claim 12 wherein said trench is aligned with the longitudinal axis of said first region of said first type dopant.

15. A semiconductor device having a channel of first type dopant, comprising:

a substrate of said first type dopant;

a super junction structure coupled to said substrate and comprising a region of second type dopant disposed between a first region of said first type dopant and a second region of said first type dopant, wherein said region of said second type dopant and said first and second regions of said first type dopant each have a first dimension greater than a second dimension, said first dimension measured in a first direction and said second dimension measured in a second direction that is orthogonal to said first direction;

a field effect transistor comprising a gate element, wherein said region of said second type dopant lies between said gate element and said substrate in said first direction; and

a layer of source metal that is electrically shorted to said region of said second type dopant in a third direction that is orthogonal to both said first direction and said second direction.

16. The semiconductor device of Claim 15 wherein said region of said second type dopant is separated from said first region of said first type dopant by a first isolation layer and from said second region of said first type dopant by a second isolation layer.

17. The semiconductor device of Claim 15 further comprising an oxide layer that separates said gate element from said region of said second type dopant.

18. The semiconductor device of Claim 15 further comprising a trench formed between said gate element and an adjacent gate element, wherein said source metal fills said trench.

19. The semiconductor device of Claim 18 further comprising a body region of said second type dopant and a source region of said first type dopant disposed between said gate element and said trench.

20. The semiconductor device of Claim 18 wherein said first region of said first type dopant lies between said trench and said substrate in said first direction.

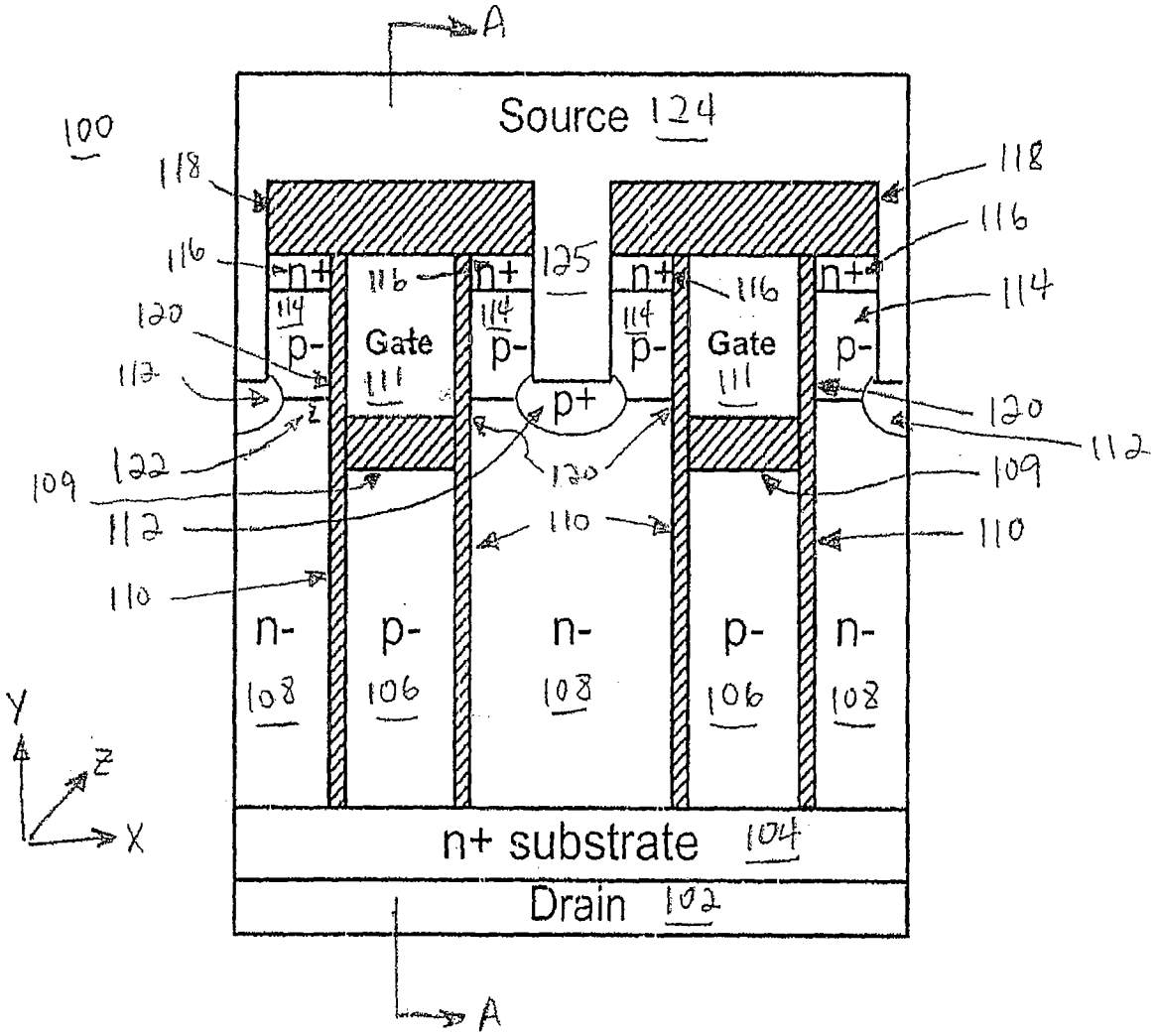

A
Source 124
100
118
116
n+
114
p-
120
117
Gate
111
125
p+
122
109
112
110
n-
108
p-
106
n+ substrate 104
Drain 102
Y
Z
X

Figure 1

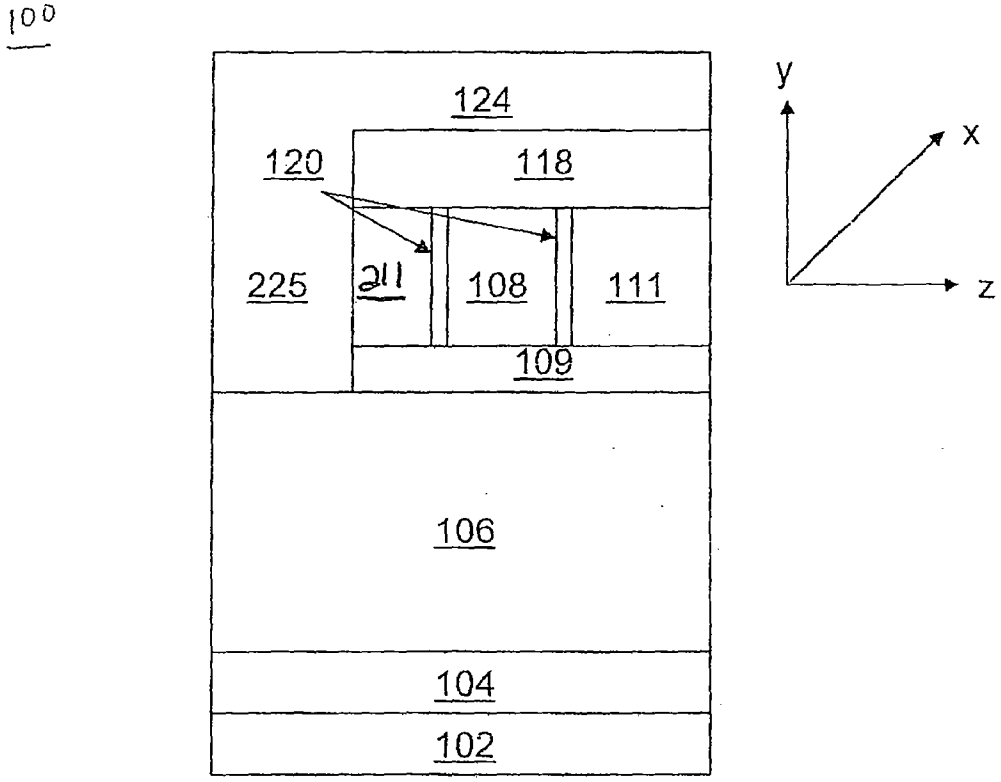


Figure 2

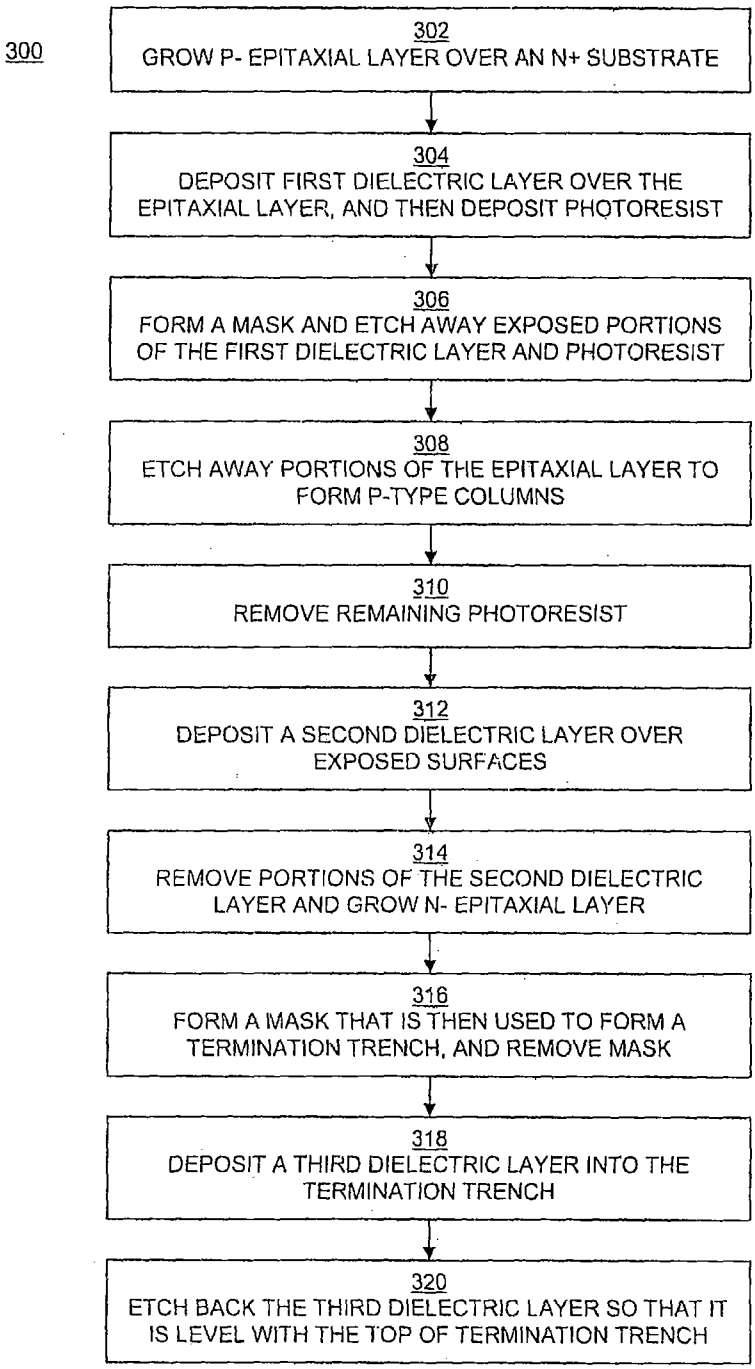

300
302
GROW P- EPITAXIAL LAYER OVER AN N+ SUBSTRATE
304
DEPOSIT FIRST DIELECTRIC LAYER OVER THE EPITAXIAL LAYER, AND THEN DEPOSIT PHOTORESIST
306
FORM A MASK AND ETCH AWAY EXPOSED PORTIONS OF THE FIRST DIELECTRIC LAYER AND PHOTORESIST
308
ETCH AWAY PORTIONS OF THE EPITAXIAL LAYER TO FORM P-TYPE COLUMNS
310
REMOVE REMAINING PHOTORESIST
312
DEPOSIT A SECOND DIELECTRIC LAYER OVER EXPOSED SURFACES
314
REMOVE PORTIONS OF THE SECOND DIELECTRIC LAYER AND GROW N- EPITAXIAL LAYER
316
FORM A MASK THAT IS THEN USED TO FORM A TERMINATION TRENCH, AND REMOVE MASK
318
DEPOSIT A THIRD DIELECTRIC LAYER INTO THE TERMINATION TRENCH
320
ETCH BACK THE THIRD DIELECTRIC LAYER SO THAT IT IS LEVEL WITH THE TOP OF TERMINATION TRENCH

Figure 3A

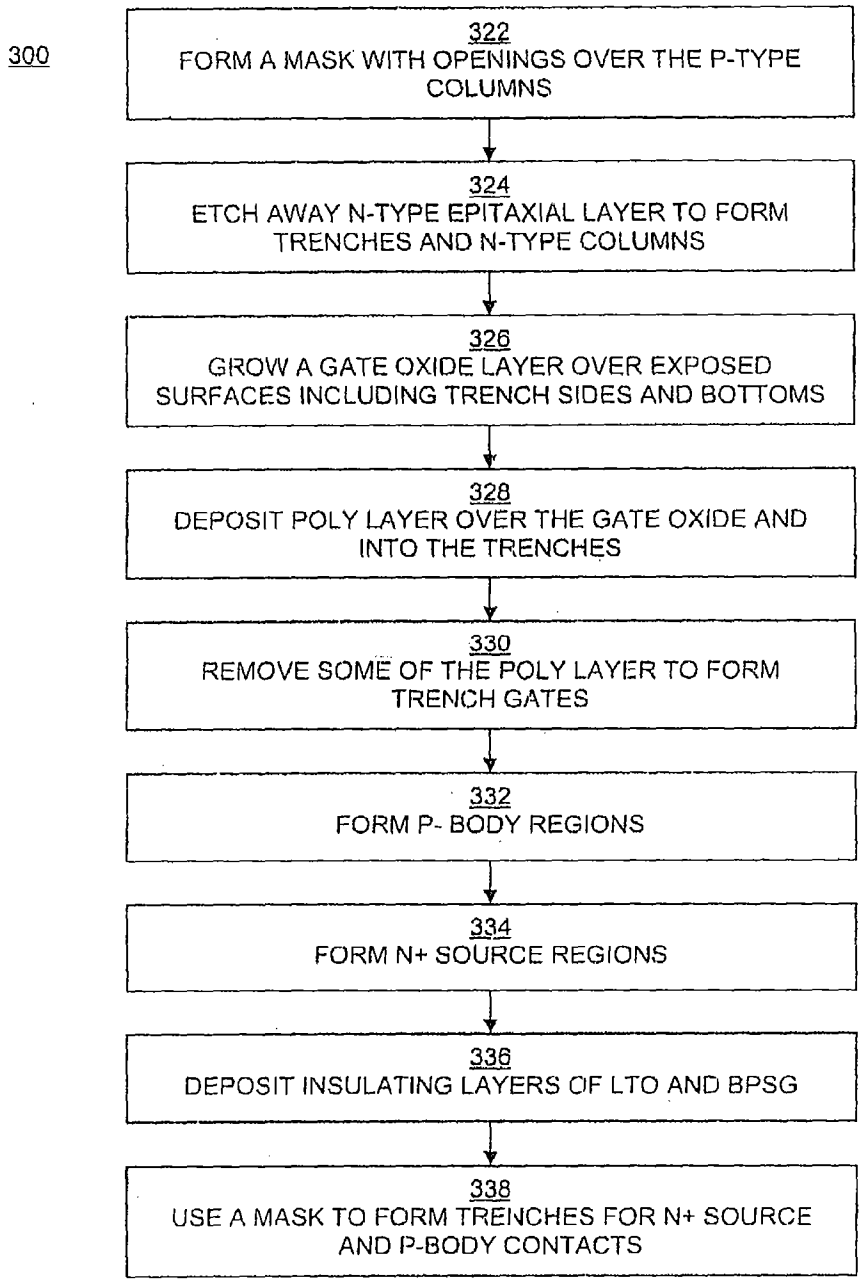

300
322
FORM A MASK WITH OPENINGS OVER THE P-TYPE COLUMNS
324
ETCH AWAY N-TYPE EPITAXIAL LAYER TO FORM TRENCHES AND N-TYPE COLUMNS
326
GROW A GATE OXIDE LAYER OVER EXPOSED SURFACES INCLUDING TRENCH SIDES AND BOTTOMS
328
DEPOSIT POLY LAYER OVER THE GATE OXIDE AND INTO THE TRENCHES
330
REMOVE SOME OF THE POLY LAYER TO FORM TRENCH GATES
332
FORM P- BODY REGIONS
334
FORM N+ SOURCE REGIONS
336
DEPOSIT INSULATING LAYERS OF LTO AND BPSG
338
USE A MASK TO FORM TRENCHES FOR N+ SOURCE AND P-BODY CONTACTS

Figure 3B

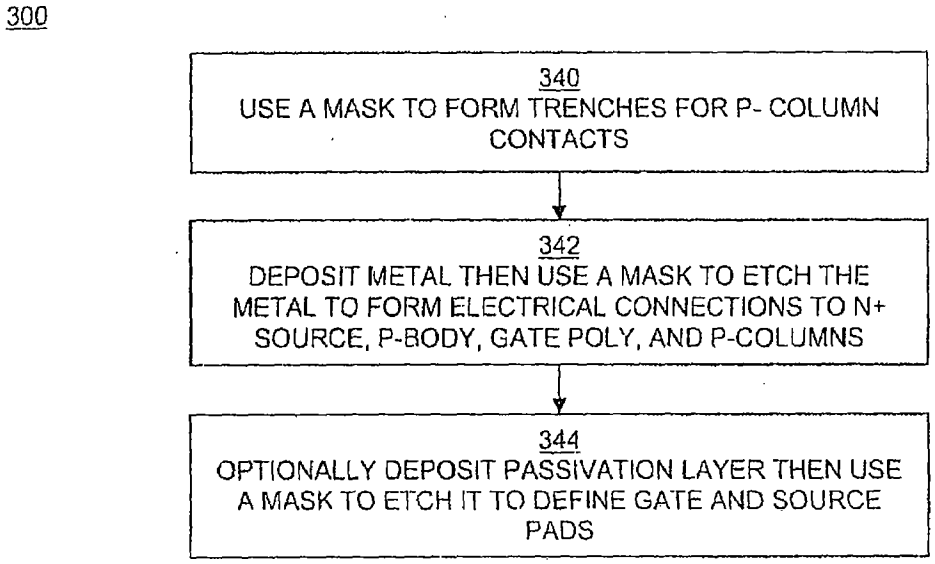

300
340
USE A MASK TO FORM TRENCHES FOR P- COLUMN CONTACTS
342
DEPOSIT METAL THEN USE A MASK TO ETCH THE METAL TO FORM ELECTRICAL CONNECTIONS TO N+ SOURCE, P-BODY, GATE POLY, AND P-COLUMNS
344
OPTIONALLY DEPOSIT PASSIVATION LAYER THEN USE A MASK TO ETCH IT TO DEFINE GATE AND SOURCE PADS

Figure 3C

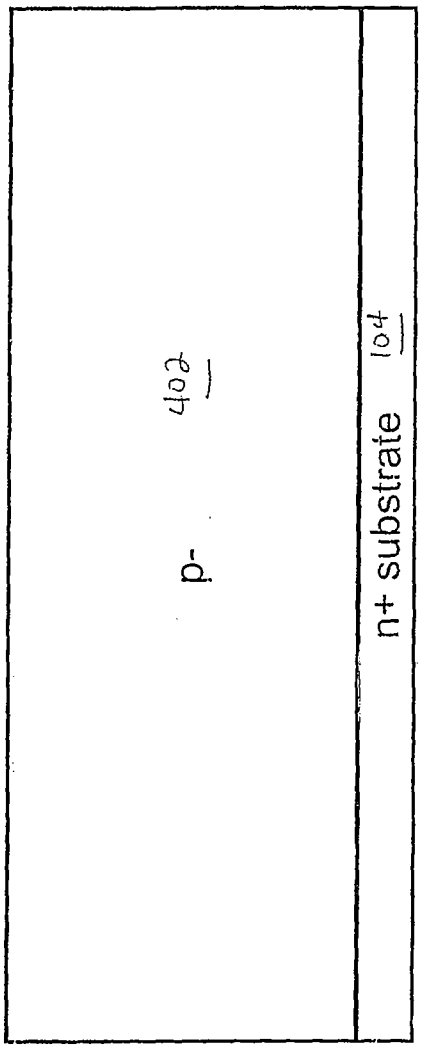
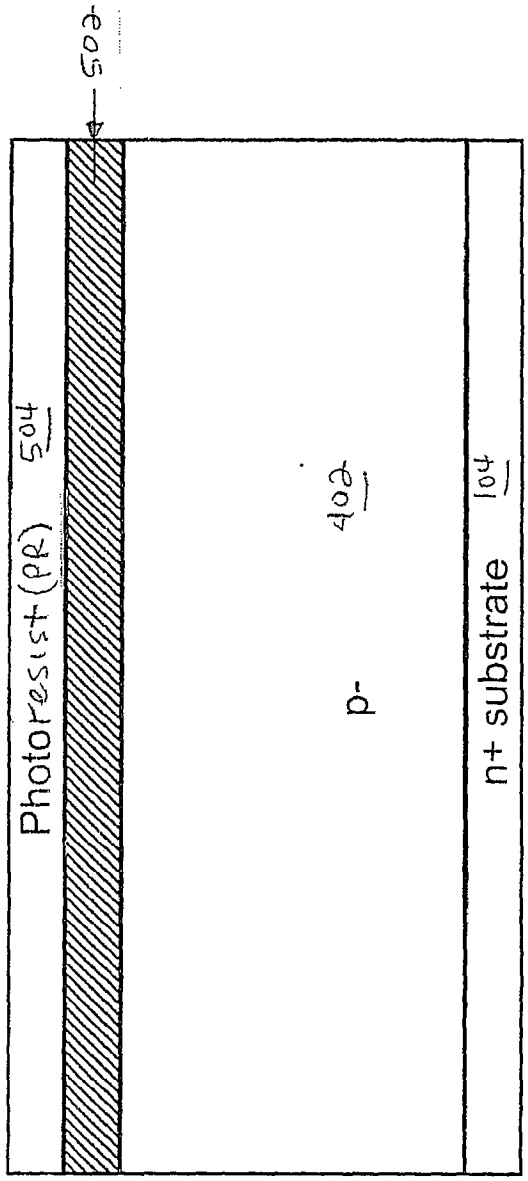


Figure 4



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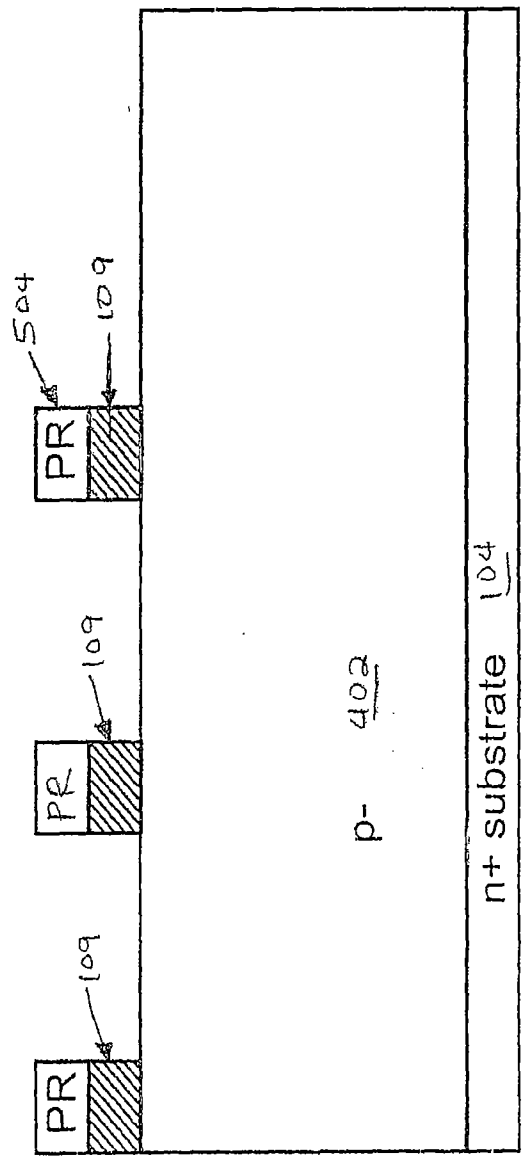
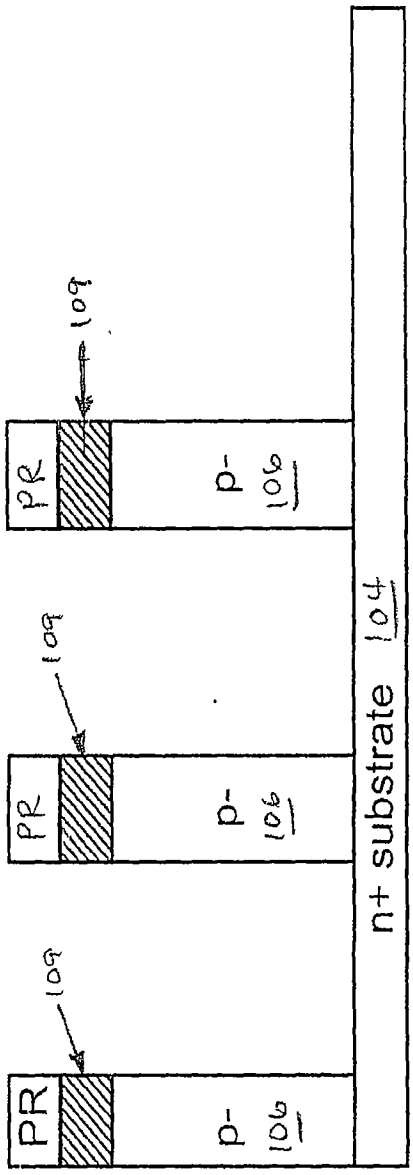


Figure 6



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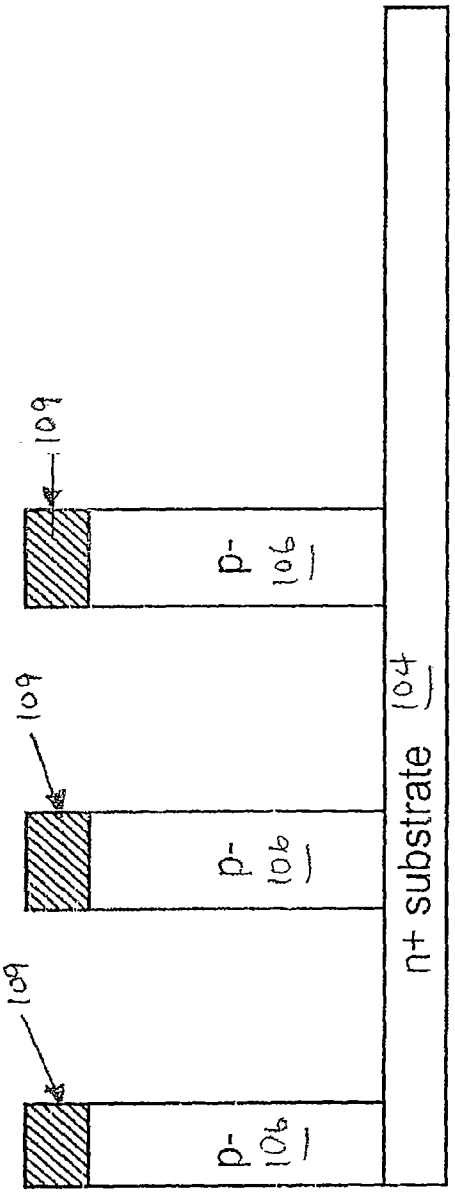


Figure 8

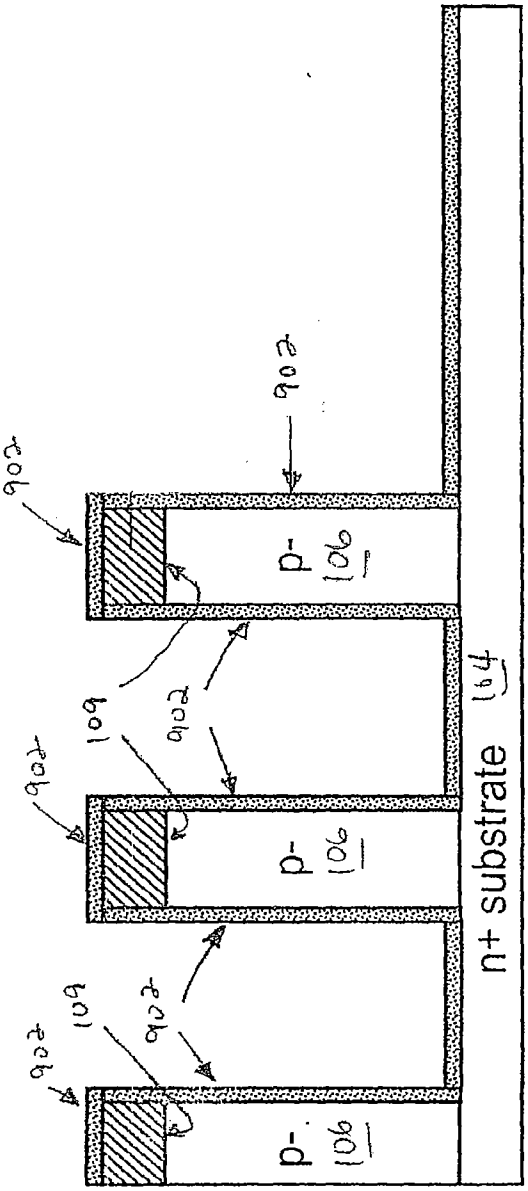


Figure 9

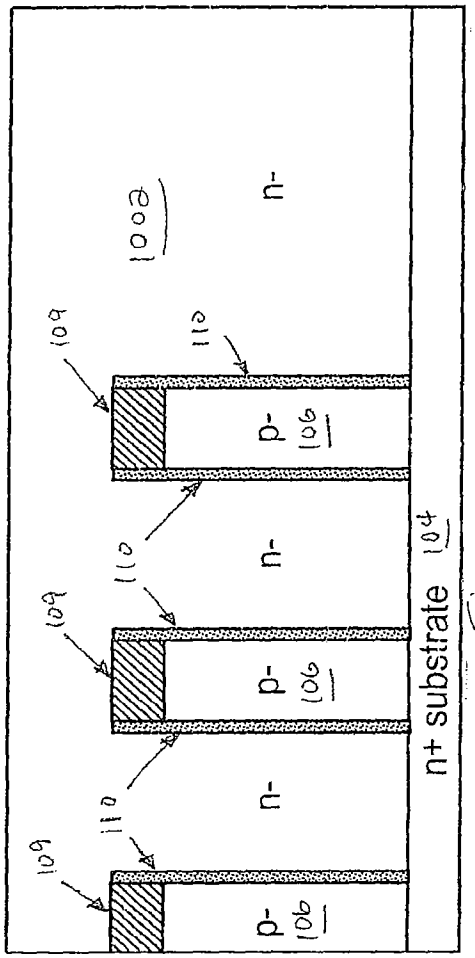


Figure 10

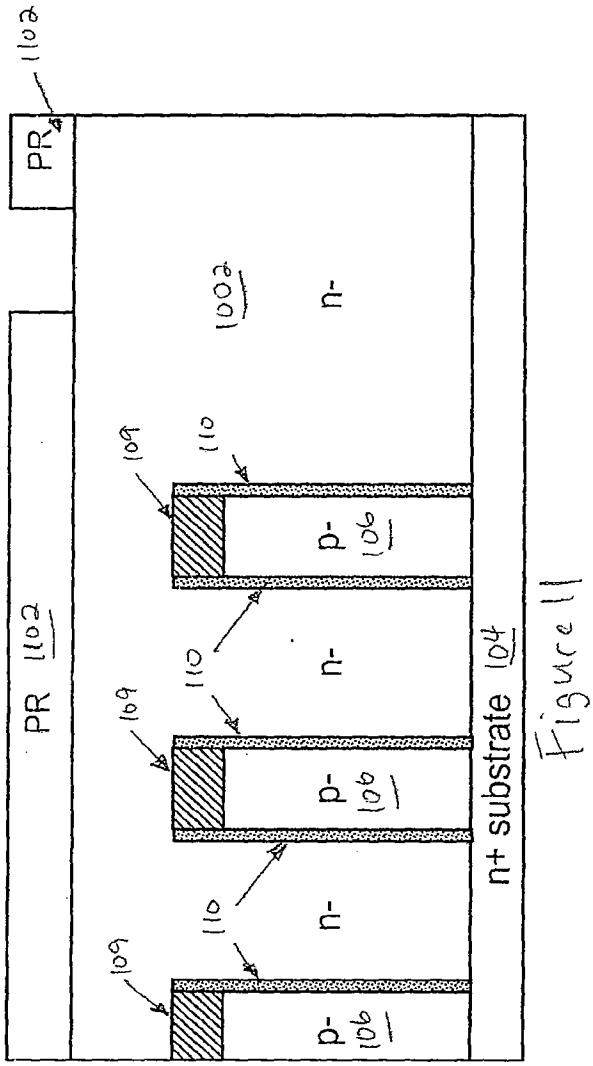


Figure 11

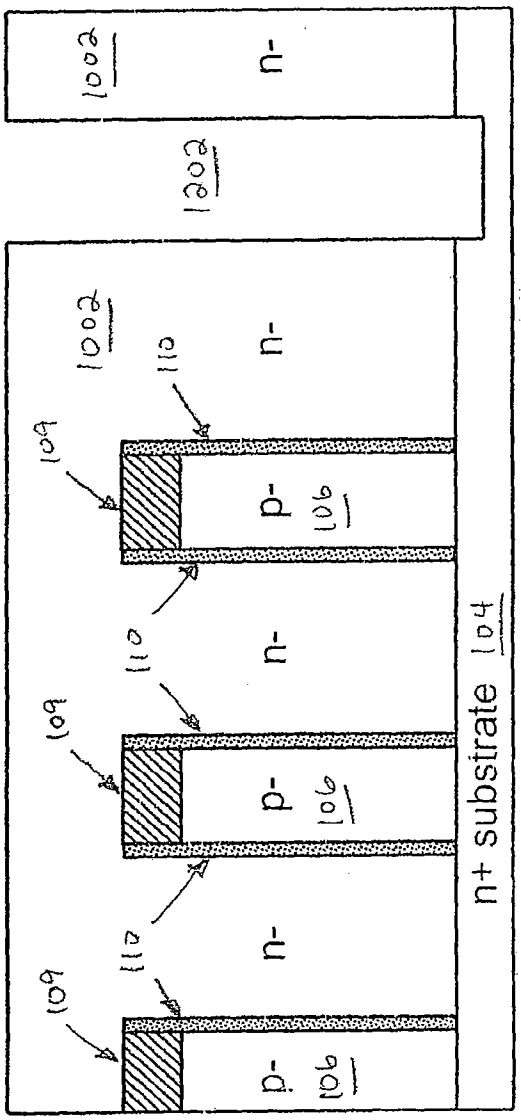


Figure 12

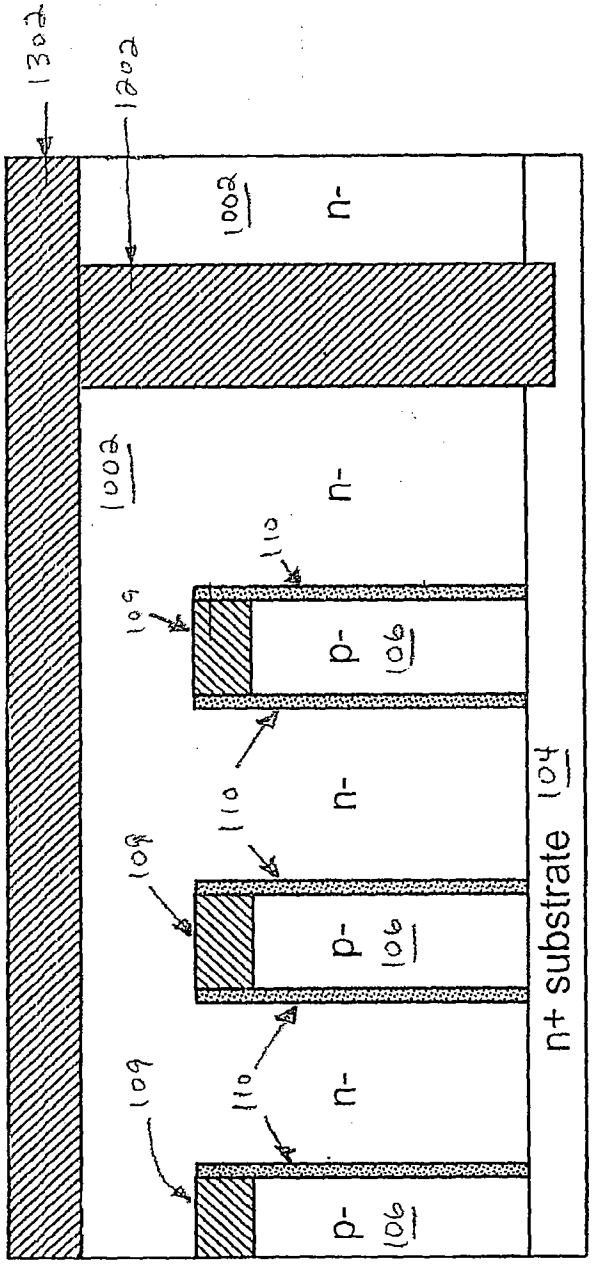


Figure 13

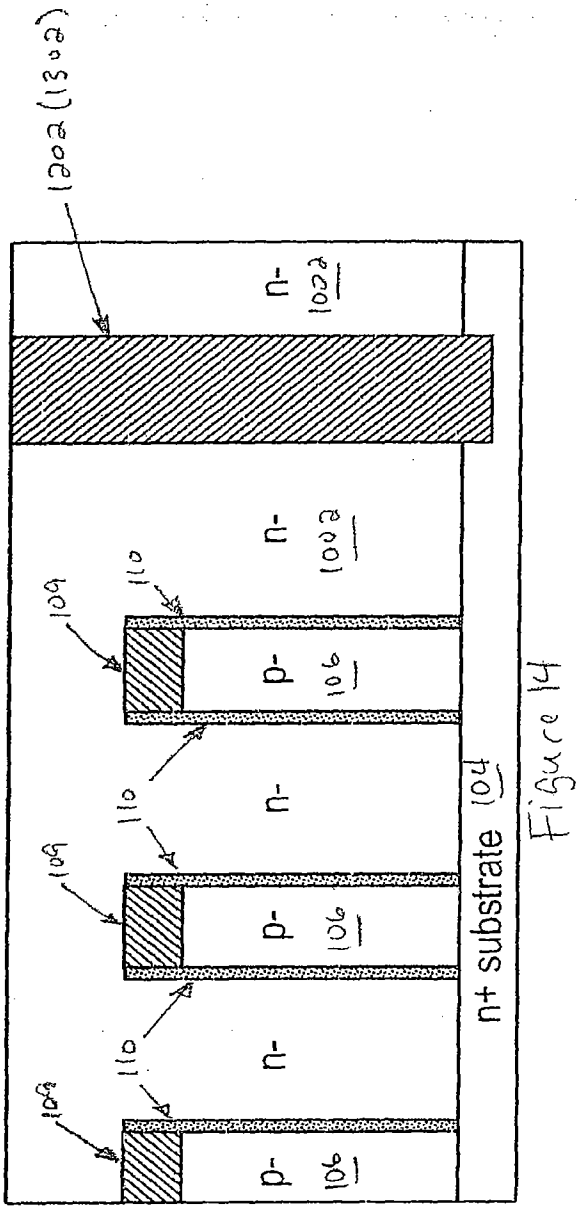


Figure 14

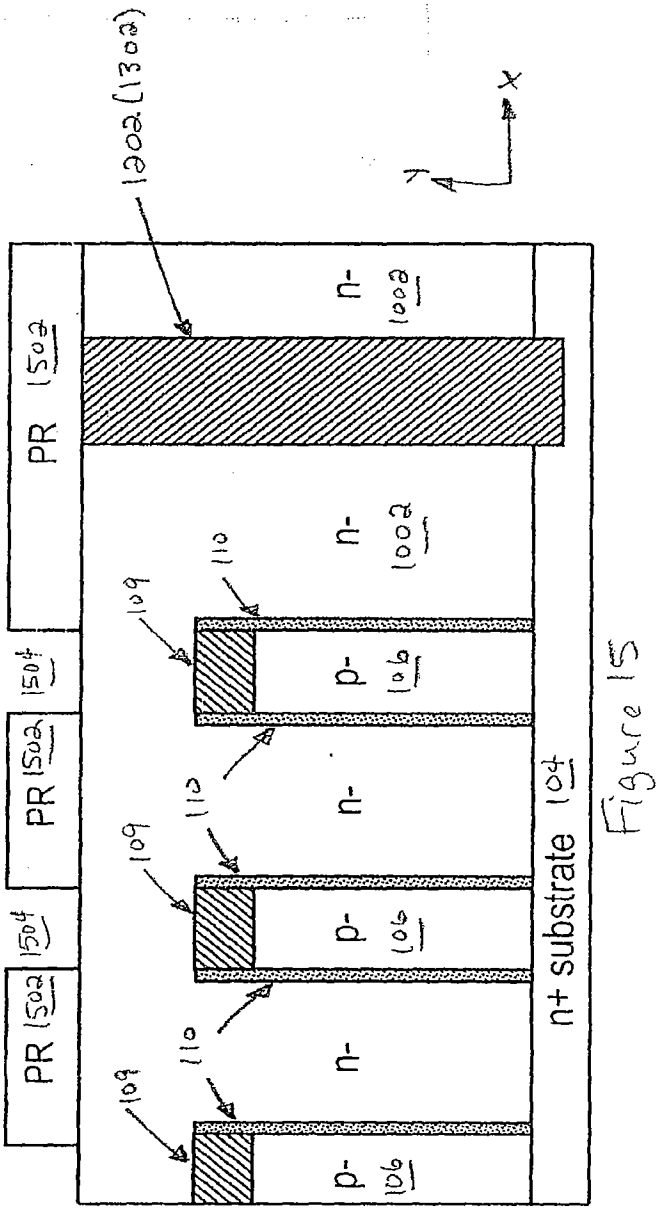


Figure 15

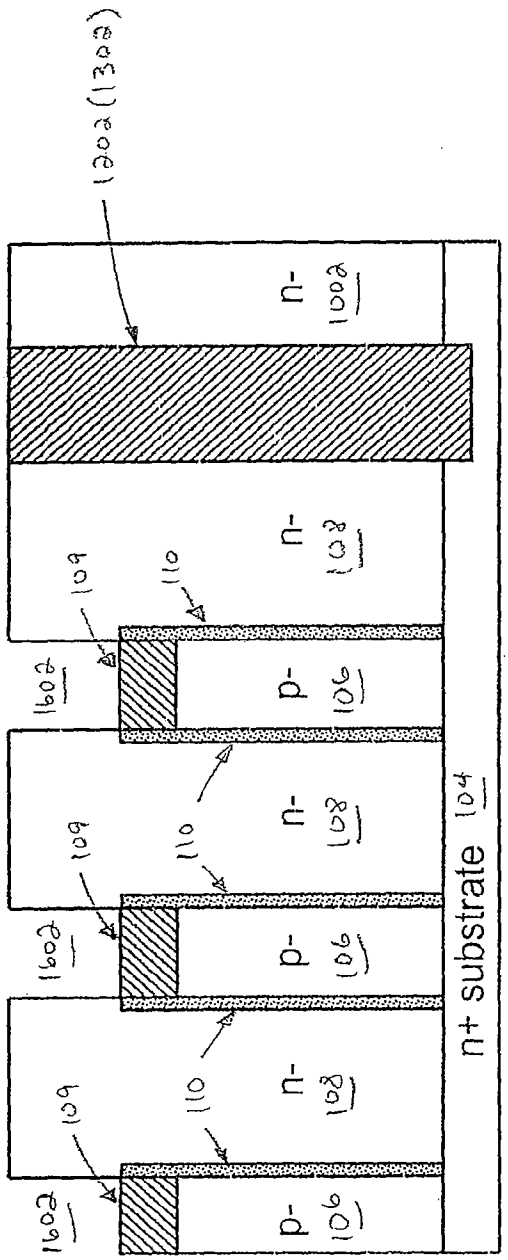


Figure 16

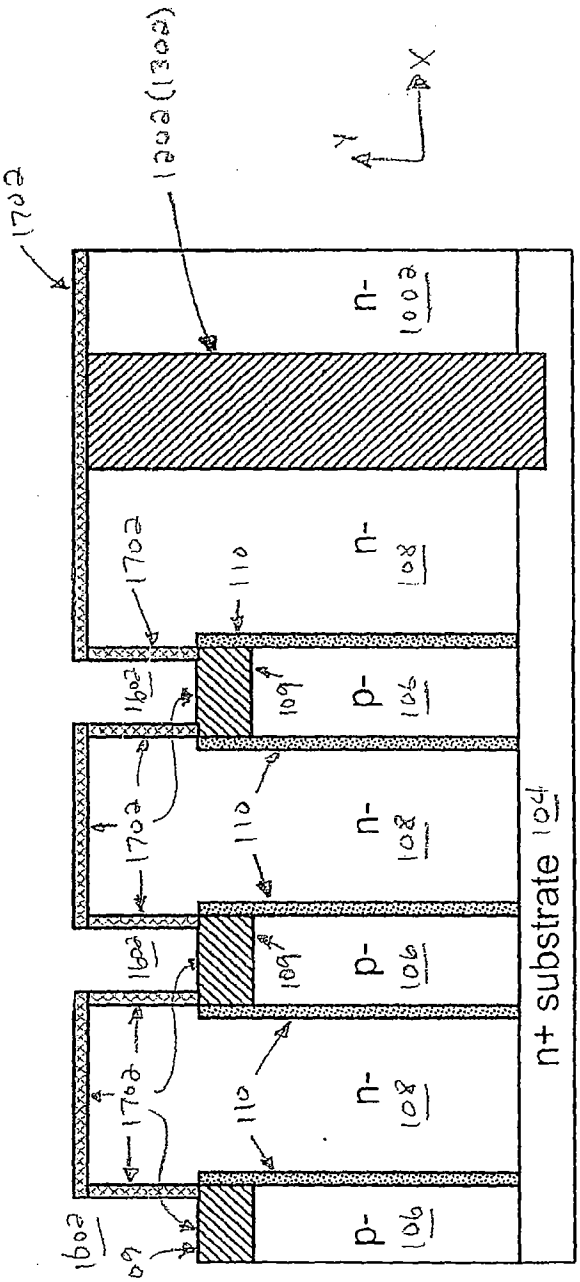


Figure 17

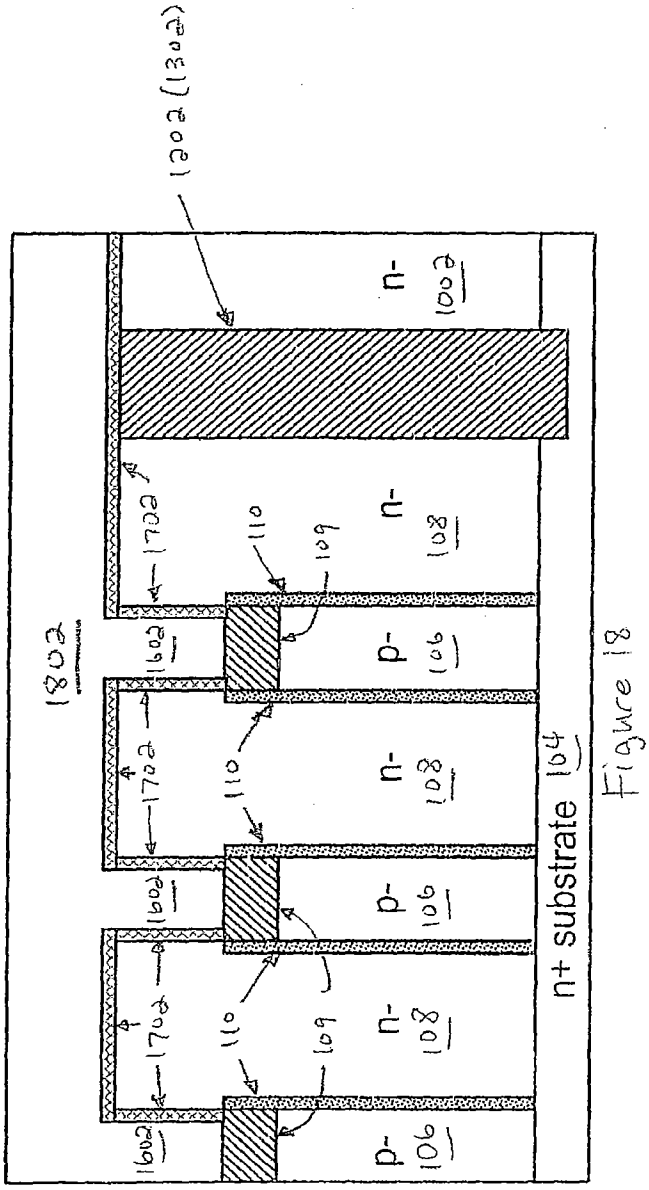


Figure 18

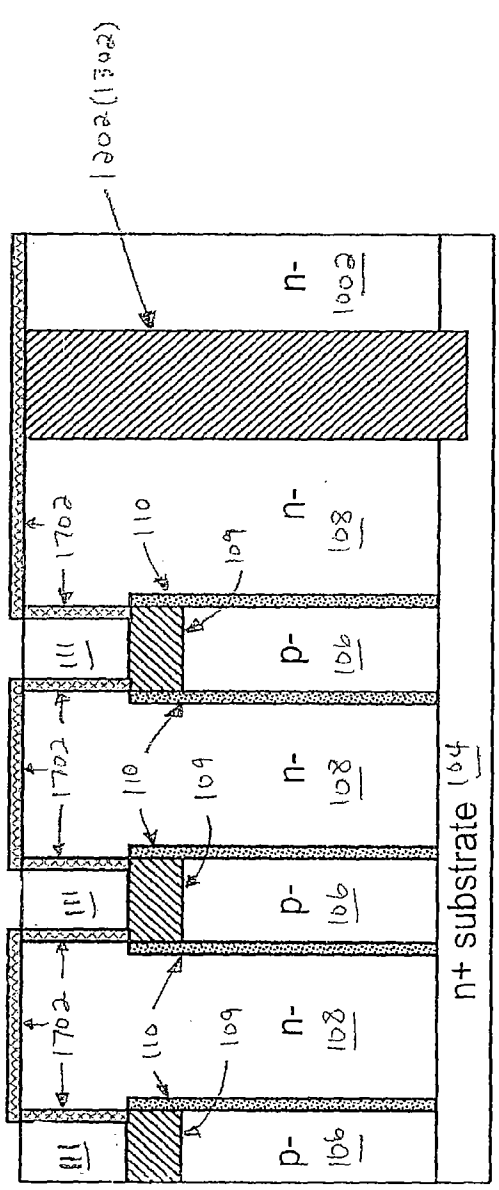


Figure 19

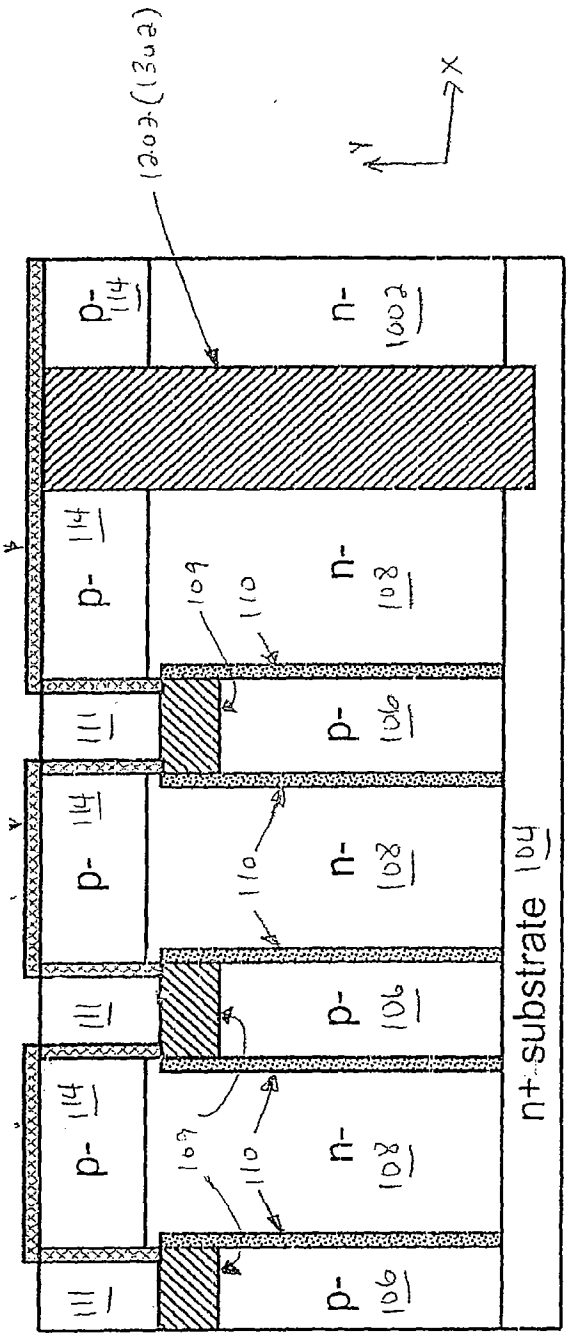


Figure 2a

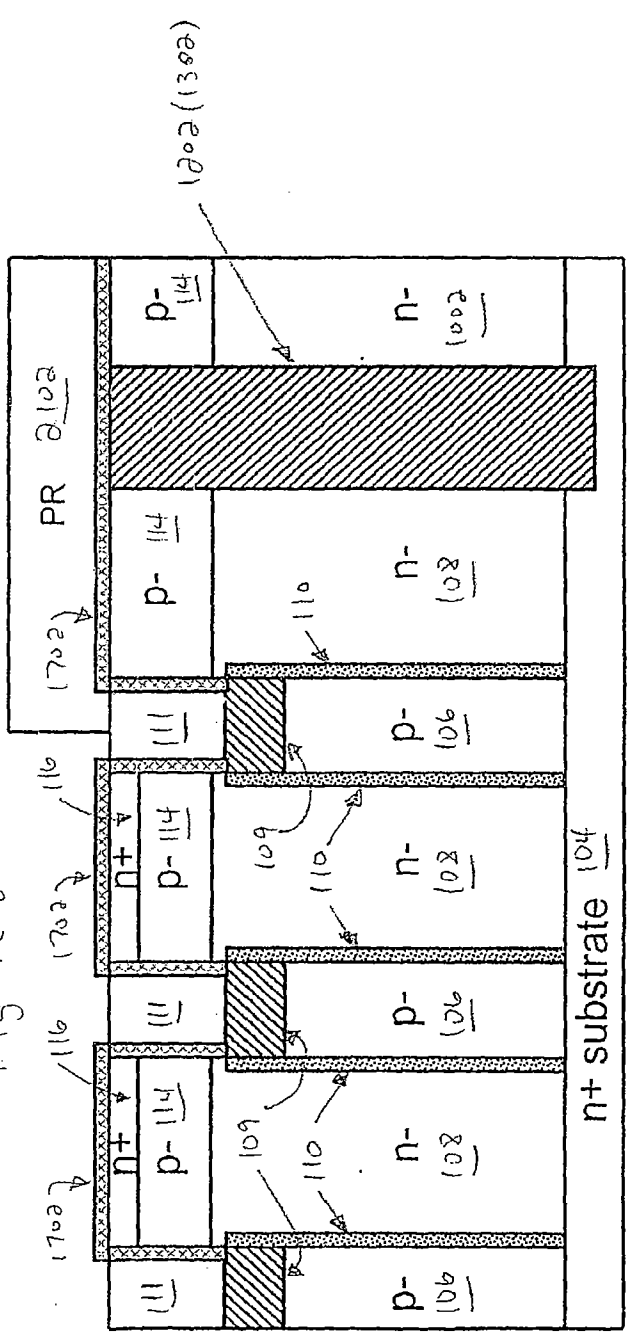
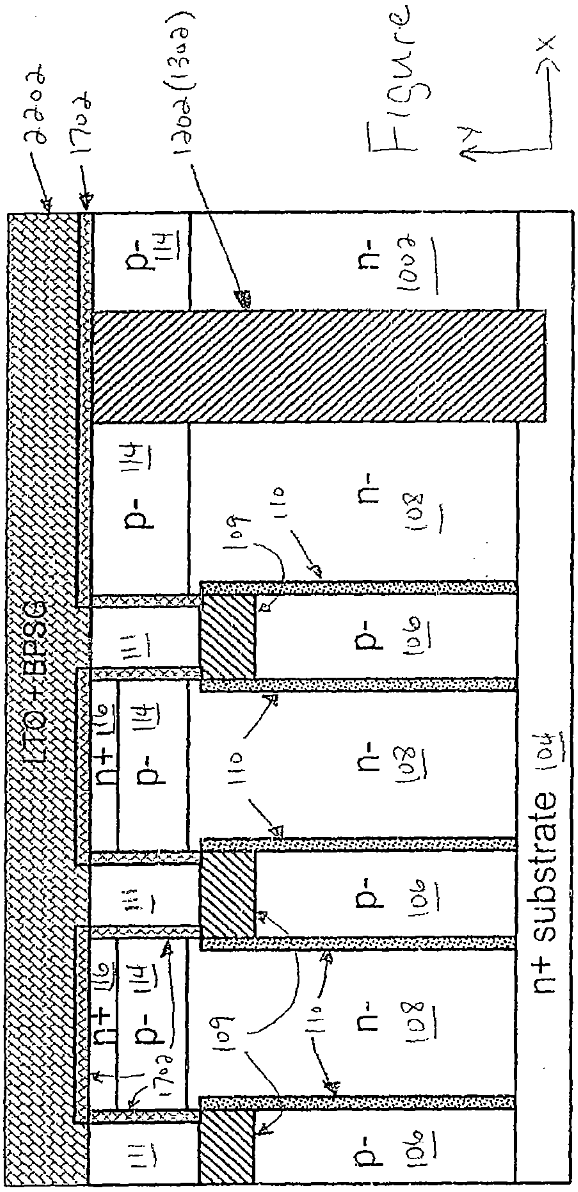


Figure 21



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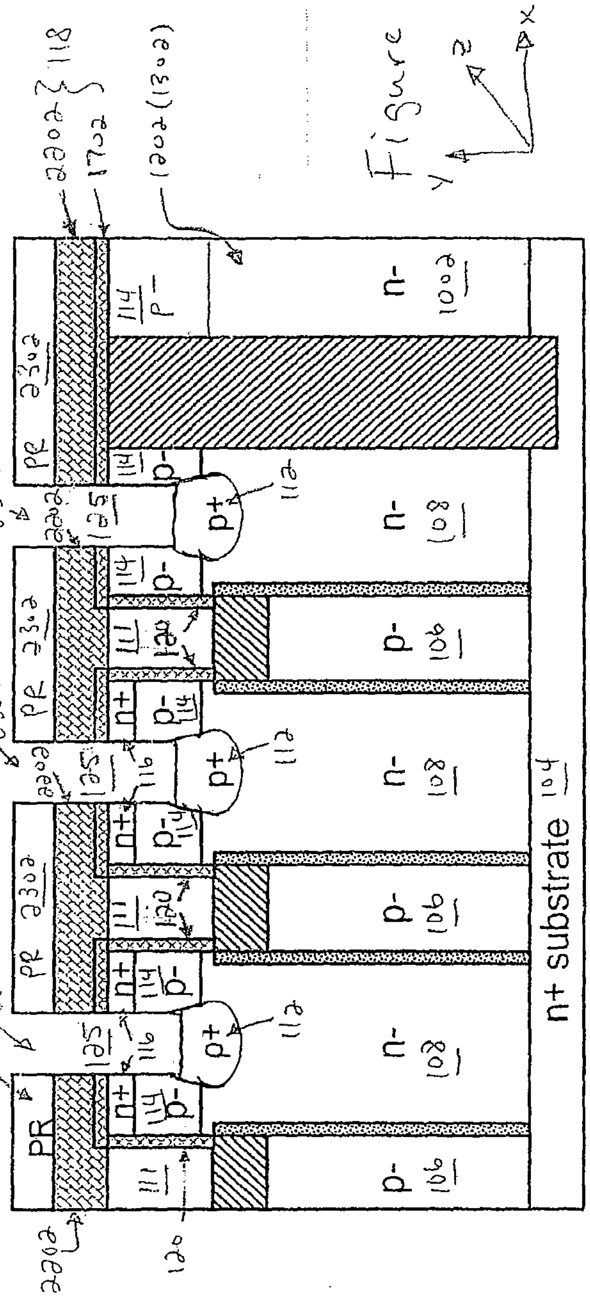
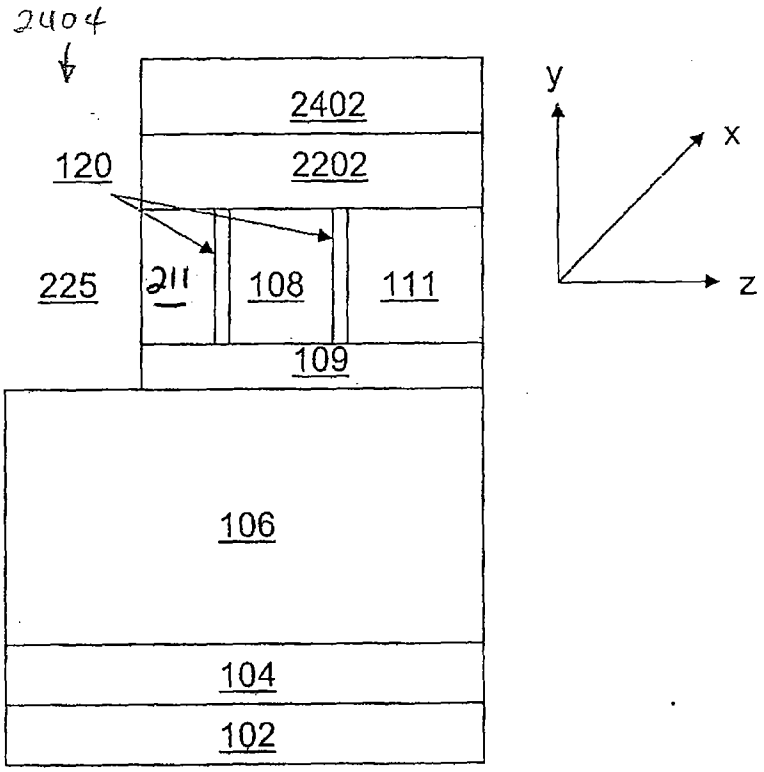


Figure 23



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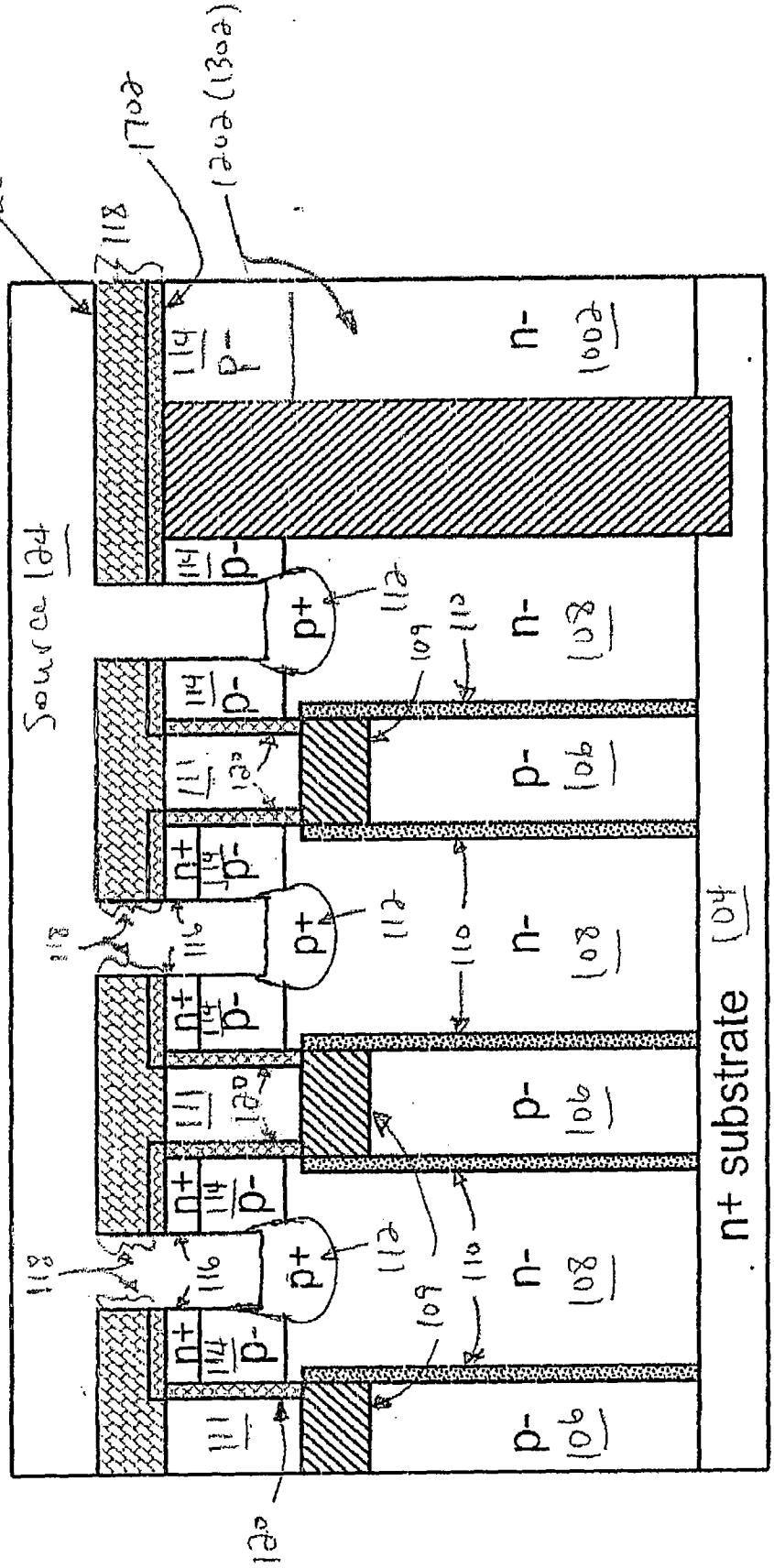
2202
1702
1202 (1302)
118
Source 124
n- 1001
p- 114
p- 111
p+ 112
n- 1081
p- 1061
110
109
n+ substrate 104
1201

Figure 25

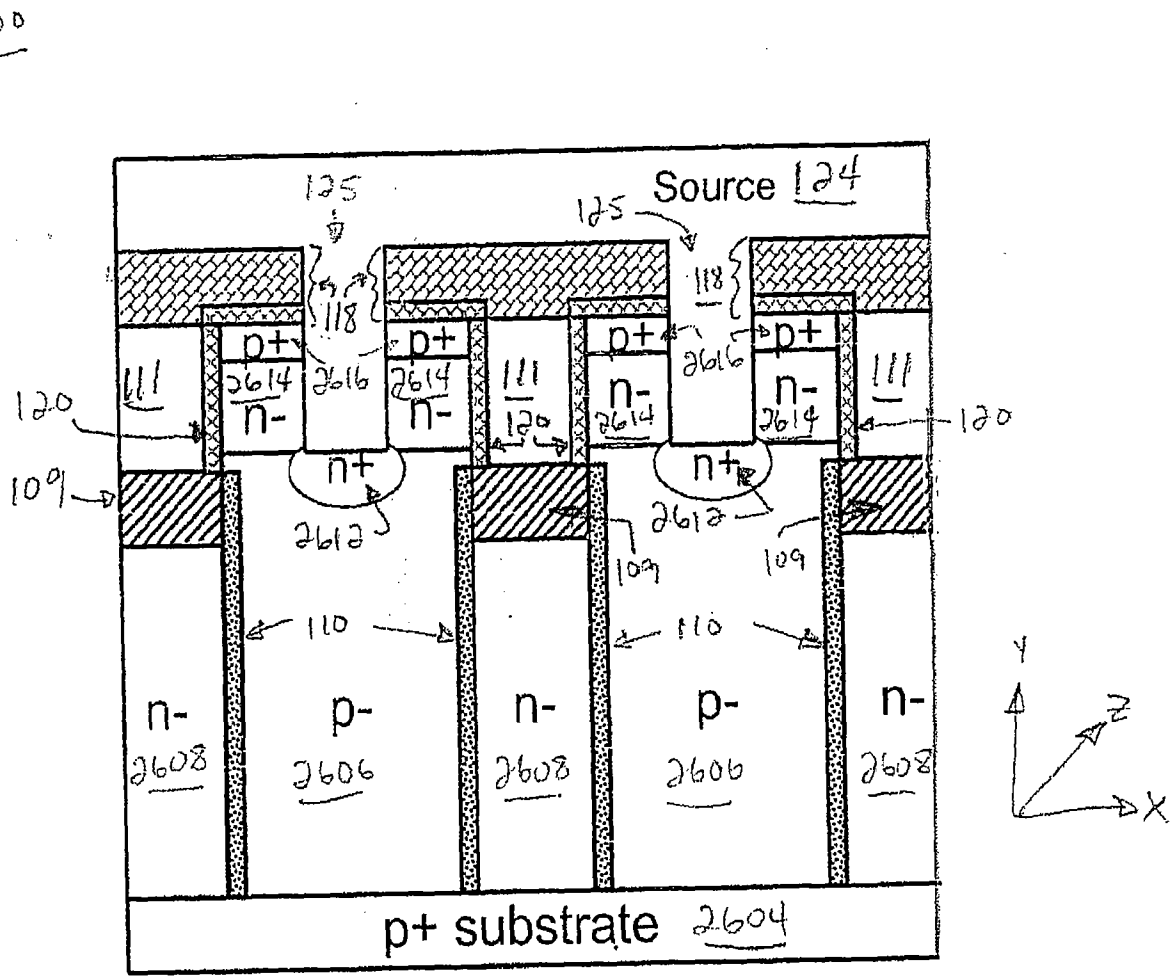
2600
Source 124
125
125
118
118
p+
2614
n-
2616
p+
2614
n-
111
120
p+
n-
2614
2616
p+
n-
2614
111
120
111
120
109
n+
2612
n+
2612
109
109
110
110
n-
2608
p-
2606
n-
2608
p-
2606
n-
2608
p+ substrate 2604
Y
Z
X

Figure 26