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Payne

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[54] **DISPLAY DRIVE MATRIX**

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Related U.S. Application Data

[63] Continuation of Ser. No. 156,773, June 25, 1971, abandoned.

[52] **U.S. Cl.** ..... **340/324 M;** 178/30

[51] **Int. Cl.** **G09f 9/32**

[58] **Field of Search** ..... 340/324 R, 324 M, 336, 340/166 R, 166 EL, 174 TB, 174 LC, 176; 178/30; 219/201, 216

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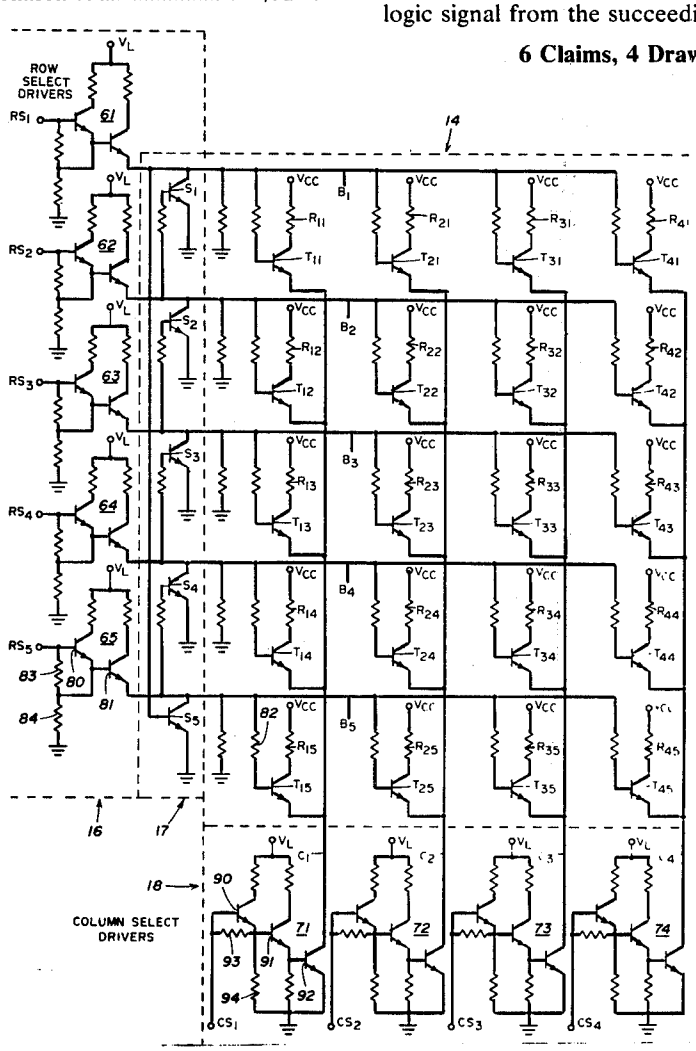
[57] **ABSTRACT**

A thermal display having a plurality of heat dissipative elements arrayed in a matrix comprising a plurality of rows and columns is disclosed. Current through each heat dissipative element is controlled by a separate heater transistor. The bases of all heater transistors in a row are connected together and the emitters of all the heater transistors in a column are connected together. A driver circuit for each row in the matrix applies a voltage to the common connected bases of the heater transistors and a column driver circuit for each column in the matrix produces a driving potential on the common connected emitters of the heater transistors. A MOS character generator produces a scanned output signal which sequentially selects the rows by turning the row driver circuits on, and simultaneously selectively turns the column driver circuits on in accordance with the image to be produced. The heater transistors for the elements which have both row and column select signals applied simultaneously are turned on to form a character within the matrix. The heater transistors in each row are positively driven off by shunting the entire row line to ground using the logic signal from the succeeding row.

6 Claims, 4 Drawing Figures



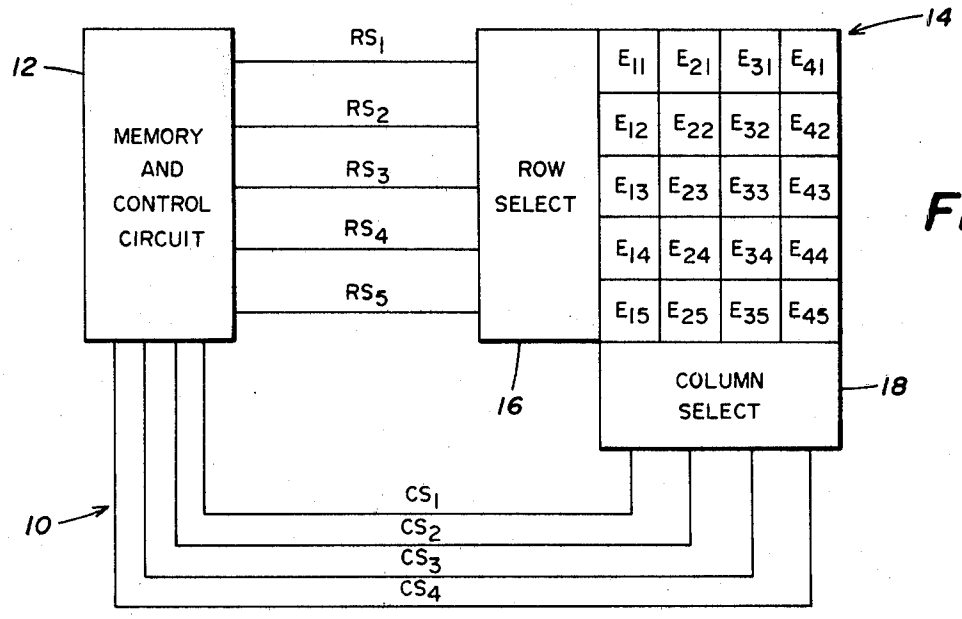


FIG. 1

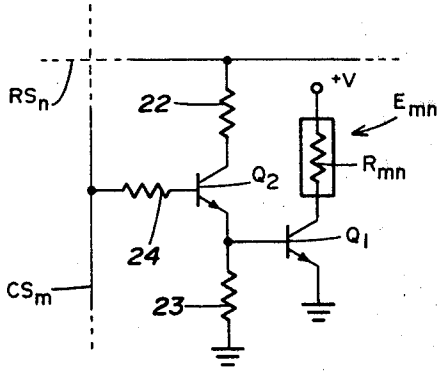


FIG. 2
PRIOR ART

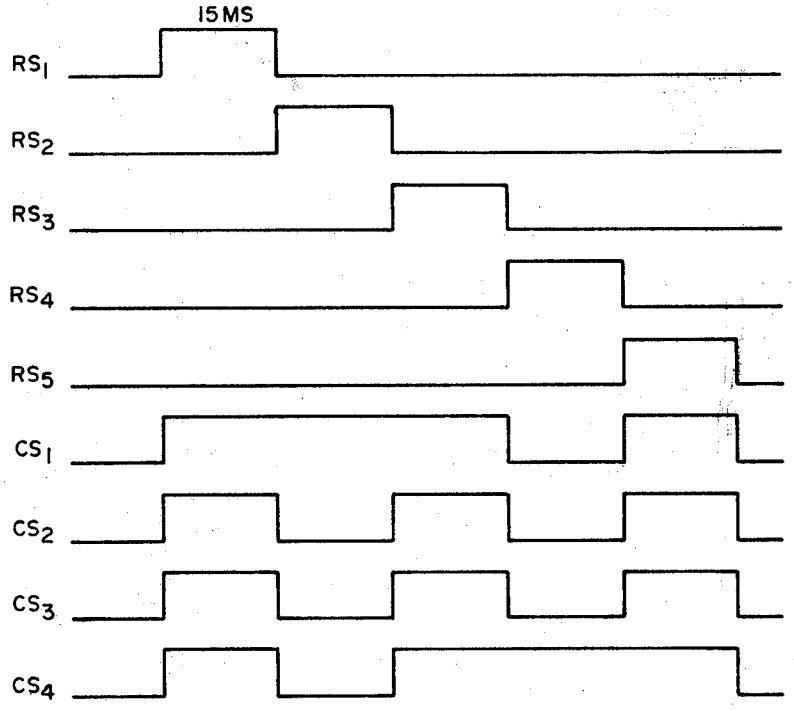
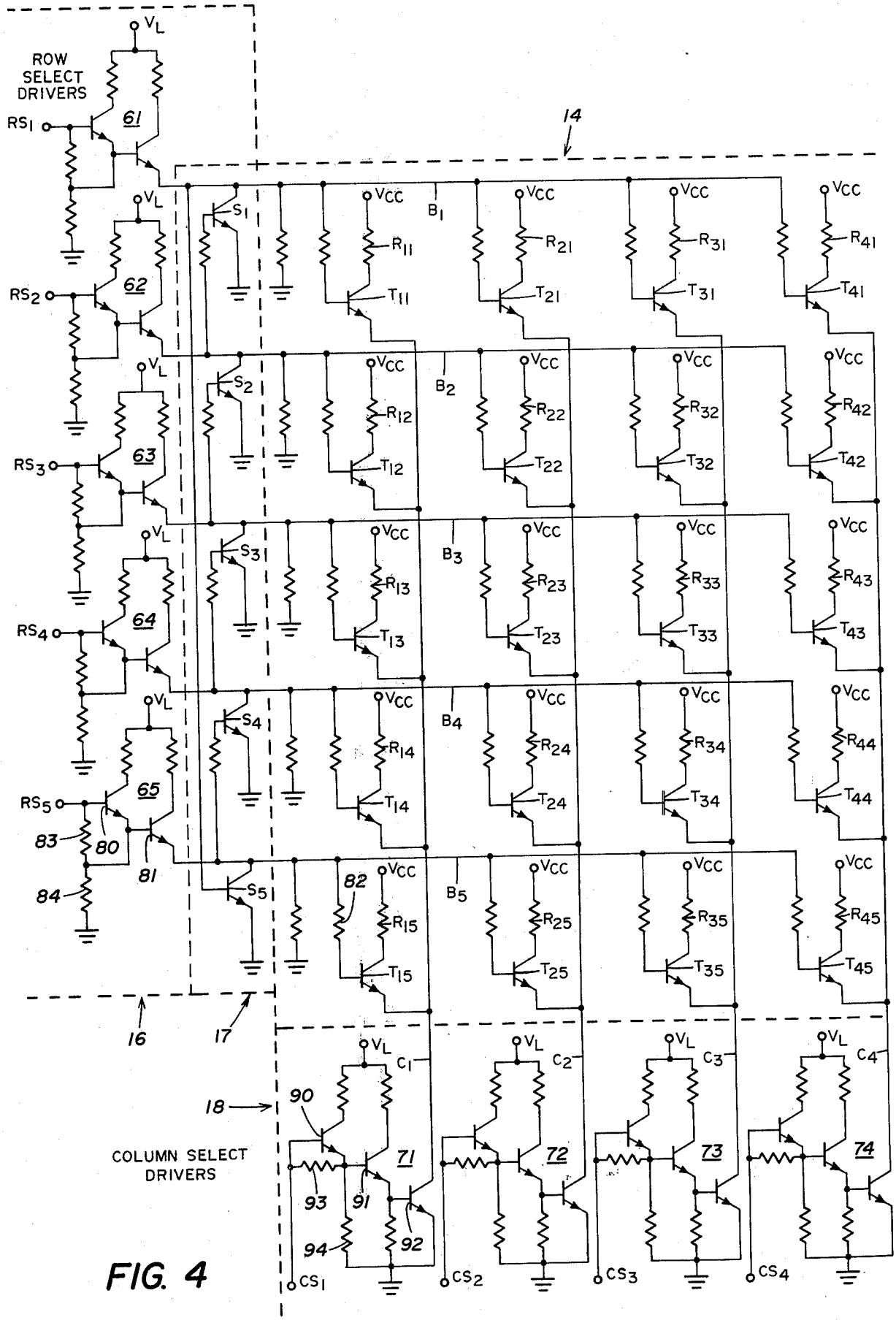


FIG. 3


ROW SELECT DRIVERS
RS1
RS2
RS3
RS4
RS5
61
62
63
64
65
14
16
17
18
83
84
80
81
82
90
91
92
93
94
71
72
73
74
B1
B2
B3
B4
B5
S1
S2
S31
S4
S5
R11
R21
R31
R41
R12
R22
R32
R42
R13
R23
R33
R43
R14
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R34
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R15
R25
R35
R45
T11
T21
T31
T41
T12
T22
T32
T42
T13
T23
T33
T43
T14
T24
T34
T44
T15
T25
T35
T45
VL
Vcc
C1
C2
C3
C4
CS1
CS2
CS3
CS4
COLUMN SELECT DRIVERS

FIG. 4

DISPLAY DRIVE MATRIX

This is a continuation, of application Ser. No. 156,773, filed June 25, 1971 now abandoned.

This invention relates generally to display systems, and more particularly, relates to an improved circuit for operating a matrix of output loads, such as a thermal display system.

A number of different devices are currently being used to display binary data presented in the form of electrical output signals from logic circuitry. For example, one form of optical display may comprise a matrix of light emitting diodes which are selectively energized to produce an alpha-numeric character image. Another form of optical display may comprise a matrix of heatable elements which, upon being energized, form alpha-numeric characters which may be imprinted on heat sensitive paper, or which may be visible directly to the human eye.

In a thermal printer, as is shown in U.S. Pat. No. 3,501,615, assigned to the assignee of the present application, each heater element in a matrix array may comprise a semiconductor body in a mesa shape. When current is passed through the mesa, the mesa heats up, thus heating a dot on a thermally sensitive paper supported adjacent the surface of the mesa. By selectively energizing the heater elements in an array, an alpha-numeric character or other information representation is printed on the thermally sensitive material.

A typical array of display elements may be in the form of a four-by-five matrix. One manner by which the display elements have been selectively energized is by providing twenty individual driving circuits, one for each of the display elements. This type of display requires a relatively large amount of storage circuitry which, even when using (MOSFET) memory and logic circuits, constitutes a significant part of the cost of a small unit, such as a hand held printing calculator. The cost of the MOS logic circuits can be reduced by using a multiplexed or scanned output wherein the rows of a matrix are sequentially addressed or scanned one by one while the columns of the same matrix are selectively energized in synchronism with the respective rows to select the elements within the row which are to be activated. With only a small loss of time, this scanning technique accomplishes the intended purpose of energizing the individual display elements in the character patterns with a minimum number of storage registers and logic circuitry. The display drive matrix of the present invention is particularly suited for use with scanned systems.

Prior art thermal display matrices which have been operated by MOS character generators using the scanned output technique have characteristically suffered from blurred and spurious images. These problems are associated with the operating characteristics of the circuits at "turn-on" and "turn-off," and are hereafter discussed in detail in connection with FIG. **2.**

In accordance with this invention, a plurality of active switching devices, such as transistors, each having input, output and control terminals are arrayed in rows and columns. The output of each active device is connected through a load to one terminal of a power supply. The control of each active device in each row is connected through a resistor to a common row line. The input of all active devices in each column are connected to a column line. A particular active device in the matrix can be switched on to energize the respective load by connecting the respective row line to a drive voltage and connecting the respective column line to the other terminal of the power supply.

The invention also contemplates a system wherein the active devices are positively turned off by a shunt device connecting the row lines to the emitter supply voltage. In the preferred embodiment, each shunt transistor is turned on in response to the drive current of the next successive row line thereby producing active turn-off with no standby power required. The last row line is not shunted but the operational sequence is such that emitter current in all the column lines is terminated. This assures a positive and fast "turn-off" of all switching transistors.

The invention also contemplates unique driver circuits which have low input impedances and a constant voltage input so as to be particularly compatible with MOS character generating logic. The invention is suitable for fabrication as an integrated circuit and for incorporation in a battery operated unit since no standby power is required.

For a more complete understanding of the present invention and for further objects and advantages thereof, reference may now be had to the following description taken in conjunction with the accompanying drawings in which:

FIG. **1** is a block diagram of a display system in accordance with the present invention;

FIG. **2** is a schematic diagram of a portion of a prior art display system;

FIG. **3** is a timing diagram illustrating the signals output from the memory and control circuit of FIG. **1** to the row select and column select circuits;

FIG. **4** is a schematic diagram of a display matrix in accordance with the invention.

Referring now to the drawings, a circuit in accordance with the present invention is indicated generally by the reference numeral **10** in FIG. **1.** The circuit **10** includes a MOS character generator memory and control circuit **12** and a display matrix **14** having elements E_{mn} where m designates columns **1–4** and n designates rows **1–5.** The elements E_{mn} are activated by row select circuitry **16** and column select circuitry **18.** The circuits **16, 17** and **18** may each be fabricated as a separate integrated circuit or all may be contained on one integrated circuit. The matrix **16** is part of the heater element array.

The memory and control circuit **12** controls the row select circuit **16** by five row select lines RS_1–RS_5. These lines are sequentially raised from a logic "0" level near ground potential to a logic "1" positive voltage level sequentially as represented by the timing diagram of FIG. **3** which depicts one scan cycle. The memory and control circuity **12** also has four column select lines CS_1–CS_5 connected to the column select circuit **18.** The levels of the column select line CS_1–CS_4 determine which elements in the selected row of the display matrix are to be energized in order to produce the desired alpha-numeric character. The levels illustrated in FIG. **3** would activate the elements E_{mn} so as to produce the character S, for example.

Before considering the novel circuit of the present invention illustrated in FIG. **4,** it is beneficial to consider the prior art circuit **20** illustrated in FIG. **2,** which is a schematic diagram of the switching circuit typically used for a single element, such as element E_{mn}, of a display matrix. In the circuit, current through a heater re-

sistor R_{mn} is controlled by a switching transistor Q1. In practice the resistor R_{mn} may be an unusually high resistance collection region of the transistor Q1, in which case the two elements may be referred to as a heater transistor. The switching transistor Q1 in turn is controlled by an emitter follower stage Q2 having collector and emitter resistors 22 and 23. The element E_{mn} is addressed and activated by applying positive voltages to a row select line RS_n and a column select line CS_m. If either select line is maintained at ground potential, transistor Q2 will be off, thus keeping transistor Q1 off.

The circuit 20 suffers from inherent problems both at turn-on and turn-off. Consider first, the turn-off problem. Because of the close proximity of transistor Q1 to the heater resistor R_{mn}, the base emitter voltage necessary to cause transistor Q1 to conduct may drop from a normal 0.8 volts to as low as 0.2 volts. Thus, even after transistor Q2 has been turned off by row select line RS_m going to its low state, transistor Q1 may continue to conduct because the collector-base leakage current flowing through transistor Q1, and then through resistor 23 may produce a base-emitter voltage at Q1 greater than that necessary to cause conduction of transistor Q1. The voltage produced across resistor 23 is further enhanced when the column select line CS_m remains high after the row select line RS_n has gone low and row select line RS_{n+1} has gone high because of the forward conduction of the base-emitter diode of transistor Q2.

Now consider the turn-on problem. The forward conduction through the base-emitter diode of transistor Q2 without the collector being energized may also be sufficiently great to spuriously turn transistor Q1 on. The base resistor 24 limits the base-emitter current through transistor Q2 and resistor 23. In order to achieve proper switching of transistor Q1, the relative values of resistors 22, 23 and 24 must be closely controlled. A failure to achieve proper values results either in spurious conduction of switching transistor Q1 or the inability to turn transistor Q2 "on" when appropriate. The spurious conduction of transistor Q1 either at turn-on or turn-off results in blurring of the image produced by the display.

Referring now to FIG. 4, there is shown a schematic diagram of the circuitry for a 4 × 5 matrix of thermal display elements in accordance with the present invention. The circuitry for each element E_{mn} is comprised of a heater resistor R_{mn} and a switching transistor T_{mn} where m is the column number and n is the row number. In practice the resistor R_{mn} may be the collector region of transistor T_{mn}. The appropriate column and row numbers are indicated as subscripts in FIG. 4. Each of the resistors R_{mn} is shown connected between a voltage source V_{cc} and the collector junction of the respective switching transistor T_{mn}. It is to be understood that the heater resistors R_{mn} shown are for use in a thermal printing system and are merely illustrative of other load elements which can be used in other embodiments of the invention.

In FIG. 4, the row select circuit 16 comprises a plurality of row driving circuits 61–65. The column select circuit 18 comprises a plurality of column driving circuits 71–74. The bases of all switching transistors T_{mn} in a row, are connected by a base resistor to a base line B_n which is the output of the respective row driver circuits 61–65. For example, the bases of transistors T_{11}, T_{21}, T_{31} and T_{41} are connected to base line B_1 which is the output of row driver 61. The emitters of all of the transistors T_{mn} in a column are connected to column lines C_m which are the outputs of the respective column driver circuit. For example, the emitters of transistors T_{11}, T_{12}, T_{13} and T_{14} are connected to column line C_1, which is the output of column driver 71.

A particular heater resistor R_{mn} is activated when both the row select line RS_n and the column select line CS_m are at positive voltages which are referred to as logic 1 levels. When RS_3 and CS_2 are both positive, row driving circuit 63 is turned on and applies a positive voltage to the bases of all transistors in the row, i.e., transistors 13, 23, 33 and 43, and the positive voltage on column select line CS_2 turns column driving circuit 72 on, thus connecting the emitters of all transistors in the column, i.e., transistors 21, 22, 23 and 24 to ground. The simultaneous occurrence of both base and emitter drive voltages causes transistor T_{23} to conduct and causes a relatively large current to flow through the heater resistor R_{23} from the source V_{cc} to ground.

In accordance with an important aspect of this invention, a circuit 17 utilizes each successive row enable logic signal to actively drive the transistors of the preceding row "off" in a manner which does not consume stand-by power. The collectors of shunt transistors S_1–S_5 are connected to row lines B_1–B_5, respectively, and the emitters are all connected to ground. The base of each shunt transistor S_1–S_5 is connected by a resistor to the row line which is energized in sequence after the row line to which the collector of the transistor is connected. Thus, the bases of transistors S_1–S_5 are connected to row lines B_2, B_3, B_4, B_5 and B_1, respectively. Thus, as the row select lines RS_1–RS_5 are sequentially brought to a logic 1 level, as illustrated in the scan cycle of FIG. 3, transistors S_1–S_5 are turned on in synchronism with the respective base line to which the collector is connected going low. This assures that the high leakage currents and low base-emitter turn-on voltage of the previously energized transistors T_{mn} which are at an elevated temperature will not result in continued conduction of those transistors T_{mn} but rather will be drained to ground. It will be noted shunt transistors S_1–S_5 are turned on only for the brief period of the next row sequenced. This eliminates standby power consumption which would occur if the shunt transistors S_1–S_5 were to be operated by the complement of the logic level on the respective row select lines RS_1–RS_5.

One of the features of this invention is that the row select circuit 16 and the column select circuit 18 are operated essentially by voltage signals. Consider row driver 65 for example. The maximum voltage on row select line RS_5 when there is a demand for drive current is equal to the sum of the base-emitter voltage drops of transistors 80 and 81 whichever transistors TM_5 of the row are turned on by the column select drivers, and the collector-emitter voltage of the saturated transistor 92 of the column driver. The base resistors 82 of switching transistors T_{mn} are only about 150 ohms and are to assure a more even distribution of the current. Thus, the input voltage is at a consistent maximum of about 4 volts, thus insuring a relatively low input voltage to the bipolar circuit and thereby maintaining a high source-drain voltage across the MOS output device for optimum drive current to the bipolar switching array, when in the logic 1 state. The maximum voltage which can be established on the column drivers 71–74, is also about three times the base-emitter voltage drop of the transis-

tors **90, 81** and **92** (see drive **71**), for example about 3 volts. Resistors **93** and **94**, which are typically about 3.2K ohms each, provide a low impedance input to prevent spurious turn-on by leakage from the MOS character generator in the logic 0 state. The resistors **83** and **84** are relatively low, typically about 4.2K and 8.4K, respectively, to provide a low input impedance. This prevents leakage currents from the MOS output device in the logic 0 state from turning the transistors **80** and **81** on.

In the operation of the system **10**, thermally sensitive paper is positioned adjacent the face of the matrix **14.** When a character is to be printed on the paper, the memory and control circuit **12** produces a scan cycle such as illustrated in FIG. **3.** During each scan cycle, the row lines RS_1–RS_5 are sequentially brought from a logic 0 level near ground potential to a logic 1 level that is sufficiently positive to turn the respective row driver circuits **61–65** on for brief periods, typically about **15** milliseconds. It will be noted that no two row select lines are at a logic 1 level at any point in time, so that only one row of transistors T_{mn} are enabled by base voltage at any time during the scan cycle. During the period when each of the rows is enabled, one or more of the columns select lines may be at a logic 1 level so that any number of the transistors in the enabled row may be turned on. For example, from FIG. **3** it will be noted that column select lines CS_1–CS_4 are all at a logic 1 level during the period of time that row select line RS_1 is at a logic 1 level. Thus, all transistors T_{11}, T_{21}, T_{31} and T_{41} are turned on during the scan cycle shown in FIG. **3** because the emitters of these transistors are near ground plus the drop across the saturated transistor **92,** and the bases at the positive voltage produced by the row drivers when turned on. During the period that row select line RS_2 is at a logic 1 level, only column select line CS_1 is at a logic 1. Thus, only transistor T_{12} is turned on and transistors T_{22}, T_{32} and T_{42} remain off because the column driver circuits **72, 73** and **74** remain off, and the emitters of these transistors are not connected to ground. During the time that row select line RS_3 is high, all four column select lines CS_1–CS_4 are also high, so that transistors T_{13}, T_{23}, T_{33} and T_{43} are all turned on. Only transistor T_{44} is turned on when row select line RS_4 is high, and transistors T_{15}, T_{25}, T_{35} and T_{45} are all turned on when row select line RS_5 is high. Thus, the character S is produced during the scan cycle shown in FIG. **3.** The paper is then stepped to the next character position and the scan cycle repeated with the appropriate levels on the column select lines CS_1–CS_4 to produce the next character.

The shunt transistors S_1–S_5 insure that all transistors T_{mn} are turned off at the time the respective row select line RS_1–RS_5 reverts to a logic 0 level. Referring to FIG. **3,** it will be noted that when row select line RS_1 transitions from a logic 1 level to a logic 0 level, row select line RS_2 transitions from a logic 0 level to a logic 1 level. The logic "**1**" level on row select line RS_2 turns shunt transistor S_1 on, thus connecting the bases of all transistors in the first row to ground to insure that these transistors turn off, even if at an elevated temperature which results in low base-emitter turn-on voltages and high leakage current. Similarly, as row select lines RS_3, RS_4 and RS_5 sequentially go positive, row lines B_2, B_3 and B_4 are grounded by shunt transistors S_2, S_3 and S_4, respectively.

The transistors in row **5** may be assured of being turned off in either one of two ways. As will be noted in FIG. **3,** all column select lines CS_1–CS_4 may be returned to a logic 0 at the end of the scan cycle, thus disconnecting the emitters of transistors T_{15}, T_{25}, T_{35} and T_{45} from ground. When operating in this mode, transistor S_5 is not required. When operating in a mode where row select RS_1 goes to a logic 1 level in synchronism with row select line RS_5 going to a logic 0 level, as might be the case when operating the matrix **14** to provide a persistent visible character, transistor S_5 can be turned on by the output from row driver **61** when row select line RS_1 goes to a logic 1 level.

From the above, it will be appreciated that the present invention provides a thermal display system that may utilize MOS memory and control circuits, which has not heretofore been satisfactorily achieved. The present invention overcomes the turn-on and turn-off problems of the prior art systems described above.

The present invention has been successfully fabricated in integrated circuit form, which is essential for all practical purposes in systems of this type. It will be noted that the column lines and column drivers which carry the relatively large collector currents of the heater transistors need control only the current through one heater resistor at any time.

In accordance with a broader aspect of the invention, the roles of the rows and columns may be reversed. In such case, five column lines and four row lines may be provided. The column lines can then be successively enabled or scanned and the row lines activated to produce the appropriate image. In such a case, opening the emitters of the transistors will ensure that the transistors are turned off after each enable period. However, the column drivers would then be required to switch four times as much current because all four elements in the column could be turned simultaneously. This would be very difficult to achieve in integrated circuit form. Thus, although the special turn-off circuitry of the circuit of FIG. **3** could be eliminated, the increased size required of the column drivers to handle the additional emitter current prevents such a system from being used, at least with current integrated circuit technology. However, such a system is useful if discrete transistors are used to switch the emitter current.

Although a thermal printer has been selected as the embodiment of the invention herein described, it should be understood that any load matrix can be driven by the invention, and that such invention is also particularly suited to drive a visable display matrix. A sustained image can be provided merely by repeating the scan cycle at a rate which would be integrated by either the display matrix or the human eye. In the latter case, shunt transistor S_5 is particularly useful.

From the above description of a preferred embodiment of the invention, it will be noted that a minimum number of active devices are required at each heater element of the matrix, thereby providing maximum reliability. The driver circuits **16** and **18** are fabricated as separate integrated circuit packages away from the heater elements for increased reliability. Base-emitter select is used in the transistors TE_{mn} rather than collector-base select which provides better control. The MOS character generator output, which is essentially a current source because of the high output impedance of the MOS device, sees a low input impedance, and also a low input voltage, at both the row and column drivers

for both the logic 0 and the logic 1 state. This provides optimum operating conditions for the MOS circuit. Leakage currents when the MOS circuit is at a logic 0 state are connected directly to ground by both the row and column drivers. The low voltage at the inputs of the driver stages result in a maximum drain-to-source voltage across the output stages of the MOS circuits thereby producing higher output currents than have heretofore been available. Static charge build-ups at the inputs are kept at a minimum because of the low input impedances. The positive turn-off of the transistors T_{mn} during succeeding row activation by way of the saturated shunt transistors S_1–S_5 provides positive and fast turn-off, thereby eliminating erroneous printing and blurring. At the end of each complete print cycle, there is a positive turn-off of all switching transistors by way of the emitters. No stand-by power is required so that the system may be used in battery operated portable units. Loose components tolerances are acceptable in both the row and column driver integrated circuits.

Having described the invention in connection with certain specific embodiments thereof, it is to be understood that further modifications may now suggest themselves to those skilled in the art, and it is intended to cover such modifications as may fall within the scope of the appended claims.

What is claimed is:

1. In a display system, the combination of:
   a. a plurality of switching transistors arranged in columns and rows with each column comprising one transistor from each row and each row comprising one transistor from each column;
   b. row lines or column lines commonly connecting the bases of all transistors in a row or column;
   c. the other of said row lines or column lines electrically connecting the emitters of all transistors in a row or column;
   d. row select means coupled to the row lines for selecting a specific row for actuation;
   e. column select means coupled to the column lines for selecting specific columns for actuation;
   f. means for sequentially actuating one of said row select means and said column select means to obtain sequential actuation of the corresponding row lines or column lines; and
   g. means for selectively actuating the other of said row select means and said column select means, in accordance with the image to be displayed, in synchronization with said sequential actuation of said one thereof, such that each coincidental actuation of a row line and a column line turns on a corresponding transistor.

2. The display system according to claim 1 and further including a matrix of load elements for generating visible character images when energized in predetermined combinations, said load elements respectively connected to a collector of a switching transistor.

3. The display system according to claim 1 wherein the row select means includes means for discharging the previous row line in response to actuation of the row line next in sequence.

4. The display system according to claim 1 further including means for deactuating all the column lines after all row lines have been sequentially actuated.

5. The display system according to claim 1 wherein said load elements comprise heat dissipating devices, and said display system constitutes a thermal printing system.

6. The display system of claim 1 wherein said means for selectively actuating the other of said row select means and said column select means includes a driver circuit for selectively connecting each corresponding row line or column line to a supply voltage in response to logic control signals; and

logic means coupled to said driver circuit for selectively operating said driver circuit to connect the corresponding row lines or column lines to the voltage supply in accordance with the image to be displayed.

* * * * *