United States Patent

Grobert et al.

[54] **FOUR QUADRANT MULTIPLIER USING BI-POLAR DIGITAL ANALOG CONVERTER**

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[57] **ABSTRACT**

There is disclosed a four quadrant multiplier circuit whose output is the bi-polar product of a signed analog voltage and a signed voltage expressed as a digital word. The circuit includes matrix resistors in a bi-polar converter which are switched between the reference voltage and the inverse of the reference voltage. Four quadrant multiplication is accomplished with only one resistor matrix and the use of complementary transistor pairs as bi-polar matrix resistor switches.

5 Claims, 1 Drawing Figure

BINARY WORD INPUT
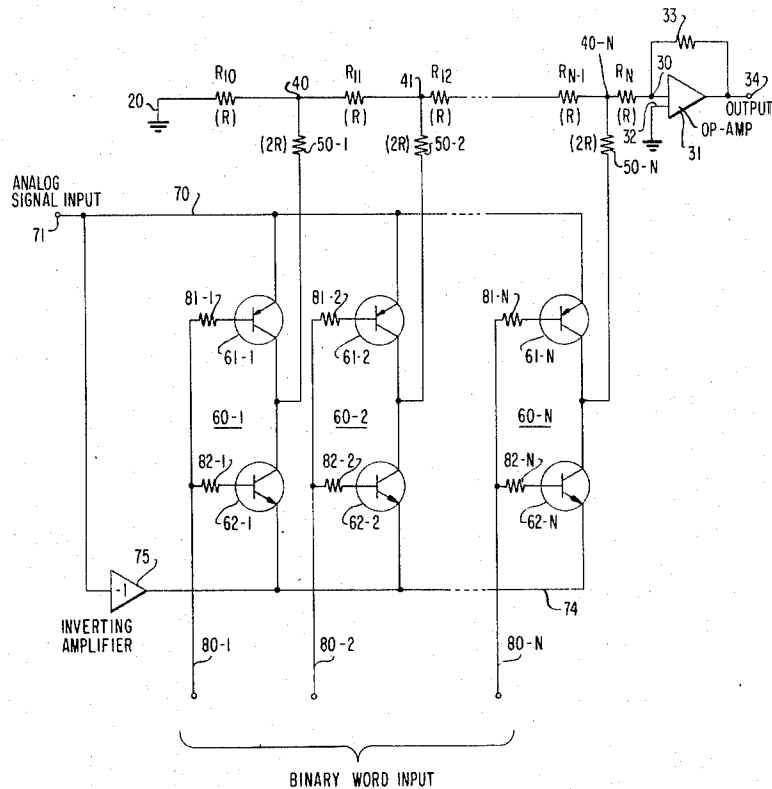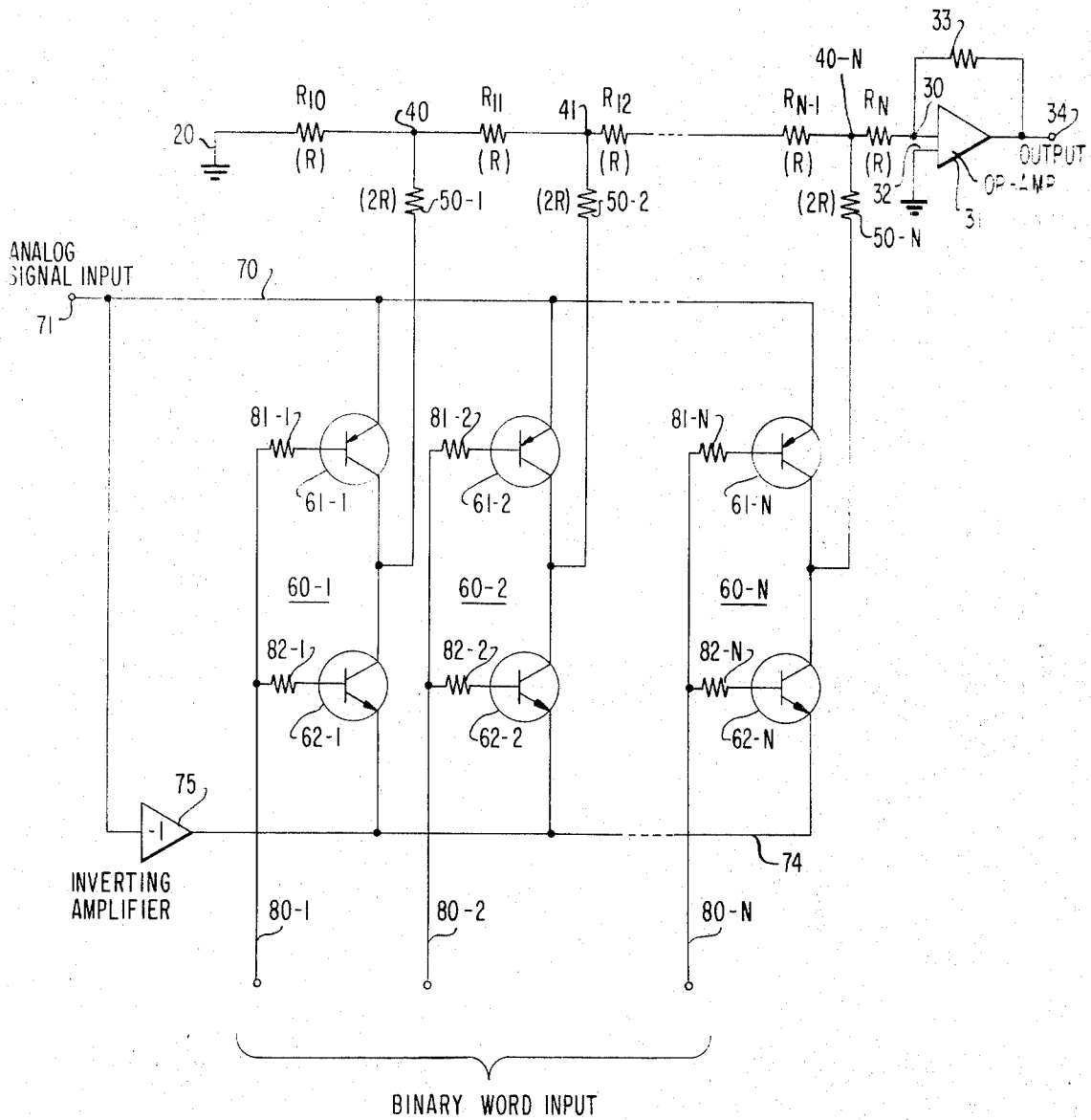
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FOUR QUADRANT MULTIPLIER USING BI-POLAR DIGITAL ANALOG CONVERTER

The invention herein described was made in the course of or under a contract or subcontract thereunder, or grant, with the Department of the Air Force.

The present invention is directed to a signal processing system and circuit for performing four quadrant multiplication.

BACKGROUND OF THE INVENTION

There are a number of four quadrant multiplier circuits known and currently used which accept plus or minus for two input signals which are to be multiplied and give a product with the correct sign. Some of these involve the use of two quadrant multipliers which are made to behave as four quadrant devices as by adding a constant voltage to a variable that is not permitted to change signs. In other prior art four quadrant multipliers, the sign digit of the digital variable is used for switching purposes at the output of an operational amplifier in order to produce a four quadrant multiplier. (See Digital Techniques in Analog Computers- Proceedings Western Joint Computer Conference 60–63, San Francisco, Calif., Feb. 1956 and Handbook of Automation Computation and Control, Vol. 2, Wiley, Page 28–16, 28–18). Other known prior art multipliers which use digital to analog converters depend upon matrix resistors which are switched between the reference voltage and ground.

In the present invention, low distortion four quadrant multiplication is achieved by using a resistor matrix and bi-polar matrix resistor switches which essentially switch the matrix resistors in the bi-polar converter between the reference voltage (a signed analog signal voltage) and the inverse of the reference voltage. In this way, the output of the operational amplifier or summing circuitry is the bi-polar product of a signed analog voltage and a signed voltage expressed as a digital word. An important feature of the invention is that four quadrant multiplication is achieved with only one resistor matrix and the use of complementary transistor pairs as bi-polar matrix resistor switches.

DESCRIPTION OF THE PREFERRED EMBODIMENT

With reference now to the drawing, the circuit includes a resistor matrix comprised of resistors R10, R11, R12, ... Rn-1 and RN connected between ground or common 20 and input terminal 30 of a conventional operational amplifier 31, the other input 32 of which is connected to ground or common. As is likewise conventional, a feedback resistor 33 between output terminal 34 and input terminal 30 is provided so that operational amplifier 31 is, in the configuration shown, a summing device. Intermediate points 40, 41...40-N between resistors R10, R11, R12, ... RN-1 and RN, respectively, are connected through like value resistors 50–1, 50–2, ... 50-N to the collector electrodes of complementary transistor pairs 60–1, 60–2, ... 60-N. These bi-polar switches are all identical circuits and each is constituted by a PNP transistor 61 and an NPN transistor 62. The emitter electrodes of all PNP transistors are connected directly to a reference line 70 to which is applied, at terminal 71, the signed analog signal input. All emitter electrodes of the NPN

transistors are directly connected to conductor line 74 to which the inverse of the analog signal on reference line 70 is applied, this being developed by means of an inverting amplifier 75 which is also connected to receive the analog signal input applied to terminal 71. The base electrodes of each complementary transistor pair, respectively is connected to a matrix switching line 80–1, 80–2, ... 80-N, the binary ones or zeros on each of the matrix switching lines being applied commonly to the bases of the PNP transistors 61 and the NPN transistors 62 of the complementary pair through like base resistors 81 and 82.

In the multiplication of two signals used in the circuit, one signal is expressed as a digital word which is applied to the matrix switching lines 80–1, 80–2 ... 80-N so that these binary bits are applied to the matrix switches constituted by the complementary transistor pairs 60–1, 60–2, ... 60-N. The analog signal voltage and the inverse thereof are applied to references lines 70 and 74, respectively. As shown in the drawing, the analog signal input is applied to line 70 while the inverse thereof as developed by inverting amplifier 75 is applied to inverse reference line 74. Each bit, being either a binary "1" or "0," switches or connects the corresponding matrix resistor 50–1, 50–2, ... 50-N to the reference voltage or its inverse.

The operation of the complementary transistor pairs as a switch is as follows. If the binary matrix switching line 80 to a particular switch is positive (assume this to be a binary "1") the PNP transistor 61 is cut off and the NPN transistor 62 is saturated, connecting the matrix resistor to the inverse reference line 74. If the signal on a particular matrix switching line 80 is negative (e.g. a binary "0") the NPN transistor 62 is cut off and the PNP transistor 61 is saturated thus connecting the matrix resistor to the reference line 70. Depending upon the polarity of the analog signal, the matrix resistor current will flow in either direction through the transistors, making use of the property that the collector and emitters can be interchanged. It should be noted that the magnitude of the voltage for a binary "1" or a binary "0" on each binary line must be greater than the maximum magnitude of the analog signal voltage on the reference lines.

Since the output of the matrix is held at a virtual ground by the operational amplifier 31 which it drives, the current into the summing node 30 will be the sum of the binary weighted currents. The magnitude and sign of this sum will depend on the binary word applied to the matrix switching lines 80 and the magnitude and sign of the signal applied to reference lines 70 and 74. Thus, for example, if the binary word is 10000000 or 01111111 (considering an eight bit word) then almost no current flows into the summing node and the multiplier output is near zero regardless of the reference voltage. If the reference voltage is zero, than the multiplier output is zero for any binary word. Thus, the multiplier output is a bi-polar product of two signed voltages.

While the invention has been described in terms of an analog signal input applied to reference terminal 70 and digital inputs supplied on each matrix switching line, it would be appreciated that the voltages may be either analog, digital, or both.

It will be understood that the foregoing disclosure relates to the preferred embodiment of the invention and that numerous modifications or alterations may be made without departing from the spirit and scope of the invention.

What is claimed is:

1. A four quadrant multiplier circuit for obtaining the bi-polar product of a pair of signed signal voltages, the first of which is a signed analog voltage and the second of which is a signed voltage in the form of a digital word, comprising,

a pair of reference conductors, means for applying said signed analog voltage to the first of said reference conductors, means for producing the inverse of said signed analog voltage and applying same to the second of said reference conductors, a resistor matrix network having a current summing node therein,

a plurality of bi-polar switch means equal in number to the number of binary bits in said digital word, each bi-polar switch means being connected between said pair of reference conductors and selectively operated in response to a voltage, each constituting a binary bit, each said voltage constituting said binary bits being greater in magnitude than the maximum magnitude of the voltages on said reference conductors, respectively, to connect one of said reference conductors to said resistor matrix and cause a current to flow therein to said summing node according to the binary significance thereof, respectively, and

an operational amplifier having one input thereof connected to said current summing node and the other input thereof connected to ground.

2. The invention defined in claim 1 wherein said bi-polar switches are constituted by complementary transistor pairs.

3. The invention defined in claim 2 wherein the emitter electrodes, respectively, of said complementary transistor pairs are connected to said reference conductors, and the collectors are connected to each other and to said resistor matrix and the binary bits are applied to the base electrodes thereof.

4. A four quadrant multiplier circuit for obtaining

the bi-polar product of a pair of signed signals, the first being a signed analog voltage and the second being a signed voltage in the form of a digital word, comprising,

a pair of reference conductors, means for applying said signed analog voltage to the first of said reference conductors, means for producing the complement of said signed analog voltage and applying same to the second of said reference conductors, a resistor matrix including a first set of like value resistors connected in series between a summing node and a point of common potential, and a second set of resistors, one end of each said second resistor set being connected to intermediate points between the resistors in said first resistor set, respectively, the number of resistors in said second set being equal to the number of binary bits in said digital word, and

a plurality of bi-polar switches, each bi-polar switch being constituted by a complementary transistor switching pair, there being one bi-polar switch for each resistor in said second set of resistors, for selectively connecting the other ends of said second set of resistors to one of said reference conductors in accordance with the character of the binary bit assigned thereto.

5. A method of obtaining the bi-polar product of two, signed signal voltages one of said signed signal voltages being an analog voltage and the other being a binary code permutation of the binary word, equivalent of the other of said signed signal voltages, comprising,

generating the inverse of said signed analog signal voltage and connecting said signed signal voltage and the inverse of said signed signal voltage to a series connected resistor matrix at a plurality of points therein in accordance with the binary code permutation of the binary word equivalent of the other of said signed signal voltages to cause a current to flow in said series resistor matrix to a summing node, said current being the sum of the binary weighted currents and having a magnitude and sign dependent on the said binary word equivalent and the magnitude and sign of said analog voltage.

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