(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
07 September 2018 (07.09.2018)

WIPO | PCT

(10) International Publication Number
WO 2018/157563 A1

(51) International Patent Classification:
G06F 3/041 (2006.01)

(21) International Application Number:
PCT/CN2017/097471

(22) International Filing Date:
15 August 2017 (15.08.2017)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
201710123374.6 03 March 2017 (03.03.2017) CN

(71) Applicants: **BOE TECHNOLOGY GROUP CO., LTD.** [CN/CN]; No. 10 Jiuxianqiao Rd., Chaoyang District, Beijing 100015 (CN). **BEIJING BOE OPTOELECTRONICS TECHNOLOGY CO., LTD.** [CN/CN]; No. 8 Xihuanzhonglu, BDA, Beijing 100176 (CN).

(72) Inventors: **LIU, Chong**; No. 9 Dize Rd., BDA, Beijing 100176 (CN). **ZHAO, Haisheng**; No. 9 Dize Rd., BDA, Beijing 100176 (CN). **XIAO, Zhilian**; No. 9 Dize Rd., BDA, Beijing 100176 (CN). **XIAO, Hongxi**; No. 9 Dize Rd., BDA, Beijing 100176 (CN). **WANG, Wei**; No. 9 Dize Rd., BDA, Beijing 100176 (CN). **PEI, Xiaoguang**; No. 9 Dize Rd., BDA, Beijing 100176 (CN).

(74) Agent: **TEE & HOWE INTELLECTUAL PROPERTY ATTORNEYS**; CHEN, Yuan, 10th Floor, Tower D, Minsheng Financial Center, 28 Jianguomennei Avenue, Dongcheng District, Beijing 100005 (CN).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report (Art. 21(3))*

(54) Title: ARRAY SUBSTRATE, FABRICATION METHOD AND DISPLAY DEVICE

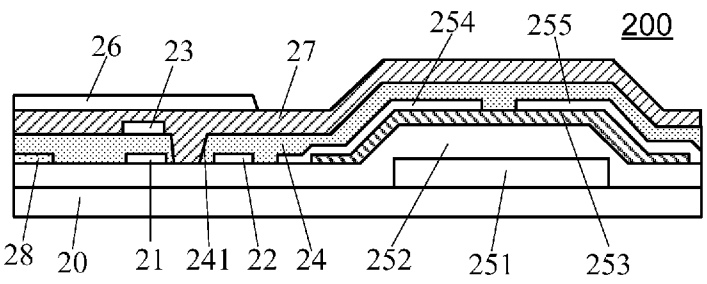


FIG. 2

(57) Abstract: An array substrate (200) includes a substrate (20), a first signal line (21) and a second signal line (22) on the substrate (20), an insulating layer (24) covering the first signal line (21) and the second signal line (22), and a groove (241) penetrating through the insulating layer (24). The first signal line (21) and the second signal line (22) are arranged in a same layer and separated from each other. The groove (241) is between the first signal line (21) and the second signal line (22).

WO 2018/157563 A1

ARRAY SUBSTRATE, FABRICATION METHOD AND DISPLAY DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This PCT patent application claims priority to Chinese Patent Application No. 201710123374.6, filed on March 3, 2017, the entire contents of which are incorporated herein by reference.

TECHNICAL FIELD

[0002] The present disclosure generally relates to display technologies and, more particularly, to an array substrate, a fabrication method thereof, and a display device containing the array substrate.

BACKGROUND

[0003] A touch display panel, such as an embedded touch display panel of a self-capacitance structure type, may include a plurality of block-shaped touch electrodes. Each touch electrode is coupled to a driving circuit through a touch signal line. The driving circuit receives a signal change through each touch signal line and the coordinate position of each touch electrode to determine the touch position.

[0004] Generally, in the existing technology, a parallel signal line is coupled to a touch signal line in parallel in an array substrate of a touch display panel. However, in a patterning process, a conductive residue may also be generated between the parallel signal line and a data line due to the influence of dust or other foreign matter, causing sub-pixels in the touch display panel not to display properly.

SUMMARY

[0005] In one aspect, the present disclosure provides an array substrate including a substrate, a first signal line and a second signal line on the substrate, an insulating layer covering the first signal line and the second signal line, and a groove penetrating through the insulating layer. The first signal line and the second signal line are arranged in a same layer and separated from each other. The groove is between the first signal line and the second signal line.

[0006] Another aspect of the present disclosure provides a fabrication method for an array substrate including providing a substrate and forming a pattern including a first signal line

and a second signal line on the substrate. The first signal line and the second signal line are arranged in a same layer and separated from each other. The method further includes forming an insulating layer covering the first signal line and the second signal line, and forming a groove penetrating through the insulating layer and between the first signal line and the second signal line.

BRIEF DESCRIPTION OF THE FIGURES

[0007] The following drawings are merely examples for illustrative purposes according to various disclosed embodiments and are not intended to limit the scope of the present disclosure.

[0008] FIG. 1 illustrates a schematic view of an array substrate in the existing technology;

[0009] FIG. 2 illustrates a schematic view of an exemplary array substrate according to various disclosed embodiments of the present disclosure;

[00010] FIG. 3 is a plan view illustrating an exemplary distribution of first signal lines and second signal lines in the exemplary array substrate in FIG. 2 according to various disclosed embodiments of the present disclosure;

[00011] FIG. 4 illustrates a flow chart of an exemplary fabrication method for an exemplary array substrate according to various disclosed embodiments of the present disclosure;

[00012] FIG. 5 illustrates another flow chart of an exemplary fabrication method for an exemplary array substrate according to various disclosed embodiments of the present disclosure; and

[00013] FIG. 6 illustrates a schematic view of an exemplary display device according to various disclosed embodiments of the present disclosure.

[00014] Reference numerals used in the drawings include: 11, touch signal line; 12, parallel signal line; 13, touch electrode; 14, data line; 15, conductive residue; 20, substrate; 21, first signal line; 22, second signal line; 23, third signal line; 24, insulating layer; 241, groove; 251, gate electrode; 252, gate insulating layer; 253, active layer; 254, source electrode; 255, drain electrode; 26, touch electrode; 27, passivation layer; 28, pixel electrode; 100, array substrate; 200, array substrate; 400, fabrication method; 500, fabrication method; 600, display device.

DETAILED DESCRIPTION

[00015] Exemplary embodiments of the disclosure will now be described in more detail with reference to the drawings. It is to be noted that, the following descriptions of some embodiments are presented herein for purposes of illustration and description only, and are not intended to be exhaustive or to limit the scope of the present invention.

[00016] FIG. 1 illustrates a schematic view of an array substrate 100 in the existing technology. In order to improve the accuracy of determining the touch position, a parallel signal line 12 and a touch signal line 11 may generally be coupled in parallel, thereby reducing the connection resistance between a driving circuit and the touch electrode 13, i.e. the total resistance of the touch signal line 11 and the parallel signal line 12 in parallel. The parallel signal line 12 and the touch signal line 11 may be coupled in parallel in the non-display region. FIG. 1, however, illustrates a sectional view of the display region and thus the connection between the parallel signal line 12 and the touch signal line 11 is not shown in FIG. 1. In order to reduce the number of process steps, the parallel signal line 12 and the data line 14 may be fabricated by a same patterning process. When the data line 14 and the parallel signal line 12 are formed in the patterning process, a conductive residue 15 may be generated between the data line 14 and the parallel signal line 12 due to the influence of dust or other foreign matter. As a result, a short circuit between the data line 14 and the parallel signal line 12 may occur.

[00017] The touch electrode 13 may function as a common electrode during a display phase. That is, the parallel signal line 12 may be loaded with a common voltage signal during the display phase. Accordingly, when the data line 14 and the parallel signal line 12 are short-circuited, the voltage on the data line 14 may be pulled down to the common voltage on the parallel signal line 12. Thus, the data line 14 may fail to provide the desired data voltage for sub-pixel during the display phase, further causing the sub-pixels not to display properly, resulting in display defects.

[00018] FIG. 2 illustrates a schematic view of an exemplary array substrate 200 according to various disclosed embodiments of the present disclosure. As shown in FIG. 2, the array substrate 200 includes a substrate 20, and a first signal line 21, a second signal line 22, and an insulating layer 24 disposed above the substrate 20. The first signal line 21 may be arranged in the same layer as the second signal line 22. That is, a layer where the first signal line 21 is

located may coincide with a layer where the second signal line 22 is located. The first signal line 21 is separated from the second signal line 22. The insulating layer 24 covers the first signal line 21 and the second signal line 22. A groove 241 is formed in the insulating layer 24 and penetrates the insulating layer 24. The position of the groove 241 may correspond to a spacing region between the first signal line 21 and the second signal line 22. That is, the groove 241 may be between the first signal line 21 and the second signal line 22. The groove 241 may extend to the bottom surface of the layer in which the first signal line 21 and the second signal line 22 are located, thereby separating the first signal line 21 and the second signal line 22. Accordingly, the first signal line 21 and the second signal line 22 can be electrically insulated from each other. In this disclosure, the layer in which the first signal line 21 and the second signal line 22 is also referred to as a signal line layer.

[00019] The first signal line 21 and the second signal line 22 may be disposed in the same layer. Thus, the first signal line 21 and the second signal line 22 may be formed by a same patterning process. In some embodiments, the patterning process may include: forming a metal layer and a photoresist layer; exposing and developing the photoresist layer to retain photoresist in a first region and a second region and to remove photoresist in other regions; etching the metal layer to remove metal not covered by the photoresist, thus to form the first signal line 21 in the first region and the second signal line 22 in the second region; and removing the remaining photoresist. In the production process, impurities such as dust or the like may attach on the metal layer or in the photoresist in the area between the first region and the second region, causing photoresist residue at the position of the dust. Accordingly, the corresponding metal portion may not be completely etched away during the etching of the metal layer. Thus, a metal residue may be generated between the first signal line 21 and the second signal line 22 (such as the conductive residue 15 in FIG. 1), thereby causing a short circuit between the first signal line 21 and the second signal line 22.

[00020] In the present disclosure, the groove 241 is disposed in the insulating layer 24 and penetrates the insulating layer 24. The groove 241 is disposed in the spacing region between the first region and the second region, and extends to the bottom surface of the layer in which the first signal line 21 and the second signal line 22 are located. In the production process, the groove 241 can be arranged at the position corresponding to the conductive residue that is formed by impurities such as dust, and the conductive residue may be exposed through the groove 241 (dust and other impurities may have already been removed when removing the

photoresist). The conductive residue in the groove 241 can then be etched away, or the conductive residue in the groove 241 can be etched together when the other signal lines are subsequently formed. The adoption of the groove 241 can ensure the electrical insulation between the first signal line 21 and the second signal line 22. Accordingly, a short circuit between the first signal line 21 and the second signal line 22 can be suppressed, and the quality of the array substrate can be improved.

[00021] As shown in FIG. 2, the array substrate 200 may further include a thin film transistor and a pixel electrode 28 disposed over the substrate 20, and other appropriate structures. In some embodiments, as shown in FIG. 2, the thin film transistor includes a gate electrode 251, a gate insulating layer 252, and an active layer 253. The gate insulating layer 252 is disposed between the gate electrode 251 and the active layer 253. In some embodiments, the gate insulating layer 252 may cover the entire substrate 20. The pixel electrode 28 and the second signal line 22 may be disposed over the gate insulating layer 252. In these embodiments, the bottom surface of the layer in which the first signal line 21 and the second signal line 22 are located corresponds to an upper surface of the gate insulating layer 252. In some other embodiments, the gate insulating layer 252 may not completely cover the substrate 20, and may cover only the gate electrode 251. Further, the first signal line 21 and the second signal line 22 may be disposed directly on the upper surface of the substrate 20. In these embodiments, the bottom surface of the layer in which the signal line 21 and the second signal line 22 are located corresponds to the upper surface of the substrate 20.

[00022] Further, as shown in FIG. 2, the array substrate 200 further includes a third signal line 23 disposed over the insulating layer 24. The position of the third signal line 23 may correspond to the position of the first signal line 21. That is, an orthogonal projection of the third signal line 23 on the substrate may at least partially overlap with an orthogonal projection of the first signal line 21 on the substrate. The third signal line 23 can be formed by forming a conductive material layer and then patterning the conductive material layer in a patterning process. When the conductive material layer is etched in the patterning process to form the third signal line 23, the portions of the conductive material layer in regions other than that corresponding to the third signal line 23, including the portion corresponding the spacing region between the first region and the second region need to be etched. Because the position of the third signal line 23 corresponds to the position of the first signal line 21, the conductive residue, which is outside the position of the first signal line 21, can also be etched

away together. Thus, the conductive residue can be removed without additional steps. As such, the short circuit between the first signal line 21 and the second signal line 22 can be suppressed.

[00023] In the present disclosure, the quantity, shape and size of the grooves 241 can be chosen according to various application scenarios. In some embodiments, for example, a plurality of cylindrical-column- or square-column-shaped grooves can be arranged along the length direction of the first signal line 21. Further, a projection of the groove 241 on the substrate 20 may be strip shaped. An extending direction of the strip may be the same or approximately the same as an extending direction of the spacing region between the first signal line 21 and the second signal line 22. In some embodiments, a length of the strip may be the same or approximately the same as a length of the spacing region between the first signal line 21 and the second signal line 22. A width of the strip may be arbitrary or be chosen as needed. As such, after the first signal line 21 and the second signal line 22 are formed by patterning, if a conductive residue coupling the first signal line 21 to the second signal line 22 exists at a position in the spacing region between the first signal line 21 and the second signal line 22, the groove 241 in the insulating layer 24 may expose at least a portion of the conductive residue. Thus, the exposed conductive residue can be removed when the third signal line 23 is formed by the subsequent etching. The electrical insulation between the first signal line 21 and the second signal line 22 can be ensured, without the need to detect the position of the conductive residue.

[00024] In some embodiments, the first signal line 21 and the second signal line 22 may be parallel to each other. In these embodiments, the groove 241 may also be parallel to the first signal line 21 and the second signal line 22.

[00025] The array substrate consistent with embodiments of the disclosure can be used in a touch display device. In some embodiments, as shown in FIG. 2, the array substrate 200 further includes a touch electrode 26. The third signal line 23 may be a touch signal line coupled to the touch electrode 26, and the second signal line 22 may be a data line. The third signal line 23 and the first signal line 21 may be coupled in parallel. The third signal line 23 may also be coupled to a driving circuit (not shown), such that the driving circuit may determine a touch position according to a signal on the touch electrode 26. The first signal line 21 and the third signal line 23 may be coupled in parallel, such that a connection

resistance between the touch electrode 26 and the driving circuit may be reduced, thereby improving the accuracy of the touch detection.

[00026] In some embodiments, as shown in FIG. 2, the array substrate 200 further includes a passivation layer 27 disposed above the third signal line 23. The touch electrode 26 is disposed over the passivation layer 27 and coupled to the third signal line 23 through at least one first via hole (not shown) penetrating through the passivation layer 27. At least two connectors, e.g., a first connector and a second connector, may be disposed over the passivation layer 27 and in the same layer as the touch electrode 26. A first end of the first connector may be coupled to a first end of the third signal line 23 through at least one of a plurality of second via holes penetrating through the passivation layer 27. A second end of the first connector may be coupled to a first end of the first signal line 21 through at least one of a plurality of third via holes penetrating through the passivation layer 27 and the insulating layer 24. A first end of the second connector may be coupled to a second end of the third signal line 23 through at least another one of the plurality of second via holes penetrating through the passivation layer 27. The second end of the second connector may be coupled to a second end of the first signal line 21 through at least another one of the plurality of third via holes penetrating through the passivation layer 27 and the insulating layer 24.

[00027] In some embodiments, the first via hole, the second via holes, and the third via holes are disposed in the non-display region. That is, the connection position of the touch electrode 26 and the third signal line 23, the connection position of the third signal line 23 and the first signal line 21 are in the non-display region. As such, because FIG. 2 illustrates a sectional view of the display region of the array substrate 200, the via holes described above are not shown in FIG. 2.

[00028] In some embodiments, the array substrate consistent with embodiments of the disclosure can include a plurality of first signal lines 21 and a plurality of second signal lines 22, and the number of the second signal lines 22 and the number of the first signal lines 21 may be different. FIG. 3 is a plan view illustrating a distribution of the first signal lines 21 and the second signal lines 22 in the array substrate 200 according to various disclosed embodiments of the present disclosure. As shown in FIG. 3, the array substrate 200 may be divided into a plurality of pixel regions arranged in a plurality of rows and a plurality of columns. Each pixel region may include a plurality of sub-pixel regions arranged in the row direction (such as P1, P2, and P3 in FIG. 3). In this disclosure, a column of pixel regions is

also referred to as a pixel region column, and may correspond to one of the first signal lines 21. Further, a column of sub-pixel regions is also referred to as a sub-pixel region column, and may correspond to one of the second signal line 22.

[00029] A short circuit may occur more easily between a first signal line 21 and a second signal line 22 closer to the first signal line 21 than between the first signal line 21 and a second signal line 22 farther away from the first signal line 21. Thus, when the groove 241 is formed in the insulating layer 24, the groove 241 may be formed only in the corresponding region between a first signal line 21 and a second signal line 22 between two adjacent pixel regions. That is, groove 241 may not need to be formed between a first signal line 21 and a second signal line 22 that are separated from each other by at least one sub-pixel region.

[00030] The touch electrode 26 may be used as a touch electrode in the touch phase and used as a common electrode in the display phase. In the present disclosure, a short circuit between the first signal line 21 and the second signal line 22 can be suppressed. Thus, in a display device including the disclosed array substrate, when a touch occurs in the display phase, the common signal on the touch electrode 26 may not influence the second signal line 22, thereby reducing display defects as compared to the existing technology.

[00031] The present disclosure also provides a method of fabricating an array substrate. FIG. 4 illustrates a flow chart of an exemplary fabrication method 400 for an exemplary array substrate according to various disclosed embodiments of the present disclosure. The exemplary fabrication method 400 will be described in more detail with reference to FIG. 2 and FIG. 4.

[00032] At S1, the substrate 20 is provided.

[00033] At S2, a pattern including the first signal line 21 and the second signal line 22 is formed over the substrate 20. The first signal line 21 and the second signal line 22 are disposed in the same layer and separated from each other.

[00034] At S3, the insulating layer 24 covering the first signal line 21 and the second signal line 22 is formed.

[00035] At S4, the groove 241 penetrating through the insulating layer 24 is formed. The position of the groove 241 corresponds to the spacing region between the first signal line 21

and the second signal line 22. That is, the groove 241 may be between the first signal line 21 and the second signal line 22.

[00036] At S5, the conductive residue between the first signal line 21 and the second signal line 22 is removed by etching the conductive residue through the groove 241, such that the groove 241 reaches the bottom surface of the layer in which the first signal line 21 and the second signal line 22 are located.

[00037] According to the method consistent with the disclosure, even if the patterning process for forming the first signal line 21 and the second signal line 22 does not completely remove the conductive material between the first signal line 21 and the second signal line 22, the conductive residue can be exposed through the groove 241 that penetrates through the insulating layer 24 at the position of the conductive residue (the dust and other impurities may have been removed together with the photoresist). Thus, the conductive residue in the groove 241 can be removed by the etching in S5, thereby ensuring that the first signal line 21 and the second signal line 22 are electrically insulated. Accordingly, a short circuit between the first signal line 21 and the second signal line 22 can be prevented, thereby improving the quality of the array substrate.

[00038] In some embodiments, the etching of the conductive residue through the groove 241 may include an etching of the conductive residue alone. In some other embodiments, the conductive residues may be etched together when other signal lines are being formed, to ensure the electrical insulation between the first signal line 21 and the second signal line 22 regardless of whether the conductive residue exists or not.

[00039] FIG. 5 illustrates another flow chart of an exemplary fabrication method 500 for an exemplary array substrate according to various disclosed embodiments of the present disclosure. The exemplary fabrication method 500 will be described in detail with reference to FIG. 2 and FIG. 5.

[00040] At S1, the substrate 20 is provided.

[00041] At S11, a pattern including the gate electrode 251 of a thin film transistor is formed over the substrate 20.

[00042] At S12, the gate insulating layer 252 is formed over the gate electrode 251.

[00043] At S13, a pattern including the active layer 253 of the thin film transistor is formed over the gate insulating layer 252.

[00044] At S14, a pattern including the pixel electrode 28 is formed.

[00045] At S2, a pattern including the first signal line 21 and the second signal line 22 is formed. In some embodiments, a pattern including the first signal line 21, the second signal line 22, a source electrode 254 of the thin film transistor, and a drain electrode 255 of the thin film transistor is formed over the gate insulating layer 252. The first signal line 21 and the second signal line 22 may be disposed in a same layer and separated from each other. The second signal line 22 may be a data line. The first signal line 21 and the second signal line 22 may be parallel to each other.

[00046] At S3, the insulating layer 24 covering the first signal line 21 and the second signal line 22 is formed.

[00047] At S4, the groove 241 penetrating through the insulating layer 24 is formed. The position of the groove 241 corresponds to the spacing region between the first signal line 21 and the second signal line 22. In some embodiments, the projection of the groove 241 on the substrate 20 may be strip shaped, the extending direction of the strip may be the same as or approximately the same as the extending direction of the spacing region between the first signal line 21 and the second signal line 22, and the length of the strip may be the same as or approximately the same as the length of the spacing region between the first signal line 21 and the second signal line 22.

[00048] At S41, a conductive material layer is formed. In some embodiments, the conductive material layer may be a metal material layer.

[00049] At S5, an etching is performed through the groove 241. The etching can remove the conductive residue between the first signal line 21 and the second signal line 22. In some embodiments, the conductive material layer is patterned to retain the conductive material at the position corresponding to the first signal line 21, and the conductive material in other regions is removed by the etching. The conductive material at the position corresponding to the first signal line 21 may be the conductive material in a portion of the conductive material layer having an orthogonal projection on the substrate which at least partially overlaps with an orthogonal projection of the first signal line 21 on the substrate. Accordingly, the third

signal line 23 corresponding to the first signal line 21 is formed. An orthogonal projection of the third signal line 23 on the substrate may at least partially overlap with the orthogonal projection of the first signal line 21 on the substrate. This etching also removes the conductive residue in the groove 241 for ensuring electrical insulation between the first signal line 21 and the second signal line 22 and causes the groove 241 to reach the bottom surface of the layer in which the first signal line 21 and the second signal line 22 are located. As a result, the area at the bottom surface of the layer in which the first signal line 21 and the second signal line 22 are located that corresponds to the groove 241 is exposed. In some embodiments, the bottom surface of the layer in which the first signal line 21 and the second signal line 22 are located may be the upper surface of the gate insulating layer 252.

[00050] The material of the conductive material layer for forming the third signal line may be the same as the material forming the first signal line 21 and the second signal line 22. When the conductive residue is present between the first signal line 21 and the second signal line 22, because the groove 241 in the insulating layer 24 may penetrate through the insulating layer 24, at least a portion of the conductive residue may be exposed by the groove 241. Accordingly, the conductive material layer formed at S41 may cover the exposed conductive residue. When the conductive material layer is etched at S5, the conductive material layer at the position of the groove 241 is etched away and the conductive residue between the first signal line 21 and the second signal line 22 is also etched away. Accordingly, the short circuit between the first signal line 21 and the second signal line 22 may be suppressed without an additional step.

[00051] At S6, the passivation layer 27 is formed.

[00052] At S7, a pattern including the touch electrode 26 is formed.

[00053] The third signal line 23 formed at S5 may be a touch signal line coupled to the touch electrode 26. The first signal line 21 and the third signal line 23 may be coupled in parallel. In some embodiments, in order to couple the touch electrode 26 to the third signal line 23, and to couple the third signal line 23 and the first signal line 21 in parallel, at least one first via hole penetrating through the passivation layer 27, and second via holes penetrating through the passivation layer 27 and third via holes penetrating through the passivation layer 27 and the insulating layer 24 may be formed after forming the passivation layer 27 and

before forming the pattern including the touch electrode 26. The second via holes and the third via holes may be disposed at both ends of the first signal line 21.

[00054] The pattern including the touch electrode 26 that is formed at S7 can also include two connectors, i.e., a first connector and a second connector. The two connectors may correspond to two ends of the third signal line 23, respectively. The first end of the first connector may be coupled to the first end of the third signal line 23 through at least one of the second via holes penetrating through the passivation layer 27. The second end of the first connector may be coupled to the first end of the first signal line 21 through at least one of the third via holes penetrating through both the passivation layer 27 and the insulating layer 24. The first end of the second connector may be coupled to the second end of the third signal line 23 through at least another one of the second via holes penetrating through the passivation layer 27. The second end of the second connector may be coupled to the second end of the first signal line 21 through at least another one of the third via holes penetrating through both the passivation layer 27 and the insulating layer 24.

[00055] The present disclosure also provides a display device comprising the disclosed array substrate. FIG. 6 illustrates a schematic view of an exemplary display device 600 according to various disclosed embodiments of the present disclosure. As shown in FIG. 6, the display device 600 includes an array substrate 601 consistent with the disclosure. The array substrate 601 can be, for example, any one of the above-described exemplary array substrates. In addition to the array substrate 601, the display device 600 may further include other suitable structures. For example, the display device 600 may include a display panel, which further includes the array substrate 601. The display device 600 can be, for example, a tablet computer, a mobile phone, a car monitor, or a television. Any display device including an array substrate consistent with the disclosure is within the scope of the present disclosure. Because a short circuit between the data line and the touch signal line in the array substrate is suppressed, the display defects caused by the influence of the touch control in the display phase can be reduced in the display device. Accordingly, the display performance can be improved.

[00056] The present disclosure provides an array substrate, a fabrication method for the array substrate, and a display device comprising the array substrate. Consistent with the disclosure, a groove penetrating through the insulating layer may be disposed in the insulating layer, and may correspond to the spacing region between the first signal line and

the second signal line. Further, the groove may extend to the bottom surface of the layer in which the first signal line and the second signal line are located, and separate the first signal line from the second signal line. Accordingly, the first signal line and the second signal line can be electrically insulated from each other, and a short circuit between the first signal line and the second signal line can be suppressed. Thus, in an embedded touch display device, the display phase may not be influenced by the touch control, thereby reducing the display defects and improving the display performance. In addition, the conductive residue exposed in the groove may be removed by etching the conductive residue in the groove together when the third signal line is subsequently formed by etching. Accordingly, the short circuit between the first signal line and the second signal line may be prevented without an additional processing step.

[00057] The present disclosure provides an array substrate comprising: a substrate; a first signal line and a second signal line disposed over the substrate, arranged in the same layer, and separated from each other; an insulating layer covering the first signal line and the second signal line; a groove formed in the insulating layer and penetrating through the insulating layer. The groove may extend to the bottom surface of the layer in which the first signal line and the second signal line are located, separate the first signal line from the second signal line and electrically insulate the first signal line from the second signal line. The disclosed array substrate may reduce the display defects and improve the display performance.

[00058] The foregoing description of the embodiments of the disclosure has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the disclosure to the precise form or to exemplary embodiments disclosed. Accordingly, the foregoing description should be regarded as illustrative rather than restrictive. Obviously, many modifications and variations will be apparent to persons skilled in this art. The embodiments are chosen and described in order to explain the principles of the technology, with various modifications suitable to the particular use or implementation contemplated. It is intended that the scope of the invention be defined by the claims appended hereto and their equivalents in which all terms are meant in their broadest reasonable sense unless otherwise indicated. Therefore, the term “the disclosure”, “the present disclosure” or the like does not necessarily limit the claim scope to a specific embodiment, and the reference to exemplary embodiments of the disclosure does not imply a limitation on the invention, and no such limitation is to be inferred. Moreover, the claims may refer to “first”, “second”, etc. followed

by a noun or element. Such terms should be understood as a nomenclature and should not be construed as giving the limitation on the number of the elements modified by such nomenclature unless specific number has been given. Any advantages and benefits described may or may not apply to all embodiments of the disclosure. It should be appreciated that variations may be made to the embodiments described by persons skilled in the art without departing from the scope of the present disclosure. Moreover, no element or component in the present disclosure is intended to be dedicated to the public regardless of whether the element or component is explicitly recited in the following claims.

WHAT IS CLAIMED IS:

1. An array substrate, comprising:

a substrate;

a first signal line and a second signal line on the substrate, wherein the first signal line and the second signal line are in a same layer and separated from each other;

an insulating layer covering the first signal line and the second signal line; and

a groove penetrating through the insulating layer, wherein the groove is between the first signal line and the second signal line.

2. The array substrate according to claim 1, further comprising:

a third signal line disposed over the insulating layer,

wherein an orthogonal projection of the third signal line on the substrate at least partially overlaps with an orthogonal projection of the first signal line on the substrate.

3. The array substrate according to claim 2, further comprising:

a touch electrode formed over the third signal line and coupled to the third signal line,

4. The array substrate according to claim 3, wherein the third signal line and the first signal line are coupled in parallel.

5. The array substrate according to any one of claims 1-4, wherein:

a projection of the groove on the substrate is a strip,

an extending direction of the strip is same or approximately same as an extending direction of the spacing region, and

a length of the strip along the extending direction of the strip is same or approximately same as a length of the spacing region along the extending direction of the spacing region.

6. The array substrate according to any one of claims 1-4, wherein the first signal line is arranged parallel to the second signal line.

7. The array substrate according to claim 6, wherein the second signal line includes a data line.

8. A fabrication method for an array substrate, comprising:

providing a substrate;

forming a pattern including a first signal line and a second signal line on the substrate, the first signal line and the second signal line being arranged in a same layer and separated from each other;

forming an insulating layer covering the first signal line and the second signal line; and

forming a groove penetrating through the insulating layer and between the first signal line and the second signal line.

9. The fabrication method according to claim 8,

wherein a conductive residue exists between the first signal line and the second signal after forming the pattern including the first signal line and the second signal line on the substrate, and

the fabrication method further comprising:

etching through the groove to remove the conductive residue between the first signal line and the second signal line.

10. The fabrication method according to claim 9, further comprising:

forming a conductive material layer after forming the groove,

wherein etching through the groove to remove the conductive residue includes:

patterning the conductive material layer to retain conductive material in a portion of the conductive material layer having an orthogonal projection on the substrate at least partially overlapping with an orthogonal projection of the first signal line on the substrate, and to etch away conductive material of other portions of the conductive material layer, until a third signal line is formed and the conductive residue in the groove is removed, an orthogonal projection of the third signal line on the substrate at least partially overlapping with the orthogonal projection of the first signal line on the substrate.

11. The fabrication method according to claim 10, further comprising:

forming a pattern including a touch electrode over the third signal line after patterning the conductive material layer,

wherein:

the third signal line is coupled to the touch electrode, and

the third signal line and the first signal line are coupled in parallel.

12. The fabrication method according to any one of claims 8-11, wherein:

forming the groove includes forming a groove having a projection on the substrate being a strip,

an extending direction of the strip is same or approximately same as an extending direction of the spacing region, and

a length of the strip along the extending direction of the strip is same or approximately same as a length of the spacing region along the extending direction of the spacing region.

13. The fabrication method according to any one of claims 8-11, wherein the first signal line is formed to be parallel to the second signal line.

14. The fabrication method according to claim 13, wherein the second signal line includes a data line.

15. A display device, comprising the array substrate according to any one of claims 1-4.

FIG. 1

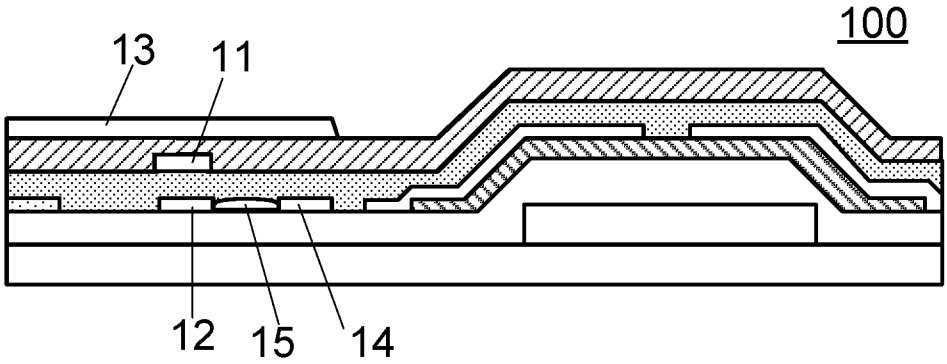

100
13
11
12
15
14

FIG. 2

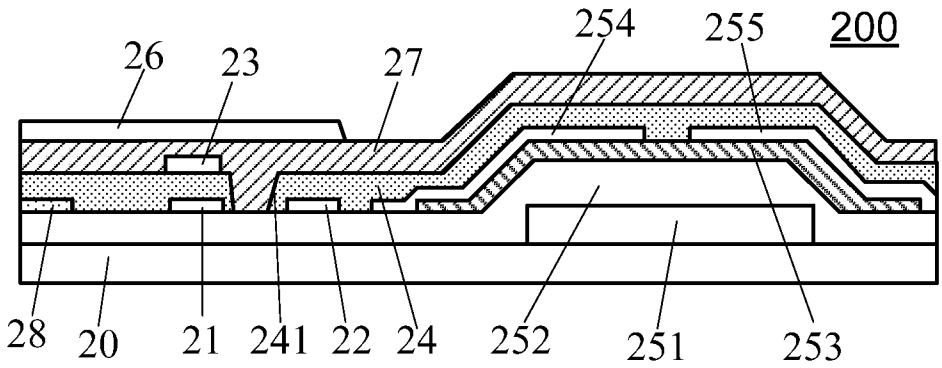

254
255
200
26
23
27
28
20
21
241
22
24
252
251
253

FIG. 3

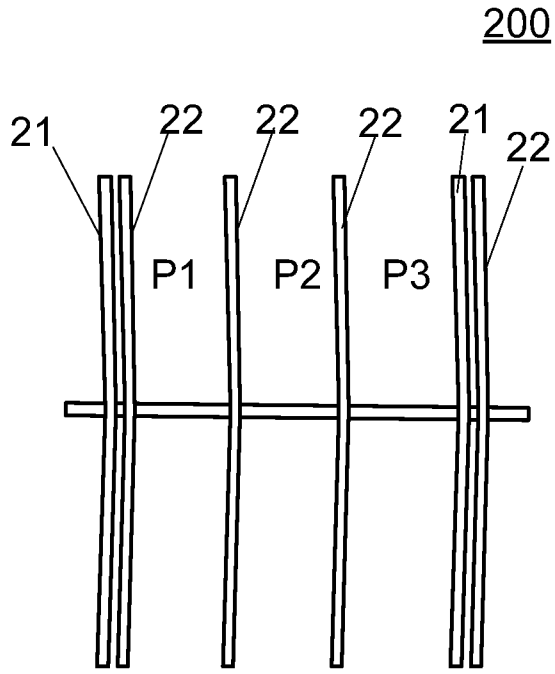


FIG. 4

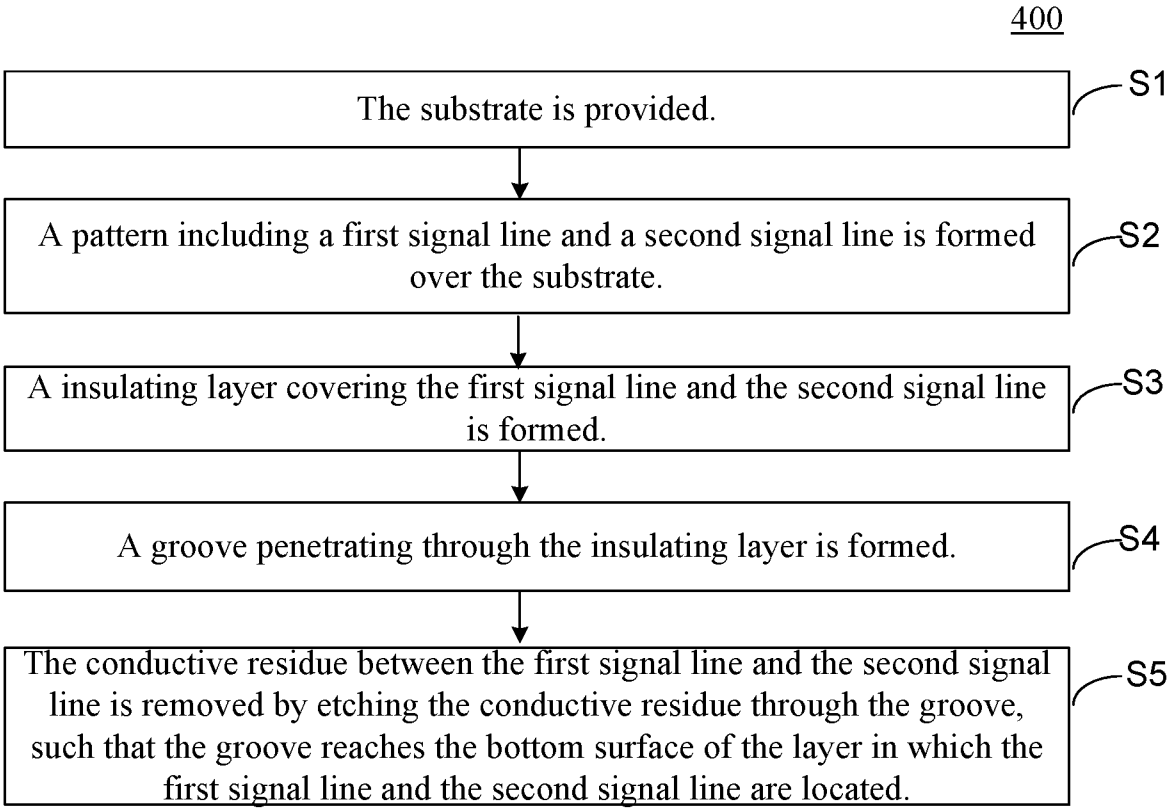

400
The substrate is provided.
S1
A pattern including a first signal line and a second signal line is formed over the substrate.
S2
A insulating layer covering the first signal line and the second signal line is formed.
S3
A groove penetrating through the insulating layer is formed.
S4
The conductive residue between the first signal line and the second signal line is removed by etching the conductive residue through the groove, such that the groove reaches the bottom surface of the layer in which the first signal line and the second signal line are located.
S5

FIG. 5

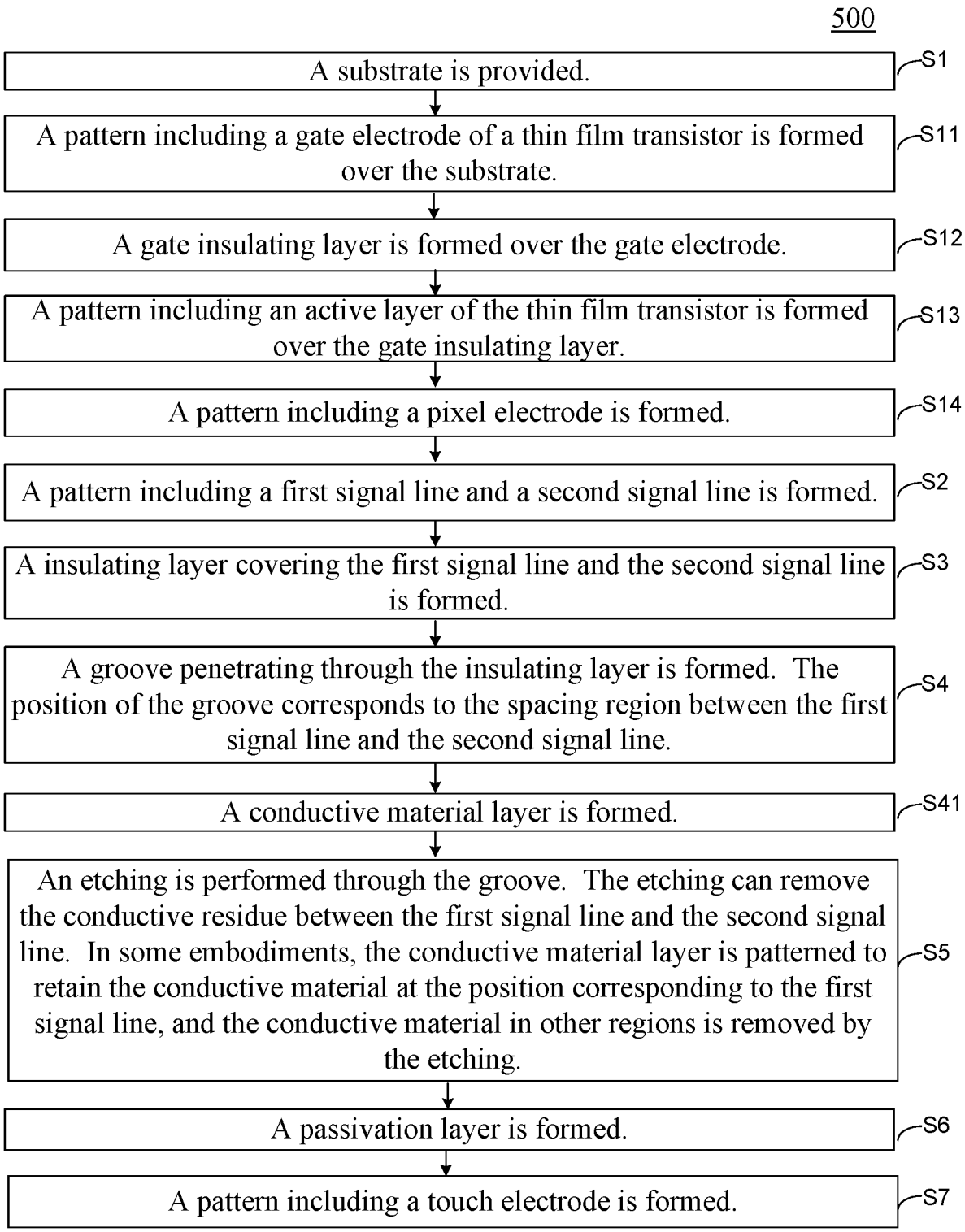
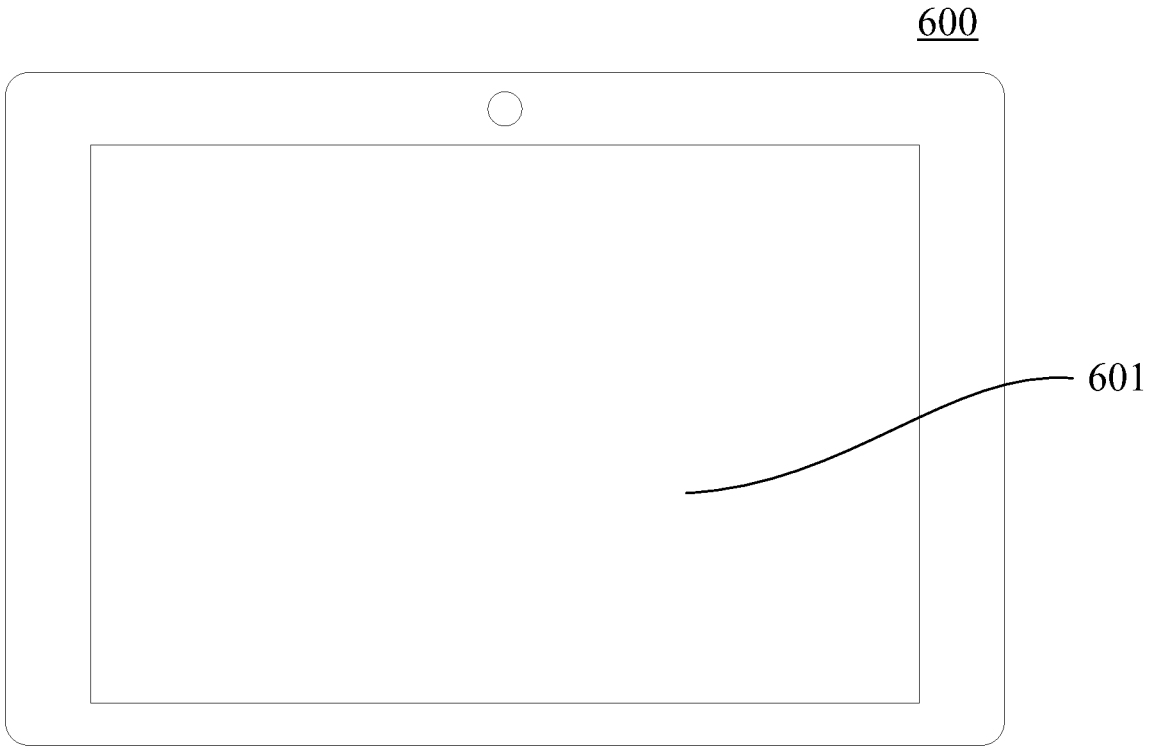

500
A substrate is provided.
S1
A pattern including a gate electrode of a thin film transistor is formed over the substrate.
S11
A gate insulating layer is formed over the gate electrode.
S12
A pattern including an active layer of the thin film transistor is formed over the gate insulating layer.
S13
A pattern including a pixel electrode is formed.
S14
A pattern including a first signal line and a second signal line is formed.
S2
A insulating layer covering the first signal line and the second signal line is formed.
S3
A groove penetrating through the insulating layer is formed. The position of the groove corresponds to the spacing region between the first signal line and the second signal line.
S4
A conductive material layer is formed.
S41
An etching is performed through the groove. The etching can remove the conductive residue between the first signal line and the second signal line. In some embodiments, the conductive material layer is patterned to retain the conductive material at the position corresponding to the first signal line, and the conductive material in other regions is removed by the etching.
S5
A passivation layer is formed.
S6
A pattern including a touch electrode is formed.
S7

FIG. 6



INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2017/097471

A. CLASSIFICATION OF SUBJECT MATTER

G06F 3/041(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT, CNKI, WPI, EPODOC: display, array, substrate, first, second, signal, line, groove, recess, channel, indent+, hole, penetrat+, insulat+, layer

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2007285594 A1 (SAMSUNG ELECTRONICS CO., LTD.) 13 December 2007 (2007-12-13) description, paragraphs [0030]-[0051], figures 1-4	1, 6-9, 13-15
A	JP 2012155198 A (SEIKO EPSON CORP.) 16 August 2012 (2012-08-16) the whole document	1-15
A	US 2014361786 A1 (TIANMA MICRO ELECTONICS CO., LTD. ET AL.) 11 December 2014 (2014-12-11) the whole document	1-15
A	US 2015301645 A1 (HEFEIBOE OPTOELECTRONICS TECHNOLOGY CO., LTD. ET AL.) 22 October 2015 (2015-10-22) the whole document	1-15
A	US 2016266677 A1 (BOE TECHNOLOGY GROUP CO., LTD. ET AL.) 15 September 2016 (2016-09-15) the whole document	1-15

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 October 2017	**01 November 2017**

Name and mailing address of the ISA/CN	Authorized officer
STATE INTELLECTUAL PROPERTY OFFICE OF THE P.R.CHINA **6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088** **China**	**ZHAO,Hui**
Facsimile No. **(86-10)62019451**	Telephone No. **(86-10)62413128**

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2017/097471

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
US	2007285594	A1	13 December 2007	EP	1865372	A1	12 December 2007
				US	7903189	B2	08 March 2011
				KR	20070117738	A	13 December 2007
				CN	101086564	A	12 December 2007
				JP	2007328340	A	20 December 2007
				TW	200745706	A	16 December 2007
JP	2012155198	A	16 August 2012	None			
US	2014361786	A1	11 December 2014	EP	2811376	A3	15 April 2015
				EP	2811376	A2	10 December 2014
				US	9666111	B2	30 May 2017
				CN	103927038	B	29 August 2017
				CN	103927038	A	16 July 2014
US	2015301645	A1	22 October 2015	CN	103186287	A	03 July 2013
				CN	103186287	B	23 December 2015
				WO	2014153854	A1	02 October 2014
US	2016266677	A1	15 September 2016	EP	3153955	A1	12 April 2017
				CN	104020913	A	03 September 2014
				WO	2015180321	A1	03 December 2015