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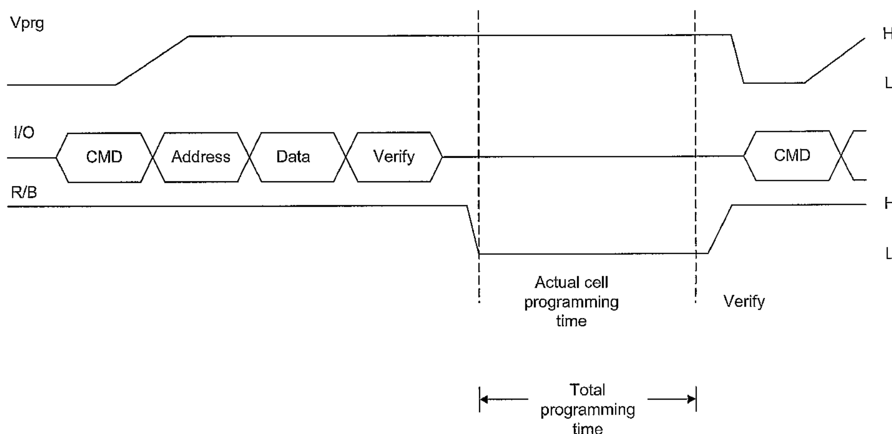

(57) Abstract: A high voltage up to 20V is usually applied to a NAND flash memory device for programming or easing a memory section. The programming/easing voltage must reach that high voltage state when the R/B signal is in the L state to start the actual cell programming or erasing. To improve the programming or erasing efficiency, the applied voltage also reaches the high voltage state before the R/B signal is set from H to L. The memory device may have one connecting pad to receive a normal operating voltage and another connection pad to receive the programming and erasing voltage. The EXT CSD register may have a mode bit to indicate whether the memory device supports the programming and erasing operation.

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METHOD FOR IMPROVING PROGRAMMING SPEED IN MEMORY DEVICES

Field of the Invention

The present invention relates generally to a memory device and, more particularly, to the programming of such device.

Background of the Invention

Flash memory is a form of EEPROM (Electronically Erasable Programmable Read Only Memory) that allows multiple memory locations to be erased or written in one programming operation. Flash memory is a transistor technology and is generally classified into NOR flash and NAND flash. The names refer to the gate logic architecture of the memory cells. NOR flash memory has a longer erase and write times than NAND flash memory, but NOR flash memory has a full address/data interface that allows random access to any location. NOR is suitable for storage of program code that needs to be infrequently updated, as in digital cameras and PDAs.

NAND flash memory has faster erase and write times (per bytes, depending on the access), higher density and lower cost per bit than NOR flash. However, its I/O interface allows only sequential access of data. NAND flash memory is popular with flash memory cards, USB flash drives for data storage and other mass memory devices. Among those flash memory card formats are MultiMediaCard (MMC), Secure Digital (SD), Memory Stick (MS) and xD Picture card.

Although NAND flash memory is faster to write as compared to other flash technologies such as NOR, improvement of the programming performance of NAND flash memory is still desirable. As density requirements in memories are increasing and content pre-programming starts to be more routine, programming performance becomes more critical from cost point of view. In the past, because of power consumption degradation, the power circuitry that is used to provide the programming or erasing voltage (up to 20V in NAND) is driven low after every block (page) access, as shown in Figure 1. As shown in Figure 1, the ready/busy signal (R/B) is in the low state after the setup in the I/O is ready. At the same time, the programming voltage Vprg is ramped up from "L" to "H". Only after the Vprg is sufficiently ramped up does the actual cell programming begin. Thus, the total programming time is the sum of the actual cell programming time and the ramping up time. As such, the programming or erasing operation is not highly efficient. In production where a large amount of data is programmed to the card prior to putting it into

a sales package, for example, it is advantageous and desirable to provide a method for improving the speed for programming the memory devices.

Summary of the Invention

5 In order to improve the programming or erasing efficiency in a memory device, the programming and erasing voltage is ready in the high voltage state before the R/B signal is set from H to L. The programming and erasing voltage can be in the high voltage state in the entire time period when the R/B signal is in the H state, or only in part of that time period. The memory device may have one connecting pad to receive a normal operating 10 voltage and another connection pad to receive the programming and erasing voltage. The EXT_CSD register may have a mode bit to indicate whether the memory device supports the programming and erasing operation.

Thus, the first aspect of the present invention provides a method for improving efficiency in performing a data change in a memory section in a memory device by 15 applying a voltage to the memory device in a time period, the time period comprising a first time segment for data setup and a second time segment following the first time segment, and wherein the applied voltage must reach a predetermined voltage value in the second time segment for effecting the data change. The method comprises:

providing the applied voltage to the memory device such that the applied voltage 20 substantially reaches the predetermined voltage value also in at least a part of the first time segment.

According to the present invention, a command signal is provided in the memory device in the first time segment for commanding the data change in the memory section, and wherein the applied voltage reaches the predetermined voltage value in the first time 25 segment before, after or during the command signal is provided.

According to the present invention, the applied voltage reaches the predetermined voltage value in the entire first time segment.

According to the present invention, the data change comprises writing data in a programming operation and removing data in an erasing operation.

30 According to the present invention, the memory section comprises a page or a block in the memory device.

According to the present invention, the time period is preceded by a preceding time period, the preceding time period also comprising a first time segment and a second time segment and wherein the applied voltage at the second state in the second time segment of

the preceding time period is changed to the first state in the first time segment of the time period.

According to the present invention, the time period is followed by a next time period, the next time period also comprising a first time segment and a second time
5 segment and wherein the applied voltage at the second state in the second time segment is maintained in at least a part of the first time segment of the next time period before it is changed to the first state.

According to the present invention, an R/B signal is provided in the memory device and wherein the R/B signal is in an "H" state in the first time segment and the R/B
10 is in an "L" state in the second time segment.

According to the present invention, the memory device comprises a NAND flash memory device and the predetermined voltage value is substantially equal to 20V.

The second aspect of the present invention provides a host device, which comprises:

15 a voltage source for providing an applied voltage to a memory device in a time period for performing a data change in a memory section of the memory device, the time period comprising a first time segment for data setup and a second time segment following the first time segment, wherein the applied voltage must reach a predetermined voltage value in the second time segment in order to effect the data change; and

20 a control unit, operatively connected to the voltage source, for controlling the applied voltage such that the applied voltage substantially reaches the predetermined voltage value also in at least a part of the first time segment.

According to the present invention, the host device further comprises a signal output for providing a command signal to the memory device in the first time segment for
25 commanding the data change in the memory device, wherein the applied voltage reaches the predetermined voltage value in the first time segment before, after or when the command signal is provided.

According to the present invention, the applied voltage reaches the predetermined voltage value in the entire first time segment.

30 The third aspect of the present invention provides a system for performing a data change in a memory section in a memory device in a time period. The system comprises:

a host device having a voltage source, a data output and a signal output; and

a signal bus comprising a plurality of lines for providing physical connections between the host device and the memory device, the lines comprising a voltage line, a signal line and at least one data line, wherein the memory device comprises:

a voltage connection pad operatively connected to the voltage source via
5 the voltage line to receive an applied voltage from the voltage source;

a signal connector operatively connected to the signal output via the signal line; and

at least one data connector operatively connected to the data output via said at least one data line, and wherein

10 the time period comprising a first time segment for data setup in said at least one data line, and a second time segment following the first time segment, and the applied voltage must reach a predetermined voltage value in the second time segment in order to effect the data change; and

a controller operatively connected to the voltage source to control the applied
15 voltage such that the applied voltage substantially reaches the predetermined voltage value also in at least a part of the first time segment.

The fourth aspect of the present invention provides a memory device having a plurality of memory sections for storing data. The memory device comprises:

at least one data connector to convey data; and

20 a voltage connector to receive a voltage in association with said data conveying, the voltage having

a first voltage setting when data in the memory sections are conveyed to an electronic device, and

a second voltage setting in at least a time period for performing a data change in
25 one of said memory sections, wherein the time period comprises a first time segment for data setup and a second time segment following the fist time segment, and wherein the voltage in the second voltage setting must reach a predetermined voltage value in the second time segment for effecting the data change, and the voltage in the second voltage setting substantially reaches the predetermined value also in at least a part of the first time
30 segment.

According to the present invention, the voltage connector comprises a first connector section for receiving the voltage in the first voltage setting and a second connection section for receiving the voltage in the second voltage setting.

According to the present invention, the memory device further comprises a signal connector for receiving a command signal in the first time segment for commanding the data change in the memory section, wherein the voltage in the second voltage setting reaches the predetermined voltage value in the first time segment before, after or when the
5 command signal is received.

According to the present invention, the voltage in the second voltage setting reaches the predetermined voltage value in the entire first time segment.

According to the present invention, the memory device comprises a NAND flash memory device.

10 According to the present invention, the voltage in the first voltage setting is substantially between 1.5V and 4.0V, and the predetermined voltage value is substantially equal to 20V.

According to the present invention, the memory device further comprises a register to indicate that the memory device supports the second voltage setting for effecting the
15 data change. The support is indicated in at least a data bit in the EXT_CSD register.

The fifth aspect of the present invention provides a software product embedded in a computer readable medium for use with a host device for performing a data change in a memory device by applying a voltage to the memory device in a time period, the time period comprising a first time segment for data setup and a second time segment following
20 the first time segment, wherein the applied voltage must reach a predetermined voltage value in the second time segment for effecting the data change, the memory device comprising:

a plurality of memory sections for storing data;

a data connector to convey data;

25 a voltage connector to receive a voltage in association with said data conveying, the voltage having

a first voltage setting when data in the memory sections are conveyed to an electronic device,

a second voltage setting in at least a time period for performing said data
30 change in at least one of said memory sections; and

at least a register to indicate that the memory device supports the second voltage setting.

The software product comprises executable codes, which, when executed, carry out:

reading the register for determining whether the memory device supports the second voltage setting; and if so,

causing the host device to apply the voltage in the second setting to the memory device for effecting said data change, wherein the voltage in the second voltage setting
5 reaches the predetermined voltage value also in at least a part of the first time segment.

The present invention will become apparent upon reading the description taken in conjunction with Figures 2a – 7d.

10 Brief Description of the Drawings

Figure 1 is a timing chart showing the voltage levels used in programming or erasing a NAND flash memory, according to prior art.

Figure 2a is a timing chart showing the voltage level used in programming or erasing a NAND flash memory, according to an embodiment of the present invention.

15 Figure 2b is a timing chart showing another voltage level used in programming or erasing a NAND flash memory, according to another embodiment of the present invention.

Figure 2c is a timing chart showing yet another voltage level used in programming or erasing a NAND flash memory, according to yet another embodiment of the present
20 invention.

Figure 3 is a block diagram illustrating a system for programming/erasing a NAND flash memory, according to an embodiment of the present invention.

Figure 4 is a block diagram showing a plurality of memory devices being simultaneously programmed or erased.

25 Figure 5 is a block diagram showing a typical MMC architecture.

Figure 6 is a block diagram showing another MMC architecture.

Figure 7a is a schematic representation showing a regular pin pad for connecting Vdd on a memory card.

Figure 7b is a schematic representation showing the splitting of a pin pad into two
30 sections.

Figure 7c is a schematic representation showing another way of splitting a pin pad.

Figure 7d is a schematic representation showing yet another way of splitting a pin pad.

Detailed Description of the Invention

In order to improve the efficiency in programming or erasing a memory device, it is possible to eliminate the ramping up time in the programming/erasing operation. According to the present invention, the programming/erasing voltage, Vprg, can be kept "high" all the time, as shown in Figure 2a. As such, actual cell programming starts as soon as the R/B signal drops to the low state. As a result, the total programming time is essentially equal to the actual cell programming time.

In another embodiment of the present invention, Vprg is ramped up during the I/O setup period. For example, it is possible to start ramping up the programming/erasing voltage Vprg right after the command (CMD) for program/erase is received, as shown in Figure 2b. Thus, Vprg can be ramped up during the I/O setup period, so long as Vprg becomes "H" before the R/B signal drops to the low state.

In yet another embodiment of the present invention, Vprg is ramped up during the I/O setup period to become "H" before the R/B signal drops to the low state, and the Vprg is maintained at the "H" state even after the R/B signal rises to the high state, as shown in Figure 2c.

Figure 3 is a block diagram showing a system for programming a memory card. As shown, the system **1** comprises a PC **10**, which controls the overall programming system. The PC **10** is operatively connected to a programming device **20** for controlling the programming operations. The programming device **20** comprises an I/O interface **22** operatively connected to a memory card **100'** via a data bus **60**, a command line (CMD) **70** and a clock line **80**. The programming device **20** has a memory unit **26** for storing data to be programmed to the memory device **100'** under the control of a CPU **24**. The memory unit **26** includes a software program **28** for storing the programming code. The programming device **20** further includes a power supply **30** operatively connected to the memory device **100'** for providing the programming voltage Vprg. The CPU **24** is operatively connected to the power supply **30** for controlling the programming voltage Vprg. As shown in Figure 3, the PC is connected to a display **5** for showing the status of the programming operation. In general, one programming device **20** can be used to simultaneously program or erase a plurality of memory devices **100'**, as shown in Figure 4. Although Figures 3 and 4 show a system for programming a memory device such as an MMC, a system for programming a NAND device is similar.

It should be noted that the regular operating voltage Vdd for an MMC or Vcc for a NAND memory device is 1.8V or 3V, whereas the programming/erasing voltage is much

higher- up to 20V. Thus, it is possible to have a power circuitry in the memory device such that when the voltage level on Vdd or Vcc is in the normal operating voltage range, then the power circuitry should perform an operation as in prior art, as shown in Figure 1. But when the power circuitry detects a much higher voltage on Vdd or Vcc, it
5 automatically switches to the efficient programming/erasing mode, according to the present invention. In this efficient mode, the programming/erasing voltage is already at the high level when the I/O setup is ready, as shown in Figures 2a and 2b.

In general, a NAND package has many unused (NC) pins. While the Vcc pin on a NAND package is used for normal operating voltage (1.8V, for example), one of the NC
10 pins can be reserved for use in the programming/erasing operation, according to the present invention. On a memory card, there may or may not be an unused pin or pad. An MMC card manufactured in accordance with MultiMediaCard Version 3.31 specification is shown in Figure 5. An MMC card manufactured in accordance with Version 4.0 specification is shown in Figure 6. As shown in Figure 5, the Version 3.31 memory card
15 **100** has a Vdd connecting pad **144** and one unused (N.C.) connecting pad **141**. The unused connecting pad **141** can be used for programming and erasing, according to the present invention. As shown in Figure 6, while the Version 4.0 memory card has a Vdd pin pad **154**, it does not have any unused pin pads. In order to perform a high-voltage programming/erasing operation, according to the present invention, it is possible to add a
20 separate pin pad, spaced from other existing pins. Alternatively, it is possible to split the existing pad **154** into two sections as shown in Figures 7b – 7d.

Figure 7a shows a regular pad **154**. Figure 7b shows a pad **155** having a first section **161** and a second section **162**. While one of the sections is used as a normal Vdd pad to receive a regular operating voltage of 1.8V, for example, the other can be used for
25 high-voltage programming/erasing, according to the present invention. It is also possible to split the pad in different ways. For example, the pad **156** is split into a section **163** and a section **164**, as shown in Figure 7c. Likewise, the pad **157**, as shown in Figure 7d, has a section **165** and a section **166**.

In an MMC (Version 4.0 or higher), it is possible to select a mode that accepts the
30 higher voltage for programming/erasing, according to the present invention. For example, it is possible to assign a mode bit in the EXT_CSD (Extended Card Specific Data) register (see Figure 6) to indicate whether the memory device supports the programming/erasing operation with high voltage Vcc, according to the present invention. The EXT_CSD register contains information about the card capabilities and selected modes as introduced

in MMC Specification Version 4. As shown in TABLE I, the properties segment in the EXT_CSD register has a "High voltage input support" property. In the corresponding field, a value of 0x00 in the register High_V means that the operation is not supported (as in legacy cards) and a value of 0x01 indicates that the operation is supported, for example.
5 This properties segment bit could also be used to indicate the support in split pad implementation without the mode segment register.

Name	**Field**	**Size (Bytes)**	**Cell Type**	**CSD-slice**
Properties segment				
Reserved		7		[511:505]
Supported Command Sets	S_CMD_SET	1	R	[504]
Reserved		300		[503:204]
Power Class for 26MHz @ 3.6V	PWR_CL_26_360	1	R	[203]
Power Class for 52MHz @ 3.6V	PWR_CL_52_360	1	R	[202]
Power Class for 26MHz @ 1.95V	PWR_CL_26_195	1	R	[201]
Power Class for 52MHz @ 1.95V	PWR_CL_52_195	1	R	[200]
High voltage input support	High_V	1	R	[205]

10

TABLE I

In the modes segment of the EXT_CSD register, a writing to the register sets the modes of the memory device. As shown in TABLE II, the EXT_CSD register modes
15 segment has a mode High Voltage Mode, with a corresponding field of High_Voltage. A writing of a 0x01 to High_Voltage would enable the programming voltage function, according to the present invention, while a writing of a 0x00 would disable it. Default value after power up should be 0x00 and the register can also be read to check the current value. The mode segment register could also be combined with the split pad
20 implementation.

25

Name	Field	Size (Bytes)	Cell Type	CSD-slice
Modes segment				
Command Set	CMD_SET	1	R/W	[191]
Reserved		1		[190]
Command Set Revision	CMD_SET_REV	1	RO	[189]
Reserved		1		[188]
Power Class	POWER_CLASS	1	R/W	[187]
Reserved		1		[186]
High Speed Interface Timing	HS_TIMING	1	R/W	[185]
Reserved		1		[184]
Bus Width Mode	BUS_WIDTH	1	WO	[183]
Reserved		183		[182:0]
High Voltage Mode	High_Voltage	1	R/W	[181]

TABLE II

In sum, the present invention provides a method for improving the efficiency in programming and erasing a memory device by eliminating the ramping up time for the programming voltage Vprg. Thus, the programming voltage Vprg has an H state and an L state according to some embodiments of the present invention. The H state is reached before the R/B signal is set from H to L. Alternatively, Vprg remains in the H state during the programming or erasing operation. Vprg is zero or equal to a low voltage when it is in the L state and is up to 20V in the H state. In a programming operation, the programming time per page is shorter than the prior art method. In an erasing operation, the erasing time per block is shorter. There is no need to increase the clock frequencies to improve the performance. Furthermore, with the present invention, it is still possible to preserve the prior art standard low power usage model for low power applications.

Although the invention has been described with respect to one or more embodiments thereof, it will be understood by those skilled in the art that the foregoing and various other changes, omissions and deviations in the form and detail thereof may be made without departing from the scope of this invention.

What is claimed is:

1. A method for improving efficiency in performing a data change in a memory section in a memory device by applying a voltage to the memory device in a time period, the time period comprising a first time segment for data setup and a second time segment following the first time segment, and wherein the applied voltage must reach a predetermined voltage value in the second time segment for effecting the data change, said method characterized by:

providing the applied voltage to the memory device such that the applied voltage substantially reaches the predetermined voltage value also in at least a part of the first time segment.

2. The method of claim 1, characterized in that a command signal is provided in the memory device in the first time segment for commanding the data change in the memory section, and that the applied voltage reaches the predetermined voltage value in the first time segment after the command signal is provided.

3. The method of claim 1, characterized in that a command signal is provided in the memory device in the first time segment for commanding the data change in the memory section, and that the applied voltage reaches the predetermined voltage value in the first time segment before the command signal is provided.

4. The method of claim 1, characterized in that a command signal is provided in the memory device in the first time segment for commanding the data change in the memory section, and that the applied voltage reaches the predetermined voltage value in the first time segment when the command signal is provided.

5. The method of claim 1, characterized in that the applied voltage reaches the predetermined voltage value in the entire first time segment.

6. The method of claim 1, characterized in that the data change comprises writing data in a programming operation.

7. The method of claim 6, characterized in that the memory section comprises a page in the memory device.

8. The method of claim 6, characterized in that the memory section comprises a block
5 in the memory device.

9. The method of claim 1, characterized in that the data change comprises removing data in an erasing operation.

10 10. The method of claim 9, characterized in that the memory section comprises a block of the memory device.

11. The method of claim 1, characterized in that the applied voltage comprises a first state and a second state, wherein
15 when the applied voltage is in the second state, the applied voltage substantially reaches the predetermined voltage value, and
when the applied voltage is in the first state, the applied voltage has a voltage value smaller than the predetermined voltage value.

20 12. The method of claim 11, characterized in that the voltage value in the first state is zero.

13. The method of claim 11, characterized in that the time period is preceded by a preceding time period, the preceding time period also comprising a first time segment and
25 a second time segment and that the applied voltage at the second state in the second time segment of the preceding time period is changed to the first state in the first time segment of the time period.

14. The method of claim 11, characterized in that the time period is followed by a next
30 time period, the next time period also comprising a first time segment and a second time segment and that the applied voltage at the second state in the second time segment is maintained in at least a part of the first time segment of the next time period before it is changed to the first state.

15. The method of claim 1, characterized in that an R/B signal is provided in the memory device and that the R/B signal is in an "H" state in the first time segment and the R/B is in an "L" state in the second time segment.

5 16. The method according to any one of claims 1 to 15, characterized in that the memory device comprises a NAND flash memory device.

17. The method of claim 16, characterized in that the predetermined voltage value is substantially equal to 20V.

10

18. A host device characterized by:

a voltage source for providing an applied voltage to a memory device in a time period for performing a data change in a memory section of the memory device, the time period comprising a first time segment for data setup and a second time segment following
15 the first time segment, wherein the applied voltage must reach a predetermined voltage value in the second time segment in order to effect the data change; and

a control unit, operatively connected to the voltage source, for controlling the applied voltage such that the applied voltage substantially reaches the predetermined voltage value also in at least a part of the first time segment.

20

19. The host device of claim 18, further characterized by:

a signal output for providing a command signal to the memory device in the first time segment for commanding the data change in the memory device, wherein the applied voltage reaches the predetermined voltage value in the first time segment after the
25 command signal is provided.

20. The host device of claim 18, further characterized by:

a signal output for providing a command signal to the memory device in the first time segment for commanding the data change in the memory section, wherein the applied
30 voltage reaches the predetermined voltage value in the first time segment before the command signal is provided.

21. The host device of claim 18, further characterized by:

a signal output for providing a command signal to the memory device in the first time segment for commanding the data change in the memory section, wherein the applied voltage reaches the predetermined voltage value in the first time segment when the command signal is provided.

5

22. The host device of claim 18, characterized in that the applied voltage reaches the predetermined voltage value in the entire first time segment.

23. A system for performing a data change in a memory section in a memory device in
10 a time period, said system characterized by:

a host device having a voltage source, a data output and a signal output; and

a signal bus comprising a plurality of lines for providing physical connections between the host device and the memory device, the lines comprising a voltage line, a signal line and at least one data line, wherein the memory device comprises:

15 a voltage connection pad operatively connected to the voltage source via the voltage line to receive an applied voltage from the voltage source;

a signal connector operatively connected to the signal output via the signal line; and

at least one data connector operatively connected to the data output via said
20 at least one data line, and wherein

the time period comprising a first time segment for data setup in said at least one data line, and a second time segment following the first time segment, and the applied voltage must reach a predetermined voltage value in the second time segment in order to effect the data change; and

25 a controller operatively connected to the voltage source to control the applied voltage such that the applied voltage substantially reaches the predetermined voltage value also in at least a part of the first time segment.

24. A memory device having a plurality of memory sections for storing data,
30 characterized by:

at least one data connector to convey data; and

a voltage connector to receive a voltage in association with said data conveying, the voltage having

a first voltage setting when data in the memory sections are conveyed to an electronic device, and

a second voltage setting in at least a time period for performing a data change in one of said memory sections, wherein the time period comprises a first time segment for data setup and a second time segment following the fist time segment, and wherein the voltage in the second voltage setting must reach a predetermined voltage value in the second time segment for effecting the data change, and the voltage in the second voltage setting substantially reaches the predetermined value also in at least a part of the first time segment.

25. The memory device of claim 24, characterized in that the voltage connector comprises a first connector section for receiving the voltage in the first voltage setting and a second connection section for receiving the voltage in the second voltage setting.

26. The memory device of claim 24, further characterized by a signal connector for receiving a command signal in the first time segment for commanding the data change in the memory section, wherein the voltage in the second voltage setting reaches the predetermined voltage value in the first time segment after the command signal is received.

27. The memory device of claim 24, further characterized by a signal connector for receiving a command signal in the first time segment for commanding the data change in the memory section, wherein the voltage in the second voltage setting reaches the predetermined voltage value in the first time segment before the command signal is received.

28. The memory device of claim 24, further characterized by a signal connector for receiving a command signal in the first time segment for commanding the data change in the memory section, wherein the voltage in the second voltage setting reaches the predetermined voltage value in the first time segment when the command signal is received.

29. The memory device of claim 24, characterized in that the voltage in the second voltage setting reaches the predetermined voltage value in the entire first time segment.

30. The memory device according to any one of claims 24 to 29 comprising a NAND flash memory device.

5 31. The memory device of claim 24, characterized in that the voltage in the first voltage setting is substantially between 1.5V and 4.0V, and the predetermined voltage value is substantially equal to 20V.

32. The memory device of claim 24, further characterized by a register to indicate that
10 the memory device supports the second voltage setting for effecting the data change.

33. The memory device of claim 32, characterized in that the register has at least a data bit for said indicating.

15 34. The memory device of claim 32, characterized in that the register comprises an EXT_CSD register.

35. A software product embedded in a computer readable medium for use with a host device for performing a data change in a memory device by applying a voltage to the
20 memory device in a time period, the time period comprising a first time segment for data setup and a second time segment following the first time segment, wherein the applied voltage must reach a predetermined voltage value in the second time segment for effecting the data change, the memory device comprising:

a plurality of memory sections for storing data;

25 a data connector to convey data;

a voltage connector to receive a voltage in association with said data conveying, the voltage having

a first voltage setting when data in the memory sections are conveyed to an electronic device,

30 a second voltage setting in at least a time period for performing said data change in at least one of said memory sections; and

at least a register to indicate that the memory device supports the second voltage setting;

said software product characterized by a plurality of executable codes, which, when executed, perform the steps of:

reading the register for determining whether the memory device supports the second voltage setting; and if so,

5 causing the host device to apply the voltage in the second setting to the memory device for effecting said data change, wherein the voltage in the second voltage setting reaches the predetermined voltage value also in at least a part of the first time segment.

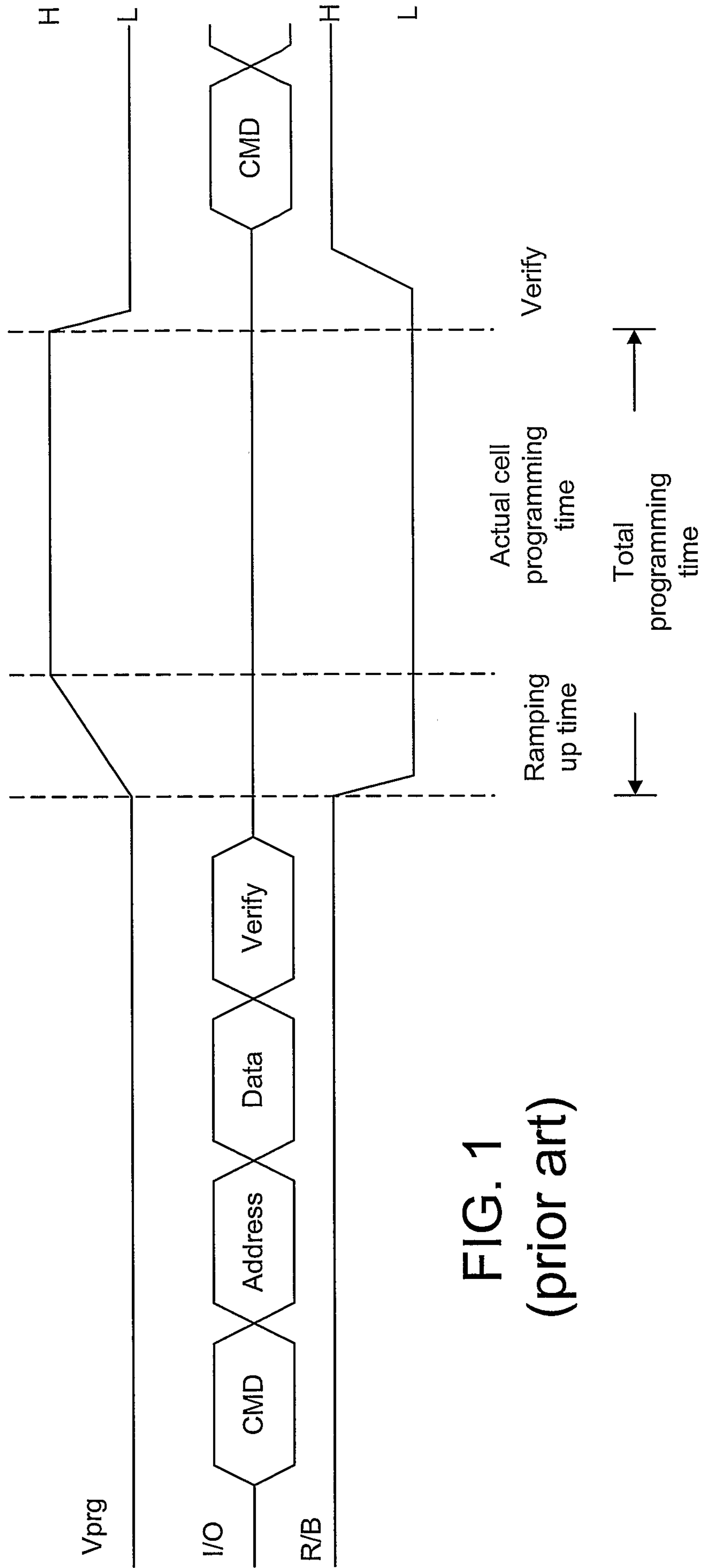


FIG. 1
(prior art)

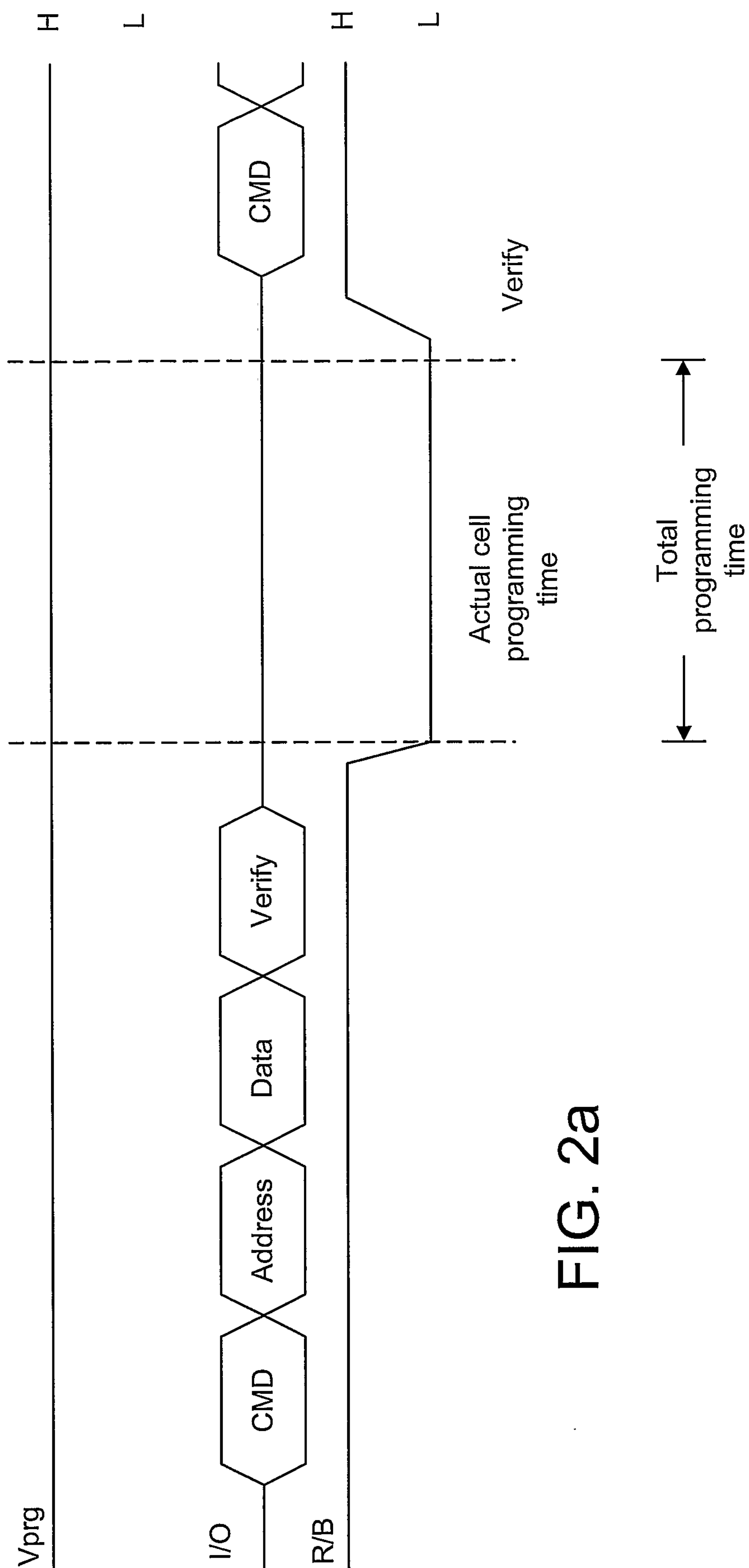


FIG. 2a

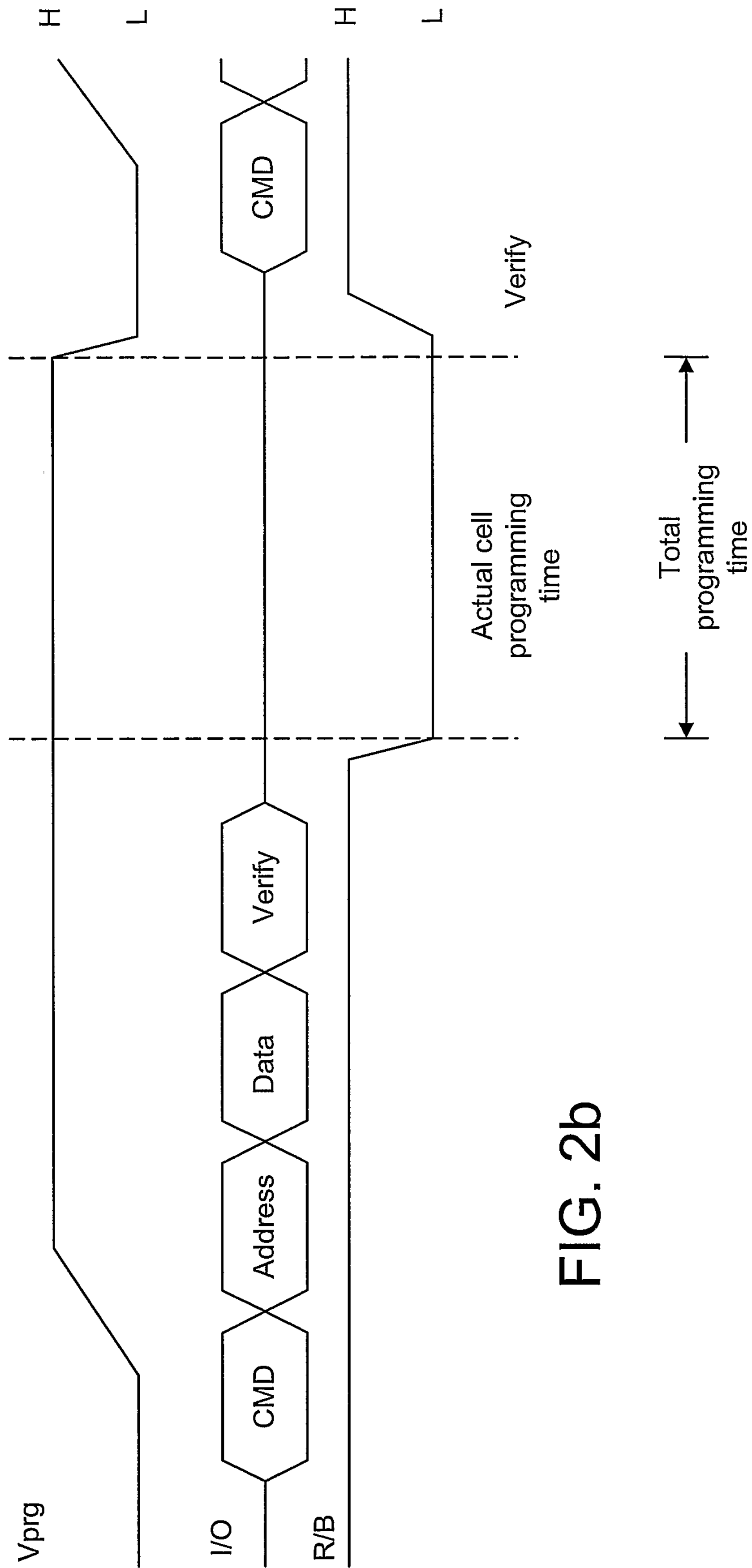


FIG. 2b

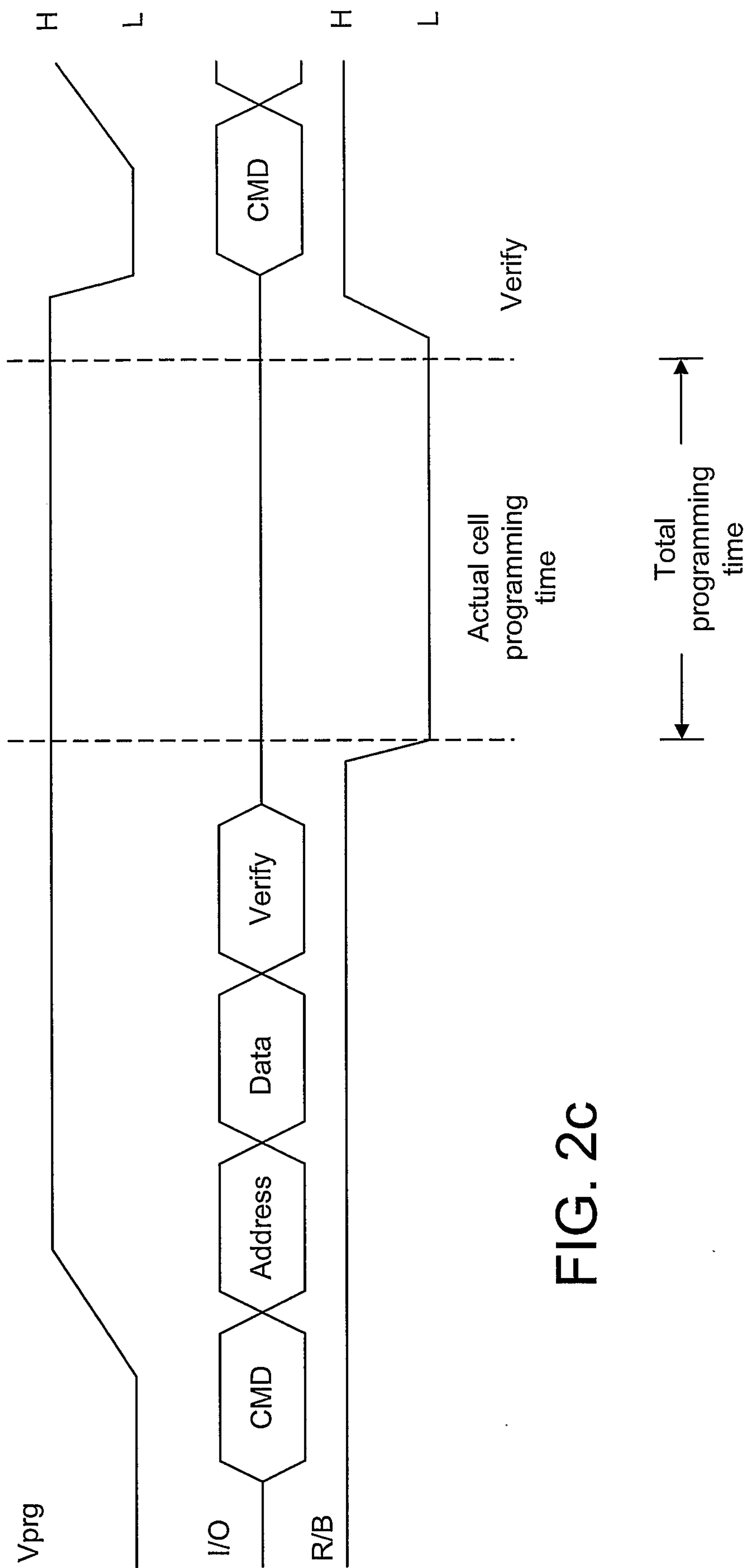


FIG. 2c

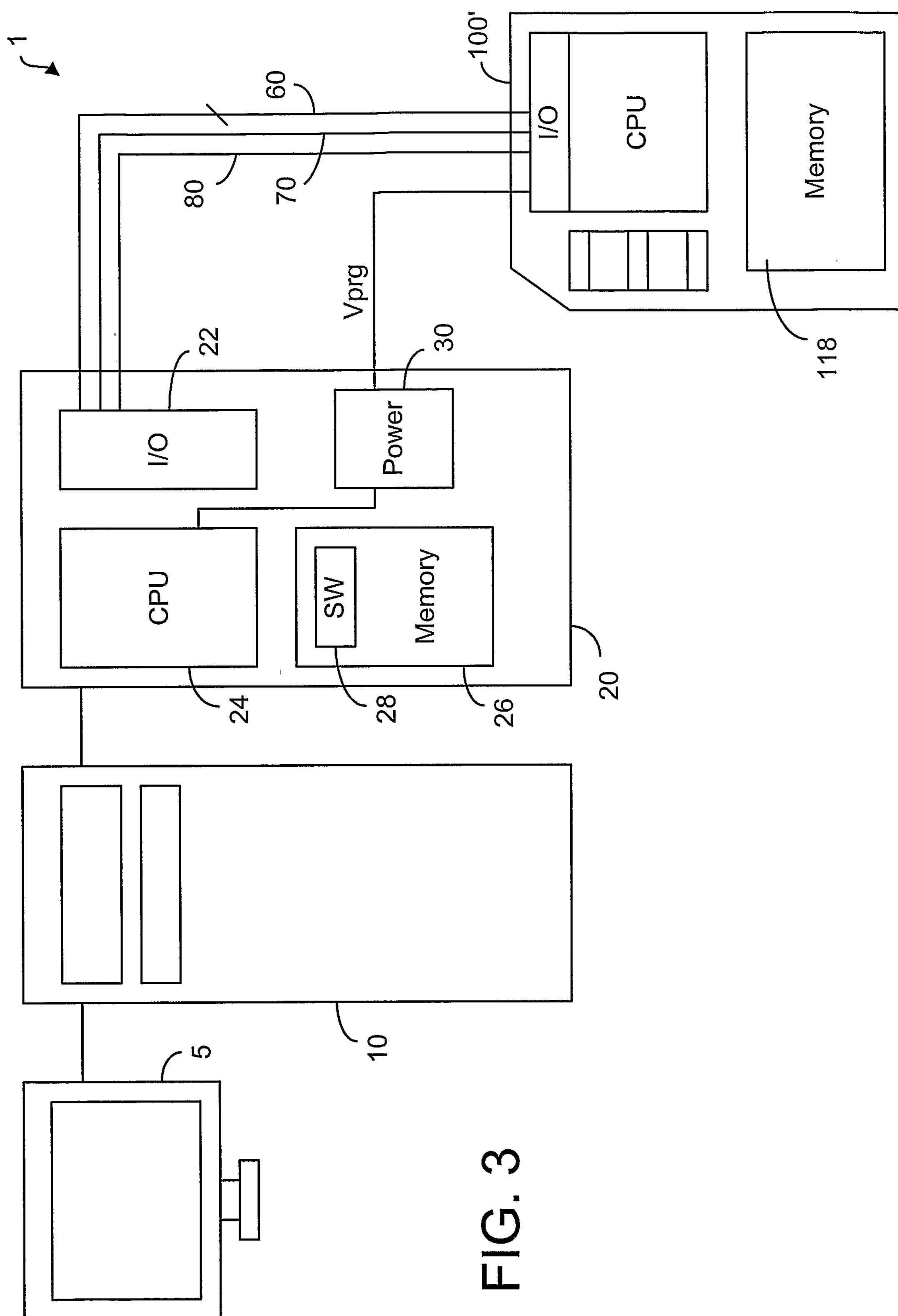


FIG. 3

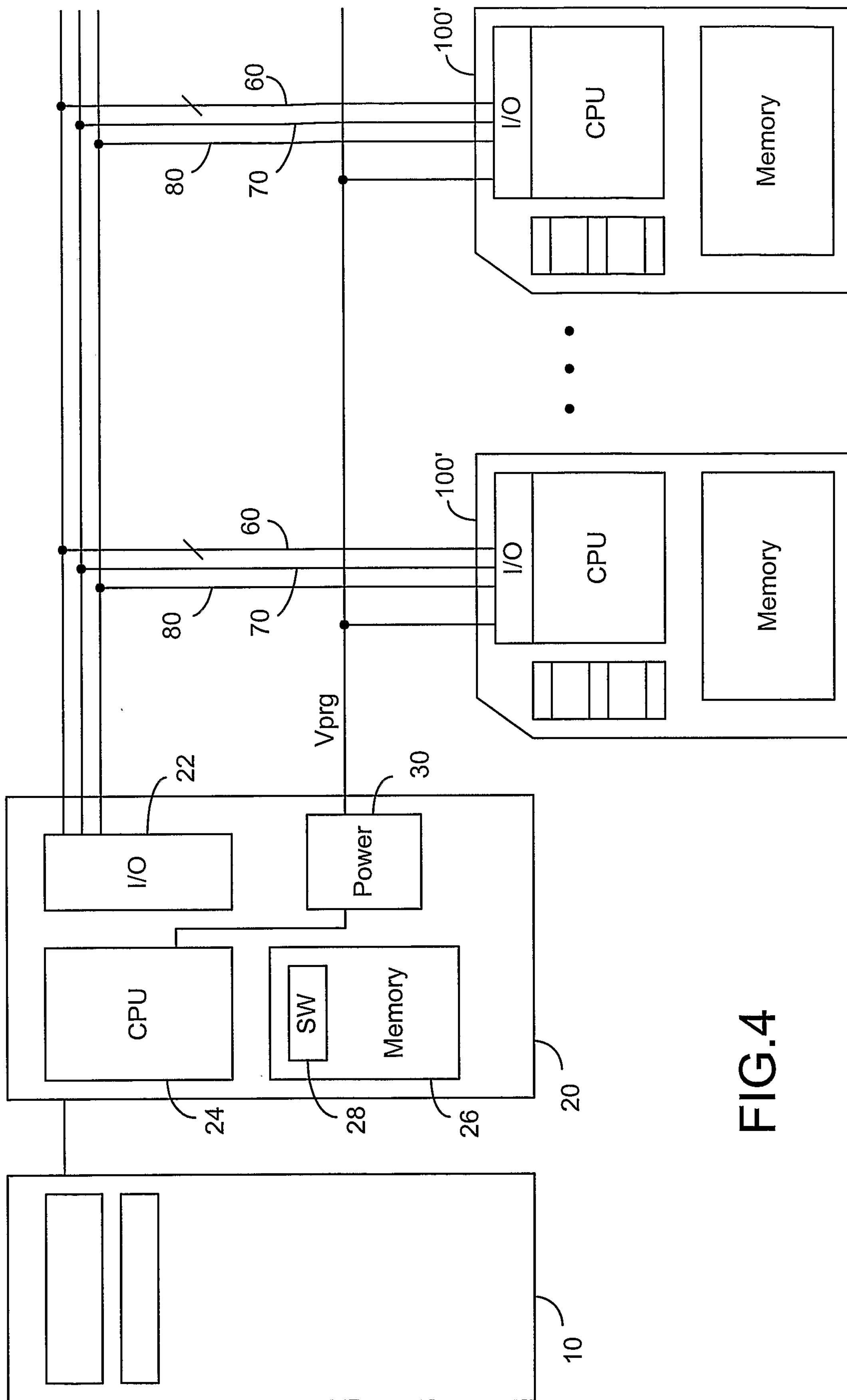


FIG.4

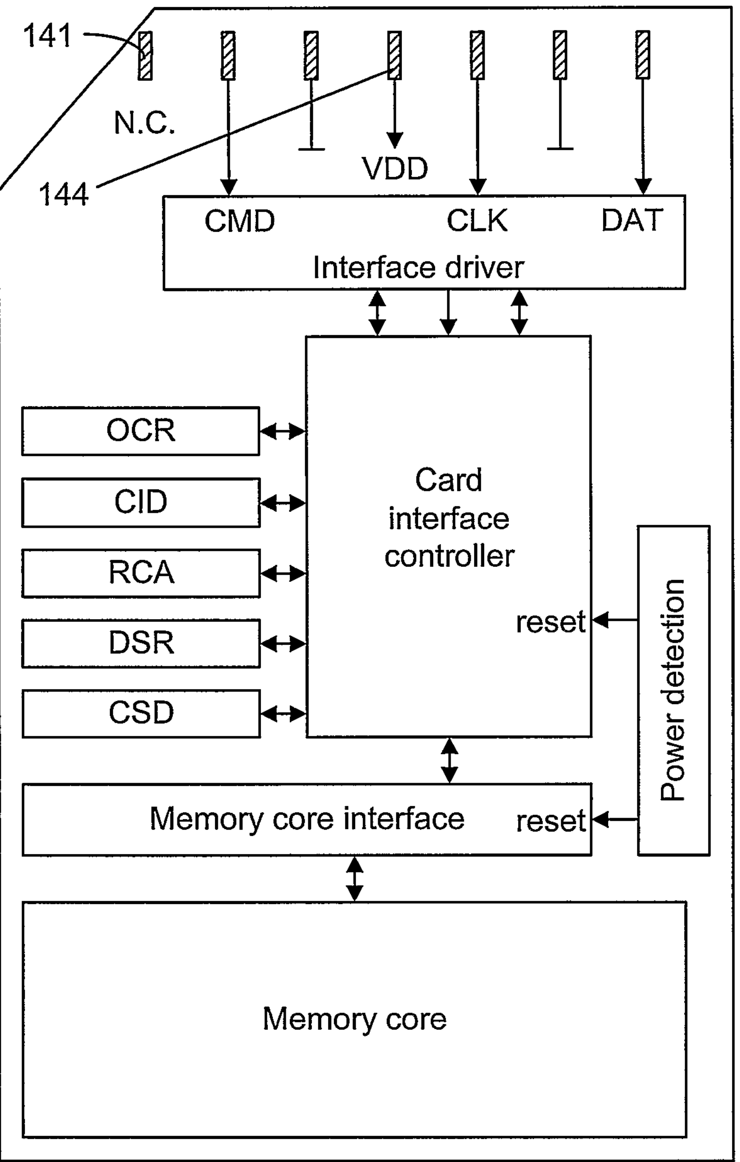
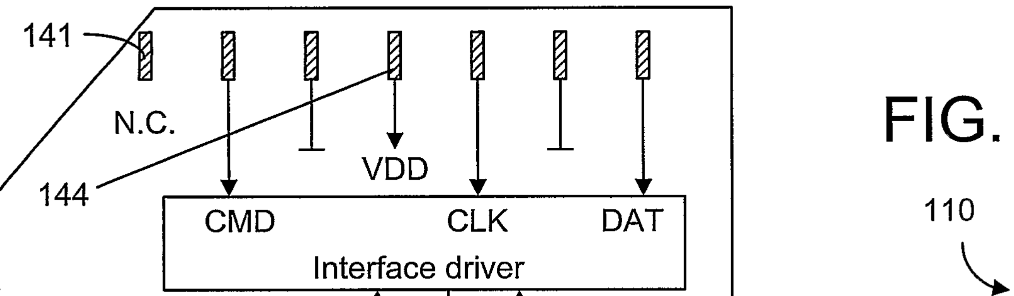


FIG. 5



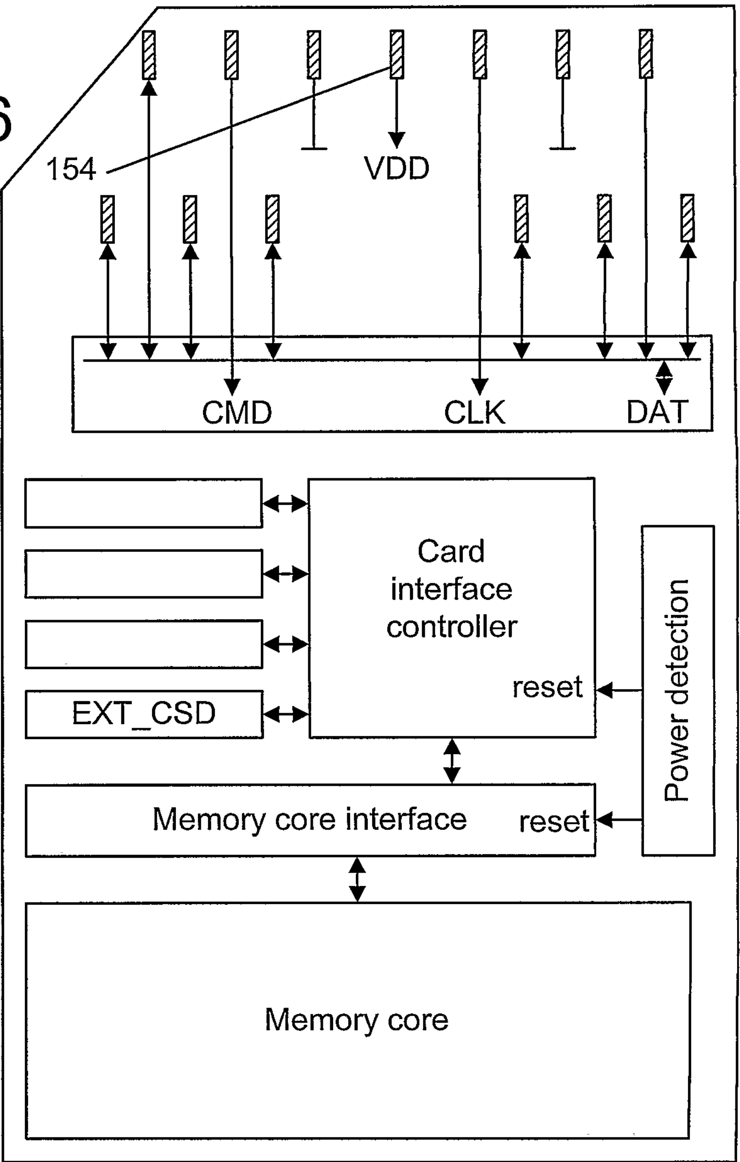
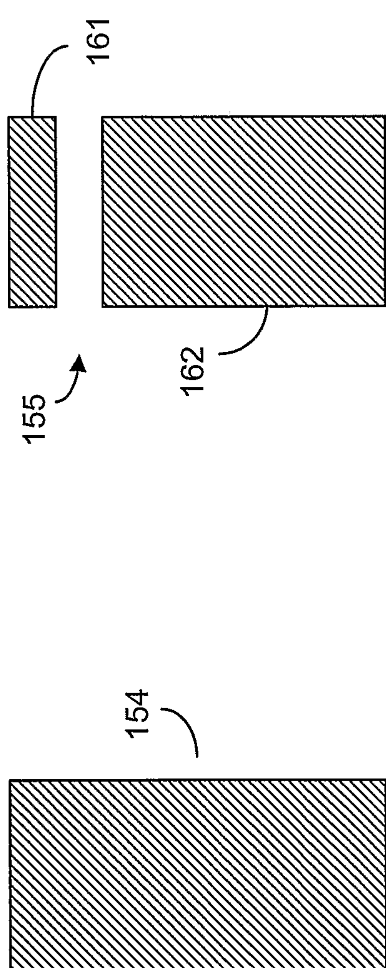
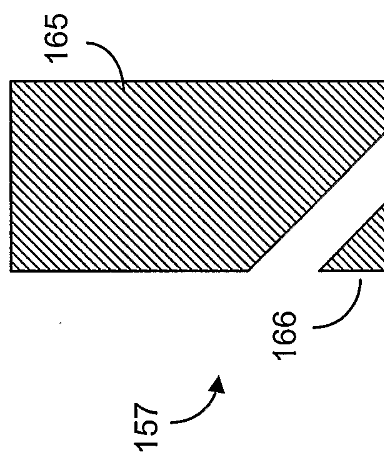
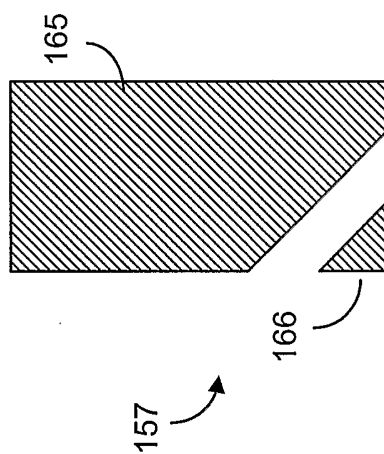


FIG. 6

FIG. 7







INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB 2005/002509

A. CLASSIFICATION OF SUBJECT MATTER

IPC: see extra sheet
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-INTERNAL, WPI DATA, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6335881 B2 (KIM, J-H ET AL), 1 January 2002 (01.01.2002), column 3, line 55 - column 6, line 4, figures 3,4 --	1-35
X	US 6128231 A (CHUNG, H-T), 3 October 2000 (03.10.2000), column 6, line 46 - column 7, line 58, figures 4,6 --	1,2,6-19,23, 24,26,30,35
X	US 5414829 A (FANDRICH, M L ET AL), 9 May 1995 (09.05.1995), column 4, line 25 - column 5, line 22; column 6, line 29 - column 7, line 46; column 9, line 49 - column 11, line 3, figures 3,4 --	1,3-18, 20-30,35

[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 January 2006	19 -01- 2006
Name and mailing address of the ISA/ Swedish Patent Office Box 5055, S-102 42 STOCKHOLM Facsimile No. +46 8 666 02 86	Authorized officer Bo Gustavsson /LR Telephone No. +46 8 782 25 00

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB2005/002509

INTERNATIONAL PATENT CLASSIFICATION (IPC):

G11C 16/32 (2006.01)
G11C 16/12 (2006.01)
G11C 16/14 (2006.01)
G11C 7/22 (2006.01)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB 2005/002509

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