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(51) INT CL[5]
H04Q 3/52

(52) UK CL (Edition L)
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(56) Documents cited
GB 2184325 A GB 2109196 A GB 1572379 A
GB 1017031 A EP 0451999 A

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UK CL (Edition K) H4K KPG KPN KRA KSA KSC KTW KWB, H4R RCT RCX
INT CL[5] H04Q

(54) Signal routing

(57) A device for providing signal routing within a circuit comprises first (30) and second (43) M x N matrices of switching elements coupled together, a plurality of inputs (31-42), coupled to said first matrix (30), for receiving a plurality of input signals and a plurality of outputs (44-55), coupled to said second matrix (43), for outputting a plurality of output signals. The first (30) and second (43) M x N matrices provide a routing path for the plurality of input signals (31-42) to the plurality of outputs (44-55).

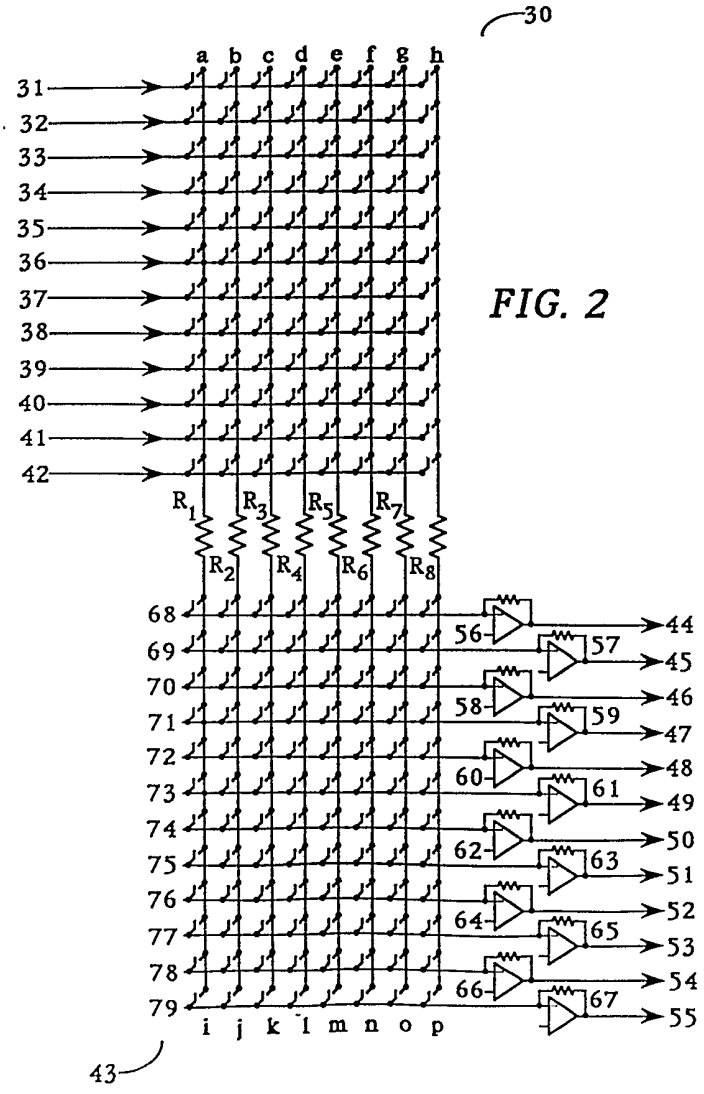

FIG. 2

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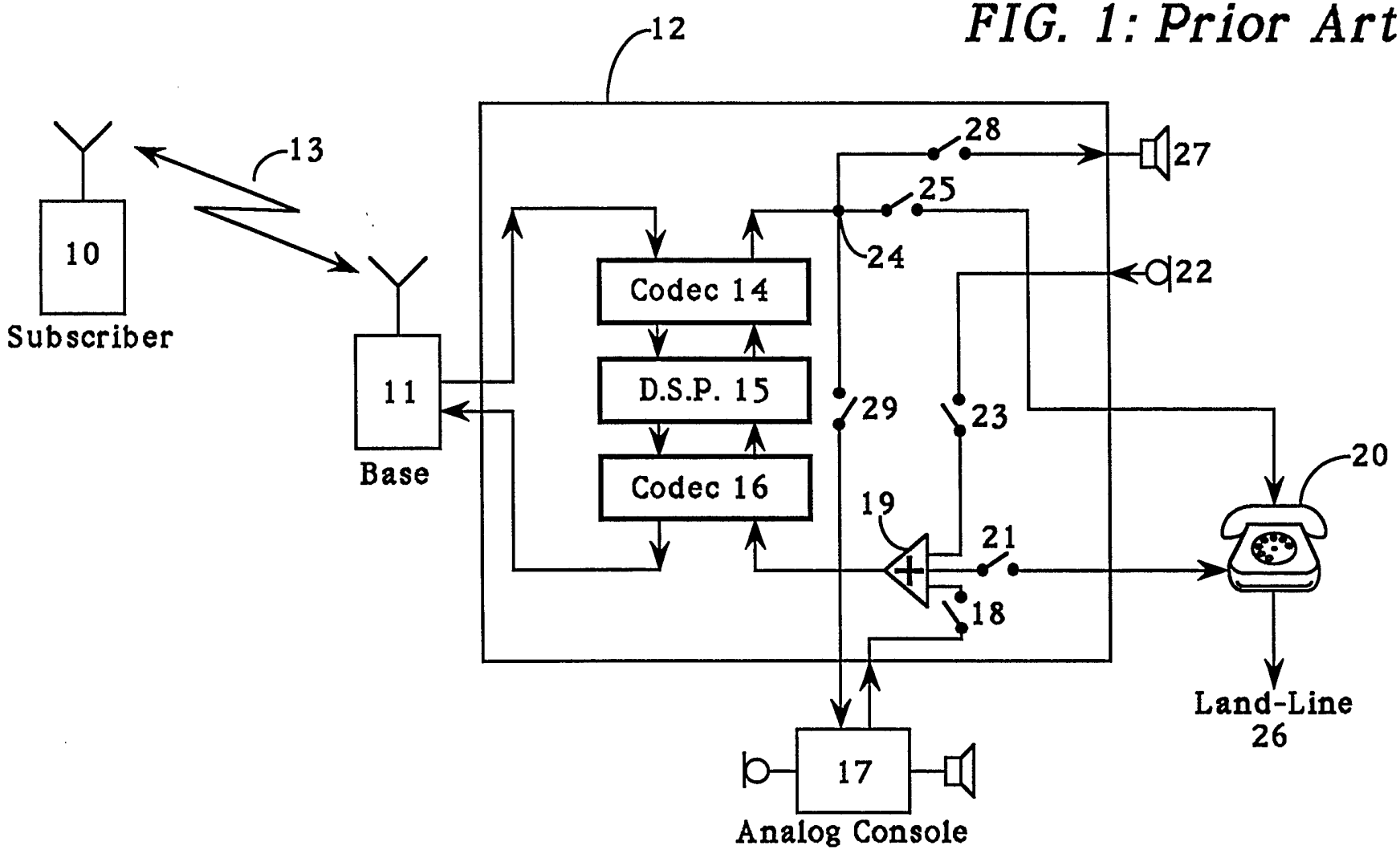
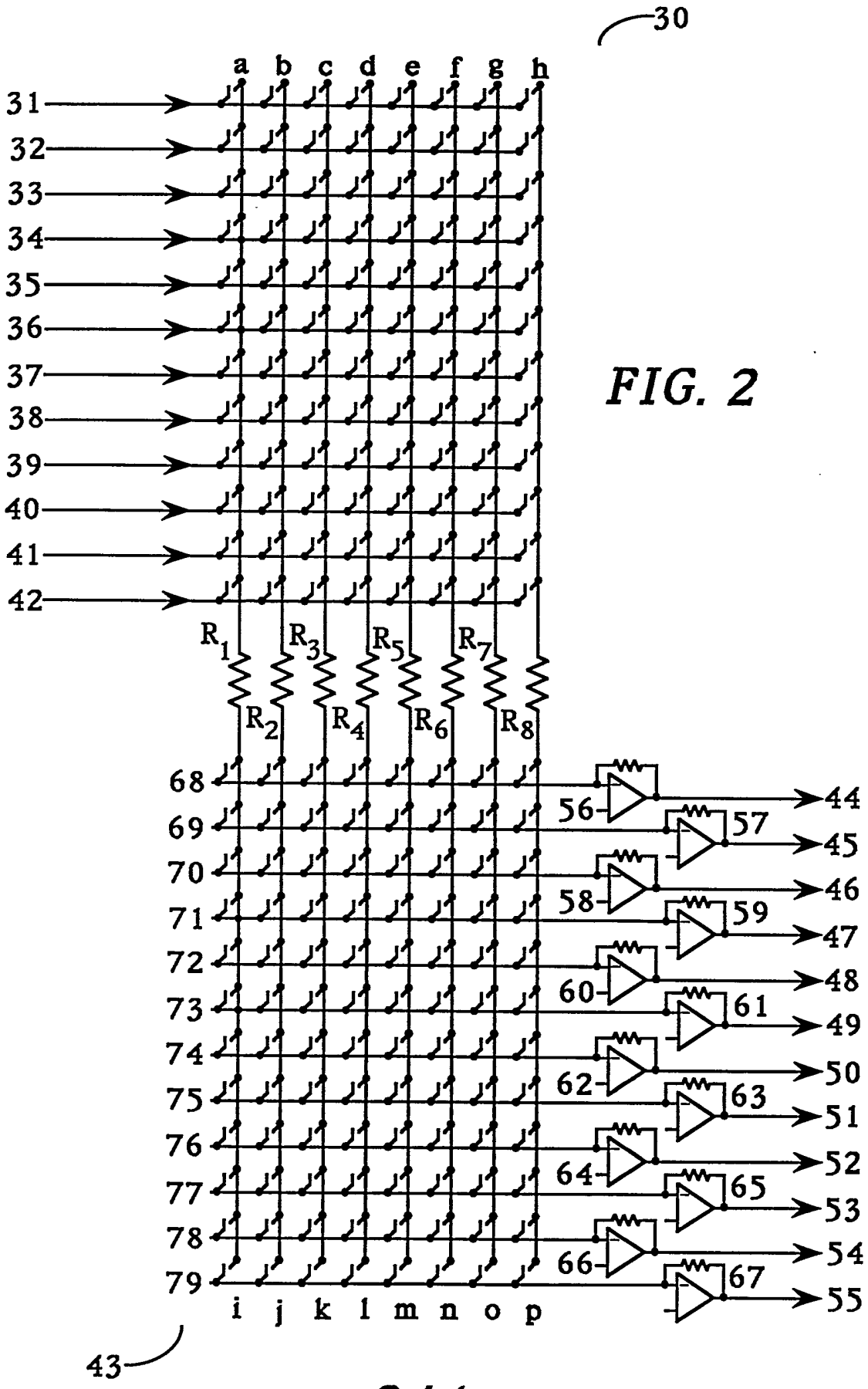
FIG. 1: Prior Art

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a b c d e f g h
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R1 R3 R5 R7
R2 R4 R6 R8
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i j k l m n o p
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FIG. 2

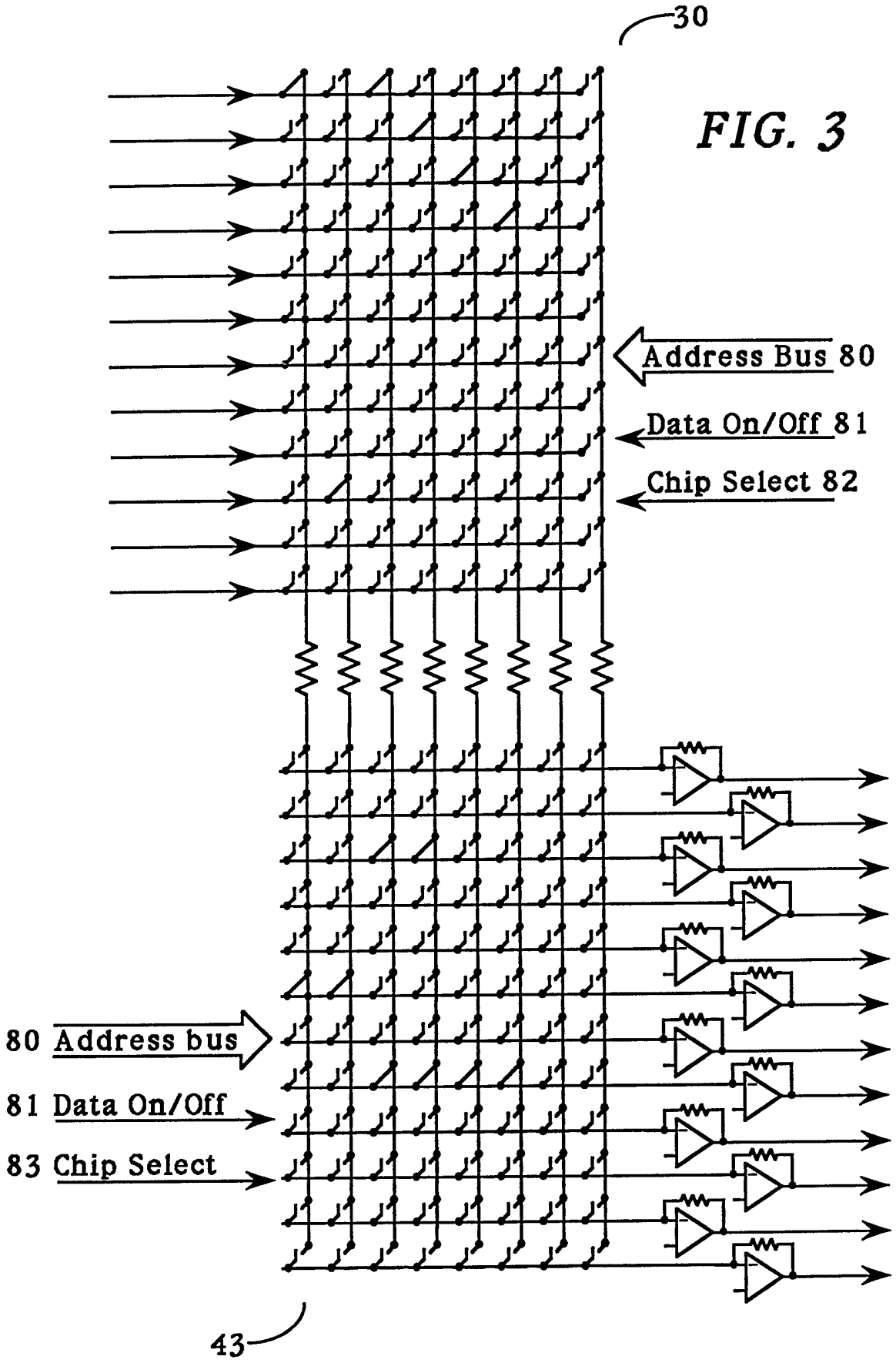
30
Address Bus 80
Data On/Off 81
Chip Select 82
80 Address bus
81 Data On/Off
83 Chip Select
43

FIG. 3

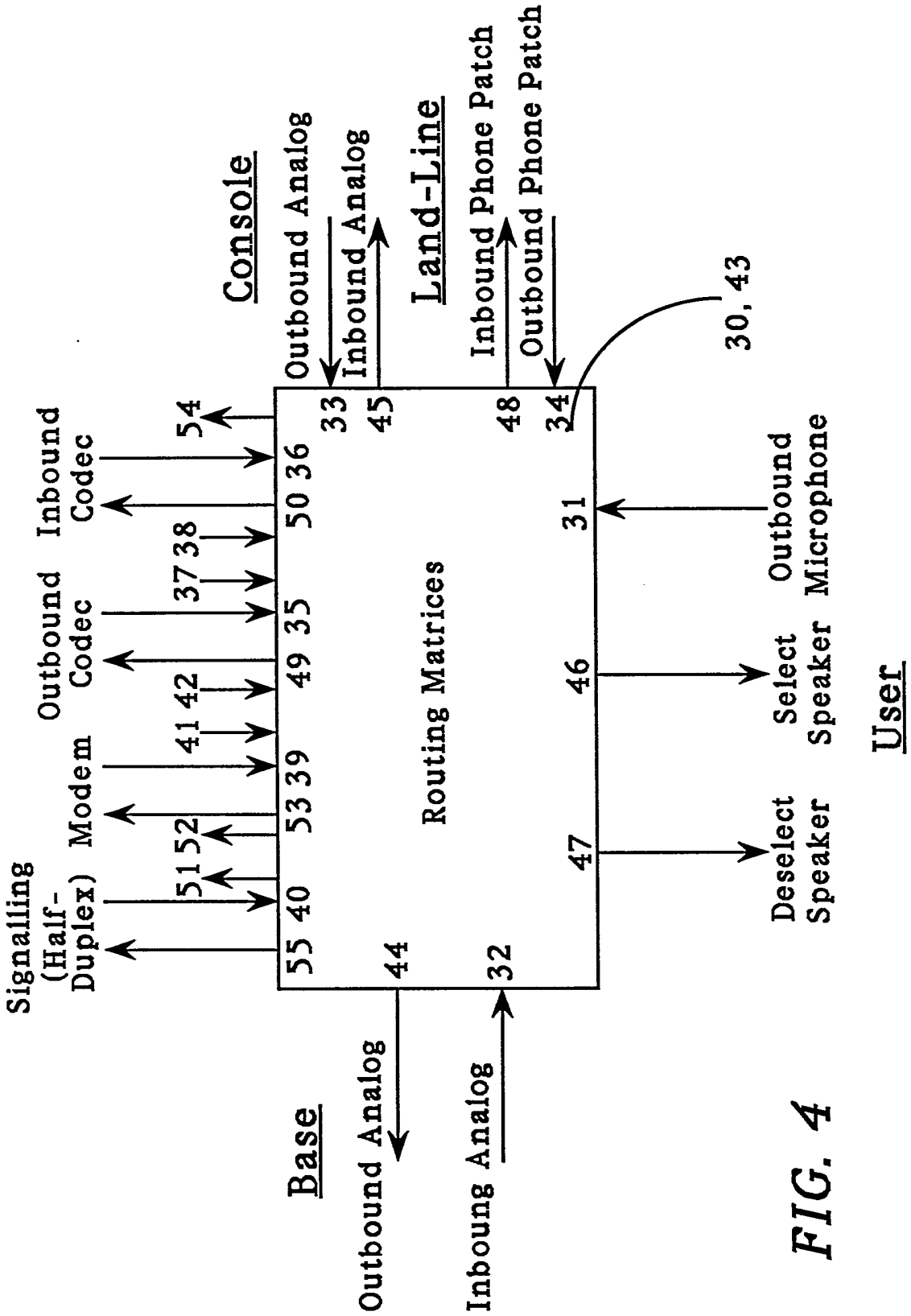
Digital Interface Unit
Signalling (Half-Duplex)
Modem
Outbound Codec
Inbound Codec
Routing Matrices
Console
Outbound Analog
Inbound Analog
Land-Line
Inbound Phone Patch
Outbound Phone Patch
Base
Outbound Analog
Inboung Analog
User
Deselect Speaker
Select Speaker
Outbound Microphone
30, 43
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FIG. 4

Signal Routing.

Background to the Invention.

This invention relates, in general, to the routing of signals within an electronic device and is particularly, but not exclusively, applicable to the routing of analog signals therein.

Summary of the Prior Art.

Analog signal routing within prior art electronic devices is usually accomplished through a combination of amplifiers, buffers and switches. However, conventional design methods and the associated limitations imposed thereby restrict signal routing to only those paths which are essential to satisfy device requirements. In a first instance, the increasing complexity of device design often warrants the use of microprocessors for control applications. These microprocessors may control the operation of analog sections within the device itself. Moreover, a proportion of devices now contain digital signal processing (DSP) technology which replaces the relatively antiquated analog processing sections. Unfortunately, loading problems within such microprocessors stipulate that the DSP must be limited to a relatively small proportion of memory and, in addition, external analog circuitry must be provided in order to serve auxiliary signal routing.

A typical environment employing a prior art analog signal routing circuit is illustrated in FIG. 1. A subscriber 10 is coupled to a base station 11 of a Digital Interface Unit (DIU) 12, such as Motorola's ASTRO† T5600 system, via a suitable communications link 13 e.g. a radio frequency (RF) link. The base station 11 is coupled to a first input of a first coder-decoder ("codec") 14. An output of said codec 14 is coupled to a first input of a DSP unit 15. A first output of DSP unit 15 is coupled to a first input of a second codec 16. A first output of the second codec 16 is coupled back to the base 11.

† ASTRO is a trade mark of Motorola.

The DSP unit 15 and the first 14 and second 16 codec are contained within the digital interface unit 12.

An external analog console 17 is coupled to a first input of a summing unit 19, of digital interface unit 12, through a first switch 18. A second input to summing unit 19 is provided by an output of an external communications device 20 via a second switch 21. The communications device 20 may be, for example, a telephone. An external input 22, such as a microphone, is coupled through a third switch 23 to a third input of summing device 19. An output from summing device 19 is coupled to a second input of the second codec 16. A second output of said second codec 16 is coupled to a second input of a DSP unit 15. A second output of DSP unit 15 is coupled to a second input of first codec 14. A second output of first codec 14 is serially coupled to the communications device 20 via circuit node 24 and a fourth switch 25. Communications device 20 is coupled to a land-line 26. An external output 27, such as an audio speaker, is coupled through a fifth switch 28 to circuit node 24. An input to the external analog console 17 is coupled through a sixth switch 29 to circuit node 24.

There is a requirement for a system of signal routing devoid of the inherent limitations associated with the prior art. Moreover, it would be a desirable asset for an analog signal routing device to have its functionality defined at some later instance of its implementation, thereby allowing an increased flexibility and an enhanced self-diagnostics capability in its subsequent application.

Summary of the Invention.

This invention addresses at least some of the deficiencies prevalent within the prior art described above. In accordance with the invention there is provided a device for providing signal routing within a circuit. The device comprises first and second M x N matrices of switching elements coupled together, a plurality of inputs, coupled to said first matrix, for receiving a plurality of input signals and a plurality of outputs, coupled to said second matrix, for outputting a plurality of output signals. The first and

second M x N matrices provide a routing path for the plurality of input signals to the plurality of outputs.

In a preferred embodiment of the invention, any one of the plurality of input signals may be simultaneously routed, through said first and second matrices, to at least one output of said plurality of outputs or any combination of input signals may be simultaneously routed to at least one output. The routing of any input signal (or any combination thereof) to a desired output or outputs is achieved by the selective activation and deactivation of a plurality of microprocessor controlled switches located within both matrices. Moreover, the plurality of inputs may be isolated from the plurality of outputs, therein providing signal muting, by deactivating all of the controllable switches in either matrix. Furthermore,the preferred embodiment is implemented using integrated chip technology.

A exemplary embodiment of the invention will now be described with reference to the accompanying drawings.

Brief Description of the Drawings.

FIG. 1 illustrates the basic configuration of a prior art digital communications system.

FIG. 2 illustrates a preferred embodiment of an analog signal switching device in accordance with the present invention.

FIG. 3 illustrates the selective control of analog signal switching within the preferred embodiment of FIG. 2, as implemented through the use of a microprocessor.

FIG. 4 illustrates a typical implementation of the preferred embodiment of FIG. 3 within an electronic device.

Detailed Description of the Preferred Embodiment.

With reference to FIG. 2, there is illustrated a novel analog signal switching device in accordance with a preferred embodiment

of the present invention. A first M x N matrix 30 comprises a plurality (N) of input conductors 31-42, for receiving a plurality (N) of input signals, and a first plurality (M) of routing conductors a-h. The matrix 30 may be an integrated circuit of the type SGS-M093, manufactured by SGS. A switch is located at each cross-over of the plurality of input 31-42 and routing a-h conductors, which, when closed, produces a coupling therebetween. Therefore, the matrix contains M x N switches which provide a means of supplying a desired input signal to a first plurality of outputs realised by the plurality of routing conductors a-h. The plurality of outputs from the first M x N matrix 30 are each respectively coupled through one of a plurality of resistors R_1-R_8 to a plurality (M) of input terminals of a second M x N matrix 43. The plurality of input terminals being realised by a second plurality of routing conductors i-p.

A second plurality of output signals is each supplied from outputs 44-55 of a plurality of "summing" feedback amplifiers 56-67, wherein inverting inputs thereof respectively receive a proportion of the output therefrom through one of a plurality of resistive feedback paths. Each inverting input of each feedback amplifier 56-67 is coupled to an output conductor 68-79. Furthermore, each output conductor 68-79 is coupled to the second plurality of routing conductors i-p through a closable switch located at each cross-over therebetween. Hence, each one of the plurality of outputs 44-55 can provide an output signal generated by any desired combination of applied input signals.

Tables 1 & 2 respectively illustrate, by way of example only, typical input and output designations for the preferred embodiment of the invention.

Table 1.

Input	Input Designation
31	Outbound Microphone
32	Inbound from Base
33	Outbound Analog from Console
34	Outbound Phone Patch
35	Outbound D/A
36	Inbound D/A
37	External In
38	Deselect Speaker
39	Modem Output
40	Tx Signalling
41	Self Hear
42	DTMF

Table 2.

Output	Output Designation
44	Outbound Analog to Base
45	Inbound to Console
46	Select Speaker
47	Deselect Speaker
48	Inbound Phone Patch
49	Outbound A/D
50	Inbound A/D
51	Peak Detector
52	Microphone Output
53	Modem Input
54	Diagnostics Output
55	Rx Signalling

FIG. 3 illustrates the selective control of analog signal switching within the preferred embodiment of FIG. 2, as implemented through the use of a microprocessor. An address bus 80 of the microprocessor is coupled to the first and second M x N matrices such that an address word on the bus uniquely identifies and opens/closes the switch which corresponds to that address. Any switch on either M x N matrix 30, 43 may be selected subject to the activation of the desired matrix, through either a first 82 or a second 83 Chip Select control line responsive to said first 30 and second 43 matrices respectively, in association with a valid switch address. Furthermore, a Data On/Off line 81 may be provided to each matrix for purposes apparent to one skilled in the art. For example, by activating Chip Select 83 and applying a valid address on the address bus 80, switch (m,78) may be selected.

By way of a further example, and with the input and output designations as prescribed within Tables 1 & 2 respectively, the closure of switches (a,31), (b,40) and (c,31), (d,32) in association with (i,73), (j,73) and (l,70), (k,70) would respectively provide a split output signal of Outbound A/D 49 and Select Speaker 46. Thus, in the preferred embodiment, a digital signal processor (DSP) would process the Outbound Microphone input 31 and the Tx Signalling through the Outbound A/D 49 whilst the Outbound Microphone input 31 and the Inbound from Base signal 32 are fed through the Select Speaker output 46.

In yet another example, specific activity diagnostics can be performed by simultaneously routing inputs 31-34, via switches (c,31), (d,32), (e,33) and (f,34), to the peak detector output 51 by closing switches (k,75), (l,75), (m,75) and (n,75). The Outbound Microphone input 31, Inbound from Base 32, Outbound from Console 33 and Outbound Phone Patch 34 are summed together and output through the Peak Detector 51. The Peak Detector 51 serves as a diagnostics probe for a microprocessor (not shown) which is used to control the DIU circuitry. The output from the Peak Detector 51 can therefore be used, by the microprocessor, to monitor the activity and diagnostics of the circuitry. Specifically, the microprocessor would use the Peak Detector 51 to distinguish between noise (low level) and pure signal (high level) activity during normal DIU

operation and to automatically verify the operation of the circuit and, in the case of failure, to identify the fault. Furthermore, the magnitude of the Peak Detector output 51 could form the basis of a decision making process within the microprocessor and therefore define an operating parameter for the DIU.

FIG. 4 refers to a typical application of the invention. This example represents the application of the invention to the prior art environment of FIG. 1. Four external devices (a User, Base, Console and Land-Line) are coupled to a DIU. The routing matrices 31, 43 of the invention serve to route signals between the external devices and circuitry within the DIU, such as the DSP (through associated Codecs), a modem and control microprocessors (not shown) of FIG. 1. It should be appreciated by one skilled in the art that modem inputs/outputs to/from the preferred embodiment of the invention are unfiltered signals whereas the inbound/outbound analog signals to/from the preferred embodiment are typically filtered through a band pass filter. The invention can clearly be seen to offer distinct advantages over the prior art configuration as realised by the flexibility of signal routing. For example, the modem can be routed to the Land-Line or the Console and not just to the Base as was the limitation imposed by the prior art of FIG. 1.

Empirical results have demonstrated that the preferred embodiment of the invention has an immunity to cross-talk between signals of better than 80dB. Furthermore, the preferred embodiment offers a signal muting ability available through the deselection of all switches within either matrix whereby isolation of the plurality of input signals 31-42 is achieved.

It can clearly be appreciated that an invention so designed and described provides a flexible method of routing one or more of a plurality of inputs to one or more of a plurality of outputs and which is implemented through a software controlled technique. Therefore, the initial requirement to define fully the functionality within a device so implemented is eliminated and, consequentially, supplemental analog routing paths can be subsequentially defined. Moreover, the invention allows the simultaneous routing of a desired input to a plurality of outputs and the ability to simultaneously sum several inputs together in order to provide a

solitary output, wherein associated cross-talk therebetween is ostensibly reduced to negligible levels. In addition, the architecture of each a M x N matrix provides the desirable benefit of a signal muting facility therein. Furthermore, such an invention offers an improved diagnostics capability without the necessity of providing hardware specifically allocated therefor.

Claims.

1. A device for providing signal routing within a circuit comprising:

i) first (30) and second (43) M x N matrices of switching elements coupled together;

ii) a plurality of inputs (31-42), coupled to said first matrix (30), for receiving a plurality of input signals; and

iii) a plurality of outputs (44-55), coupled to said second matrix (43), for outputting a plurality of output signals, wherein

said first and second M x N matrices provide a routing path for the plurality of input signals (31-42) to the plurality of outputs (44-55).

2. A device for signal routing in accordance with claim 1, wherein any one of the plurality of input signals may be simultaneously routed to at least one output of said plurality of outputs (44-55) or any combination of input signals (31-42) may be simultaneously routed to at least one output.

3. A device for signal routing in accordance with claim 1 or 2, wherein the matrices (30, 43) each comprise a first plurality of conductors (a-h, i-p) and a second plurality of conductors (31-42, 68-79) wherein each one of the first plurality of conductors is independently coupled to each one of said second plurality through a controllable switch.

4. A device for signal routing in accordance with claim 3, wherein the first (30) and second (43) matrices are responsive to control means (80-83) through which said switches are selectively activated and deactivated such that routing of at least one input signal to at least one output of the device is achieved.

5. A device for signal routing in accordance with claim 4, characterised in that:

the first matrix (30) may divide each of the plurality of input signals into a multitude of inputs as realised by the first plurality of

conductors (a-h) in association with the closure of switches coupled thereto, wherein each of said multitude of inputs are individually coupled through a resistive means (R_1-R_8) to the first plurality of conductors (i-p) of the second matrix (43); and

the second matrix (43) may combine said multitude of inputs to provide an output (44-55) as realised by the closure of switches coupled between the first (i-p) and second (68-79) plurality of conductors of the second matrix (43).

6. A device for signal routing in accordance with claim 4 or 5, wherein the control means (80-83) is provided by a microprocessor.

7. A device for signal routing in accordance with any preceding claim, wherein

the plurality of outputs (44-55) are each amplified through an amplifier stage (56-67).

8. A device for providing signal routing within a circuit comprising:

i) first (30) and second (43) M x N matrices coupled together and comprising:

a) a first plurality of conductors (a-h, i-p);

b) a second plurality of conductors (31-42, 68-79); and

c) a plurality of controllable switches which couple said first plurality of conductors to said second plurality;

ii) a plurality of inputs (31-42), coupled to said first matrix (30), for receiving a plurality of input signals from said circuit;

iii) a plurality of outputs (44-55), coupled to said second matrix (43), for outputting a plurality of output signals, wherein

selective activation/deactivation of the controllable switches within the matrices (30, 43) provide a routing path, for the plurality of input signals (31-42) to the plurality of outputs (44-55); and

the plurality of input signals (31-42) may be isolated from the plurality of outputs (44-55) by deactivating all switches within either matrix (30, 43).

9. A method for routing signals through a device characterised in the steps of:

i) providing a plurality of input signals (31-42) to a plurality of inputs;

ii) providing a plurality of routing paths, as realised by a plurality of switches and a plurality of routing conductors (a-h, i-p, 68-79), between said inputs and a plurality of outputs (44-55);

iii) providing control means (80-83) for selectively activating a combination of switches so as to route at least one of said plurality of input signals, through said plurality of conductors, to at least one output.

10. A device for signal routing in accordance with any preceding claim, wherein the input signals are analog input signals.

11. A device for signal routing in accordance with any preceding claim, wherein the device is realised as an integrated circuit.

12. A device for signal routing substantially as described herein and with reference to FIGs. 2 and 3 of the accompanying drawings.

13. A method for signal routing substantially as described herein and with reference to FIGs. 2 and 3 of the accompanying drawings.

Patents Act 1977
Examiner's report to the Comptroller under Section 17 (The Search Report)

Application number
9124857.5

Relevant Technical fields

(i) UK Cl (Edition K) H4K: KPG; KPN; KRA; KSA; KSC; KTW; KWB
H4R: RCT; RCX

(ii) Int Cl (Edition 5) H04Q

Search Examiner
A C STRAYTON

Databases (see over)
(i) UK Patent Office

(ii)

Date of Search
2 APRIL 1992

Documents considered relevant following a search in respect of claims ALL

Category (see over)	Identity of document and relevant passages	Relevant to claim(s)
Y	GB 2184325 A page 2, lines 96-101	2, 5
X	GB 2109196 A figure 3	1, 3, 4, 6, 8, 9, 10
Y	GB 1572379 figure 1, 4	11
X	GB 1017031 figure 1	1, 3, 4, 6, 8, 9, 10
X	EP 0451999 figure 3	1, 3, 4, 6, 8, 9, 10

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Category	Identity of document and relevant passages	Relevant to claim(s)

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