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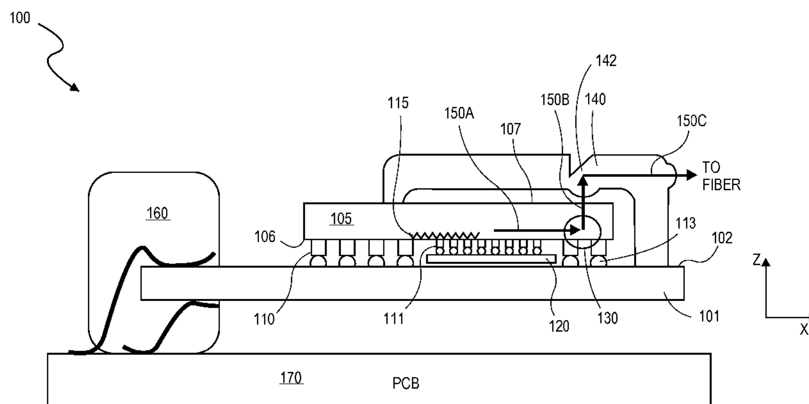

FIG. 1

(57) Abstract: Photonic integrated circuit (PIC) chips with backside vertical optical coupler and packaging into an optical transmitter/receiver. A grating-based backside vertical optical coupler functions to couple light to/from a plane in the PIC chip defined by thin film layers through a bulk thickness of the PIC chip substrate to emit/collect via a backside surface of the PIC chip where it is to be coupled by an off-chip component, such as an optical fiber. Embodiments of a grating-based backside vertical optical coupler include a grating coupler with a grating formed in a topside surface of the thin film. A reflector is disposed over the grating coupler to reflect light emitted from the grating coupler through the substrate to emit from the backside of the PIC chip or to reflect light collected from the backside of the PIC chip through the substrate and to the grating coupler.

AN EFFICIENT BACKSIDE-EMITTING/COLLECTING GRATING COUPLER

RELATED APPLICATION

[0001] This application is related to U.S. Patent Application No. 13/075,949, entitled "EFFICIENT SILICON-ON-INSULATOR GRATING COUPLER," filed on March 30, 2011.

TECHNICAL FIELD

[0002] Embodiments of the invention are generally related to photonic integrated circuits (PICs), and more particularly pertain to optical couplers for backside vertical light emission and collection.

BACKGROUND

[0003] Monolithically integrated photonic circuits are useful as optical data links in applications such as, but not limited to, optical communications, high performance computing and data centers. For mobile computing platforms too, a PIC is a useful means of I/O to rapidly update or sync a mobile device with a host device and/or cloud service where a wireless link has insufficient bandwidth. Such optical links utilize an optical I/O interface that includes an optical transmitter and an optical receiver. One challenge with the optical I/O interface is coupling light between monolithically integrated photonic circuits, which are fabricated on a micrometer scale, and separately packaged components (e.g., optical fiber, etc.) which are assembled on the millimeter scale. A PIC may utilize vertical or edge-based optical I/O coupling techniques. The edge coupling technologies have a substantial drawback in that device testing requires an edge to be provided, typically by singulating the substrate upon which the PIC was fabricated into individual PIC chips. The vertical coupling technologies, while advantageously amenable to "wafer-level" PIC testing, typically have lower coupling efficiency than do the edge technologies. For example, a surface coupled PIC may have an emission efficiency in the range of about 50%.

[0004] Another limitation with vertical coupling techniques is that the presence of optical I/O on a top side of the PIC is generally incompatible with advanced flip-chip or controlled collapse (C4) packaging techniques in which the top side of an IC is affixed to a package substrate (e.g., by bumps and solder balls). For such flip-chip techniques, it is difficult to provide a package substrate that doesn't occlude the vertical optical coupling.

[0005] As such, a vertical coupling technique that offers improved coupling efficiency and is amendable to flip-chip packaging would be highly advantageous in the provision of PICs, such as optical transmitters.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Embodiments of the present invention are illustrated by way of example, and not by way of limitation, and can be more fully understood with reference to the following detailed description when considered in connection with the figures in which:

[0007] Figure 1 is an illustration of a cross-section through an optical transmitter, in accordance with embodiments of the present invention;

[0008] Figure 2A is an illustration showing an expanded view of a cross-section through the vertical coupler section of an optical transmitter, in accordance with embodiments of the present invention;

[0009] Figure 2B is an isometric view of the optical transmitter illustrated in Figure 2A;

[0010] Figure 3A is a plot illustrating the emission efficiencies of a grating-based backside emitting vertical coupler in accordance with embodiments of the present invention;

[0011] Figure 3B is a plot illustrating insertion loss of a backside emitting vertical coupler as a function of wavelength in accordance with embodiments of the present invention;

[0012] Figure 4 is a schematic diagram of a mobile device including an optical transmitter, in accordance with embodiments of the present invention;

[0013] Figure 5 is a function block diagram of the mobile device illustrated in Figure 4, in accordance with an embodiment of the present invention; and

[0014] Figure 6 is a flow diagram illustrating a method of manufacturing an optical transmitter, in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION

[0015] In the following description, numerous details are set forth, however, it will be apparent to one skilled in the art, that the present invention may be practiced without these specific details. In some instances, well-known methods and devices are shown in block diagram form, rather than in detail, to avoid obscuring the present invention. Reference throughout this specification to "an embodiment" means that a particular feature, structure, function, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. Thus, the appearances of the phrase "in an embodiment" in various places throughout this specification are not necessarily referring to the same embodiment of the invention. Furthermore, the particular features, structures, functions, or characteristics may be combined in any suitable manner in one or more embodiments. For example, a first embodiment may be combined with a second embodiment anywhere the two embodiments are not mutually exclusive.

[0016] The terms "coupled" and "connected," along with their derivatives, may be used herein to describe functional or structural relationships between components. It should be understood that these terms are not intended as synonyms for each other. Rather, in particular embodiments, "connected" may be used to indicate that two or more elements are in direct physical, optical, or electrical contact with each other. "Coupled" my be used to indicated that two or more elements are in either direct or indirect (with other intervening elements between them) physical, optical, or electrical contact with each other, and/or that the two or more elements co-operate or interact with each other (e.g., as in a cause an effect relationship).

[0017] The terms "over," "under," "between," and "on" as used herein refer to a relative position of one component or material layer with respect to other components or layers where such physical relationships are noteworthy. For example in the context of material layers, one layer disposed over or under another layer may be directly in contact with the other layer or may have one or more

intervening layers. Moreover, one layer disposed between two layers may be directly in contact with the two layers or may have one or more intervening layers. In contrast, a first layer "on" a second layer is in direct contact with that second layer. Similar distinctions are to be made in the context of component assemblies.

[0018] Described herein are architectures for PIC chips, particularly optical transmitters, that include a backside vertical optical coupler. In the exemplary optical transmitter, the backside vertical optical coupler functions to couple light from a plane in the PIC chip defined by thin film layers and through a bulk thickness of the PIC chip substrate to emit from a backside surface of the PIC chip where it is to be collected by an off-chip component, such as a wire terminal. It should also be noted, that while a detailed description of an optical receiver application of the backside vertical optical coupler is omitted for the sake of brevity, one or ordinary skill would be able to apply the backside vertical optical coupler architecture and techniques described herein to achieve a vertical collection of light from a backside surface of the PIC chip. As such, the architectures described in detail herein are applicable to both emission and collection of light for optical transceiver (I/O).

[0019] Figure 1 is an illustration of a cross-section through an optical transmitter 100, in accordance with embodiments of the present invention. The optical transmitter 100 includes a PIC chip 105 flip-chip bonded to a package substrate 101. Embodiments of the present invention are not limited with respect to the package substrate 101. For example, in one embodiment the package substrate 101 is an organic substrate (e.g., comprising a core with build-up layers and plated interconnects) and in an alternate embodiment, the package substrate 101 is an interposer which is then to be bonded to a packaging substrate or a printed circuit board (PCB). Likewise, while the package substrate 101 is illustrated as being coupled to the PCB 170 through a high speed electrical connector 160, embodiments of the present invention are not limited in this respect.

[0020] As shown in Figure 1, the PIC chip has a frontside 106 and a backside 107. Flip-chip, also known as controlled collapse (C4) bonding of the PIC chip 105 entails electrically coupling bumps 110 present on the PIC chip frontside 106 to a side 102 of the package substrate 101 (e.g., via solder balls 113) so that the

PIC chip frontside 106 faces the package substrate 101. Proximate to the PIC chip frontside 106 (i.e., distal from the backside 107) are thin film layers in which an optical device(s) 115 is fabricated and encapsulated. The optical device(s) 115 includes at least a monolithically integrated optical waveguide and in the exemplary embodiment, where the PIC 105 is an integrated photonic transmitter (Tx), the optical device(s) 115 further includes a laser optically coupled to the waveguide, and may also include at least one modulator (e.g., based on Mach-Zehnder interferometer, ring resonator, etc.) coupled to the waveguide. The PIC chip backside 107 is a major surface (non-edge surface) of the chip that is most distal from the optical device(s) 115.

[0021] In the exemplary embodiment, the optical transmitter 100 includes a second IC chip 120 integrated with the PIC chip 105 at the package level. As shown, the second IC chip 120 is bonded to the PIC chip 105 to be disposed between the PIC chip 105 and the package substrate 101. To minimize routing length, the second IC chip 120 may be flip chip bonded to the PIC chip 105 (e.g., with bumps 111) such that the PIC chip frontside 106 faces a frontside of the second IC chip 120. Depending on the embodiment, the second IC chip 120 may serve a number of functions and may generally be any integrated electrical circuit which is not monolithically integrated into the PIC chip 105 but benefits the optical transmitter 100 when directly coupled to the PIC chip 105 as illustrated in Figure 1. For example, in the exemplary embodiment, the second IC chip 120 is a driver for the optical device(s) 115, such as a driver of a laser and/or a modulator disposed on the PIC chip 105.

[0022] As further illustrated in Figure 1, the optical transmitter 100 further includes a backside emitting vertical coupler in region 130. The backside emitting vertical coupler couples light from the optical device(s) 115, through the bulk thickness of the PIC chip 105 to be emitted from the PIC chip backside 107 where it is collected by lens 140 for further coupling into a downstream component, such as an optical wire. During operation of the optical transmitter 100, a light signal 150A emitted from (e.g., a laser) or contained in (e.g., by an optical waveguide) is predominantly confined to paths which are substantially parallel to the PIC chip frontside 106 (e.g., parallel to the X-axis) until the light signal reaches

the region 130, at which point the light signal 150A is coupled into a direction substantially perpendicular to the PIC chip frontside 106(e.g., parallel to the Z-axis). In embodiments, the light signal 150B passes through a bulk thickness of the PIC chip 105 as confined only by the bulk material (e.g., without a waveguide). In the illustrative example, the lens 140 is integrated with a 45 ° mirror 142 to redirect light signal 150B back to a path substantially parallel to the PIC chip topside frontside 106 (e.g., parallel to the X-axis) for coupling to a wire terminal. In alternate embodiments however, any manner of beam collection, conditioning and steering known in the art may be adapted to the light signal 150B as emitted from the PIC chip backside 107.

[0023] Generally, the backside emitting vertical coupler 130 may take a number of structural forms. For example, in one embodiment the backside emitting vertical coupler 130 is a 45° mirror (analogous to the mirror 142) formed in a thin film layer of the PIC chip 105, such as a silicon nitride layer. In the exemplary embodiment however, backside emitting vertical coupler is based on an optical grating. Optical gratings offer some manufacturing advantages over a 45° mirror as grayscale lithography or other commonly employed techniques for sloping features is difficult and/or expensive. In particular embodiments described herein however, grating-based vertical couplers offer a further advantage of lower loss, lower back reflection, and lower numerical aperture (NA) than 45° mirror embodiments.

[0024] Figure 2A is an illustration showing an expanded view of the optical transmitter 100 along a cross-sectional plane A-A', in accordance with embodiments of the present invention. In one embodiment, the PIC chip 105 includes a silicon substrate. Silicon-based photonic ICs advantageously integrate well with conventional semiconductor fabrication techniques that have been developed for fabrication of CMOS electrical integrated circuits. A silicon substrate may be either bulk crystalline silicon or a silicon-on-insulator (SOI) substrate. In the exemplary embodiment illustrated in Figure 2A, the PIC chip 105 includes a bulk single crystalline silicon support substrate 105A, a single crystalline silicon device layer 105C, and an intervening insulator layer 105B (e.g., buried silicon dioxide layer). While thicknesses (in the z-dimension) of the various layers in an SOI substrate may vary, the device layer 105C and insulator layer 105B are

considered thin films relative to the support substrate 105A. In the exemplary embodiment, the support substrate 105A is between approximately 100 and 800 μιη thick while the insulator layer 105B is approximately 1 μιη thick, and the device layer 105C is approximately 400 nm thick.

[0025] As depicted in Figure 2A, at least the silicon device layer 105C is fabricated into a waveguide 260 that conducts the light signal 150A parallel to the PIC chip frontside 106 (i.e., along x-dimension) during chip operation. The waveguide 260 may take many forms, such as rib and/or slab, as known in the art. As further illustrated in Figure 2A, the waveguide 260 is optically coupled to a grating coupler 265. The grating coupler 265 is generally a waveguide that comprises a grating lines 265A formed into a top surface of the waveguide. The grating lines 265A have a grating period *P* and a height *H* and extending along the longitudinal axis of the grating coupler (e.g., x-dimension in Figure 2). Notably, the grating lines 265A are proximate the PIC chip frontside 106, facing a mirror or reflector 233 disposed between the grating coupler 265 and the PIC chip frontside 106 to be between the optical grating coupler 265 and the package substrate 101, when the PIC chip 105 is flip-chip bonded.

[0026] Returning to Figure 2A, during operation, a fraction of the light within the grating coupler 265 is scattered towards the PIC chip backside 107 while the rest of the optical power is emitted toward the reflector 233. For grating lines 265A having a certain grating pitch and duty cycle (line:space ratio), a reflector 233 of sufficiently high reflectivity and properly spaced from the grating line by spacing *V*, reflects the topside directed optical emission to constructively interfere with the scattered light leaked from the grating coupler 265 and constitute the light signal 150B which is propagated through the bulk substrate 105A and emitted from the PIC chip backside 107. With this vertical coupling architecture, very high efficiency (e.g., greater than 90%) can be achieved.

[0027] Of course, in the context of an optical receiver, the grating coupler 265 may also serve to collect light from the PIC chip backside 107. In this mode of operation, the reflector 233 then reflects a bottomside directed optical emission to the grating coupler 265 which is then propagated through the waveguide 260.

[0028] Figure 2B is an isometric view of an architecture for coupling light

in a waveguide to a backside vertical emitting grating coupler, in accordance with an embodiment. The A-A' plane illustrated of Figure 2A is illustrated as a dashed line A-A' in Figure 2B with the PIC chip 105 oriented as it would during fabrication of the grating coupler 265 with the axis legend reoriented from Figure 2A accordingly. As shown, light signal 150A is first carried by a rib waveguide 260A, a taper 261 then couples the light through a slab waveguide 260B that is adiabatically coupled into the grating coupler 265. As illustrated, the waveguide 260, (rib 260A or slab 260B) includes opposing sidewalls 166 that are nominally vertical (i.e., with 5° of the z-axis) with a top surface 167 disposed there between. In the grating coupler 265, the grating line height (e.g. H in Figure 2A) is such that a top surface of the grating lines are coplanar with a top surface of the rib waveguide 260A and therefore extend above the top surface of the region beyond the ends of the grating lines 265A. Thus, relative to the surrounding regions, the grating lines 265A are well-described as fins. The grating lines 265A extend in the y-dimension across a top surface of the grating coupler with spaces between the grating lines recessed to define a recessed top grating coupler surface which is below the top surface of the region beyond the ends of the grating lines 265A. Opposing sidewalls of the optical grating coupler therefore entail both opposing ends of the grating lines 265A and adjacent ends of trenches between the lines. As further shown in Figure 2B, where the slab waveguide 260A is defined by sidewalls 166 that extend to the insulator layer 105B, recesses or trenches corresponding to spaces between the grating lines 265A do not perforate the device layer 105C to expose the insulator layer 105B.

[0029] In the exemplary embodiment, the taper 261 entails a reduction in the y-dimension of the rib waveguide 260A. In other embodiments however, the taper 261 may include a taper in the z-dimension in the alternate, or in combination with the y-dimension taper. It should be noted that while the structures illustrated in Figure 2B efficiently couple the light signal 150A into the grating coupler 265, other designs may be utilized without departing from the spirit of the backside vertical emission grating couplers described herein.

[0030] As shown in Figure 2B, the reflector 233 is dimensioned to occupy at least the area of the grating coupler 265 with the reflector 233 disposed in

substantial alignment with the grating coupler 265 in the vertical (z) dimension. Smaller reflector dimensions or misaligned reflectors will generally disadvantageously reduce emission efficiency. Thus, in the exemplary embodiment shown in Figures 2A and 2B, the reflector 233 has a length L that is at least equal to the longitudinal length of the grating coupler (i.e., reflector 233 extends over all grating lines 265A and spaces there between) and the reflector width *W* is similarly at least equal to the transverse length of the grating lines 265A (y-dimension).

[0031] Generally, the reflector 233 is to have a high reflectivity over the wavelengths of interest. Embodiments employing a metal thin film for the reflector 233 advantageously offer high reflection over a wide spectral bandwidth. In embodiments, the reflector 233 is a thin film of metal such as aluminum with aluminum embodiments offering the advantage of greater compatibility with silicon CMOS-type fabrication constraints while offering a higher reflectivity than that of other metals such as copper, titanium, or the like frequently utilized as interconnect metals in CMOS ICs. The thickness of the thin film metal need only be a few tens of nanometers (e.g., 10-20 nm), but in the exemplary embodiment is greater than 100 nm for sake of controlling the process utilized for forming of the reflector 233. In other embodiments, the reflector 233 may comprises a stack of dielectric materials of alternating high and low refractive index (i.e., a H-L index stack).

[0032] As illustrated in Figure 2A, disposed over the waveguide 260 and between the grating coupler 265 and the reflector 233 is an interlayer dielectric (ILD) 235, such as silicon dioxide or other material offering suitable index contrast. Additional ILD may be disposed over the reflector 233 encapsulating the reflector 233, augmenting the thickness of the dielectric waveguide cladding, etc. As such, because the grating lines 265A can be fabricated using known techniques and formation of the reflector 233 is straightforward as it is disposed over the grating lines 265A (i.e., formed after the grating lines 265A are etched rather than as a buried layer), the backside emitting vertical grating coupler embodiments described herein are highly manufacturable.

[0033] Figure 3A is a plot illustrating the emission efficiencies of a backside emitting vertical coupler as a function of wavelength (λ) and the spacing *V* between the reflector 233 and grating line 265A in accordance with embodiments of

the present invention. Figure 3B is a plot illustrating insertion loss of a backside emitting vertical coupler as a function of free space wavelength for $V=0$ in accordance with embodiments of the present invention. For Figures 3A and 3B, the backside vertical grating coupler having the architecture illustrated in Figures 2A and 2B is implemented with a grating period P of approximately 500 nm, a grating duty cycle of approximately 70% and a grating height H of approximately 220 nm for a 400 nm thick silicon device layer 105C. For these parameters in the exemplary SOI substrate, the light signal 150B is emitted as a beam in substrate 105A with an effective numerical aperture (NA) of approximately 0.1 and an emission angle of less than 5° in silicon substrate.

[0034] As shown in Figure 3A, backside emission efficiency is as high as -91.4% as a function of wavelength (λ) and the spacing V between the reflector 233 and grating line 265A. As illustrated, because aluminum reflector embodiments have broadband low-loss reflection, embodiments described herein have a large bandwidth (e.g., >80 nm at ldB full-width) making the architectures suitable for multi-wavelength systems such as wavelength division multiplexing (WDM) optical links. The dependency on the spacing *Vis* due to the optical interference between light leaked toward the PIC chip backside 107 and that reflected toward the PIC chip backside 107 by the reflector 233. However, as shown in Figure 3A, this dependency in spacing *Vis* relatively weak with efficiency being over 85% for a 0.1 μιη (100 nm) range, which can be easily achieved as the spacing V may be defined by a thin film deposition (e.g., by a silicon dioxide CVD) process. For example, at a wavelength of 1.3μιη, 91% efficiency occurs at a spacing V of 0.4 μιη and is not significantly reduced until *V is* greater than approximately 0.44 um or is less than approximately 0.34.

[0035] As shown in Figure 3B, an embodiment of the backside emitting grating coupler where the spacing V is 0 (i.e., an aluminum reflector 233 is disposed directly on the grating lines 265A) illustrated insertion loss to be as low at 0.5dB at a spectral peak. As such, the backside emitting vertical grating coupler embodiments described herein offer high emission efficiency.

[0036] While the optical transmitter 100 including a backside emitting vertical grating coupler described herein may be utilized in many system-level

applications, Figure 4 is a schematic diagram of a mobile computing platform including an optical transmitter in accordance with embodiments of the present invention. The mobile computing platform 400 may be any portable device configured for each of electronic data display, electronic data processing, and wireless electronic data transmission. For example, mobile computing platform 400 may be any of a laptop, a netbook, a notebook, an ultrabook, a tablet, a smart phone, etc. and includes a display screen 402, which may be a touchscreen (e.g., capacitive, resistive, etc.) the optical transmitter 410, and a battery 413.

[0037] The optical transmitter 410 is further illustrated in the expanded functional block view 420 illustrating an array of electrically pumped lasers 401 controlled by circuitry 462 coupled to a passive semiconductor layer over, on, or in, substrate 403. The semiconductor substrate 403 further includes a plurality of optical waveguides 405A - 405N over which a bar of gain medium material 423 is bonded to create, along with the reflectors 409A-409N, an array of lasers that during operation generate a plurality of optical beams 419A - 419N in the plurality of optical waveguides 405A - 405N, respectively. The plurality of optical beams 419A - 419N are modulated by modulators 4 13A- 4 13N and then selected wavelengths of the plurality of optical beams 419A - 419N are then combined with optical multiplexer 417 to output a single optical beam 421, which is then to be optically coupled through the backside emitting vertical coupler 130, for example using a grating-based backside emitting vertical coupler substantially as describe elsewhere herein, and into an optical wire 453. The optical wire 453 is further coupled to a downstream optical receiver external to the mobile computing platform 400 (i.e., coupled through the platform optical I/O terminal) or is further coupled to a downstream optical receiver internal to the mobile computing platform 400 (i.e., a memory module).

[0038] In one embodiment, the grating-based backside emitting vertical coupler is capable of transmitting data at the multiple wavelengths included in the optical beam 421 over the single optical wire 453 at speeds of at least 25 Gb/s and potentially more than 1 Tb/s. In one example, the plurality of optical waveguides 405 A - 405N are spaced approximately 50-100 μιη apart in a single silicon layer for an entire bus of optical data occupying a PIC chip of less than 4 mm on a side.

[0039] Figure 5 is a functional block diagram of the mobile computing platform 400 in accordance with one embodiment of the invention. The mobile computing platform 400 includes a board 1002. The board 1002 may include a number of components, including but not limited to a processor 1004 and at least one communication chip 1006. The processor 1004 is physically and electrically coupled to the board 1002. In some implementations the at least one communication chip 1006 is also physically and electrically coupled to the board 1002. In further implementations, the communication chip 1006 is part of the processor 1004. Depending on its applications, mobile computing platform 400 may include other components that may or may not be physically and electrically coupled to the board 1002. These other components include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory, a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, touchscreen display, touchscreen controller, battery, audio codec, video codec, power amplifier, global positioning system (GPS) device, compass, accelerometer, gyroscope, speaker, camera, and mass storage device (such as hard disk drive, solid state drive (SSD), compact disk (CD), digital versatile disk (DVD), and so forth).

[0040] At least one of the communication chips 1006 enables wireless communications for the transfer of data to and from the mobile computing platform 400. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 1006 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.1 1 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The mobile computing platform 400 may include a plurality of communication chips 1006. For instance, a first communication chip

1006 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 1006 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

[0041] The processor 1004 includes an integrated circuit die packaged within the processor 1004. The term "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory. Either of the communications chip 1006 may entail the optical transmitter 100, substantially as described elsewhere herein.

[0042] With the device and system-level architectures described, methods for forming the optical transmitter 100 are now described in reference to Figure 6. The method 600 is illustrated in Figure 6 by high level operations which may each further include a number of separate processing operations, as known in the art. No order is to be implied by the relative position of the operations in Figure 6, however an order of operations may be implicit where one operation necessarily operates on the output of another operation.

[0043] Method 600 begins at operation 601 with fabrication of a waveguide and grating coupler on a substrate, such as an SOI substrate, as a function region of an optical transmitter PIC chip. Any techniques known in art, such as photolithography and anisotropic silicon plasma etch, etc. may be utilized to form a grating coupler (e.g., the grating coupler 265 illustrated in Figures 2A and 2B) and a waveguide (e.g., the waveguide 260 in Figures 2A and 2B). For example, a silicon layer of a silicon-on-insulator (SOI) substrate is etched to define horizontal sidewalls and recesses are etched into a top surface of the rib or slab between the horizontal sidewalls.

[0044] At operation 605, an ILD is deposited over the grating coupler and waveguide formed in operation 601. For example, in one embodiment a layer of silicon dioxide is deposited with a conventional CVD or plasma enhanced (PE)CVD process.

[0045] At operation 610, a reflector (e.g., reflector 233) is formed on the ILD layer deposited at operation 605. In one embodiment, a thin film of metal, such

as aluminum, is deposited by physical vapor deposition (PVD), masked in regions aligned with the grating coupler with known photolithography techniques, and etched with conventional plasma or wet chemical techniques. In certain embodiments the metal thin film utilized for the reflector is also utilized for interconnects in the Tx PIC, for example with aluminum traces coupling to ohmic metal contact regions of a laser or modulator portion of the waveguide.

[0046] At operation 615, the reflector formed at operation 610 is encapsulated by a ILD layer, such as silicon dioxide deposited with a CVD or PECVD process. Conventional backend processing (e.g., C4-type build up layers and bumping) completes the PIC chip, as known in the art, with top side functional/parametric test of the PIC is also performed prior to PIC chip singulation.

[0047] At operation 620, a die-on-die stacking process may be optionally performed to flip-chip bond a driver IC chip to the Tx PIC chip, so that a frontside of the PIC chip faces a frontside of the drive IC chip, (e.g., as illustrated in Figure 1).

[0048] At operation 625, a singulated Tx PIC chip is flip-chip bonded to a package substrate, such as the package substrate 101 illustrated in Figure 1, using known packaging/soldering techniques so that a frontside of the PIC chip faces the package substrate.

[0049] At operation 630 a lens is affixed to align with a region of the Tx PIC chip backside where the grating coupler is to emit a beam from the PIC chip backside. Conventional lens bonding techniques may be utilized to bond the lens (e.g., lens 140) to either the package substrate or directly to the PIC chip.

[0050] Method 600 is then completed with operation 640, where the packaged Tx PIC is assembled onto a PCB using any techniques conventional to the art.

[0051] It is to be understood that the above description is illustrative, and not restrictive. For example, while flow diagrams in the figures show a particular order of operations performed by certain embodiments of the invention, it should be understood that such order may not be required (e.g., alternative embodiments may perform the operations in a different order, combine certain operations, overlap certain operations, etc.). Furthermore, many other embodiments will be apparent to

those of skill in the art upon reading and understanding the above description. Although the present invention has been described with reference to specific exemplary embodiments, it will be recognized that the invention is not limited to the embodiments described, but can be practiced with modification and alteration within the spirit and scope of the appended claims. The scope of the invention should, therefore, be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

CLAIMS

What is claimed is:

1. An integrated optical transmitter, comprising:

a package substrate;

a photonic integrated circuit (PIC) chip flip-chip bonded to the package substrate with a optical waveguide and an optical grating-based vertical coupler disposed in thin film layers on a frontside of the PIC facing the package substrate; and

an optical lens to couple light to the vertical coupler through a backside of the PIC chip.

2. The optical transmitter of claim 1, further comprising a second integrated circuit (IC) chip flip-chip bonded to the PIC chip and disposed between the PIC chip and the package substrate.

3. The optical transmitter of claim 2, wherein the PIC further comprises a laser coupled to the optical waveguide and wherein the second IC comprises a driver electrically coupled to the laser.

4. The optical transmitter of claim 1, wherein the vertical coupler further comprises:

an optical grating coupler to receive light from the optical waveguide; and

a reflector disposed between the optical grating coupler and the package substrate to reflect light emitted from the optical grating coupler toward the backside of the PIC chip.

5. The optical transmitter of claim 4, wherein the optical grating coupler comprises a grating formed in a thin film surface that faces the reflector.

6. The optical transmitter of claim 4, wherein the reflector comprises a metal

thin film having a surface area facing the optical grating coupler that is at least equal to a chip area occupied by the optical grating coupler.

7. The optical transmitter of claim 6, wherein the metal is selected from the group consisting of aluminum, silver, and gold.

8. The optical transmitter of claim 4, wherein the optical waveguide and optical grating coupler consists essentially of single crystalline silicon and wherein the reflector is spaced apart from the optical grating coupler by an interlayer dielectric (ILD).

9. The optical transmitter of claim 8, wherein the single crystalline silicon is spaced apart from a single crystalline substrate by an insulator layer, and wherein the ILD comprises silicon dioxide.

10. A photonic integrated circuit, comprising:

a substrate;

a first thin film dielectric layer disposed over a frontside of the substrate;

an optical waveguide and an optical grating coupler disposed over the thin film dielectric layer;

a second thin film dielectric layer disposed over the optical grating; and

a thin film metal layer disposed over the second thin film dielectric layer, wherein the thin film metal layer is aligned with the optical grating coupler to reflect light from the optical grating coupler through a backside of the substrate or to reflect light from the backside of the substrate to the optical grating coupler.

11. The photonic integrated circuit of claim 10, wherein the optical waveguide comprises a first top surface between first opposing sidewalls along a first longitudinal length and wherein the optical grating coupler comprises second top surface between second opposing sidewalls along a second longitudinal length, wherein the second top surface has recesses defining a grating period in a direction parallel to the second longitudinal length.

12. The photonic integrated circuit of claim 10, wherein the recesses are facing the thin film metal layer.

13. The photonic integrated circuit of claim 10, wherein the thin film metal layer is disposed a distance apart from the optical grating coupler to constructively interfere with scattered light leaking into the substrate from a bottom surface the optical grating coupler opposite the top surface.

14. The photonic integrated circuit of claim 11, wherein the substrate, optical waveguide, and optical grating coupler consist essentially of single crystalline silicon, and wherein first thin film dielectric layer, and the single crystalline silicon are each layers of an SOI wafer.

15. The photonic integrated circuit of claim 14, wherein a beam of light emitted through the substrate has an NA of approximately 0.1 with an emission angle of less than 5°.

16. The photonic integrated circuit of claim 14, wherein a beam of light emitted from the backside of the substrate has an emission efficiency greater than 85%.

17. A method of manufacturing an optical transmitter, comprising:

fabricating a photonic integrated circuit chip, the fabricating further comprising:

forming an optical waveguide and an optical grating coupler in a thin film disposed on a frontside of a substrate;

depositing an interlayer dielectric over the optical waveguide and optical grating coupler; and

depositing and patterning a metal thin film later to form a reflector aligned over the optical grating coupler.

18. The method of claim 17, wherein forming the optical grating coupler further

comprises etching a silicon layer of a silicon-on-insulator (SOI) substrate into a rib or slab having recesses disposed in a top surface between opposing sidewalls, and wherein depositing the metal thin film further comprises depositing aluminum.

19. The method of claim 17, further comprising:

flip-chip bonding the PIC chip to a package substrate, the frontside of the PIC chip facing the package substrate; and

affixing a lens to receive light emitted from a backside of the PIC chip.

20. The method of claim 17, flip-chip bonding an integrated circuit (IC) chip to the PIC chip, a frontside of the PIC chip facing a frontside of the IC chip, wherein the reflector is disposed between the optical grating coupler and at least one of the IC chip and the package substrate.

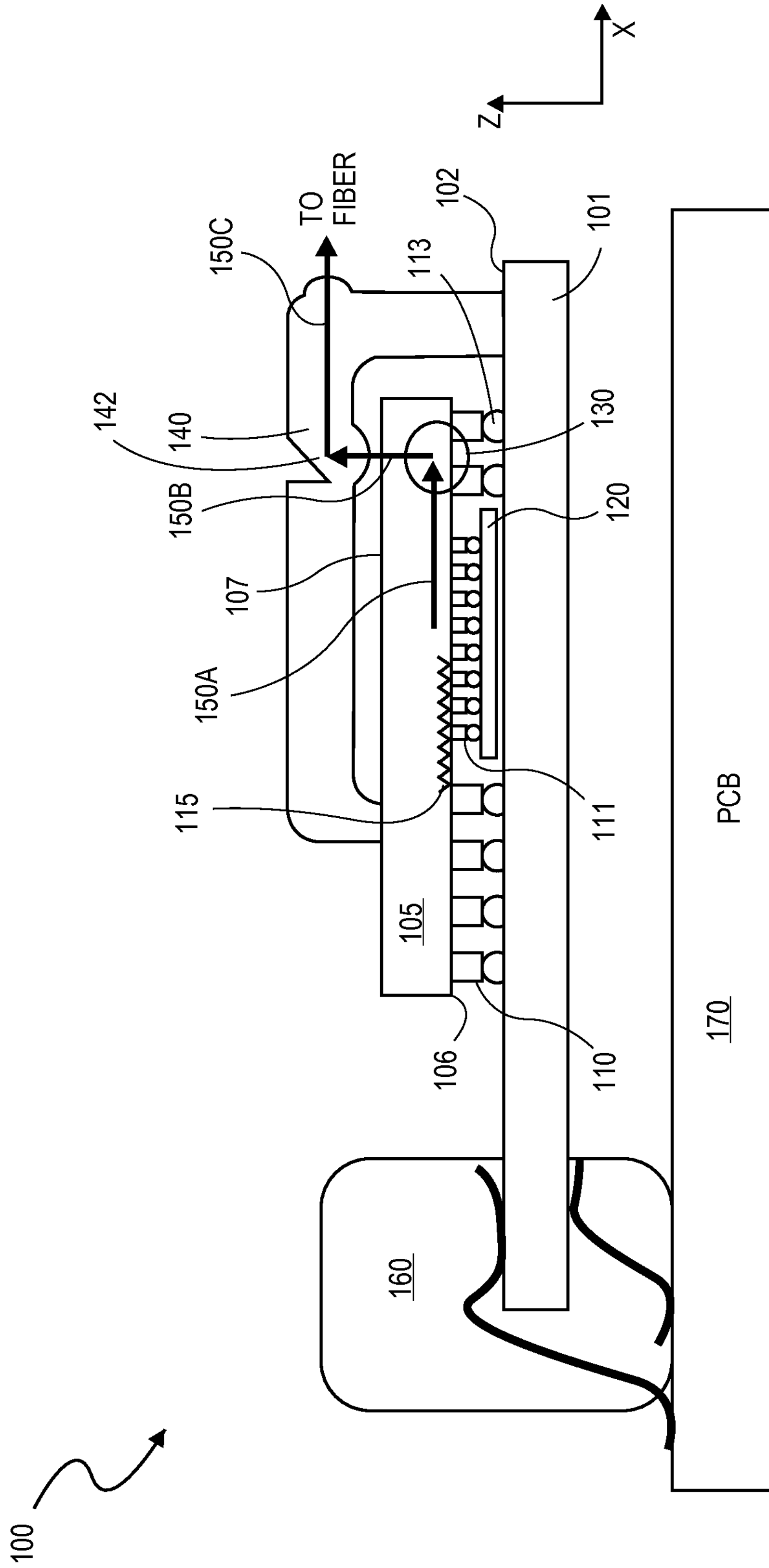

FIG. 1

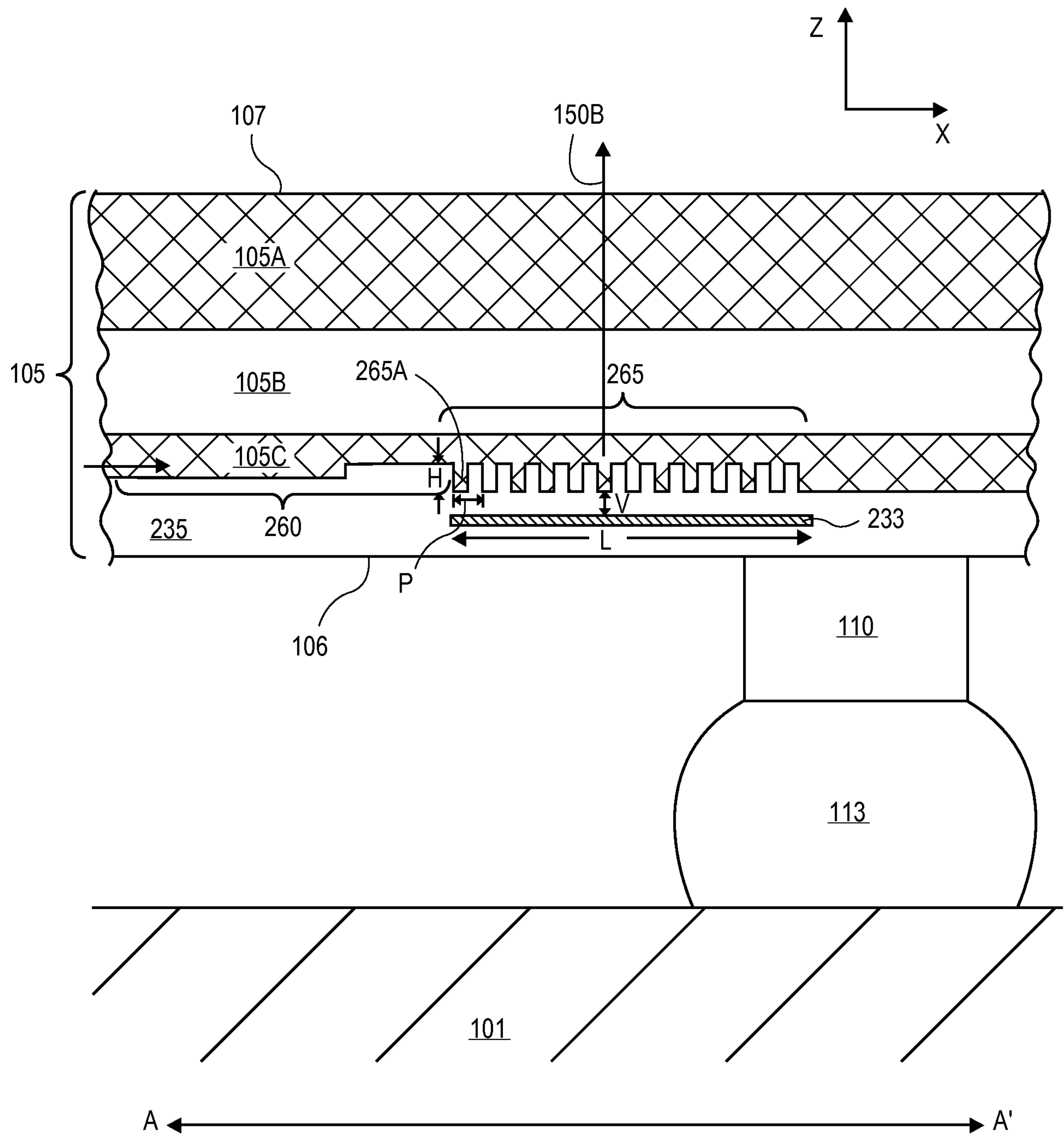

FIG. 2A

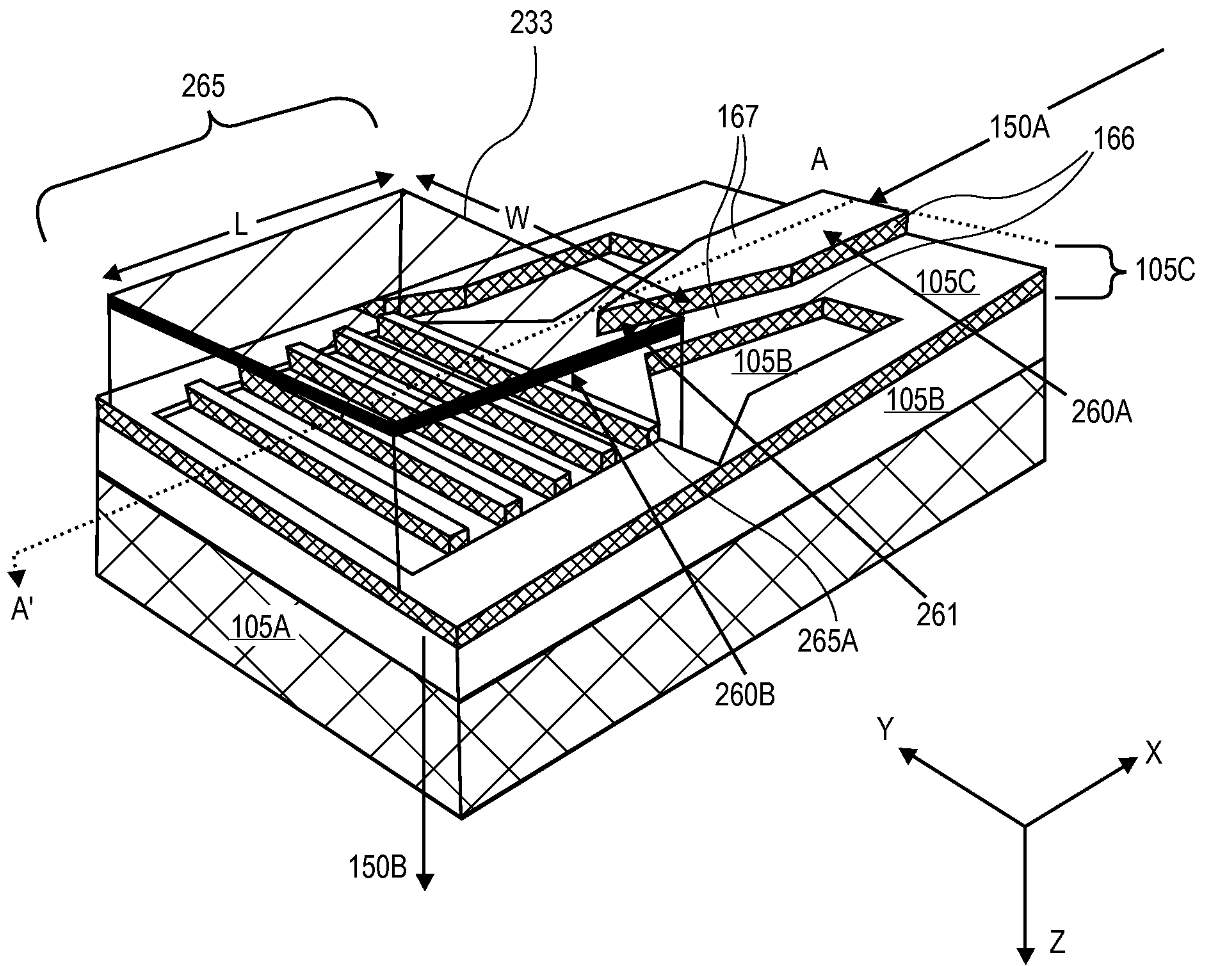

FIG. 2B

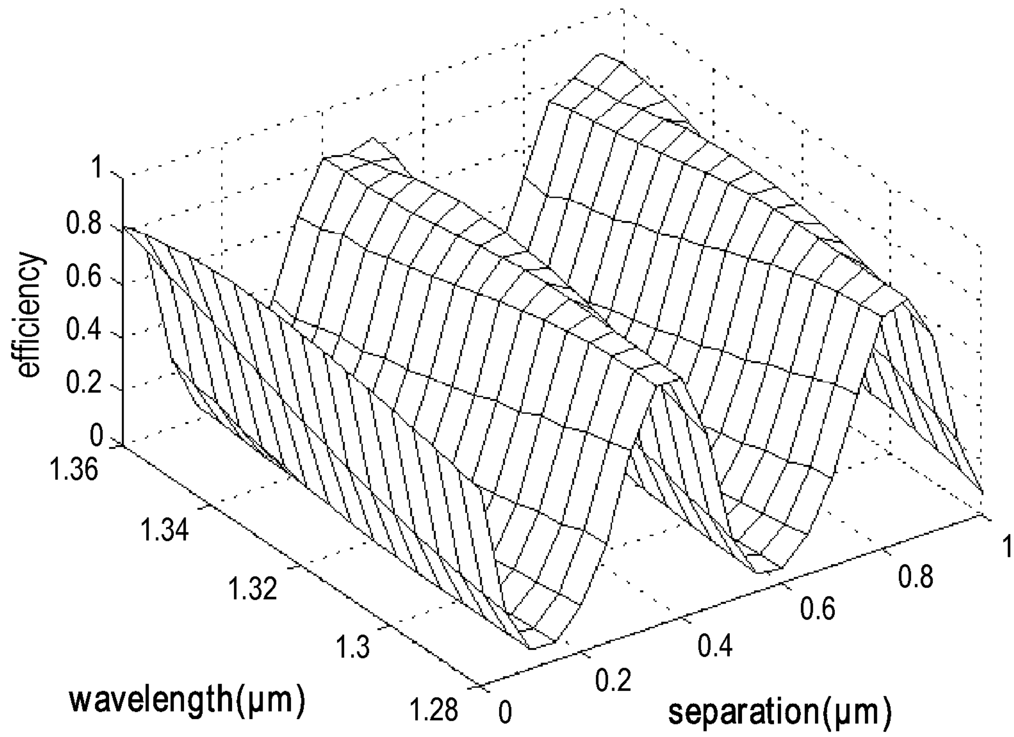

FIG. 3A

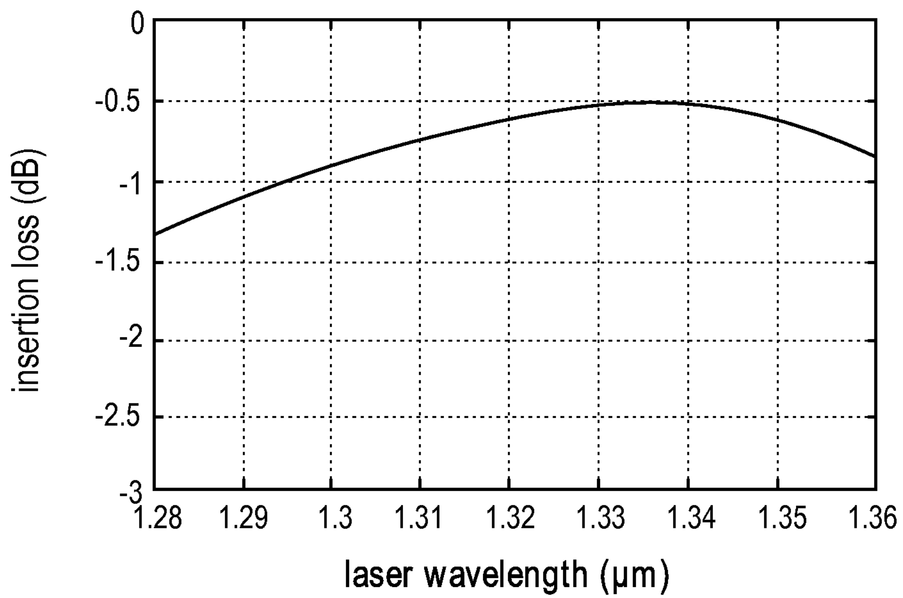

FIG. 3B

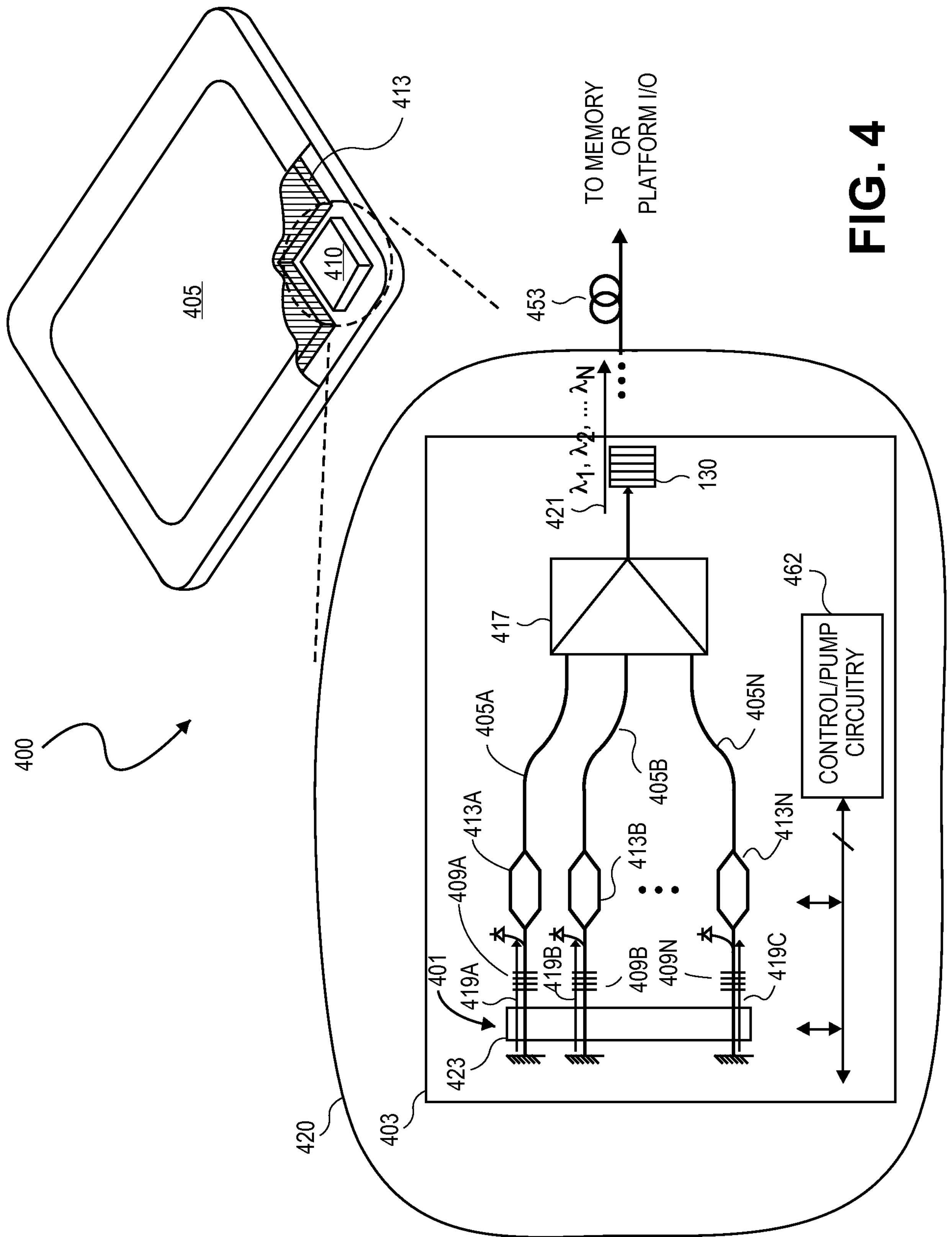

FIG. 4

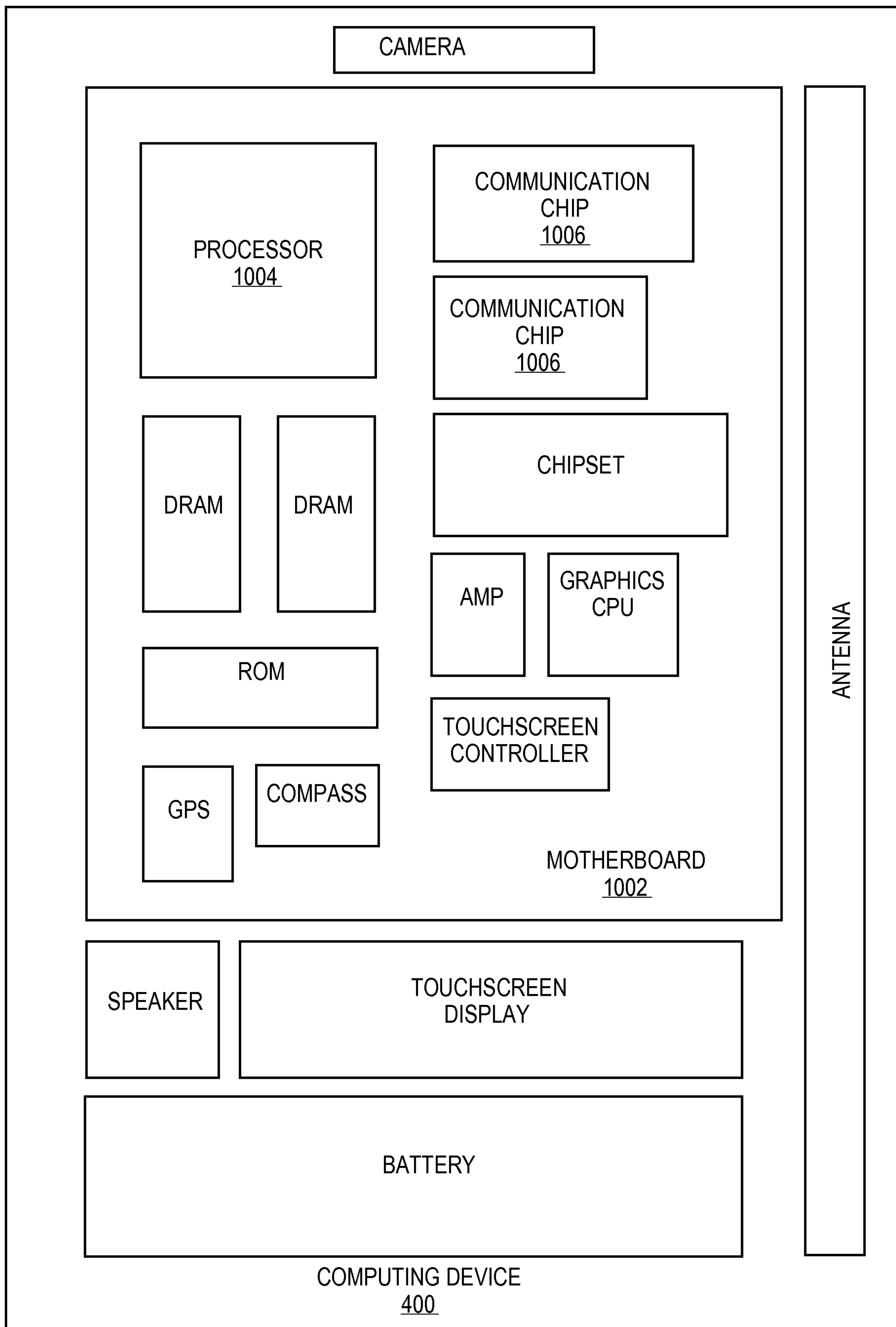

FIG. 5

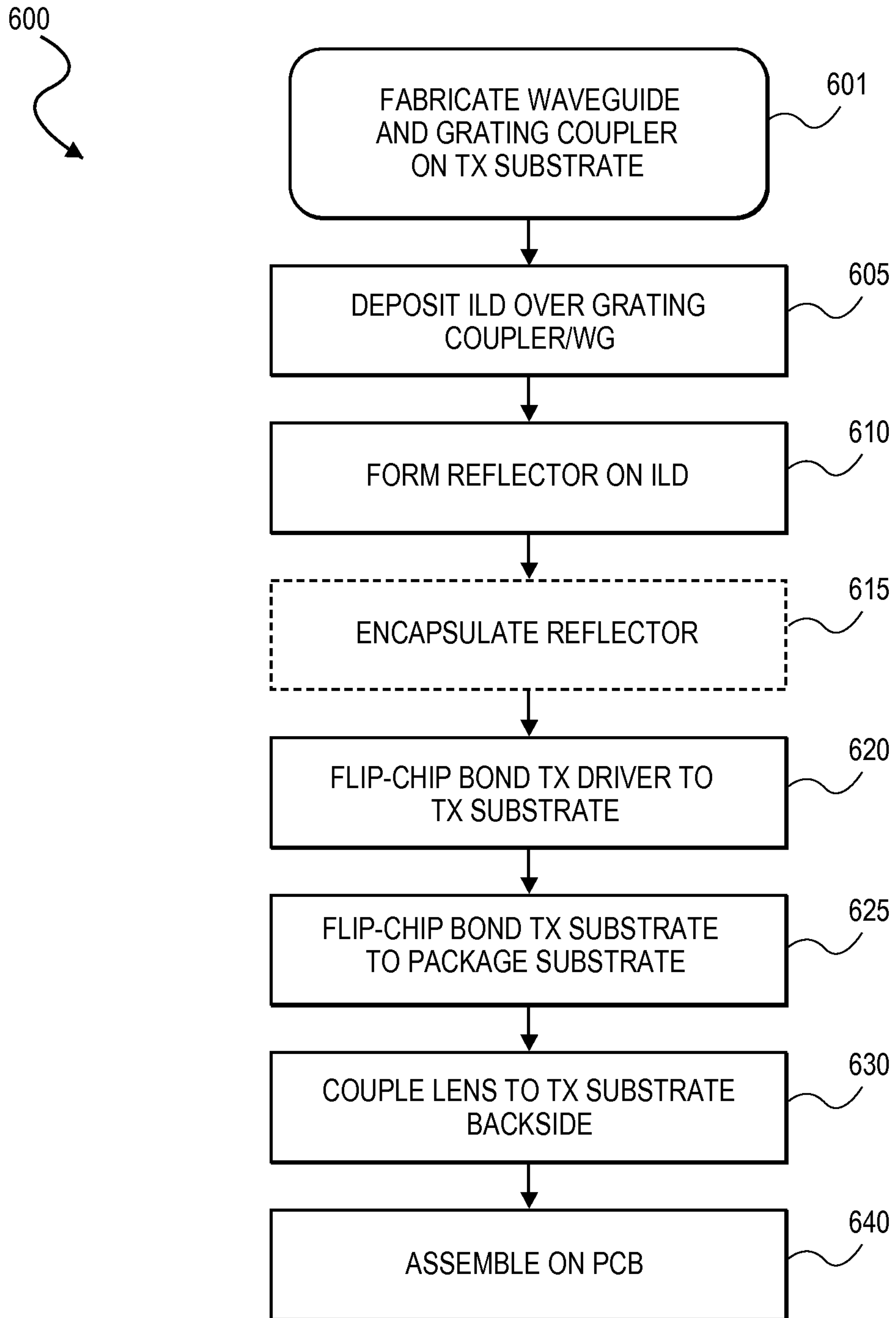

FIG. 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2011/065271

A. CLASSIFICATION OF SUBJECT MATTER

G02B 6/42(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G02B 6/42; HOIS 5/026; G02B 6/10; HOIS 3/08

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: grating coupler, filp-chip, reflector

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 2008-0253423 Al (K0PP CHRIST0PHE) 16 October 2008 See abstract; figures 1, 3A-3D; claim 1	1-3 4-20
Y	US 2011-0038588 Al (KIM DUK JUN et al.) 17 February 2011 See abstract; figure 4; claim 1	4-20
A	US 7627018 Bl (GUILFOYLE PETER et al.) 01 December 2009 See abstract; figures 2-3; claim 1	1-20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 JUNE 2012 (29.06.2012)	**29 JUNE 2012 (29.06.2012)**

Name and mailing address of the ISA/KR

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Facsimile No. 82-42-472-7140

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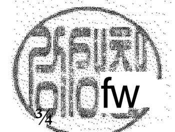

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US201 1/065271

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