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(71) Applicant

Christopher Harding Moller,

7 Rosemary Drive, Bromham, Bedford MK43 8PL

(72) Inventor

**Christopher Harding Moller** 

(74) Agent and/or Address for Service

Christopher Harding Moller,

7 Rosemary Drive, Bromham, Bedford MK43 8PL

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GB A 2162666

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EP A1 0129487 EP A1 0123806

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G4A

НДР

Selected US specifications from IPC sub-class G06F

# (54) Automatic computer peripheral switch

(57) A device is described which permits several computers to access a peripheral which is designed for connection to only one computer. Selection of the relevant computer is achieved without any special signalling requirement. As shown, computer interfaces 1 have shared access to a peripheral 5 via buffers 2, 4 and bus 3. Timer 6 monitors activity on the peripheral interface. Access of a requesting computer to the peripheral is controlled on the basis of the time since a previous computer last accessed it, and according to a daisy-chain priority scheme. A single character sent from a computer acts as an access request.

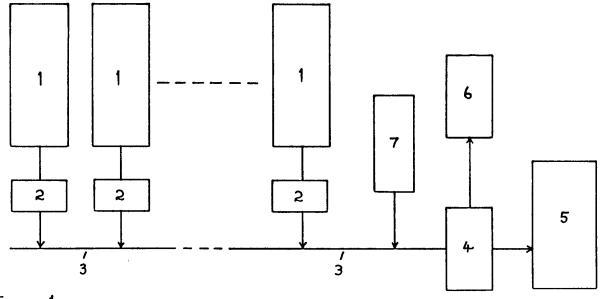
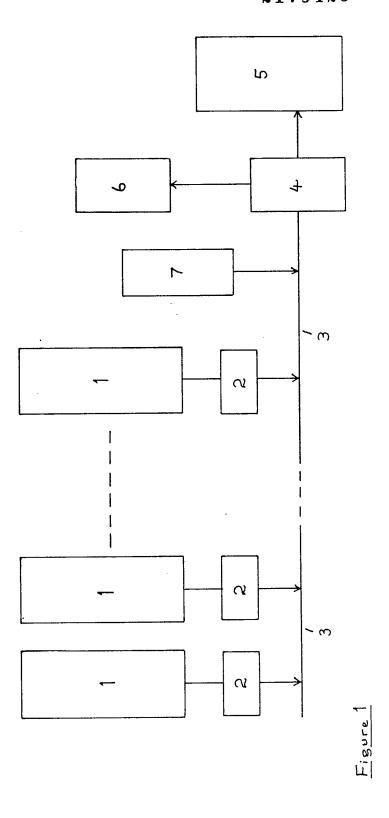


Figure 1



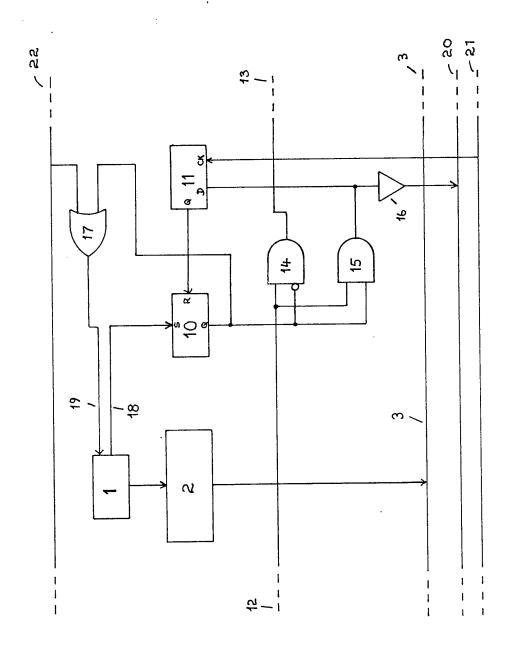
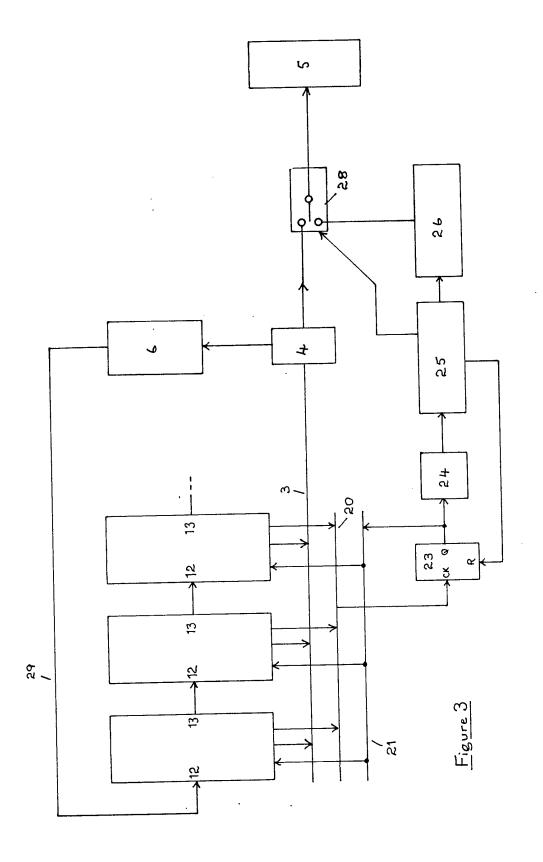


Figure 2



#### SPECIFICATION

## Automatic computer peripheral switch

5 This application relates to an automatic switch to permit several computers to access a peripheral which is designed for connection to only one computer.

Computer peripherals are relatively expen10 sive, and often used for only a small percentage of the time. A method of sharing a peripheral between computers therefore makes economic sense. Switches are available to perform this function, but they require the user to operate the switch before communicating with the peripheral.

According to the present invention, a device is provided to which several computers may be connected, and one peripheral which is designed to respond to data from the computer (eg by printing the data, or returning data as requested).

Any computer may attempt to send data to the peripheral at any time, but only one may continue to do so (one might say it 'own' the peripheral). The other computers receive an indication that the peripheral is not ready. Any character(s) they have sent are saved until such time as that computer receives owner-30 ship of the peripheral.

When the computer with ownership of the peripheral has not sent any data for a predetermined amount of time, the peripheral becomes available to the other computers, according to some arbitration scheme. This may be pre-defined in hardware or software, or may be a first-come first-served queue.

Optionally, the computer may send a special code, when its requirement for the peripheral 40 ceases. This removes the need to wait for the timer to expire. Unless this option is exercised, there is no requirement for any special action on the part of the computer.

If a change of ownership occurs, the device 45 may optionally send a pre-determined character sequence to the peripheral to indicate the change of ownership.

The relationship between the component parts of a specific embodiment of the invention is shown in Fig. 1.

Referring to the drawing, several computer interfaces 1 are connected via buffer circuits 2 to a common data bus 3, which connects via buffer circuit 4 to the peripheral 5. A timer 6 monitors activity on the peripheral interface. Circuitry 7 is included to send a control sequence to the peripheral when change of user occurs.

Fig. 2 shows the implementation of one of 60 several identical channels.

When a character is received from the computer without the computer having ownership of the peripheral, latch 10 is set by the strobe line from the computer 18, registering a re-

that no lower-numbered channel is waiting to send and the activity timer has expired, line 12 is asserted, and thus the request is transmitted to the change-of-user circuitry via gate 15, buffer 16 and line 20. Line 22 is the Busy line from the peripheral. While the channel is waiting for its request for the peripheral to be honoured, the computer is made to wait by gate 17 via control line 19. When the

75 change-of-user sequence is completed, the change-of-user circuitry asserts line 21, setting latch 11, which resets latch 10 and indicates to the computer via gate 17 and line 19 that the peripheral is no longer busy.

80 Fig. 3 shows the change-of-user circuitry and its relationship with the control lines from the individual channels.

The peripheral is offered to connection 12 of the lowest-numbered channel on expiry of timer 6 by line 29. If the lowest-numbered channel does not have an ownership request pending, it will pass it on via line 13 to line 12 of the next-lowest channel, and so on. A channel which does have an ownership request pending indicates the request to the change-of-user circuitry as described above.

The change-of-user circuitry consists of a latch 23 which is set by a request from a channel, a gated oscillator 24 and a counter 25. The counter sequences out first the character(s) of the change-of-user control sequence from data generator 26, and then buffered character from the channel that is about to gain ownership of the peripheral, via 100 buffer 27 and data selector switch 28. The last action of the counter is to reset the latch 23, and signal that ownership is granted to the appropriate channel via line 21. The computer interface is then free to send additional 105 data directly, at whatever rate the peripheral can accept it.

### **CLAIMS**

- An electronic device which allows sev-110 eral computers to communicate with a single peripheral, and which controls access by a new computer to the peripheral on the basis of the time since the previous computer last sent data, characterised in that a change of ownership of the peripheral occurs as a result of a request received from a computer, in the form of a single character sent from the requesting computer; that when several computers are waiting to transmit, the one that 120 gets access is determined by a hardware-implemented daisy-chain scheme; that the change of ownership causes a character or sequence of characters to be sent to the peripheral prior to the character that originally 125 caused the change of ownership.
  - 2. A device as in Claim 1 characterised in that the computer interface used is a byte-parallel interface.
- A device as in Claim 2, wherein the
  byte-parallel interface adderes to the well-

known Centronics (R.T.M.) interface specification.

4. A device as in Claim 1, 2 or 3, characterised in that the implementation is achieved5 without the use of programmable devices.

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