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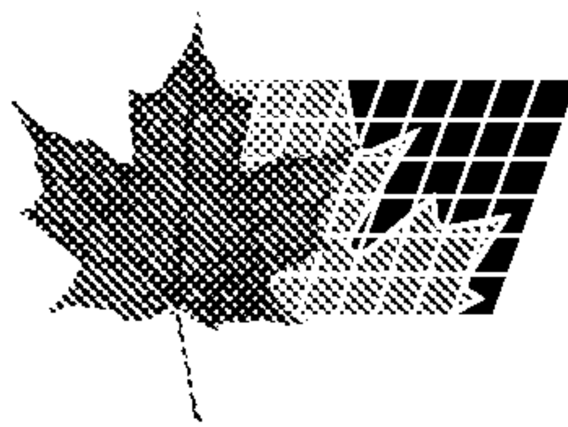

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(12) (19) (CA) **Demande-Application**

(21) (A1) **2,275,632**
(86) 1997/12/19
(87) 1998/06/25

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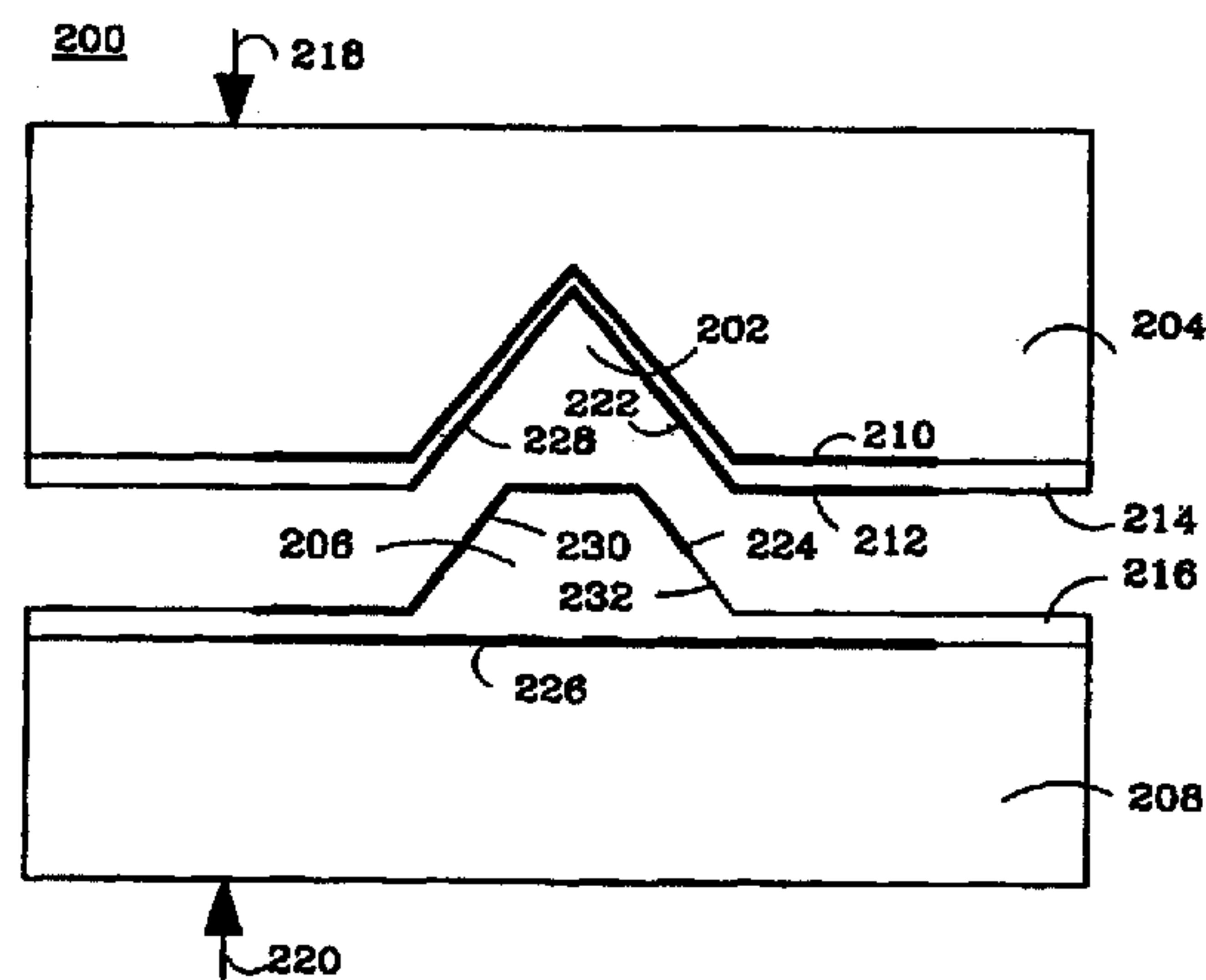
(51) Int.Cl.[6] H01L 29/41, H01L 23/42, H01L 29/06
(30) 1996/12/19 (9604677-6) SE

(54) **CONNECTEURS ELECTRIQUES HAUTE DENSITE**

(54) **HIGH DENSITY ELECTRICAL CONNECTORS**



(57) L'invention concerne des connecteurs électriques haute densité auto-alignés souples, réglés en impédance et mis en application dans des systèmes micro-électronique. Cette invention permet de résoudre le problème posé par un branchement électrique et un alignement simultanés. Un connecteur (200) possédant une première partie (204) est constitué par deux structures de couches métalliques, un premier trajet de signal (212) et un premier trajet de masse (210) recouvre la rainure en V (202). Ce connecteur possède également une deuxième partie (208) constituée par deux couches métalliques correspondantes, un deuxième trajet de signal (224) recouvrant la bosse élastique (206), ainsi qu'un deuxième plan de masse de signal (226) s'introduisant dans la rainure en V (202). Le premier et le deuxième trajets de signal (212) (224) viennent en contact l'un avec l'autre quand on met en contact la première et la deuxième parties (204) (208). Ce contact est auto-aligné quand on l'établit. Le contact électrique reste permanent même s'il est déplacé sous l'effet de la dilatation thermique.

(57) The present invention relates to self-aligned, flexible high density and impedance adjusted electrical connectors used in microelectronic systems. This invention solves the problem of having electrical connection and alignment at the same time. One connector (200) having a first part (204) consists of two metal layer structures, a first signal path (212) and a first ground path (210), covering the V-groove (202). The connector also has a second part (208) consisting of corresponding metal layers, a second signal path (224) covering the elastic bump (206) and a second signal ground plane (226), which fits into the V-groove (202). The first and the second signal path (212, 224) are in contact with each other when the first and the second part (204, 208) are brought together. The contact is self-aligned when put together. The electrical contact will remain even if displaced due to the thermal expansion.

CA 02275632 1999-06-18

PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification [6] :
H01L 29/41, 29/06, 23/42 // 21/60, H05K 3/40 A1

(11) International Publication Number: **WO 98/27596**

(43) International Publication Date: 25 June 1998 (25.06.98)

(21) International Application Number: PCT/SE97/02178

(22) International Filing Date: 19 December 1997 (19.12.97)

(30) Priority Data:
9604677-6 19 December 1996 (19.12.96) SE

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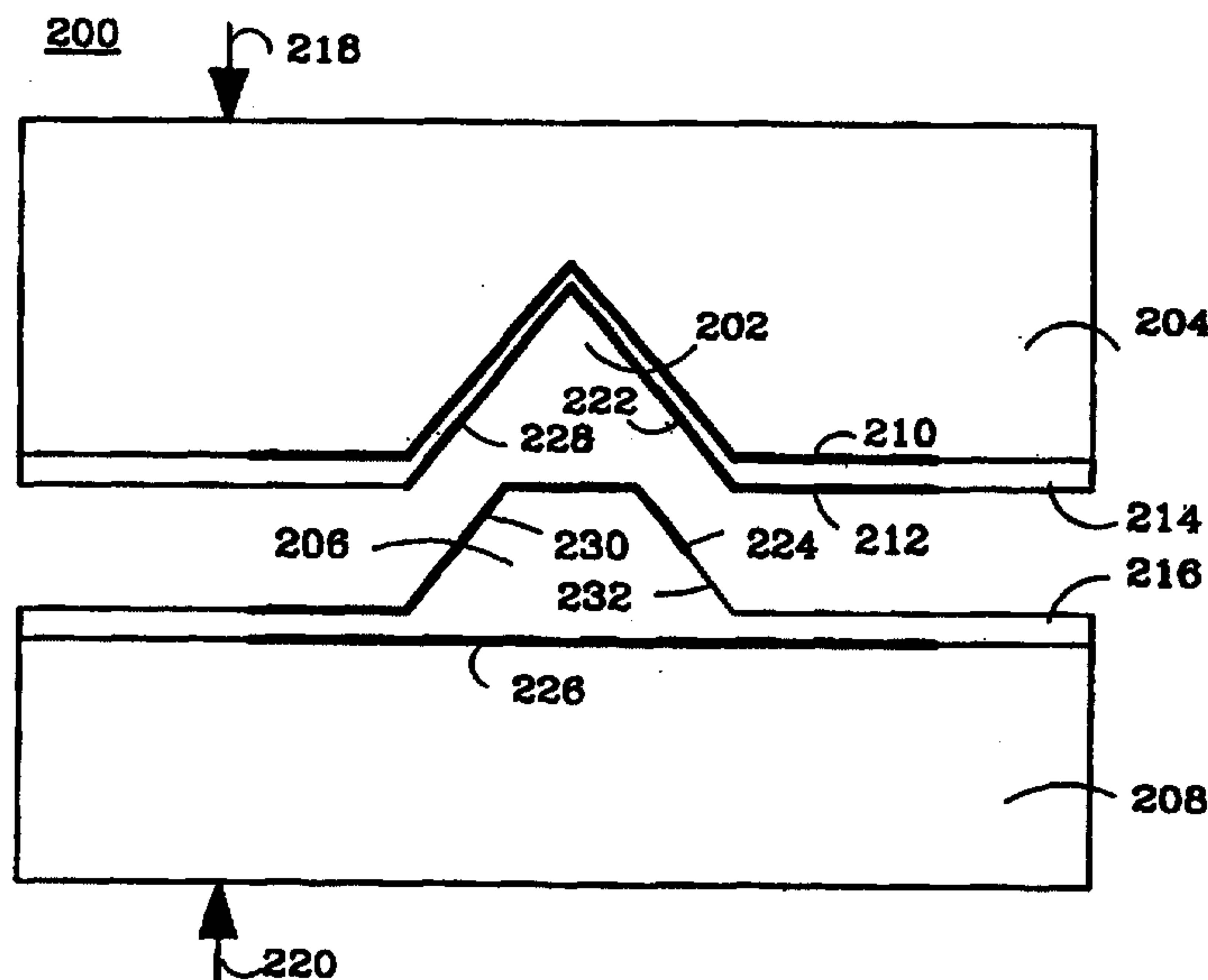
(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: HIGH DENSITY ELECTRICAL CONNECTORS



(57) Abstract

The present invention relates to self-aligned, flexible high density and impedance adjusted electrical connectors used in microelectronic systems. This invention solves the problem of having electrical connection and alignment at the same time. One connector (200) having a first part (204) consists of two metal layer structures, a first signal path (212) and a first ground path (210), covering the V-groove (202). The connector also has a second part (208) consisting of corresponding metal layers, a second signal path (224) covering the elastic bump (206) and a second signal ground plane (226), which fits into the V-groove (202). The first and the second signal path (212, 224) are in contact with each other when the first and the second part (204, 208) are brought together. The contact is self-aligned when put together. The electrical contact will remain even if displaced due to the thermal expansion.

HIGH DENSITY ELECTRICAL CONNECTORS

TECHNICAL FIELD OF THE INVENTION

The present invention relates to interconnection of electric devices, more particular to self-aligned, flexible high density and impedance adjusted electrical connectors.

5 **DESCRIPTION OF RELATED ART**

The technical evolution in the field of integrated circuits, IC:s, has resulted in a demand for faster and more compact systems. In many applications a compact structure combined with a low weight is in itself a requirement. The technical evolution 10 also tends towards more complex systems involving a greater and greater number of components which need to communicate with each other. In order for the new systems to meet the requirement of quick access between different components, the length of the paths between different components of the system must be kept 15 within certain limits.

When the complexity of a system grows, the length of the paths between components also grows. In order not to exceed the maximum usable distance between such components, these components have been built smaller and smaller and they have 20 also been packed more and more densely. Thus, multi-chip modules have been developed, which makes a very dense packaging of unencapsulated IC:s possible.

In fact, the distance between different active components do not become much larger than if the whole system had been integrated 25 on the same plane monolith. The maximal distance, determined by the performance requirements, between components which need to communicate with each other in a complex system becomes unnecessarily large if only one plane of connected chips/components can be used, since only components in the same 30 plane then can be reached within the maximal distance.

Three dimensional constructions can be used to overcome this problem. This means that the communication lines extending from one component can not only reach components in the same plane but also components in planes located above and underneath the component can be directly accessed. This can be obtained in some different manners: firstly, systems having modules connected to a back plane; secondly, systems consisting of chips glued together; thirdly, systems having vertical connections at the side of a tower built of chips are in one sense three dimensional. These three dimensional constructions do not solve the problem with short paths between all components. This can not be achieved when components are close in space and are connected by long lines. This becomes obvious when two components are connected according to the first of the methods described above, e.g. connection of two centrally located components on two different neighbouring multi-chip modules, which are in their turn connected through a lateral path, a short vertical path at the side of the chips, and then a final lateral path on the other chip. If more than one pile of chips is used, the second described method does not either make short interconnection lines between adjacent chips possible. This is easily realised if one considers the case of two chips located next to each other, but on the top of each pile, which are to communicate with each other.

As the complexity of electronic circuits increases there is a growing demand on the density of in/out-connections having properties not to deteriorate the performance, i.e. impedance adjustment or negligible inductance/capacitance. As the density increases the demand on alignment is also increased and the greater this demand the more important becomes the use of self-

aligning procedures due to the accelerating costs of active alignment at high precision.

When connecting parts of a complex system, the risk of having to replace one or more of these parts to obtain a functioning system increases with the complexity of the system. The difficulty accelerates to fully test the constituent parts at relevant frequencies and operating conditions.

There are concepts that use high density micro bumps, but these are not really impedance controlled, which also implies quasi impedance control.

The European patent application 0 295 914 A3, Maracos Karnezos, describes elastic bumps which are metallized. The bumps are used to connect two surfaces electrically through clamp connection. Through the elasticity almost all thermal induced mechanical stress can be eliminated. Conducting surfaces can be separated without disordering.

SUMMARY

This invention describes a technology to achieve elastic electrical connectors which are impedance controlled, have high density of interconnects and are high precision self-aligned during mounting and under performance. The functions of alignment and electrical interconnect are in the same structure. The alignment is based on protruding V-shaped bumps in one part and V-grooves in the other part. The groove may be of 5 corner pentahedron or pyramidical form and the bump may be of truncated 5 corner pentahedron or truncated pyramidical form. The bumps and grooves have corresponding connector paths.

The basic idea with this invention is that it is using the alignment of the structure itself. This means that the site of multiple contact points may be obtained by high impedance controlled contact densities, while the aligning structure is relatively much larger. This results in high precision and at the same time elastic connections. This invention handles minor imperfections in the metal or other layers and possible thermal mismatch when in use. Simultaneous multiple, more than three, connections require individual contact point flexibility or deformability or else, the demand on precision, i.e. the requirement that all the contact points be in the same plane, will be enormous and hardly realisable.

This invention has a multi-path impedance controlled very high density bus, made by patterning metal lines, e.g. paths, on a precision moulded elastic bump which mates to similarly patterned lines on the walls of a precision etched groove.

This invention is able to obtain impedance adjusted high density multi-path connectors at no physical fan out using low cost lithography and Si micro structure technology. It is also a self-aligning concept requiring no separate body and made essentially simultaneously with the patterning of the metal interconnects on the substrate utilising a pre-made change of the structure of the substrates.

This invention could be used in various microelectronic systems, for instance miniature high density modules, between modules and motherboards, between IC:s and modules or boards, between different levels in 3D structures, or generally as a very high density dismountable connection between substrates.

In many cases there is a requirement to be able to disassemble electronic systems and to put them back again without using soldering or equivalent. This implies using connectors. There are numerous connectors available, but none that has the density corresponding to this one, which is both impedance controlled, for frequencies up to several GHz, as well as very high density, i.e. without requiring physical fan out. The elasticity is an important feature securing sufficient contact pressure for all paths even if there are slight physical defects or variation in size due to different thermal or other expansions. Regarding alignment, many connectors utilise the contact points for alignment. For very small sizes of the individual contact points, this would require a high degree of pre-alignment or might lead to destruction when forcing alignment. Instead, elastic alignment structures and corresponding mating grooves are patterned with similar metal lines which are part of the metal lines extending from the circuit. This implies that a robust alignment yet at very high precision is obtained, and which does not occupy extra space. By making ground paths or planes and contact paths in the grooves and also make similar ground paths on the substrate and contact paths on the bumps it will result in an connector structure. With the exception of the formation of the bump and the groove, which requires simple extra steps, the contact points and the connection of the electrical lines are integral to the general interconnect patterning processes.

One advantage of the present invention is that it offers a solution for systems where very short electrical pathways are required.

Another advantage of the present invention is that it offers a compact packaging system.

A further advantage of the present invention is that the hole system is easy to repair and, because of that, individual parts
5 are easy to replace and it could be done without any real costs or potential damages associated with the removal of faulty parts. An attachment does not involve soldering or gluing etc.

The invention is now being described further with the help of the detailed description of the preferred embodiments and the
10 attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a cross-section of a three dimensional multi-chip module.

Figure 2 shows a schematic cross-section of self-aligned and
15 impedance adjusted connector.

Figure 3 shows an alternative schematic cross-section of self-aligned and impedance adjusted connector with double density conductors.

4 shows an alternative schematic cross-section of self-aligned
20 and impedance adjusted connector with ground paths following the signal paths through the connector.

Figure 5 shows a schematic top view of the Fig. 3.

Figures 6a-b show a cross section of an alternative connector.

Figure 7 shows a cross-section of an alternative double density
25 connector with conductors.

DETAILED DESCRIPTION OF EMBODIMENTS

This invention can be used in various micro-electronic systems, which are used for elastic electrical contacts and built-in chip alignment. It could be used in multi-chip modules, especially

where it is hard to determine the quality of chips before they are mounted. The invention would be used where there presently are several problems, e.g. with flip-chip or on board due to high mis-match of thermal expansion coefficients between board 5 and chip. Repair can often be risky and expensive and, in some types of MCM, essentially impossible.

First figure shows an example where this invention can be used, but it is not restricted to this area. This invention can of course be used in any kind of micro or even sub-micro systems. 10 Figure 1 shows a cross section for a three dimensional, 3D, multi-chip module 100. The 3D module is formed by two dimensional, 2D, multi-chip modules consisting of Si substrates 106-114 having integrated circuit chips 122-136 mounted thereon. The Si substrates 106-114 are provided with a grounded plane 15 whereby a good screening is obtained between the different planes of the module as well as for the entire 3D multi-chip module 100. On the substrate 106-114, in particular the ones not located at the top 106 or the bottom 114 of the stack of two dimensional, 2D, multi-chip modules, there are also mounted 20 passive chips, via chips or vias 116-121 constituting interconnections between adjacent levels of the 3D multi-chip module 100.

In order to obtain impedance matched connectors, see Fig. 2, V-groove etched contact grooves 202 are used. On the top of the 25 via chips 116-121 elastic bump structures 206 are applied and on the backsides of the substrates V-shaped contact grooves 202 are made, which are provided for obtaining a connection which is easy to assemble/disassemble and for obtaining a good alignment, see simultaneously filed patent application "Packaging structure 30 for integrated circuits".

The IC chips 122-136 and the via chips 116-121 are, in the preferred embodiment, flip-chip mounted on the substrates 106-114. This arrangement makes it possible to provide a good thermal contact between the backsides of the flip-chip mounted
5 IC chips 122-136 and the backside of the adjacent substrates 106-114.

Each level of the IC chip 122-136 and each individual via chip 116-121 of the 3D multi-chip module 100 is only kept together by a compressing force 142 applied on top plane 138 of the top
10 cooler 102 and bottom plane 140 of the bottom cooler 104 of the structure.

In order to accomplish this piled structure, elastic bumps are provided which connect via chips 116-121 to adjacent planes of the substrates 106-114, and contact is obtained by pressing the
15 module together at the top plane 138 and the bottom plane 140 of the cooler 102, 104. The compressing force 142 is provided by means of clamps applied to the outermost part of the module 100.

Patterned metal layers are used to establish multiple electrical pressure type, non permanent, connections which are impedance
20 adjusted for high speed data transmission.

Figure 2 shows a cross-section of one such connector structure 200. A first part 204 consists of two metal layer structures, a first signal path 212 and a first ground path or plane 210 with a dielectric between them, covering the anisotropically etched
25 V-groove 202. A second part 208 consists of corresponding metal layers, a second ground plane 226, and a second signal path 224 covering the elastic bump 206, which fits into the V-groove 202. The first and the second signal path 212 and 224 are in contact with each other when the first and the second part 204 and 208

are brought together. The contact is self aligned when put together, see a simultaneously filed patent application "Bumps in grooves for elastic positioning". Because of the elastic bump 206, electrical contact will remain even if displacement due to,
5 for example, the thermal expansion occurs. The first and the second signal paths 212, 224, configured as in Fig. 2 implies double safety since both side walls of the elastic bump 206 and the V-groove 202, respectively, are covered with the same paths. In other words, if large displacement occurs and only one side
10 wall of the bump 206 is touching the V-groove 202, then electrical contact will still remain. The first and the second ground paths or planes 210, 226 consist of any suitable metal. The first signal path metal 212 needs to be a metal free from any insulating surface oxide layer, i.e. any noble metal. The
15 second signal path metal 224 needs to be a ductile metal free from any insulating surface oxide layer, e.g. gold. The paths and ground metal layers are separated by dielectric layers 214 and 216. The first dielectric layer 214 consist of any dielectric layer conformally covering the V-groove walls, e.g.
20 Parylene. The second dielectric layer 224 consist of any dielectric layer, or of the same elastic material as in the bump 206.

This invention is based on high precision, elastic alignment of two parts of any function, where elastic bumps are
25 simultaneously used for high precision alignment and flexible, elastic, electrical connectors. Patterned metal layers are used to establish multiple electrical pressure type, non permanent connections. These connections are impedance adjusted for high speed data transmission.

The most precise alignment will be obtained when the alignment groove 202 is made using anisotropic etching of e.g. Si (100) wafer. Likewise, the most perfect elastic bump 206 will be formed by using: an anisotropically etched (100) Si wafer and high precision lithography, a conformally covering release agent layer, and a curable silicone compound. In simultaneously filed patent applications "Method for making elastic bumps" and "Bumps in grooves for elastic positioning" are described a more detailed way how the bumps and the grooves are made and alignment thereof. When the V-groove 202 and the truncated bump 206 have been made, parts will be placed by some pre-alignment such that the top of the bump 206 is within the periphery of the groove 202. By cautiously applying pressure 218, 220, possibly gravity, inclined walls 230, 232 of the bump will slide on inclined walls 222, 228 to get very precise alignment in the directions parallel to a base surface of the bump 206 or the groove 202 and then aligning the bump 206 in the groove 202. The paths 212, 224 which were placed at high precision using lithography relative to the bump 206 in the groove 202 are automatically aligned and, utilising the elasticity of the bump 206, the paths 212, 224, will contact its counterpart regardless of minute thickness, metal roughness due to micro crystallisation etc., differences. Also, due to the elasticity, small differences in expansion between the parts 204, 208 could occur without losing contact or exposing the parts 204, 208 for severe strain.

How to make the connector 200 is hereby described. A polished (100) silicon wafer, this wafer is from here on referred to as the mould wafer, is covered using SiN after which resist is deposited and patterned using a mask which is well aligned relative to the crystal axis directions of the mould wafer.

Openings as defined by the mask are then etched in the SiN layer, then the mould wafer is exposed to an anisotrophic etchant, which produces grooves which side walls are limited by the silicon {111} planes. The etch may be continued until complete, elongated, structure has been etched or preferably may be stopped prior to this, such that truncated, elongated, structure is formed.

A similar, but mirrored, mask which with very high precision, replicates the first mask is then used to, by equivalent procedure, obtain similar but mirrored grooves in a wafer which contains the parts which are to be aligned. These grooves must be as deep or deeper than those in the first wafer. The mould wafer may also contain some further alignment structures to enable it to be self aligned to the substrate onto which the elastic bumps are moulded. The mould wafer is covered with some release agent, which is deposited very thinly and conformally in order to preserve the precise geometry. For the part to be provided with bumps the most rational procedure is to first create the metal and dielectric layers as usual. Either the plate with the unseparated substrates or the mould wafer is then covered with a curable elastic compound to a controlled thickness using spinning, scraping or spraying. Then the mould wafer and the unseparated substrates are pressed using the alignment features for precision alignment of the bumps versus the substrate structures, allowing the compound to wet the opposing surfaces. The package is then possibly placed in a vacuum to remove air bubbles, and then at elevated temperature to cure the compound. The mould wafer is then separated from the substrate. Using stiff mould wafers and substrates this would be done in a vacuum, due to the hermetic fit of the compound to the

mould. For special applications the substrate could be made of flexible material, which would facilitate separation.

For the bump structure part the most rational procedure is to first create the metal layer 226 and the dielectric layer 214 as usual, then to make the bump, then a separate metal path 224 is patterned over the bump and makes contact to the previous metal layers through vias. It would, in principle, be possible to first make the ground path or plane, then continue with the depositions of metals and dielectric on the bump. This would, however, exclude the possibility to pass lines or ground planes beneath the bump and it is not always the case that the various dielectric and metal paths would be flexible enough to survive on the flexing bump.

By using photolithographic masking aligned to already existing structures on e.g. lasers or IC:s or substrates before they have been separated, grooves are made either using anisotropic etching or other techniques. The grooved part 204 is then processed normally, i.e. depositing the metal layer 210 and dielectric layer 214, with the exception that the dielectric layers 214 and patterning the metal path 212 have to be deposited conformally, in order to preserve the alignment properties of the groove 202. Also, the resist has to be deposited sufficiently conformally to allow resolution of the exposed pattern in the resist and the depth of focus of the exposing equipment must be sufficient.

After separation of the grooves etc. they may now be placed onto the bumped part, self-aligning grooves with the bumps. Depending on the shape and size of the bumps and the grooves the degree of pre-alignment varies.

It would, in principle, be possible to first make the general deposition and patterning of the dielectric layer and metal path, then to etch away metal and dielectric from the area of the groove, pattern and etch the groove, further to re-deposit 5 and pattern the metal path and the dielectric and resist, which would only be used locally.

As the parts are mating together using external pressure no permanent attachment is made, allowing the part to be easily separated from its aligning structure for replacement or repair.

10 In the thin parts of the moulded material outside of the bump, vias are formed to the metal paths, which are to be contacted very close to the bump.

In Figure 3 is a first alternative embodiment described. This figure shows a possibility of having a double density connector. 15 The manufacturing process steps and materials involved are identical with the case described in Fig. 2 However, in this case shown in Fig. 3 there are two different paths on each side of the bump as well as the grove. The paths pattern is also illustrated in the schematic top view of a bus contact in Fig. 20 5.

A second alternative embodiment of the present invention is described in Fig. 4. The manufacturing process steps and materials involved are identical with the case described in Fig. 2 except that the ground plane is connected up to the level of 25 the signal lines using vias. Fig. 4 shows schematically a cross-section of self aligned and impedance adjusted connector with ground paths following the signal paths through the connector. To achieve ultimate electrical performance both the signal line

and the ground plane are connected at essentially the same position using the same elastic bump.

Figure 5 shows schematically a top view of self aligned and impedance adjusted connector with double density conductors of
5 the alternative embodiment, Fig 3.

Figures 6a-b show a cross section of an alternative connector 600. The connector 600 having a first part 602 and a second part 604. The first part having signal paths 606 along the edge of the part 602, see Fig. 6b, connected to contact pads 612 at
10 bottom of the first part. The second part 604 having a guiding frame 610 on a substrate 614 and signal paths 608 along the guiding frame 610. The two parts have such a structure that at least one edge of each of the parts have inclined walls 616, 618. If chips are provided with inclined walls the normal pads
15 could be exchanged with paths extending over the inclined walls and mating the guiding frame with patterned metal paths as described earlier.

The previously described preferred embodiment could be modified, but at some loss of precision. The bumps could have a different
20 shape than the grooves. For this, one would not use anisotrophic etching, but rather some other etching, or machining. For this, the grooves and the bumps do not have to have the same shape as long as the bump would fit in the groove, in a self centring fashion, and contacts were being made. The compound could be
25 other than Silicone, e.g. polyurethane or some other elastic or semi-elastic compound.

By replicating using several steps, a flexible mould could be made, facilitating the detachment of the mould from the substrate but only at a loss of accuracy.

Assuming that the metal patterning resolution is better than the minimum size of the bumps the preferred embodiment gives the highest contact density in one dimension, i.e. the closest possible line spacing. If the minimum size of the bumps is equivalent to the metal patterning resolution it would be possible to obtain higher contact densities per area. In this case self centring multiple super micro bumps densely packed on a surface, where the metal is patterned not on the bump but outside the bump would be used.

In this case the connections would also appear to be impedance controlled due to the very small size of the bumps. This, however, would be much harder to pre-align as the peak of the bump must be within the perimeter of the now very small groove, unless there are also some gross alignment features in the structure.

If elastic material could be "perfectly" conformally deposited on the walls of the groove a stiff bump could be used instead. One way to accomplish this would probably be to use a mould, which would fill part, but not all of the groove so as to leave a thin distance to the groove walls where the elastic compound would cure.

There are several possible applications for the present type of connection. Bus contacts between MCM:s in the same plane, or also vertical signal transmission between stacked MCM:s are achievable, in combination with through-hole vias. In combination with different fan out schemes as required, these can be used as general fine pitch high frequency connectors. They would occupy much less space per connection than conventional electrical ones, while maintaining correct

characteristic impedance. This is due to the fine pitch and high alignment, and the fact that the ground plane is brought into contact point.

Except for standard process technology for fabrication of 5 electronic devices, this connector device requires processes such as a V-groove etching, casting of bumps, deposition of conformal insulator coating, and lithography over large steps. All these can be achieved by existing or modified semiconductor/thin film processes.

10 In order to get maximum precision, there must be means to cover the mould with releasing agents as very conformal and thin layers. Methods for this were described above. For this maximum precision case single crystals with surfaces well aligned to the crystal directions that can be used for anisotrophic etching are 15 available as commercial Si-wafers.

The dielectric metal and resist layers are required to be deposited relatively conformally, in comparison to the layer thickness and topography of the groove and the bump. For the metal layer deposition, this is normally the case using standard 20 thin film deposition techniques. For the dielectric, spin-coating can most likely not be used, limiting the choice of materials. However, there is still a number of materials and processes to choose from, e.g. the Parylene method. The choice of resist becomes more narrow as the vast majority of resists 25 are made to be deposited by spin-coating, which is not deemed possible in this case. There are still two known alternatives. One is using novel resist materials, which are deposited by evaporation in vacuum. For this method there is no real commercial process available, but there exist commercially 30 available materials, which have resist properties and can be

deposited this way. The other alternative is a type of resist, which is electroplated. It is commercially available and primarily used to protect the metal in through-plated holes on printed circuit boards. These electroplated resists require that there be a metal layer which can be biased for growth to occur, which will be the case as the only layer that needs to be patterned on the bumps and in the grooves are the metal layers. The dielectric also needs to be patterned to get vias, however this will not be on the bumps or in the grooves but rather outside of these where more conventional resists can be used provided they cover the hole or the groove to allow patterning, even if they are too unevenly thick. It is also possible to deposit and pattern a metal hard mask for patterning of the dielectric.

Using micro machining technologies, very high density connectors have been shown to create micro parts looking much the same as conventional connectors, but being much smaller in size. These are edge type connectors and can, in principle, be made so small that they require no physical fan out of the line pattern. However, they are not made as an integral part of the metallization. Instead, they are separate parts that require soldering or equivalent to be used. Little is known about their robustness and wear resistance.

Elastic bumps have been shown to be used for single path purposes. Here each path has one separate bump mating a surface on the opposing substrate. In principle these could be made as small as to not require physical fan out. In this case they could also be regarded as impedance controlled. However, these schemes lack any inherent means of alignment.

Solutions requiring separate micro parts that have to be individually precision handled will never be very cheap compared to thin film like processes where many items pre-placed are produced with lithographic methods.

5 Figure 7 shows a cross section of an alternative connector bump 700. The connector bump consist of a two metal layer structure, a dielectric medium 704 and a elastic structure 216. The metal layer structure can be a ground path or plane 702 and a signal path 706. The ground plane 702 is made on the bump 206 where the 10 bump is including in the elastic structure 216. The ground plane also has a connection through the dielectric medium 704 up over and covering partly the dielectric medium 704. The other metal layer structure, the signal path 706, is made on the dielectric medium 704.

15 The invention described above may be embodied in yet another specific forms without departing from the spirit or essential characteristics thereof. Thus, the present embodiments are to be considered in all .respects as illustrative and not restrictive, the scope of the invention being indicated by the appended 20 claims rather than by the foregoing descriptions, and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced therein.

CLAIMS

1. A connector comprising at least a first part and a second part, where the first and second part each has at least one inclined wall, wherein the inclined wall of the first part and the inclined wall of the second part have the same inclination, where the first part has at least one conducting path and the second part has at least one conducting path, wherein the conducting paths are in contact with each other when the first and second part are mated together, where the first part having V-grooves and the second part having bumps, wherein the V-groove has at least one conducting path, the bump structure has at least one conducting path and the bump fits into the V-groove, wherein the conducting paths are in contact with each other when the first and second part are mated together, **characterized** in that the first part (204) has a two metal layer structure, at least one first conducting path (212) and at least one first ground plane (210), wherein the metal layers are covering the V-groove (202) and/or in that the second part (208) has a two metal layer structure, at least one second signal path (224) and at least one second ground plane(226), wherein the signal path is partially covering the bump (206).

2. A connector according to claim 1, **characterized** in that the second part (208) has a two metal layer structure consisting of at least one conducting path (706), at least one ground plane (702) and a dielectric medium (704), wherein the ground plane and the conducting path are made on top of the bump (206) and the dielectric medium separates the conducting path from the ground plane.

3. A connector according to claim 1, **characterized** in that the conducting paths consist of metal layers, which are of double density, the first part (204) has at least one first signal path (306), at least one third signal path (310) and at least one first ground plane (302), wherein the metal layers are covering

the V-groove (202), in that the second part (208) has at least one second signal path (308), at least one fourth signal path (312) and at least one second ground plane (304), wherein the signal paths are partially covering the bump (206) and in that
5 the first and third signal paths (306, 304) and the second and fourth signal paths (310, 312) are in contact with each other when the first and second part are mating.

4. A connector according to claim 1, **characterized** in that the conducting paths consist of metal layers, which are of double
10 density, wherein the first part (204) having at least one first signal path (402) and at least one first ground path (406), wherein the first signal path is partially covering the V-groove (202), in that the second part (208) has at least one second signal path (408) and at least one second ground path (408),
15 wherein the metal layer is covering the bump (206) and thereby the second ground path is covering the V-groove and in that the first and second signal paths and the first and the second ground paths are in contact with each other when the first and second parts are mating.

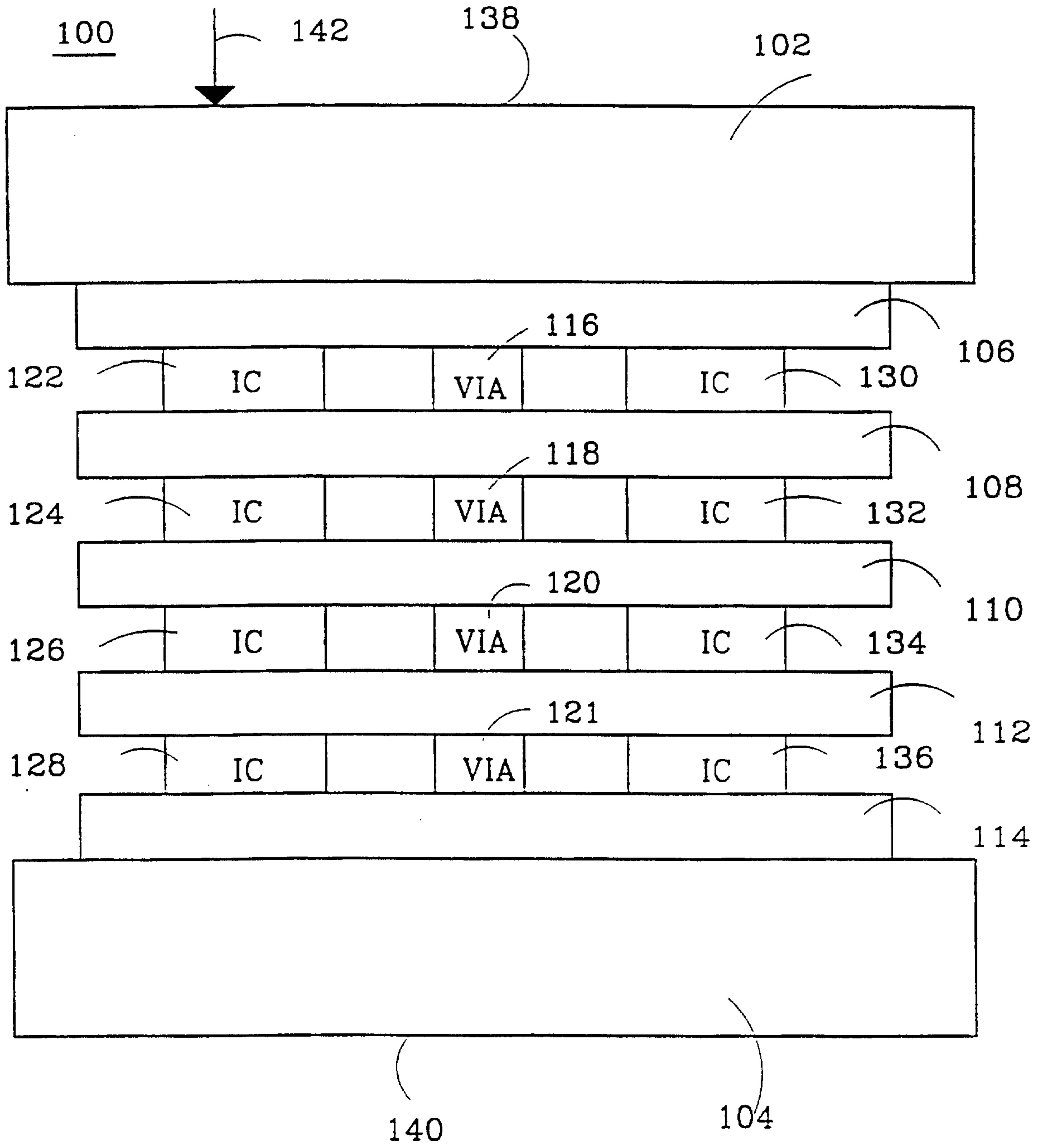


Fig. 1

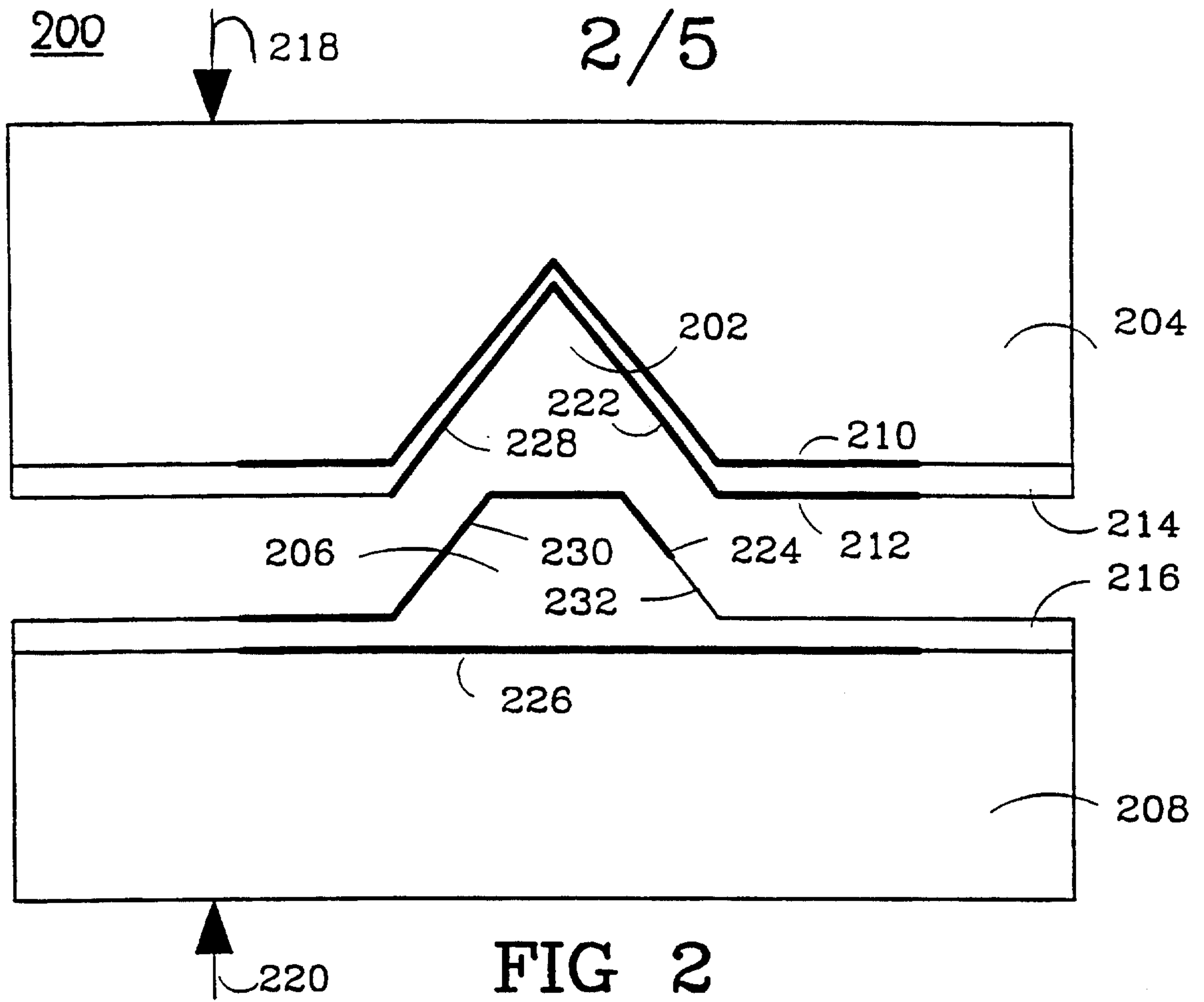


FIG 2

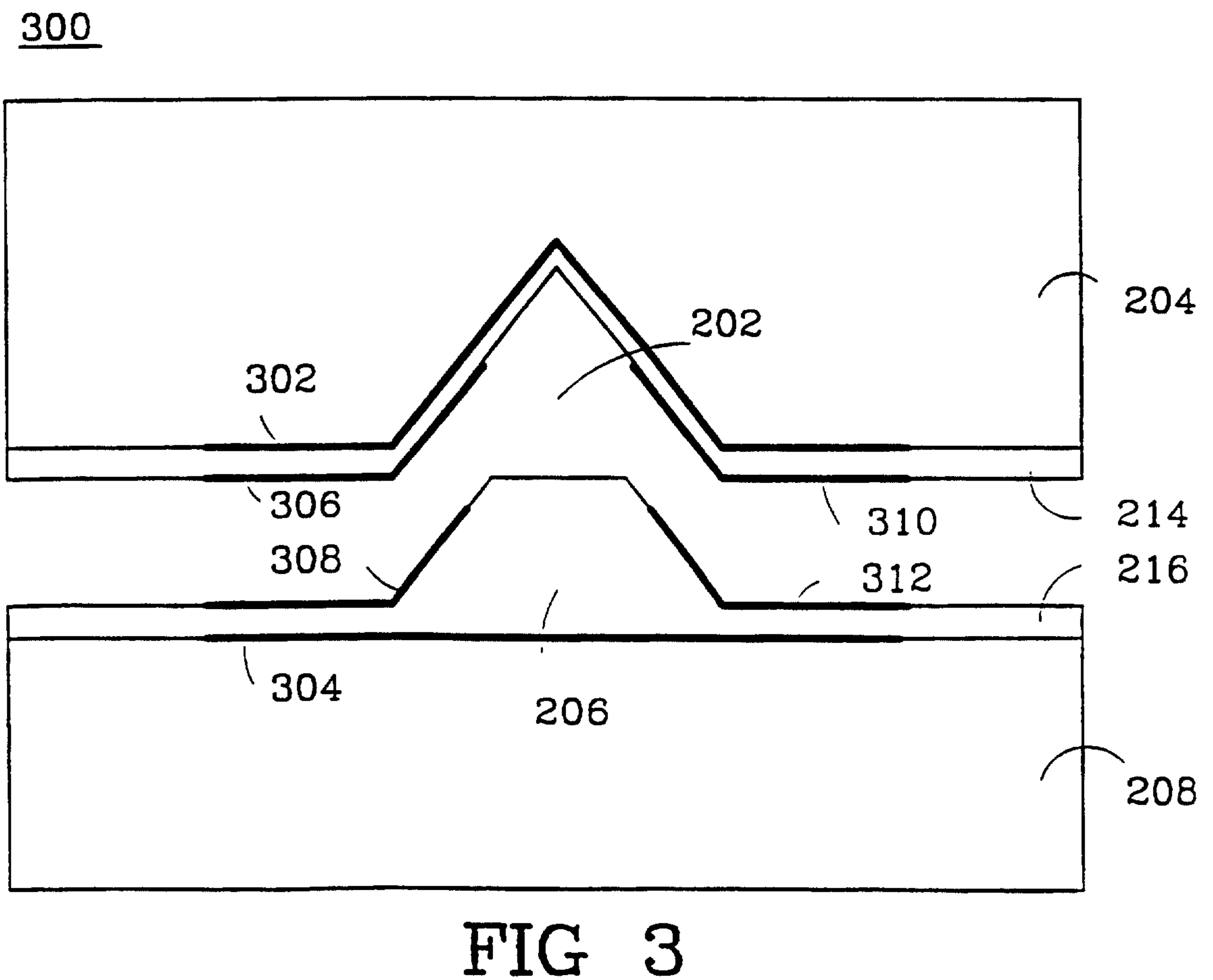


FIG 3

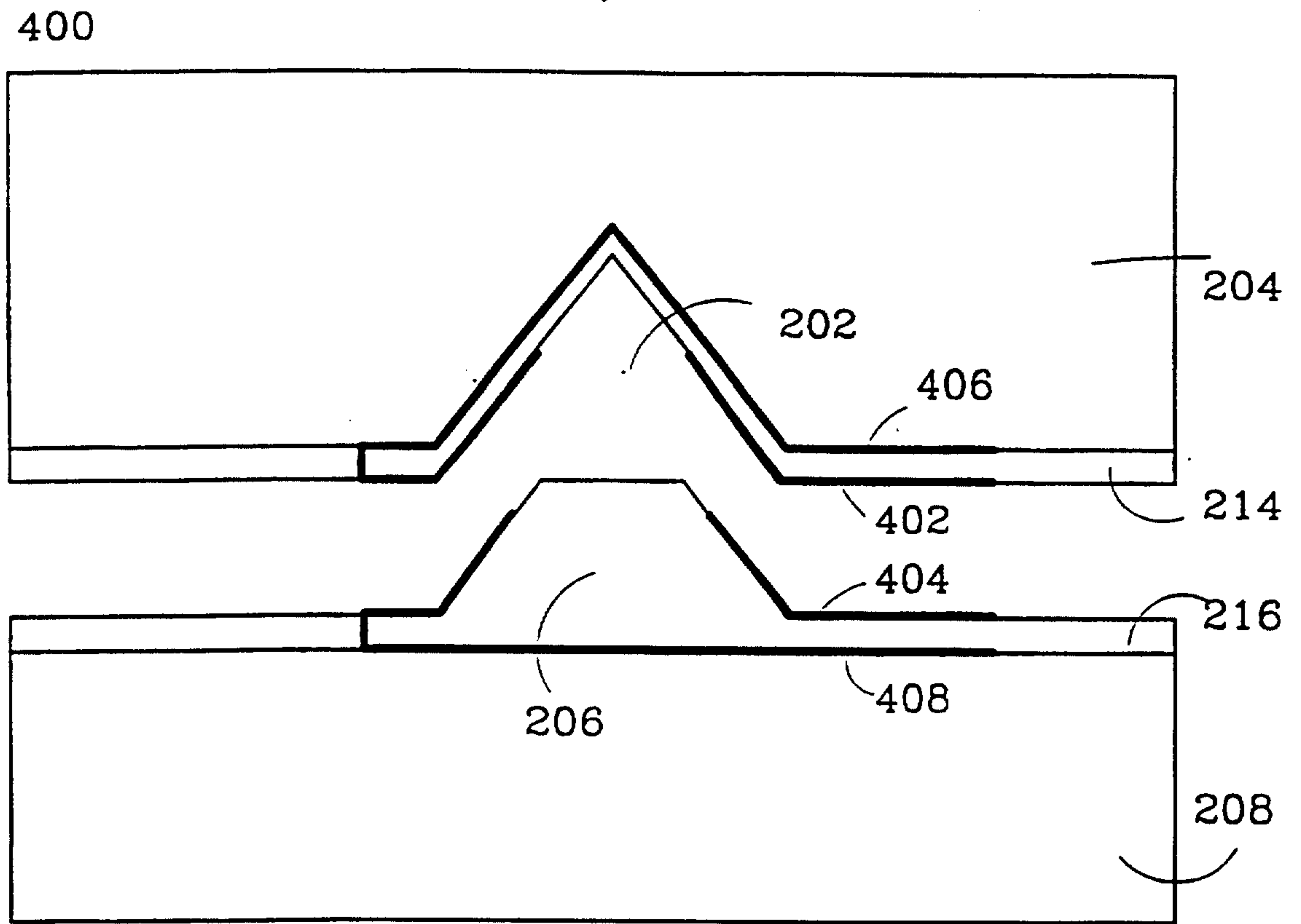


FIG 4

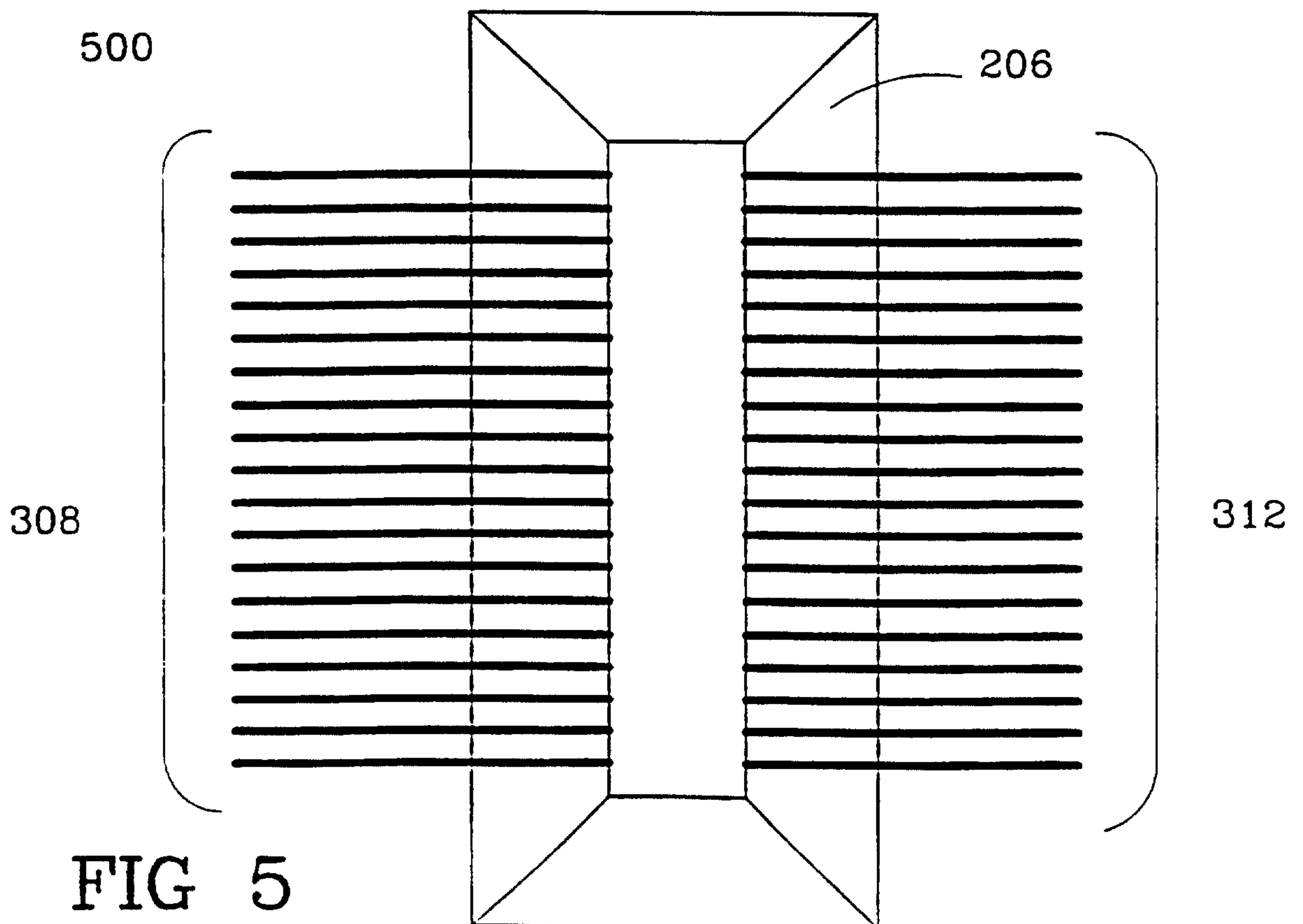


FIG 5

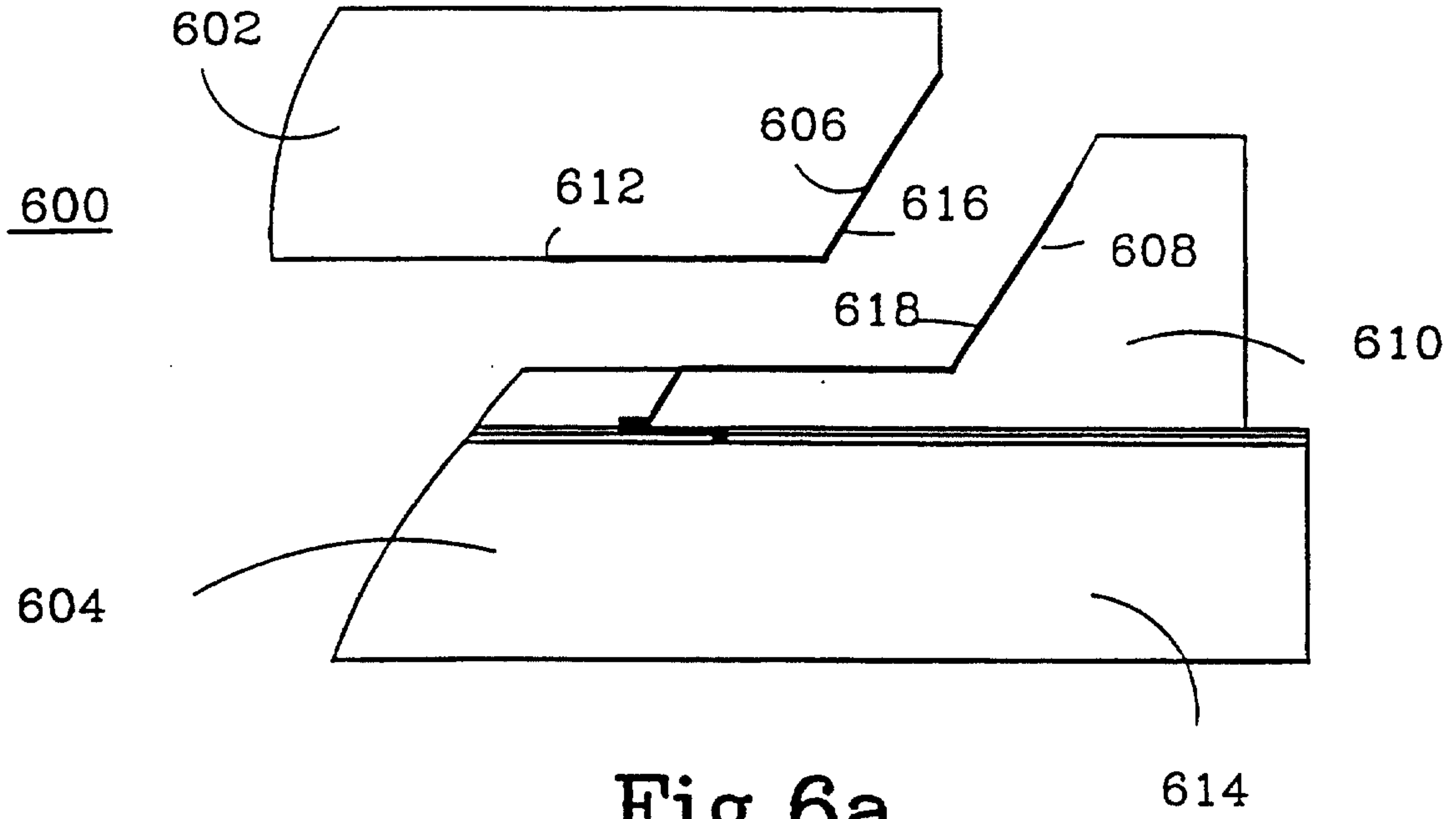


Fig.6a

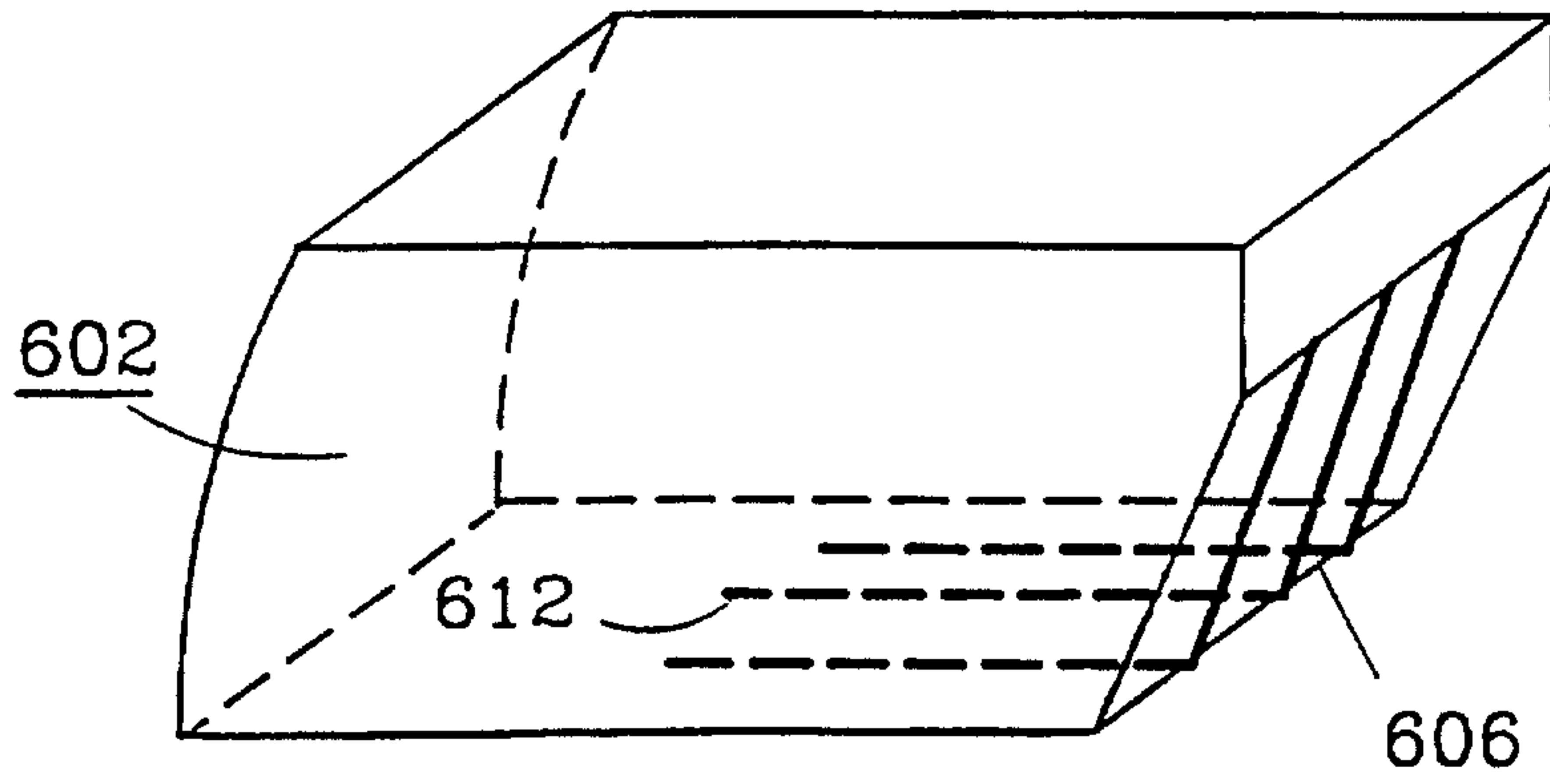


Fig. 6b

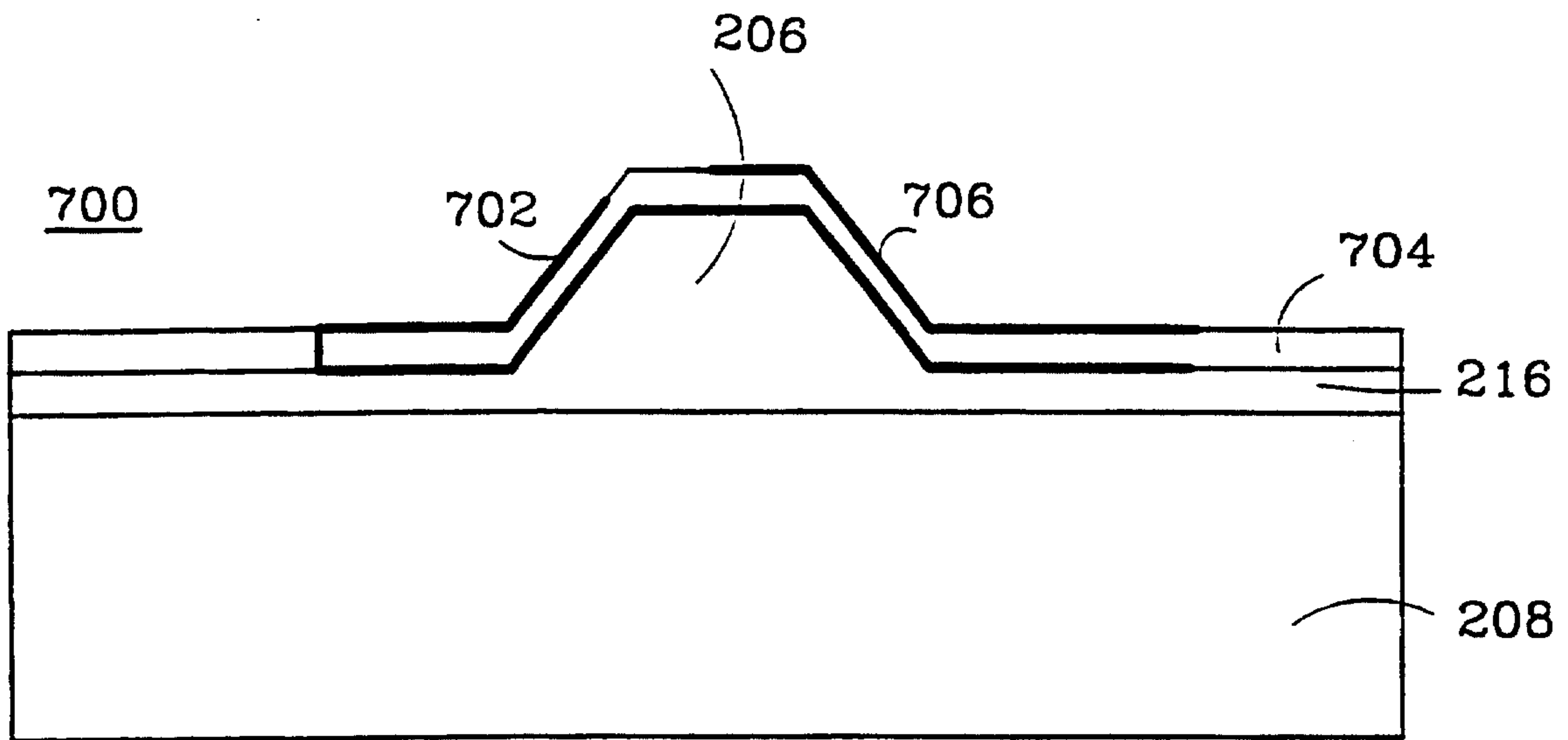


FIG 7