(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
06 September 2024 (06.09.2024)

WIPO | PCT

(10) International Publication Number
WO 2024/178543 A1

(51) International Patent Classification:
H04N 5/268 (2006.01)

(21) International Application Number:
PCT/CN2023/078453

(22) International Filing Date:
27 February 2023 (27.02.2023)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant: **HUAWEI TECHNOLOGIES CO., LTD.** [CN/CN]; Huawei Administration Building, Bantian, Longgang, Shenzhen, Guangdong 518129 (CN).

(72) Inventors: **TAKAHASHI, Seiji**; Huawei Administration Building, Bantian, Longgang, Shenzhen, Guangdong 518129 (CN). **HUANG, Zhijian**; Huawei Administration Building, Bantian, Longgang, Shenzhen, Guangdong 518129 (CN).

(74) Agent: **LONGSUN LEAD IP LTD.**; Room 801-1, Floor 8, Building 3, Block 2, No. 81 Beiqing Road, Haidian District, Beijing 100094 (CN).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CV, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IQ, IR, IS, IT, JM, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(54) Title: AN IMAGING DEVICE, A MEHOED FOR DRIVING THE IMAGING DEVICE AND ELECTRONIC DEVICES

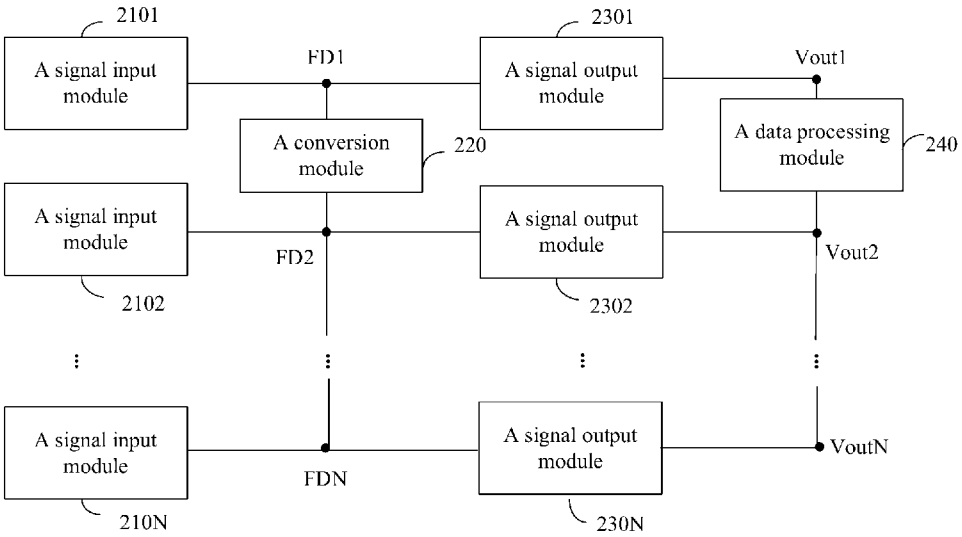

FIG. 2

(57) Abstract: Embodiments of the present application provide an imaging device, a method for driving the imaging device and electronic devices. The imaging device includes N signal input modules, N signal output modules, a conversion module, and a data processing module, where N terminals of the N signal input modules are electrically connected to N first terminals of the N signal output modules through N floating diffusion nodes, respectively, the conversion module is coupled to the N floating diffusion nodes, N second terminals of the N signal output modules are electrically connected to the data processing module, and N is an integer greater than 2, where the N signal input modules are configured to generate electrical charges by sensing an image; the conversion module is configured to control whether the N floating diffusion nodes are electrically connected; the N signal output modules are configured to amplify the electrical charges in the N floating diffusion nodes, respectively; and the data processing module is configured to obtain imaging data of the image based on the amplified electrical charges. According to the above technical solution, a signal-to-noise ratio of an imaging device can be improved.

WO 2024/178543 A1

[Continued on next page]

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, CV, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SC, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, ME, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

AN IMAGING DEVICE, A MEHOED FOR DRIVING THE IMAGING DEVICE AND ELECTRONIC DEVICES

TECHNICAL FIELD

[0001] Embodiments of the present application relate to the field of imaging technologies, and more specifically, to an imaging device, a method for driving the imaging device and electronic devices.

BACKGROUND

[0002] A unit pixel may include multiple pixels, photo electrons generated by the multiple pixels may be summed up in order to increase effective pixel size. The unit pixel may also be referred to as a pixel binning or a full pixel. For example, the unit pixel may include 4-merged pixels arranged in a 2×2 matrix, and photo electrons generated by the 4 pixels may be summed up by a data processing module. However, the sensitivity of the merged pixels increases for merging, and a signal-to-noise ratio is low due to lower conversion gain. Therefore, an urgent technical problem that needs to be solved is how to improve a signal-to-noise ratio of an imaging device.

SUMMARY

[0003] Embodiments of the present application provide an imaging device, a method for driving the imaging device and electronic devices. The technical solutions may improve a signal-to-noise ratio of an imaging device.

[0004] According to a first aspect, an embodiment of the present application provides an imaging device, including N signal input modules, N signal output modules, a conversion module, and a data processing module, where N terminals of the N signal input modules are electrically connected to N first terminals of the N signal output modules through N floating

diffusion nodes, respectively, the conversion module is coupled to the N floating diffusion nodes, N second terminals of the N signal output modules are electrically connected to the data processing module, and N is an integer greater than 2, where the N signal input modules are configured to generate electrical charges by sensing an image; the conversion module is configured to control whether the N floating diffusion nodes are electrically connected; the N signal output modules are configured to amplify the electrical charges in the N floating diffusion nodes, respectively; and the data processing module is configured to obtain imaging data of the image based on the amplified electrical charges.

[0005] According to the above technical solution, the N signal input modules, the N signal output modules and the conversion module can form the N floating diffusion nodes by an electrical connection. The electrical charges generated by the N signal input module may averagely distributed across the N floating diffusion nodes, and an averaging circuit has a noise reduction effect, thereby improving the signal-to-noise ratio of the imaging device.

[0006] In a possible design, the data processing module includes at least N analog to digital converters, when the conversion module is configured to control the N floating diffusion nodes to be connected, one analog to digital converter among the at least N analog to digital converters is configured to obtain the imaging data based on the amplified electrical charges; and when the conversion module is configured to control the N floating diffusion nodes to be electrically disconnected, the N analog to digital converters are configured to obtain the imaging data based on the amplified electrical charges.

[0007] According to the above technical solution, the data processing module may be in different circuit states based on whether the N floating diffusion nodes are connected, the N second terminals of the N signal output modules may be connected to the same or different analog to digital converters. When the N second terminals of the N signal output modules are connected to the same analog to digital converters, the noise can be reduced, and the signal-to-noise ratio of the imaging device can be further improved.

[0008] In a possible design, the data processing module includes a first set of switches and a second set of switches, when the first set of switches is turned on and the second set of switches is turned off, the one analog to digital converter among the at least N analog to digital converters is configured to obtain the imaging data based on the amplified electrical charges;

and when the first set of switches is turned off and the second set of switches is turned on, the N analog to digital converters are configured to obtain the imaging data based on the amplified electrical charges.

[0009] According to the above technical solution, at least two sets of switches in the data processing module may be configured to change a data processing circuit state based on whether the N floating diffusion nodes are connected.

[0010] In a possible design, each of the N analog to digital converters includes a signal input port and a reference input port, the signal input port and the reference input port each includes N terminals, where N terminals of the signal input port are configured to be electrically connected to at least one of the N second terminals of the N signal output modules through N first capacitors respectively, and N terminals of the reference input port are configured to be electrically connected to a reference node through N second capacitors respectively.

[0011] According to the above technical solution, the number of the capacitors connected to the signal input port and the number of the capacitors connected to the reference input port are same, the data processing module can match different modes.

[0012] In a possible design, the conversion module includes N dual conversion gain switches, and at least N-1 tunable conversion gain switches, where N first terminals of the N dual conversion gain switches are configured to be connected to the N floating diffusion nodes, respectively, and the at least N-1 tunable conversion gain switches are configured to control whether N second terminals of the N dual conversion gain switches are electrically connected, where when the N dual conversion gain switches are turned on and the at least N-1 tunable conversion gain switches are turned on, the N floating diffusion nodes are electrically connected; and when the N dual conversion gain switches or the at least N-1 tunable conversion gain switches are turned off, the N floating diffusion nodes are electrically disconnected.

[0013] According to the above technical solution, the capacitance of dual conversion gain switches, tunable conversion gain switch and wiring can help increase the floating diffusion capacitance, and the floating diffusion capacitance can hold electrical charges generated by signal input modules, and a dynamic range of the imaging device can be improved.

[0014] In a possible design, when the conversion module is configured to control the N floating diffusion nodes to be disconnected, the N dual conversion gain switches are turned on.

[0015] According to the above technical solution, if the N floating diffusion nodes are disconnected, turning on the dual conversion gain switches can help increase the floating diffusion capacitance, and the dynamic range of the imaging device can be improved.

[0016] In a possible design, the conversion module includes at least N-1 tunable conversion gain switches, and the at least N-1 tunable conversion gain switches are configured to control whether the N floating diffusion nodes are electrically connected.

[0017] In a possible design, the each of the N signal input modules include at least two photoelectric conversion units, and each of the at least two photoelectric conversion units is connected to the corresponding floating diffusion node through a transmission transistor.

[0018] According to the above technical solutions, pixels in a unit pixel may be distributed across the N signal input modules, and the number of photoelectric conversion units in the N signal input modules may be greater than the number of pixels in the unit pixel.

[0019] In a possible design, the transmission transistors connected to the photoelectric conversion units with same color filters in the N signal input modules are turned on at the same time.

[0020] According to the above technical solution, the photoelectric conversion units with the same color filters may form a unit pixel.

[0021] In a possible design, at least one signal input module among the N signal input modules includes at least two photoelectric conversion units with different color filters.

[0022] According to the above technical solution, the photoelectric conversion units in the N signal input modules may form multiple unit pixels.

[0023] According to a second aspect, an embodiment of the present application provides a method for driving the imaging device, where the imaging device includes N signal input modules, N signal output modules, a conversion module, and a data processing module, where N terminals of the N signal input modules are electrically connected to N first terminals of the N signal output modules through N floating diffusion nodes respectively, the conversion module is coupled to the N floating diffusion nodes, N second terminals of the N signal output modules are electrically connected to the data processing module, and N is an integer greater than 2, where generating, by the N signal input modules, electrical charges by sensing an image; controlling, by the conversion module, whether the N floating diffusion nodes are electrically

connected; amplifying, by the N signal output modules, the electrical charges in the N floating diffusion nodes respectively; and obtaining, by the data processing module, imaging data of the image based on the amplified electrical charges.

[0024] According to a third aspect, an embodiment of the present application provides an electronic device including the imaging device according to the first aspect.

DESCRIPTION OF DRAWINGS

[0025] FIG. 1 is a schematic structure of an imaging device.

[0026] FIG. 2 is a circuit diagram of an imaging device according to an embodiment of the present application.

[0027] FIG. 3 is a circuit diagram of two signal input modules according to an embodiment of the present application.

[0028] FIG. 4 is a circuit diagram of a conversion module according to an embodiment of the present application.

[0029] FIG. 5 is a circuit diagram of a signal output module according to an embodiment of the present application.

[0030] FIG. 6 is a circuit diagram of a data processing module according to an embodiment of the present application.

[0031] FIG. 7 is a circuit of a data processing module when a conversion module works in a binning mode according to an embodiment of the present application.

[0032] FIG. 8 is a circuit of a data processing module when a conversion module works in a non-binning mode according to an embodiment of the present application.

[0033] FIG. 9 is a schematic timing diagram of control signals when a conversion module works in a binning mode according to an embodiment of the present application.

[0034] FIG. 10 is a schematic timing diagram of control signals when a conversion module works in a non-binning mode according to an embodiment of the present application.

[0035] FIG. 11 is a schematic diagram of a connection way of multiple signal input modules according to a first implementation of the present application.

[0036] FIG. 12 is a circuit diagram of an imaging device according to the first

implementation of the present application.

[0037] FIG. 13 is a schematic timing diagram of control signals in a binning mode according to the first implementation of the present application.

[0038] FIG. 14 is a schematic timing diagram of control signals in a non-binning mode according to the first implementation of the present application.

[0039] FIG. 15 is a schematic diagram of a connection way of multiple signal input modules according to a second implementation of the present application.

[0040] FIG. 16 is a circuit diagram of an imaging device according to the second implementation of the present application.

[0041] FIG. 17 is a schematic diagram of a connection way of multiple signal input modules according to a third implementation of the present application.

[0042] FIG. 18 is a schematic diagram of a connection way of multiple signal input modules according to a fourth implementation of the present application.

[0043] FIG. 19 is a schematic diagram of a connection way of multiple signal input modules according to a fifth implementation of the present application.

[0044] FIG. 20 is a schematic diagram of a connection way of multiple signal input modules according to a sixth implementation of the present application.

[0045] FIG. 21 is a schematic diagram of a connection way of multiple signal input modules according to a seventh implementation of the present application.

[0046] FIG. 22 is a schematic diagram of a connection way of multiple signal input modules according to an eighth implementation of the present application.

[0047] FIG. 23 is a schematic architecture diagram of a signal input module according to an embodiment of the present application.

[0048] FIG. 24 is a schematic architecture diagram of multiple signal input modules according to an embodiment of the present application.

[0049] FIG. 25 is a schematic diagram of a signal input module according to an embodiment of the present application.

[0050] FIG. 26 illustrates some schematic diagrams of possible imaging devices according to embodiments of the present application.

[0051] FIGS. 27-29 illustrate some schematic diagrams of possible imaging systems

according to embodiments of the present application.

DESCRIPTION OF EMBODIMENTS

[0052] The following describes technical solutions of the present application with reference to the accompanying drawings.

[0053] FIG. 1 is a schematic structure of an imaging device.

[0054] The imaging device includes a pixel array 110, a control module 120 and a data processing module 130. The pixel array 110 includes a matrix in which X rows and Y columns are arranged and a unit pixel is provided at each of cross points of rows and columns (X and Y are integers). The pixel array 110 may sense an image of a subject. The control module 120 controls the pixel array 110, for example, the control module 120 may generate a shutter signal for the pixel array 110. Photo electrons generated by the pixel array 110 are read out and processed by the data processing module 130.

[0055] The imaging device may be also named as an imaging sensor device, which may be applied to electronic devices in a wide range of fields, including sport gears, such as wearable cameras; medical devices, such as endoscopes; cosmetic equipments; vehicles or transport equipments, such as trucks; entertainment devices, such as mobile phones, game consoles, digital cameras, and video camcorders; agricultural field, such as a farmland surveillance camera; home appliances, such as televisions and refrigerators; and the security field, such as monitoring cameras, network cameras, and machine vision cameras. The present application does not specifically limit this.

[0056] In some embodiments, focus detecting pixels as well as imaging pixels are implemented in the pixel array. In order to perform an auto focus function, the unit pixel may include at least two photoelectric conversion units, such as photodiodes.

[0057] The unit pixel may include multiple pixels, the photo electrons generated by the multiple pixels may be summed up in order to increase the effective pixel size. The unit pixel may also be referred to as a pixel binning or a full pixel. The multiple pixels of the unit pixel may have the same color filters or different color filters. For example, the unit pixel may include 4-merged pixels arranged in a 2×2 matrix, and photo electrons generated by the 4 pixels may

be summed up by the data processing module. However, the sensitivity of the merged pixels increases for the merging, and a signal-to-noise ratio is low due to lower conversion gain Therefore, an urgent technical problem that needs to be solved is how to improve the signal-to-noise ratio of the imaging device.

[0058] It should be noted that a signal input module may be referred to as a module in the pixel array in FIG. 1 or other possible modules. A conversion module may be referred to as a module in the pixel array, a module in the control circuit in FIG. 1 or other possible modules. A signal output module may be referred to as a module in the pixel array or a module in the readout circuit in FIG. 1 or other possible modules. A data processing module may be referred to as a module in the readout circuit, a module in the signal processing circuit in FIG. 1 or other possible modules. The present application does not specifically limit this.

[0059] The embodiments of the present application provide an imaging device, a method for driving the imaging device and related devices. The technical solution may improve the signal-to-noise ratio of the imaging device. The imaging device provided in the present application is first described below.

[0060] FIG. 2 is a circuit diagram of an imaging device according to an embodiment of the present application.

[0061] The imaging device includes N signal input modules (such as signal input modules 2101 to 210N shown in FIG. 2), N signal output modules (such as signal output module 2301 to 230N shown in FIG. 2), a conversion module (such as a conversion module 220 shown in FIG. 2), and a data processing module (such as a data processing module 240 shown in FIG. 2), where N terminals of the N signal input modules are connected to N first terminals of the N signal output modules through N floating diffusion (FD) nodes (such as FD1 to FDN shown in FIG. 2), respectively, the conversion module is coupled to the N FD nodes. N second terminals of the N signal output modules are connected to the data processing module. The second terminals of the N signal output modules may also be referred to as N readout nodes (such as Vout1 to VoutN shown in FIG. 2), respectively, where the N is an integer greater than 2.

[0062] The N signal input modules are configured to generate electrical charges by sensing an image. For example, the N signal input modules may sense the image and generate the electrical charges based on the image. The electrical charges may be merged at a floating

diffusion area, in other words, the electrical charges may be accumulated at the N FD nodes. For example, electrical charges generated by the signal input module 2101 are accumulated at FD1 node and electrical charges generated by the signal input module 2102 are accumulated at FD2 node.

[0063] It should be noted that the N signal input modules may contain a unit pixel, in other words, pixels of a unit pixel may be distributed across the N signal input modules, at least two pixels of the unit pixel have different FD nodes.

[0064] The conversion module is configured to control whether the N floating diffusion nodes are connected. For example, the conversion module may work in a binning mode or a non-binning mode. The binning mode may be also referred to as a pixel binning readout mode or a full pixel readout mode. If the conversion module is configured to work in the binning mode, the N floating diffusion nodes are connected and the electrical charges flow between the N floating diffusion nodes through the conversion module, if the conversion module is configured to work in the non-binning mode, the N floating diffusion nodes are disconnected.

[0065] The N signal output modules are configured to amplify the electrical charges in the N floating diffusion nodes, respectively. The data processing module is configured to obtain imaging data of the image based on electrical charges in the N readout nodes. The N floating diffusion nodes are connected to the N readout nodes through the N signal output modules. At least two pixels of the unit pixel have different readout nodes.

[0066] According to the embodiments provided by the present application, N signal input modules, N signal output modules and a conversion module can form N floating diffusion nodes by an electrical connection. The electrical charges generated by the N signal input module may averagely distributed across the N floating diffusion nodes, an averaging circuit has a noise reduction effect, thereby improving the signal-to-noise ratio of the imaging device.

[0067] It should be noted that the noise reduction effect is related to the number of floating diffusion N, the noise may be reduced by a factor of 1/sqrt(N) theoretically.

[0068] The data processing may read the voltages of the N readout nodes. Optionally, the data processing module includes at least N analog to digital converters (ADCs), if the conversion module is configured to work in a first mode, the N readout nodes are connected to an analog to digital converter among the at least N ADCs; and if the conversion module is

configured to work in a second mode, the N readout nodes are connected to N ADCs, respectively.

[0069] The data processing module may be controlled to make the N readout nodes as an input of the same ADC when the conversion module works in the first mode, and the data processing may be controlled to make the N readout nodes as inputs of N different ADCs when the conversion module works in the second mode. The pixels of the unit pixel may be summed up as the input of the same ADC, and the effective pixel size can be increased.

[0070] In addition, both the conversion module and the data processing module can work in two modes and can be switched between the two modes, application scenarios of the imaging device can be expanded.

[0071] In order to facilitate understanding of the embodiment of the present application, the following describes the possible structure of the modules provided by the embodiments of the present application in combination with FIGS. 3 to 29. It should be noted that the switches of the present application may be transistors, and in the description below, some of the switches are illustrated exemplarily with the transistors.

[0072] FIG. 3 is a circuit diagram of two signal input modules according to an embodiment of the present application.

[0073] The signal input module 2101 may include at least one photodiode, as shown in FIG.3, the signal input module 201 includes 8 photodiodes (PD), namely PD1-8. An anode of each of the 8 photodiodes is electrically connected to an analog voltage source source (AVSS). A cathode of each of the 8 photodiodes is electrically connected to a source of a transmission transistor (TX), and 8 transmission transistors are named TX1-8. Drains of all the 8 transmission transistors are connected at a floating diffusion node FD1. A gate of each of the 8 transmission transistors is controlled by a transmission control signal. The transmission control signal is used to control the corresponding TX transistor to be turned on or to be turned off.

[0074] Each of the 8 photodiodes may convert electromagnetic wave into electrical charges. When a TX transistor is turned on, electrical charges converted by the corresponding photodiode may flow to the floating diffusion node FD1. Conversely, when the TX transistor is turned off, the electrical charges converted by the corresponding photodiode may not flow to the floating diffusion node FD1.

[0075] In some embodiments, all or part of the photodiodes in the signal input module 211 are selected to transmit the electrical charges to the floating diffusion node FD1 through the corresponding TX transistor. For example, as referred to FIG. 3, if all photodiodes PD1-8 are selected, the all transmission transistor TX1-8 are turned on. If 4 photodiodes are selected, the photodiodes PD1-4 may be selected, corresponding transmission transistors TX1-4 may be turned on and the transmission transistors TX5-8 may be turned off. If 2 photodiodes are selected, the photodiodes PD1-2 may be selected, corresponding transmission transistors TX1-2 may be turned on and the transmission transistors TX3-8 may be turned off. The embodiments of the present application does not specifically limit this.

[0076] The structure of the signal input module 2102 may be similar to that of the signal input module 2101, and a more detailed description can be found in the description of the signal input module 2101 above, which will not be repeated here.

[0077] If the signal input module 2101 and the signal input module 2102 contain a unit pixel, for example, the unit pixel includes 4 pixels, and 4 pixels are represented by 4 photodiodes. As shown in FIG. 3, PD1 and PD2 in the signal input module 2101 and PD1 and PD2 in the signal input module 2102 are 4 pixels in the unit pixel.

[0078] It should be noted that the number of photodiodes in the signal input module 2101 and the number of photodiodes in the signal input module 2102 may be the same or different, and the embodiments of the present application do not specifically limit this.

[0079] It also should be noted that an imaging device may include multiple signal modules, the N signal input modules among the multiple signal modules may contain at least one unit pixel, and the embodiments of the present application do not specifically limit this.

[0080] Signal input modules are described above, and a conversion module provided by the embodiments of the present application is described below.

[0081] In a first possible implementation, the conversion module includes N dual conversion gain (DCG) transistors, and at least N-1 tunable conversion gain (TCG) transistors, N first terminals of the N DCG transistors are connected to the N floating diffusion nodes, respectively, and the at least N-1 TCG transistors are used to connect N second terminals of the N DCG transistors. If the conversion module is configured to work in a first mode, the N DCG transistors are turned on, and the at least N-1 TCG transistors are turned on. If the conversion

module is configured to work in a second mode, the at least N-1 TCG transistors are turned off.

[0082] For example, a TCG transistor is connected between every two DCG transistors. Therefore, the capacitance of a DCG transistor, the capacitance of a TCG transistor and wiring may help increase the floating diffusion capacitance, the floating capacitance may hold electrical charges generated by signal input modules, and a dynamic range of the imaging device can be improved.

[0083] In a second possible implementation, the conversion module includes at least N-1 tunable conversion gain transistors, where the at least N-1 tunable conversion gain transistors are configured to connect the N floating diffusion nodes. If the conversion module is configured to work in the first mode, the at least N-1 tunable conversion gain transistors are turned on. If the conversion module is configured to work in the second mode, the at least N-1 tunable conversion gain transistors are turned off.

[0084] For example, a TCG transistor is connected between every two floating diffusion nodes, and the TCG transistor and wiring between the floating diffusion may also help increase the floating diffusion capacitance, and a dynamic range of the imaging device can be improved.

[0085] FIG. 4 is a circuit diagram of a conversion module according to an embodiment of the present application. In order to facilitate understanding of the embodiment, a partial circuit of the conversion module between a floating diffusion node FD1 and a floating diffusion node FD2 with DCG transistors and a DCG transistor is shown in FIG. 4.

[0086] The conversion module 220 may also include reset (RST) transistors (such as RST1 and RST2 in FIG. 4), two DCG transistors (such as DCG1 and DCG2 in FIG. 4), and a TCG transistor (such as TCG in FIG. 4). A source of the DCG1 is electrically connected to the FD1 (that is, the source of the DCG1 is electrically connected to at least one drain of at least one TX in a signal input module), and a drain of the DCG1 is electrically connected to a source of the RST1. A drain of the RST1 is connected to an analog voltage drain drain (AVDD). Similarly, a source of the DCG2 is electrically connected to the FD2, and a drain of the DCG2 is electrically connected to a source of the RST2. A drain of the RST2 is connected to an AVDD.

[0087] A node between the DCG1 and the RST1 may be referred to as a first node N1, and a node between the DCG2 and the RST2 may be referred to as a second node N2. The TCG is electrically connected between the N1 and the N2. For example, a source of the TCG is

electrically connected to the N1 and a drain of the TCG is electrically connected to the N2.

[0088] A gate of the RST1 is controlled by a first reset signal. The first reset signal is configured to control the RST1 to be turned on or to be turned off. A gate of the RST2 is controlled by a second reset signal. The second reset signal is configured to control the RST2 to be turned on or to be turned off. A gate of the DCG1 is controlled by a first dual conversion signal. The first dual conversion signal is configured to control the DCG1 to be turned on or to be turned off. A gate of the DCG2 is controlled by a second dual conversion signal. The second dual conversion signal is configured to control the DCG2 to be turned on or to be turned off. A gate of the TCG is controlled by a tunable conversion signal. The tunable conversion signal is configured to control the TCG to be turned on or to be turned off.

[0089] When the RST1 and the DCG1 are turned on, electrical charges accumulated in the FD1 may be discharged. When the RST2 and the DCG2 are turned on, electrical charges accumulated in the FD2 may be discharged.

[0090] If the conversion module 220 works in a first mode, the RST1 and the RST2 are turned off, and the DCG1, the DCG2 and the TCG are turned on, electrical charges in the FD1 and FD2 may flow into each other through a pathway formed by the DCG1, the DCG2 and the TCG, and the electrical charges in the FD1 and the FD2 may be averaged.

[0091] If the conversion module 220 works in a second mode, the RST1, the RST2 and the TCG are turned off, a pathway between the N1 and the N2 are cut off, the electrical charges in the FD1 and the FD2 may not flow into each other, the FD1 aggregates electrical charges generated by a signal input module 2101 and the FD2 aggregates electrical charges generated by a signal input module 2102.

[0092] It should be noted that when the conversion module 220 works in the second mode, the DCG1 may be turned on or turned off and the DCG2 may be turned on or turned off. The capacitance of the FD1 to accumulate the electrical charges may be increased due to the turning-on DCG1, and similarly, the capacitance of the FD2 to accumulate the electrical charges may be increased due to the turning-on DCG2.

[0093] A conversion module is described above, and a signal output module provided by the embodiments of the present application is described below.

[0094] FIG. 5 is a circuit diagram of a signal output module according to an embodiment

of the present application.

[0095] The signal output module may include an amplifier (AMP) transistor, a selecting SEL transistor, and optionally a current source Ic. A gate of the AMP transistor is electrically connected to a FD node, a drain of the AMP transistor is electrically connected to an AVDD, and a source of the AMP transistor is electrically connected to a drain of the SEL transistor. If the signal output module also includes the current source Ic, the drain of the SEL transistor may be electrically connected to an AVSS through the Ic. A gate of the SEL transistor is controlled by a first selecting signal, the first selecting signal is configured to control the SEL transistor to be turned on or to be turned off. A voltage output line may be electrically connected to the drain of the SEL transistor, and a node of the drain of the SEL may be referred to as a readout node, which may also be named a voltage readout (Vout) node.

[0096] Optionally, an AVSS may be ground or a negative voltage is in a range of -5.0 V to 0 V.

[0097] Optionally, an AVSS connected to a photodiode and an AVSS connected to a SEL transistor or a current source may be the same.

[0098] Optionally, an AVDD connected to a RST transistor and an AVDD connected to an AMP transistor are the same.

[0099] The AMP transistor may operate as a source follower buffer amplifier, which may amplify electrical charges accumulated in the FD node. When the SEL transistor is turned on, the voltage of the Vout may be read out.

[0100] Optionally, at least one of the following transistors is positive channel metal oxide semiconductor (PMOS): RST transistor, DCG transistor, AMP transistor, SEL transistor, TX transistor or TCG transistor.

[0101] A signal output module is described above, and a data processing module provided by the embodiments of the present application is described below.

[0102] FIG. 6 is a circuit diagram of a data processing module according to an embodiment of the present application.

[0103] A data processing module may include at least N ADCs and at least N sets of switches, the at least N sets of switches are configured to control inputs of the N ADCs. Optionally, each of the N ADCs includes two input ports (a signal input port connected to the

signal output modules and a reference input port connected to a reference node (which may be a output port of a reference signal source)), each of the two input ports includes N terminals, and each of the N terminals is connected to a capacitor.

[0104] In order to facilitate understanding of the embodiment, a data processing module with two sets of switches and two ADCs are introduced in FIG. 6. The first set of switches includes four switches (such as SW2, 4, 5 and 6 in FIG. 6) and the second set of switches includes two switches (such as SW1 and SW3 in FIG. 6). Each ADC may include a comparator and a counter. Each ADC includes two input ports, each of the two input ports includes 2 terminals, and each of the 2 terminals is connected to a capacitor, such as 8 capacitors C1-8 in FIG. 6. One input port of an ADC may be a positive input port, which is connected to a reference signal generator through a reference node. For example, as shown in FIG. 6, a positive input port of the first ADC may be connected to the reference node through a first capacitor C1 and a second capacitor C2 connected in parallel, and the positive input port of the second ADC may be connected to the reference node through a fifth capacitor C5 and a sixth capacitor C6 connected in parallel.

[0105] Another input port of the ADC may be referred to as a negative input port, which is connected to one or more readout nodes through switches. For example, as shown in FIG. 6, a terminal of a negative input port of the first ADC is connected to a terminal of a first switch SW1 through a third capacitor C3, and another terminal of the SW1 is connected to a Vout1. A second switch SW2 and a third switch SW3 are connected in series between the Vout1 and a Vout2. A second terminal of the negative input port of the first ADC is connected to a connection node between the SW2 and the SW3 through a fourth capacitor C4. A fourth switch SW4 is connected between the connection node of the SW2 and the SW3 and a connection node of the C3 and SW1. A first terminal of a negative input port of the second ADC is connected to a terminal of a fifth switch SW5 through a seventh capacitor C7, and another terminal of the SW5 is connected to the Vout2. A second terminal of the negative input port of the second ADC is connected to a terminal of a sixth switch SW6 through an eighth capacitor C8, and another terminal of the SW6 is connected to a connection node between the C7 and the SW5.

[0106] In order to facilitate understanding of the embodiment, FIG. 7 is a circuit of a data processing module when a conversion module works in a binning mode, and FIG. 8 is a circuit

of a data processing module when a conversion module works in a non-binning mode.

[0107] If a conversion module 220 works in a binning mode, SW1 and SW3 are turned on and SW2, SW4, SW5 and SW6 are turned off, the circuit shown in FIG. 6 may be equal to be a circuit shown in FIG. 7. A Vout1 and a Vout2 are inputs of the same ADC.

[0108] If the conversion module 220 works in a non-binning mode, the SW1 and the SW3 are turned off and the SW2, the SW4, the SW5 and the SW6 are turned on, the circuit shown in FIG.6 may be equal to a circuit shown in FIG. 8. The Vout1 is an input of a first ADC and the Vout2 is an input of a second ADC, that is, the Vout1 and the Vout2 are inputs of different ADCs.

[0109] It can be understood that an imaging device may also include a control module (not shown in FIG. 2) that provides control signals to other modules, such as signal input modules, second signal input modules, a conversion module, signal output modules, and a data processing module.

[0110] In order to facilitate understanding of the embodiment, FIG. 9 is a schematic timing diagram of control signals when a conversion module works in a binning mode, and FIG. 10 is a schematic timing diagram of control signals when a conversion module works in a non-binning mode.

[0111] A control module may provide transmission signals (such as signals TX1, 2 shown in FIG. 9 and FIG. 10) to gates of TX transistors in signal input modules. The control module may provide reset signals (such as signals RST1, 2, DCG1, 2 and TCG shown in FIG. 9 and FIG. 10) to gates of RST transistors, dual conversion gain signals to gates of DCG transistors and a tunable conversion gain signal to a gate of a TCG transistor in a conversion module. The control module may provide selecting signals (such as signals SEL1, 2 shown in FIG. 9 and FIG. 10) to gates of SEL transistors in the signal output modules. The control module may also provide switch signals (such as signals SW1-6 shown in FIG. 9 and FIG. 10) to control switches in a data processing module.

[0112] A process of the imaging device to obtain image data may be divided into three stages, a first stage is a shutter stage, a second stage is an exposure stage, and a third stage is a readout stage. The shutter stage may be configured to discharge electrical charges accumulated in floating diffusion nodes. The exposure stage is a period of sensing an image. The readout stage is configured to obtain the image data of the sensed image.

[0113] If a conversion module 220 works in the binning mode, the control signals are shown in FIG. 9. In the shutter stage, the RST1, 2, the DCG1, 2, the TCG and the TX1, 2 are controlled to be turned on, and electrical charges in the FD1 and the FD2 may be discharged. In the exposure stage, photodiode(s) in a signal input module 2101 converts electromagnetic wave into electrical charges and the electrical charges float to the FD1. Photodiode(s) in a signal input module 2102 converts electromagnetic wave into electrical charges and the electrical charges float to the FD2.

[0114] After the exposure stage and in the readout stage, the SEL1 and the SEL2 are turned on, which means that the signal input module 2101 and the signal input signal 2102 are selected to provide the electrical charges. The RST1, 2, the DCG1, 2, the TCG, and SW1, 3 are controlled to be turned on and the TX1, 2 and SW2, 4, 5, 6 are controlled to be turned off. Then the RST1, 2 are controlled to be turned off, Vout1 and Vout2 are read out by the same ADC (as shown in FIG. 7) at time t4, and a LCG RST value is obtained. Then the DCG1, 2, the TCG, and the SW1, 3 are controlled to be turned off, the SW2, 4, 5, 6 are controlled to be turned on, the Vout1 and the Vout2 are read out by two different ADCs (as shown in FIG. 8) at time t5, and a HCG RST value is obtained. Then the TX1, 2 are controlled to be turned on for a short period of time, the Vout1 and the Vout2 are read out by two different ADCs at time t6 after the TX1, 2 are turned off, and a HCG SIG value is obtained. Then the DCG1, 2, the TCG, and the SW1, 3 are controlled to be turned on, the TX1, 2 are controlled to be turned on for a short period of time, the SW2, 4, 5, 6 are controlled to be turned off, the Vout1 and the Vout2 are read out by the same ADC at time t7 after the TX1, 2 are turned off, and a HCG SIG value is obtained. Image data may be obtained by the above values. A signal is obtained by carrying out a correlating double sampling (CDS) which uses a difference between a reset level and a signal level in the readout stage, in order to reduce the fixed pattern noise and reset noise.

[0115] If the conversion module 220 works in the non-binning mode, control signals are shown in FIG. 10. In the shutter stage, the RST1, 2, the DCG1, 2 and the TX1, 2 are controlled to be turned on, and the electrical charges in the FD1 and the FD2 may be discharged. In the exposure stage, photodiode(s) in the signal input module 2101 converts electromagnetic wave into electrical charges and the electrical charges float to the FD1. Photodiode(s) in the signal input module 2102 converts electromagnetic wave into electrical charges and the electrical

charges float to the FD2.

[0116] After the exposure stage and in the readout stage, the SEL1 and the SEL2 are turned on, which means that the signal input module 2101 and the signal input signal 2102 are selected to provide electrical charges. The RST1, 2, the DCG1, 2, and the SW2, 4, 5, 6 are controlled to be turned on and the TCG, the TX1, 2 and the SW1, 3 are controlled to be turned off. Then the RST1, 2 are controlled to be turned off, the Vout1 and the Vout2 are read out by the same ADC (as shown in FIG. 7) at time t4, and a LCG RST value is obtained. Then the DCG1, 2 are controlled to be turned off, the Vout1 and the Vout2 are read out by the same ADC at time t5, and a HCG RST value is obtained. Then the TX1, 2 are controlled to be turned on for a short period of time, the Vout1 and the Vout2 are read out by the same ADC at time t6 after the TX1, 2 are turned off, and a HCG SIG value is obtained. Then the DCG1, 2 are controlled to be turned on, the TX1, 2 are controlled to be turned on for a short period of time, the Vout1 and the Vout2 are read out by the same ADC at time t7 after the TX1, 2 are turned off, and a HCG SIG value is obtained. Image data may be obtained by the above values.

[0117] In some embodiments, the capacitor, for example, which is made by pn-junction capacitor, MOS capacitor, metal-oxide-metal (MOM) capacitor, metal-insulator-metal (MIM) capacitor, polysilicon-insulator-polysilicon (PIP) capacitor, dynamic random access memory (DRAM), magneto resistive random access memory MRAM, other type of on-chip memory, or combinations thereof, is electrically connected to the node between a DCG drain and a RST source. In a high-illuminance mode, a floating diffusion area is electrically connected to the above capacitors. For example, in the high-illuminance mode, overflowed charges from the photodiode are not drained, but are held by using an expanded full well capacity. The expanded full well capacity may make a potential change of the floating diffusion area relatively small compared with the amount of overflowed charges. For example, a conversion gain becomes small in the high-illuminance mode. This is accomplished by activating a DCG control signal to be provided to a solid-state imaging device such that a DCG transistor is turned on. In this case, the DCG transistor may always be maintained in a turning-on state while an operation is performed in the high-illuminance mode.

[0118] The present embodiment describes an example of reading out data on a frame-by-frame basis composed of all of pixels in an array by sequentially reading out pixel charges

stored in all of the pixels in the array by using SEL transistors. However, alternatively, instead of reading out the data on the frame-by-frame basis, an imaging device operating in a way referred to as an event driven type can be embodied by using the pixel of the present embodiment. In the imaging device, data can be output asynchronously at any time in response to changes in the intensity of the electromagnetic wave incident on the pixel. Specifically, for example, when the pixel charges generated by the electromagnetic wave incident on the pixel and stored in the pixel exceeds a predetermined threshold, data can be output to indicate that the intensity of the electromagnetic wave exceeds a threshold value or the intensity of the electromagnetic wave, in combination with coordinates and time information of the pixel.

[0119] In some embodiments, the pixel has a global shutter scheme, and the solid-state imaging device has an all pixel simultaneous electronic shutter function through a voltage domain or a charge domain.

[0120] The basic structure of the imaging device is described above. Pixels in a unit pixel can be distributed in different signal input modules in a variety of ways, with different numbers of floating diffusion nodes, as illustrated below in combination with FIGS. 11 to 26.

[0121] FIG. 11 is a schematic diagram of a connection way of multiple signal input modules according to a first implementation of the present application. Photodiodes with the same color filters are arranged in 2x2 unit pixel, a 2x2 unit pixel has two floating diffusion nodes with two signal input modules. A signal input module may include four photodiodes, photodiodes with the same color filters in two signal input modules form a unit pixel. For example, as shown in FIG. 11, each signal input module arranged in the same row includes two photodiodes with blue filters and two photodiodes with green filters, and each signal input module arranged in the next row includes two photodiodes with red filters and two photodiodes with green filters. There are two different color filters arranged in the same floating diffusion shared by 2x2 unit pixels. The same color filters arranged in different signal input modules may share the same ADC when a conversion module between the signal input modules works in a binning mode.

[0122] FIG. 12 is a circuit diagram of an imaging device based on the schematic diagram in FIG. 11. An electrical connection mode of 6 signal input modules in FIG. 11 is shown in FIG. 12. Two adjacent signal input modules in the same row are connected through a conversion module. For example, a signal input module 21011 and a signal input module 21012 are

connected through a conversion module, the signal input module 21011 is connected to a Vout1 line through an output signal module, the signal input module 21012 is connected to a Vout2 line through a output signal module. When the conversion module works in a binning mode, the Vout1 and the Vout2 are read by an ADC. When the conversion module works in a non-binning mode, the Vout1 and the Vout2 are read by different ADCs. Signal input modules 21014, 21015 and 21016 in a second row may be referred to the description of signal input modules 21011, 21012 and 21013. A more specific description can be found in the description of FIG. 2 to FIG. 10, which will not be repeated here.

[0123] In order to facilitate understanding of the embodiment, FIG. 13 is a schematic timing diagram of control signals based on the circuit diagram shown in FIG. 12 working in a binning mode. Signals SEL#1 are supplied on selecting transistors in signal input modules in the same row, such as signal input modules 21011, 21012 and 21013. Signals RST#1 are supplied on reset transistors in the signal input modules in the same row. Signals DCG#1 are supplied on dual conversion gain transistors in conversion modules, such as a conversion module between a signal input module 21011 and a signal input module 21012, and a conversion module between the signal input module 21012 and a signal input module 21013. Signal TCG#11 is supplied on a tunable conversion gain transistor in the conversion module between the signal input module 21011 and the signal input module 21012. Signal TCG#12 is supplied on a tunable conversion gain transistor in the conversion module between the signal input module 21012 and the signal input module 21013. Signals TX#green are supplied on transmission transistors, which are corresponding to photodiodes with green filters in the signal input modules in the same row. Signals TX#blue are supplied on transmission transistors, which are corresponding to photodiodes with blue filters in the signal input modules in the same row. Signals SW#1, signals SW#2 and signals SW#3 are supplied on switches in output signal modules connected to the signal input modules 21011, 21012 and 21013. When the SW#1 are turned on and the SW#2 and the SW#3 are turned off, the signal input modules 21011, 21012 and 21013 are working in a non-binning mode, and the Vout1, the Vout2 and a Vout3 are read out by different ADCs. When the SW#2 are turned on and the SW#1 and the SW#3 are turned off, the signal input modules 21011 and 21012 are working in a binning mode, the Vout1 and the Vout2 are read by the same ADC. When the SW#3 are turned on and the SW#1 and the SW#2 are turned

off, the signal input modules 21012 and 21013 are working in the binning mode, the Vout2 and the Vout3 are read by the same ADC.

[0124] A process of the imaging device to obtain image data may be divided into a shutter stage, an exposure stage and a readout stage. The RST#1, the DCG#1, the TCG#11, the TCG#12 and the TX#green are controlled to be turned on once, then the RST#1, the DCG#1, the TCG#11, the TCG#12 and the TX#blue are controlled to be turned on once in the shutter stage. Then the exposure stage is a period of sensing an image. After the exposure stage and in the readout stage, the SEL#1, the RST#1, the DCG#1, the TCG#11 and the SW#1 are controlled to be turned on, then the RST#1 are controlled to be turned off, and a low conversion gain LCG RST value is obtained at time t4. Then the DCG#1, the TCG#11 and the SW#1 are turned off and the SW#2 are turned on, and a high conversion gain HCG RST value is obtained at time t5. Then the TX#green are turned on for a short period of time, and a HCG SIG value is obtained after the TX#green are shut down at time t6. Then the DCG#1, the TCG#11, the SW#1 are turned on, the SW#2 are turned off, and the TX#green are turned on for a short period of time, and a LCG SIG value is obtained at time t7. Then the RST#1, the DCG#1, the TCG#12 and the SW#1 are turned on, then the RST#1 are turned off, and a LCG RST value is obtained at time t8. Then the DCG#1, the TCG#12 and the SW#1 are turned off and the SW#3 are turned on, and a HCG RST value is obtained at time t9. Then the TX#blue are turned on for a short period of time, and a HCG SIG value is obtained after the TX#blue are turned off at time t10. Then the DCG#1, the TCG#11, the SW#1 are turned on, the SW#2 are shut down, and the TX#blue are turned on for a short period of time, and a LCG SIG value is obtained at time t11. Image data may be obtained by the above values.

[0125] FIG. 14 is a schematic timing diagram of control signals based on the circuit diagram shown in FIG. 12 working in a non-binning mode. The description of controlling signals may be referred to the description in FIG. 13. In a shutter stage, RST#1, DCG#1 and TX#green are controlled to be turned on once, then the RST#1, the DCG#1 and TX#blue are controlled to be turned on once in a shutter stage. Then an exposure stage is a period of sensing an image. After the exposure stage and in a read out stage, SEL#1, the RST#1, the DCG#1 and SW#2 are controlled to be turned on, then the RST#1 are controlled to be turned off, and a LCG RST value is obtained at time t4. Then the DCG#1 are turned off, and a HCG RST value is obtained

at time t5. Then the TX#green are turned on for a short period of time, and a HCG SIG value is obtained after the TX#green are turned off at time t6. Then the DCG#1 are turned on, and the TX#green are turned on for a short period of time, and a LCG SIG value is obtained at time t7. Then the RST#1, the DCG#1, SW#1 and SW#3 are turned on and the SW#2 are turned off, then the RST#1 are turned off, and a LCG RST value is obtained at time t8. Then the DCG#1 and the SW#1 are turned off, and a HCG RST value is obtained at time t9. Then the TX#blue are turned on for a short period of time, and a HCG SIG value is obtained after the TX#blue are turned off at time t10. Then the DCG#1, the SW#1 are turned on, and the TX#blue are turned on for a short period of time, and a LCG SIG value is obtained at time t11. Image data may be obtained by the above values.

[0126] Based on the above solution, for HCG values (the HCG RST value and the HCG SIG value) above, for example, when a pixel signal is small, such as under a low light condition, a HCG is preferred in terms of a signal-to-noise ratio. A pair of photodiodes with green filters in the signal input module 21011, and a pair of photodiodes with green filters in a signal input module 21012 are summed up in a charge domain, a FD1 node and a FD2 node, respectively. FD charge domain binning is a binning method that may be done without noise, thus increasing the signal-to-noise ratio. After that, a Vout1 corresponding to an output voltage of a source follower device with an input of FD1, and a Vout2 corresponding to an output voltage of a source follower device with an input of FD2, may be averaged in a comparator 1 circuit as different input nodes of a comparator. Eventually, electrical charges generated by all of four photodiodes are merged. An averaging circuit has a random noise reduction effect. Therefore the signal-to-noise ratio can be improved. In this case, random noise may reduce by a factor of 1/sqrt(2).

[0127] For LCG values (the LCG RST value and the LCG SIG value) above, for example, when a pixel signal is large, such as under a high light condition, a low conversion gain is desired in terms of a dynamic range. A pair of photodiodes with green filters in the signal input module 21011, and a pair of photodiodes with green filters in the signal input module 21012 are summed up in a charge domain, floating diffusion FD1, which is electrically coupled to FD2 by way of an appropriate control circuit of DCG transistors and TCG transistors. The capacitance of DCG transistors and the capacitance of TCG transistors and wiring can help

increase the FD capacitance, and the floating capacitance can hold all of electrical charges generated by all of four photodiodes, then the Vout1 and the Vout2, may be averaged in a comparator circuit as different input nodes of the comparator. As a result, a high dynamic range can be achieved.

[0128] FIG. 15 is a schematic diagram of a connection mode of multiple signal input modules according to a second implementation of the present application. Photodiodes with the same color filters are arranged in a 2x2 unit pixel, the 2x2 unit pixel has four floating diffusion nodes with four signal input modules, such as a 2x2 signal input module shown in FIG. 15. A signal input module may include four photodiodes, photodiodes with the same color filters in signal input modules form a unit pixel.

[0129] FIG. 16 is a circuit diagram of an imaging device based on the schematic diagram in FIG. 15. An electrical connection mode of 4 signal input modules in FIG. 15 is shown in FIG. 16. Four adjacent signal input modules in 2x2 are connected through a conversion module. For example, signal input modules 21021, 21022, 21021 and 21022 are connected through the conversion module, the signal input module 21021 is connected to a Vout1 line through an output signal module, and the signal input module 21022 is connected to a Vout2 line through the output signal module. The signal input module 21023 and the signal input module 21024 are connected to a Vout4 line through the output signal module. When the above conversion modules work in a binning mode, the Vout1, the Vout2, the Vout3 and the Vout4 are read by an ADC. When the above conversion modules work in a non-binning mode, the Vout1, the Vout2, the Vout3 and the Vout4 are read by four different ADCs. A more specific description can be found in the description of FIG. 2 to FIG. 10, which will not be repeated here. A timing diagram of control signals may be obtained by analogy with the description above.

[0130] FIG. 17 is a schematic diagram of a connection mode of multiple signal input modules according to a third implementation of the present application. Photodiodes with the same color filters are arranged in a 4x4 unit pixel, the 4x4 unit pixel has six floating diffusion nodes with six signal input modules, such as a 2x3 signal input module shown in FIG. 17. A signal input module may include four photodiodes, photodiodes with the same color filters in the six signal input modules form a unit pixel. The six signal input modules with the six floating diffusion nodes are connected to Vout1 to Vout6 lines, respectively. When conversion modules

between the six signal input modules are working in a binning mode, the Vout1 to Vout6 may be read out by the same ADC. When conversion modules between the six signal input modules are working in a non-binning mode, the Vout1 to Vout6 may be read out by six different ADCs. A circuit diagram and a timing diagram of control signals may be obtained by analogy with the description above.

[0131] FIG. 18 is a schematic diagram of a connection mode of multiple signal input modules according to a fourth implementation of the present application. Photodiodes with the same color filters are arranged in a 4x4 unit pixel, the 4x4 unit pixel has nine floating diffusion nodes with nine signal input modules, such as a 3x3 signal input module shown in FIG. 18. A signal input module may include four photodiodes, photodiodes with the same color filters in the nine signal input modules form a unit pixel. The nine signal input modules with the nine floating diffusion nodes are connected to Vout1 to Vout9 lines, respectively. When conversion modules between the nine signal input modules are working in a binning mode, the Vout1 to Vout9 may be read out by the same ADC. When conversion modules between the nine signal input modules are working in a non-binning mode, the Vout1 to Vout9 may be read out by nine different ADCs. A circuit diagram and a timing diagram of control signals may be obtained by analogy with the description above.

[0132] FIG. 19 is a schematic diagram of a connection mode of multiple signal input modules according to a fifth implementation of the present application. Photodiodes with different color filters are arranged in a 4x4 quad Bayer unit pixel, the 4x4 quad Bayer unit pixel has six floating diffusion nodes with six signal input modules, such as a 2x3 signal input module shown in FIG. 19. For example, a 4x4 quad Bayer unit pixel includes a set of 2x2 photodiodes with red filters, a set of 2x2 photodiodes with blue filters and two sets of 2x2 photodiodes with green filters. A circuit diagram and a timing diagram of control signals may be obtained by analogy with the description above.

[0133] FIG. 20 is a schematic diagram of a connection mode of multiple signal input modules according to a sixth implementation of the present application. Photodiodes with different color filters are arranged in a 4x4 quad Bayer unit pixel, the 4x4 quad Bayer unit pixel has nine floating diffusion nodes with nine signal input modules, such as a 3x3 signal input module shown in FIG. 20. For example, the 4x4 quad Bayer unit pixel includes a set of 2x2

photodiodes with red filters, a set of 2x2 photodiodes with blue filters and two sets of 2x2 photodiodes with green filters. A circuit diagram and a timing diagram of control signals may be obtained by analogy with the description above.

[0134] FIG. 21 is a schematic diagram of a connection mode of multiple signal input modules according to a seventh implementation of the present application. Photodiodes with different color filters are arranged in a 6x6 quad Bayer unit pixel, the 6x6 quad Bayer unit pixel has twelve floating diffusion nodes with twelve signal input modules, such as a 3x4 signal input module shown in FIG. 21. For example, the 6x6 quad Bayer unit pixel includes four sets of 2x2 photodiodes with red filters, four sets of 2x2 photodiodes with green filters and one set of 2x2 photodiodes with blue filters. A circuit diagram and a timing diagram of control signals may be obtained by analogy with the description above.

[0135] FIG. 22 is a schematic diagram of a connection mode of multiple signal input modules according to an eighth implementation of the present application. Photodiodes with different color filters are arranged in a 6x6 quad Bayer unit pixel, the 6x6 quad Bayer unit pixel has sixteen floating diffusion nodes with sixteen signal input modules, such as a 4x4 signal input module shown in FIG. 22. For example, the 6x6 quad Bayer unit pixel includes four sets of 2x2 photodiodes with red filters, four sets of 2x2 photodiodes with green filters and one set of 2x2 photodiodes with blue filters. A circuit diagram and a timing diagram of control signals may be obtained by analogy with the description above.

[0136] FIG. 23 is a schematic architecture diagram of a signal input module according to an embodiment of the present application. A signal input module includes four photodiodes in a 2x2 architecture. A RST resistor, a TCG resistor, a DCG resistor and two AVDDs in a conversion module and a SEL resistor, an AMP resistor and an AVSS1 in a signal output module are shown in FIG. 23. A schematic architecture diagram of multiple signal input modules can be shown in FIG. 24.

[0137] FIG. 25 is a schematic diagram of a signal input module according to an embodiment of the present application. FIG. 25 shows a cross-section of two N-type photodiodes and corresponding TX transistors. The embodiments of the present application do not specify whether the imaging device is a backside illuminated imaging device or a frontside illuminated imaging device, and the backside illuminated imaging device is shown in FIG. 25. Optionally,

its deep trench isolation DTI depth may be less than, equal to or greater than the radiation sensitive depth.

[0138] A base substrate may include a semiconductor material such as silicon or germanium. In some embodiments, the substrate may include at least one or more of other photosensitive materials, such as silicon germanium, silicon carbide, gallium arsenide, gallium phosphide, indium gallium arsenide, indium phosphide, indium arsenide, indium antimonide, semiconductor on insulator or combinations thereof.

[0139] Optionally, each of the plurality of unit pixels in the pixel array may include a red color filter, a blue color filter, a green color filter, a yellow color filter, a cyan color filter, a magenta color filter, a white color filter, or an infrared color filter.

[0140] Optionally, a TX transistor has an embedded portion in a substrate.

[0141] Optionally, device isolation may be achieved by shallow trench isolation (STI), or doping isolation.

[0142] Optionally, a signal is obtained by carrying out a correlating double sampling (CDS) using a difference between a reset level and a signal level, in order to reduce fixed pattern noise and reset noise.

[0143] Optionally, charge voltage conversion is done by an amplifier device using a source follower operation with a gain equal to or less than unity, and in some embodiments, the charge voltage conversion is done by the amplifier device with the gain greater than the unity, where a differential amplification mode can be adopted, for instance.

[0144] Optionally, PD is made by n-type doping and pixel to pixel isolation is made by p-type doping, and in some embodiments, PD is made by the p-type doping and pixel to pixel isolation is made by the n-type doping.

[0145] FIG. 26 illustrates some schematic diagrams of possible image devices according to embodiments of the present application. Firstly, a possible solid-state imaging device is described with reference to a diagram A in FIG. 26. The solid-state image device includes a pixel array, a control circuit, and a logic circuit for signal processing, and all of which are mounted on a single semiconductor chip. In general, an image sensor includes the pixel array and the control circuit. The pixel array may be frontside illuminations, or may be backside illuminations. The semiconductor substrate may be bulk or a semiconductor on an insulator.

[0146] As shown in a diagram B in FIG. 26, a solid-state image device according to the embodiments of the present application includes a pixel array, a control circuit (a control region) mounted on a first semiconductor chip section and a logic circuit including a signal processing circuit for signal processing mounted on a second semiconductor chip section. The first semiconductor chip section and the second semiconductor chip section are electrically connected to each other, and can form a single semiconductor chip to be provided to the imaging device.

[0147] As shown in a diagram C in FIG. 26, a pixel array is mounted on a first semiconductor chip section. Further, a control circuit and a logic circuit including signal processing circuit are mounted on a second semiconductor chip section. The first semiconductor chip section and the second semiconductor chip section are electrically connected to each other, and can form a single semiconductor chip to be provided to the imaging device.

[0148] As shown in a diagram D in FIG. 26, a pixel array is mounted on a first semiconductor chip section. Also, a memory circuit is mounted on a second semiconductor chip section. Then, a control circuit and a logic circuit including signal processing circuit are mounted on a third semiconductor chip section. The first semiconductor chip section, the second semiconductor chip section and the third semiconductor chip section are electrically connected and can form a single semiconductor chip or two semiconductor chips to be provided to the solid-state imaging device.

[0149] As shown in a diagram E in FIG. 26, a pixel array is mounted on a first semiconductor chip section. Also, a pixel circuit is mounted on a second semiconductor chip section. Then, a control circuit and a logic circuit including signal processing circuit are mounted on a third semiconductor chip section. The first semiconductor chip section, the second semiconductor chip section and the third semiconductor chip section are electrically connected and can form a single semiconductor chip or two semiconductor chips to be provided to the solid-state imaging device.

[0150] An embodiment of the present application further provides an electronic device. The electronic device includes the above imaging device. The electronic device may be a smartphone, a tablet, a smart-watch, a television or the like.

[0151] An embodiment of the present application further provides an imaging system. The

imaging system includes the above imaging device. FIGS. 27-29 illustrate some schematic diagrams of possible imaging systems according to embodiments of the present application. As shown in FIG. 27, an imaging system is an electronic device exemplified by an imaging device such as a digital still camera or a video camera, or a portable terminal device such as a smartphone or a tablet terminal. The imaging system includes, for example, the above imaging device, a signal processing circuit, a monitor unit, a memory unit, and a control circuit unit, according to the above embodiments and modifications thereof. The signal processing circuit may be configured to process imaging data, the memory may be configured to store the imaging data, and the monitor may be configured to monitor an operating status of the signal processing circuit. As shown in FIG. 28, an imaging device may be applied to a variety of wide fields including sport gear such as a wearable camera, medical devices such as an endoscope, a cosmetic equipment, vehicles or transport equipment such as a truck, entertainment devices such as a mobile phone, a game console, a digital camera, and a video camcorder, the agricultural field such as a farmland surveillance camera, home appliances such as a television and a refrigerator, and the security field such as a monitoring camera, a network camera, and a machine vision camera. As shown in FIG. 29, an imaging device may be applied to a vehicle control system.

[0152] It may be clearly understood by a person skilled in the art that, for the purpose of convenient and brief description, for a detailed working process of the foregoing system, apparatus, and unit, refer to a corresponding process in the foregoing method embodiment. Details are not described herein again.

[0153] In the several embodiments provided in the present application, it should be understood that the disclosed system, apparatus, and method may be implemented in other manners. For example, the described apparatus embodiment is merely an example. For example, the unit division is merely logical function division and may be other division in actual implementation. For example, a plurality of units or components may be combined or integrated into another system, or some features may be ignored or not performed. In addition, the displayed or discussed mutual couplings or direct couplings or communication connections may be implemented through some interfaces. The indirect couplings or communication connections between the apparatuses or units may be implemented in electronic, mechanical, or other forms.

[0154] The units described as separate parts may be or may not be physically separate, and parts displayed as units may be or may not be physical units, may be located in one position, or may be distributed on a plurality of network units. Some or all of the units may be selected based on actual requirements to achieve the objectives of the solutions of the embodiments.

[0155] In addition, functional units in the embodiments of the present application may be integrated into one processing unit, or each of the units may exist alone physically, or two or more units are integrated into one unit.

[0156] The foregoing descriptions are merely specific implementations of the present application, but are not intended to limit the protection scope of the present application. Any variation or replacement readily figured out by a person skilled in the art within the technical scope disclosed in the present application shall fall within the protection scope of the present application. Therefore, the protection scope of the present application shall be subject to the protection scope of the claims.

CLAIMS

What is claimed is:

1. An imaging device, comprising N signal input modules, N signal output modules, a conversion module, and a data processing module, wherein N terminals of the N signal input modules are electrically connected to N first terminals of the N signal output modules through N floating diffusion nodes, respectively, the conversion module is coupled to the N floating diffusion nodes, N second terminals of the N signal output modules are electrically connected to the data processing module, and N is an integer greater than 2, wherein

the N signal input modules are configured to generate electrical charges by sensing an image;

the conversion module is configured to control whether the N floating diffusion nodes are electrically connected;

the N signal output modules are configured to amplify the electrical charges in the N floating diffusion nodes, respectively; and

the data processing module is configured to obtain imaging data of the image based on the amplified electrical charges.

2. The imaging device according to claim 1, wherein the data processing module comprises at least N analog to digital converters, wherein

when the conversion module is configured to control the N floating diffusion nodes to be connected, one analog to digital converter among the at least N analog to digital converters is configured to obtain the imaging data based on the amplified electrical charges; and

when the conversion module is configured to control the N floating diffusion nodes to be electrically disconnected, the N analog to digital converters are configured to obtain the imaging data based on the amplified electrical charges.

3. The imaging device according to claim 2, wherein the data processing module comprises a first set of switches and a second set of switches, wherein

when the first set of switches is turned on and the second set of switches is turned off, the one analog to digital converter among the at least N analog to digital converters is configured

to obtain the imaging data based on the amplified electrical charges; and

when the first set of switches is turned off and the second set of switches is turned on, the N analog to digital converters are configured to obtain the imaging data based on the amplified electrical charges.

4. The imaging device according to claim 2 or 3, wherein each of the N analog to digital converters comprises a signal input port and a reference input port, the signal input port and the reference input port each comprises N terminals, wherein N terminals of the signal input port are configured to be electrically connected to at least one of the N second terminals of the N signal output modules through N first capacitors, respectively, and N terminals of the reference input port are configured to be electrically connected to a reference node through N second capacitors, respectively.

5. The imaging device according to any one of claims 1 to 4, wherein the conversion module comprises N dual conversion gain switches, and at least N-1 tunable conversion gain switches, wherein N first terminals of the N dual conversion gain switches are configured to be connected to the N floating diffusion nodes, respectively, and the at least N-1 tunable conversion gain switches are configured to control whether N second terminals of the N dual conversion gain switches are electrically connected, wherein

when the N dual conversion gain switches are turned on and the at least N-1 tunable conversion gain switches are turned on, the N floating diffusion nodes are electrically connected; and

when the N dual conversion gain switches and/or the at least N-1 tunable conversion gain switches are turned off, the N floating diffusion nodes are electrically disconnected.

6. The imaging device according to claim 5, wherein when the conversion module is configured to control the N floating diffusion nodes to be disconnected, the N dual conversion gain switches are turned on.

7. The imaging device according to any one of claims 1 to 4, wherein the conversion module comprises at least N-1 tunable conversion gain switches, and the at least N-1 tunable conversion gain switches are configured to control whether the N floating diffusion nodes are electrically connected.

8. The imaging device according to any one of claims 1 to 7, wherein the each of the N

signal input modules comprises at least two photoelectric conversion units, and each of the at least two photoelectric conversion units is connected to the corresponding floating diffusion node through a transmission transistor.

9. The imaging device according to claim 8, wherein the transmission transistors connected to the photoelectric conversion units with same color filters in the N signal input modules are turned on at the same time.

10. The imaging device according to claim 8 or 9, wherein at least one signal input module among the N signal input modules comprises at least two photoelectric conversion units with different color filters.

11. A method for driving an imaging device, wherein the imaging device comprises N signal input modules, N signal output modules, a conversion module, and a data processing module, wherein N terminals of the N signal input modules are electrically connected to N first terminals of the N signal output modules through N floating diffusion nodes, respectively, the conversion module is coupled to the N floating diffusion nodes, N second terminals of the N signal output modules are electrically connected to the data processing module, and N is an integer greater than 2, wherein

generating, by the N signal input modules, electrical charges by sensing an image;

controlling, by the conversion module, whether the N floating diffusion nodes are electrically connected;

amplifying, by the N signal output modules, the electrical charges in the N floating diffusion nodes, respectively; and

obtaining, by the data processing module, imaging data of the image based on the amplified electrical charges.

12. An electronic device, comprising an imaging device according to any one of claims 1 to 10.

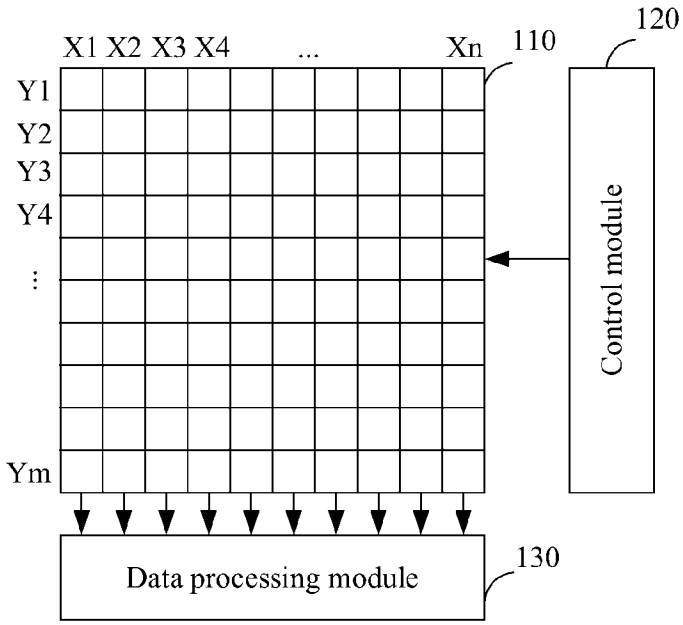
X1 X2 X3 X4 ... Xn
110
120
Y1
Y2
Y3
Y4
Ym
Control module
Data processing module
130

FIG. 1

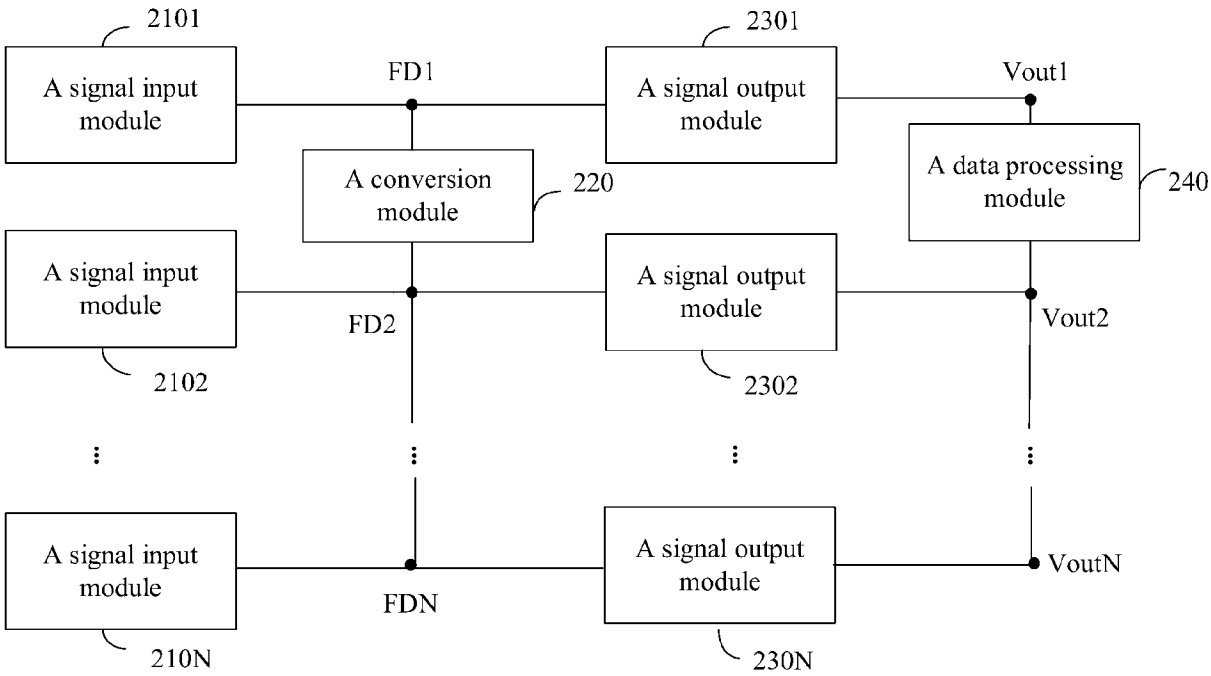
2101
A signal input module
FD1
2301
A signal output module
Vout1
A conversion module
220
A data processing module
240
A signal input module
2102
FD2
A signal output module
2302
Vout2
A signal input module
210N
FDN
A signal output module
230N
VoutN

FIG. 2

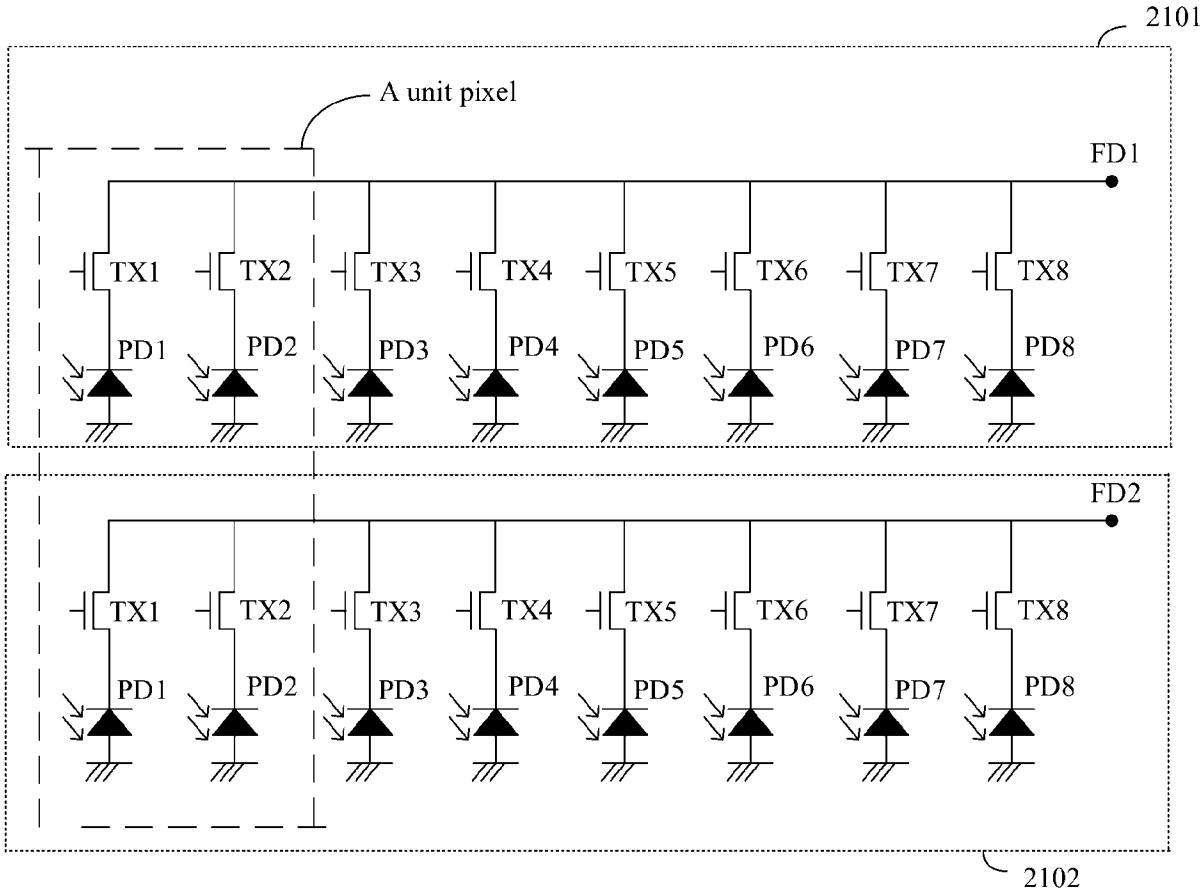
2101
A unit pixel
FD1
TX1
TX2
TX3
TX4
TX5
TX6
TX7
TX8
PD1
PD2
PD3
PD4
PD5
PD6
PD7
PD8
FD2
TX1
TX2
TX3
TX4
TX5
TX6
TX7
TX8
PD1
PD2
PD3
PD4
PD5
PD6
PD7
PD8
2102

FIG. 3

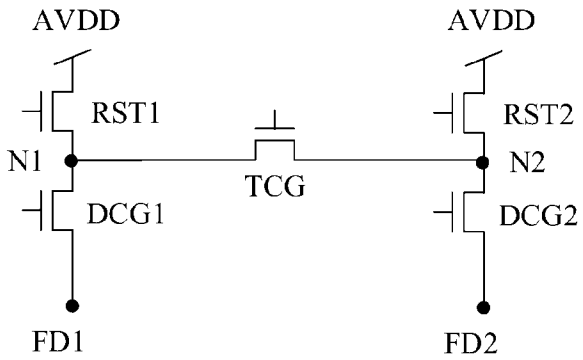
AVDD
AVDD
RST1
RST2
N1
N2
TCG
DCG1
DCG2
FD1
FD2

FIG. 4

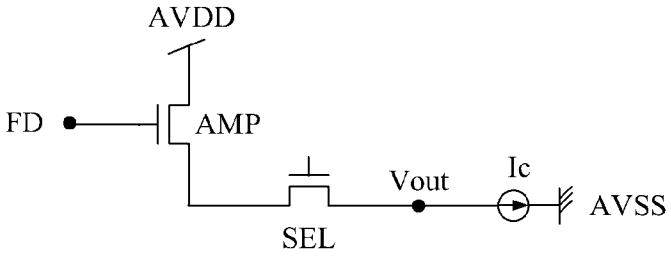
AVDD
FD
AMP
Vout
Ic
AVSS
SEL

FIG. 5

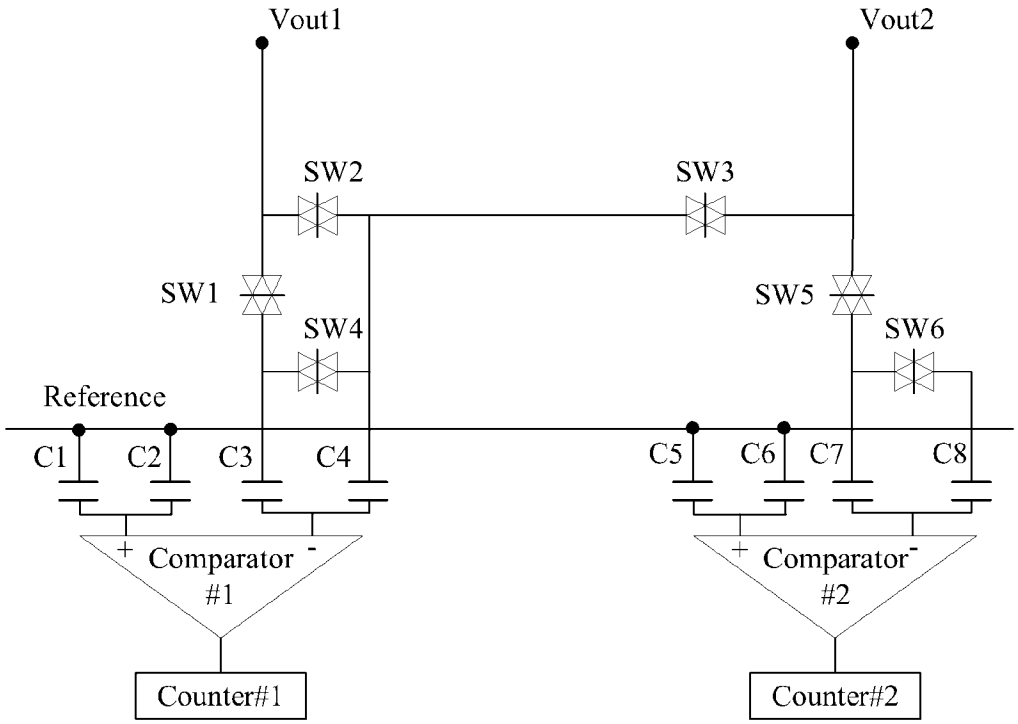
Vout1
Vout2
SW2
SW3
SW1
SW5
SW4
SW6
Reference
C1
C2
C3
C4
C5
C6
C7
C8
+
Comparator
-
#1
+
Comparator
-
#2
Counter#1
Counter#2

FIG. 6

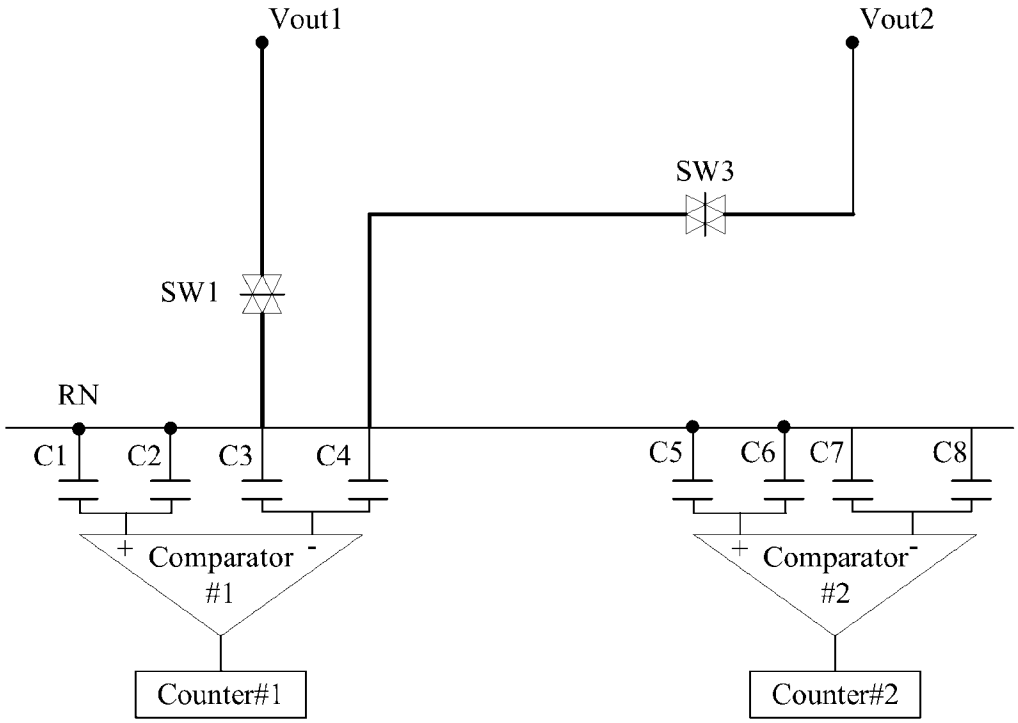
Vout1
Vout2
SW3
SW1
RN
C1
C2
C3
C4
C5
C6
C7
C8
+
Comparator
-
#1
+
Comparator
-
#2
Counter#1
Counter#2

FIG. 7

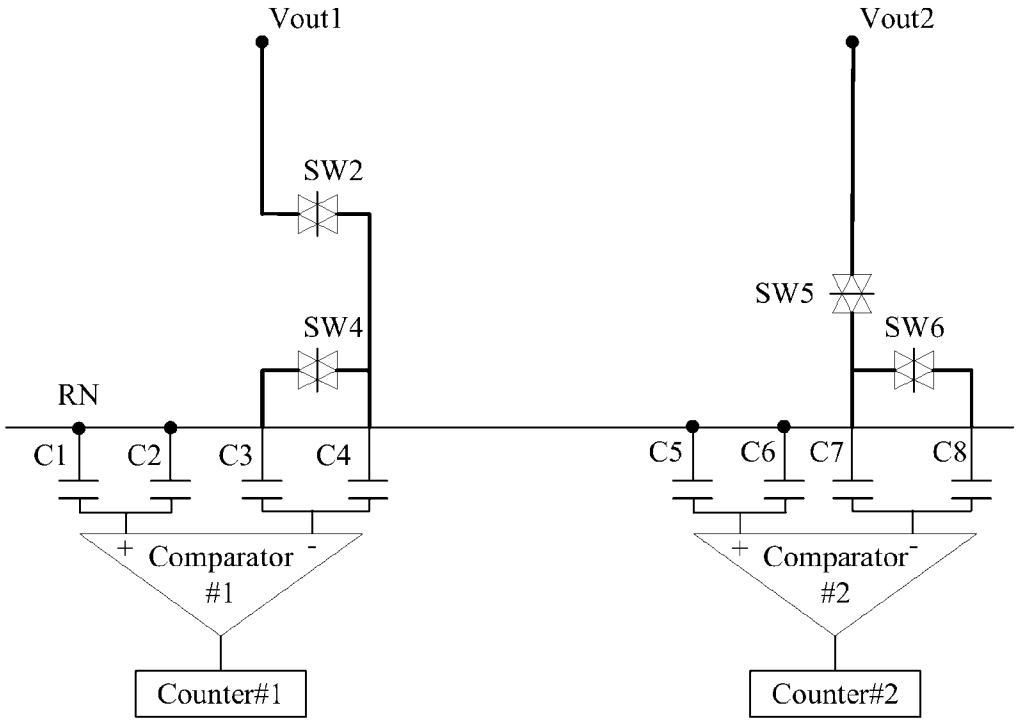
Vout1
Vout2
SW2
SW5
SW4
SW6
RN
C1
C2
C3
C4
C5
C6
C7
C8
+
Comparator
-
#1
+
Comparator
-
#2
Counter#1
Counter#2

FIG. 8

Working in a binning mode

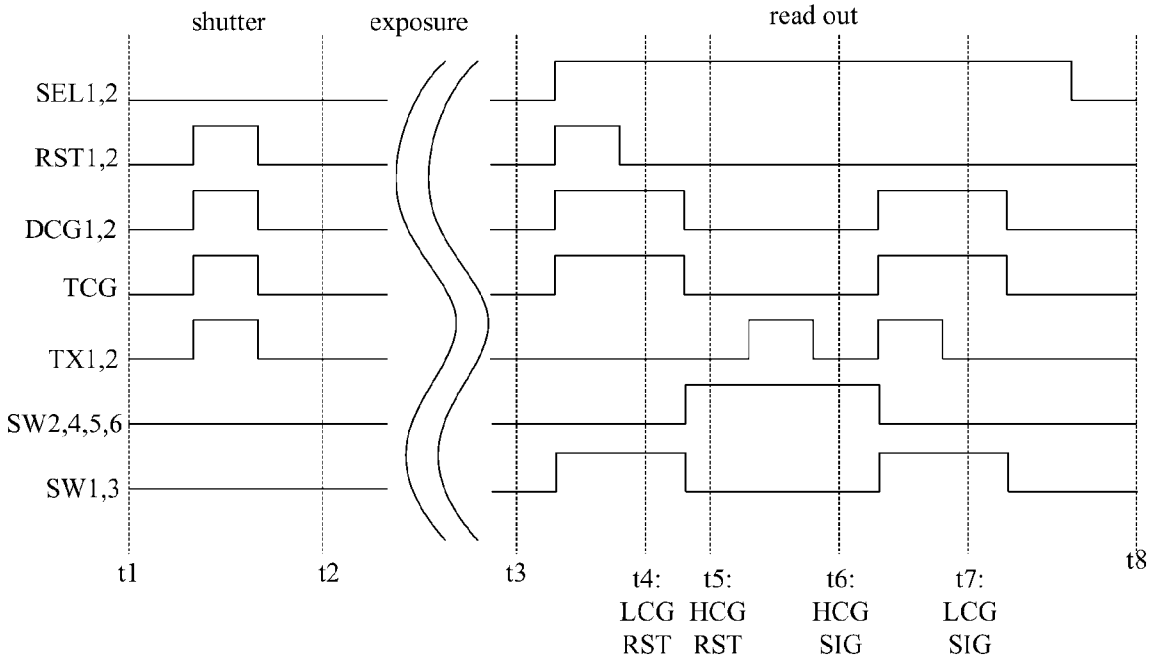

FIG. 9

Working in a non-binning mode

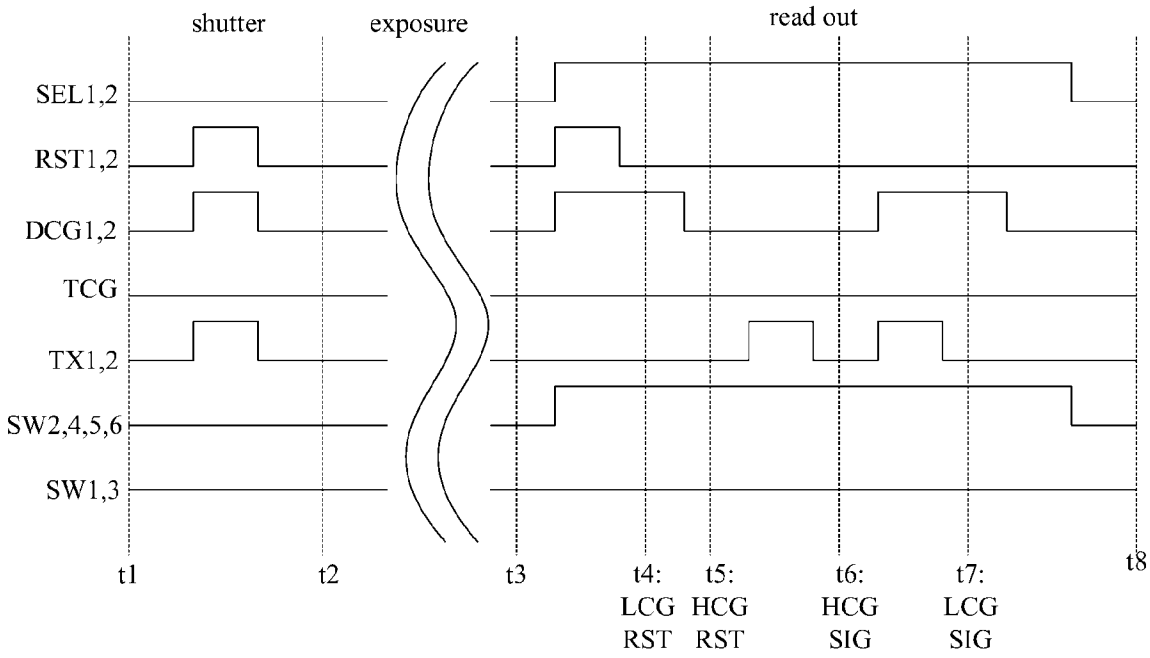

FIG. 10

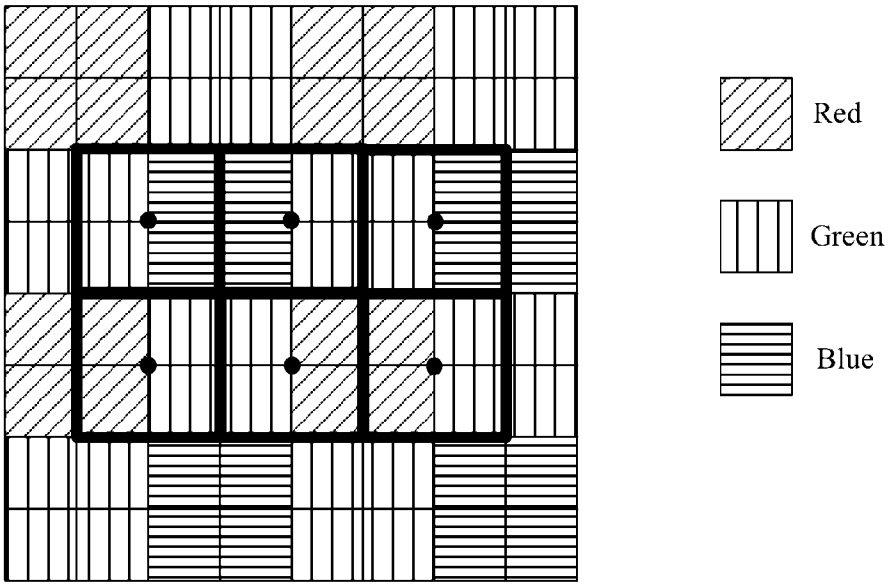

FIG. 11

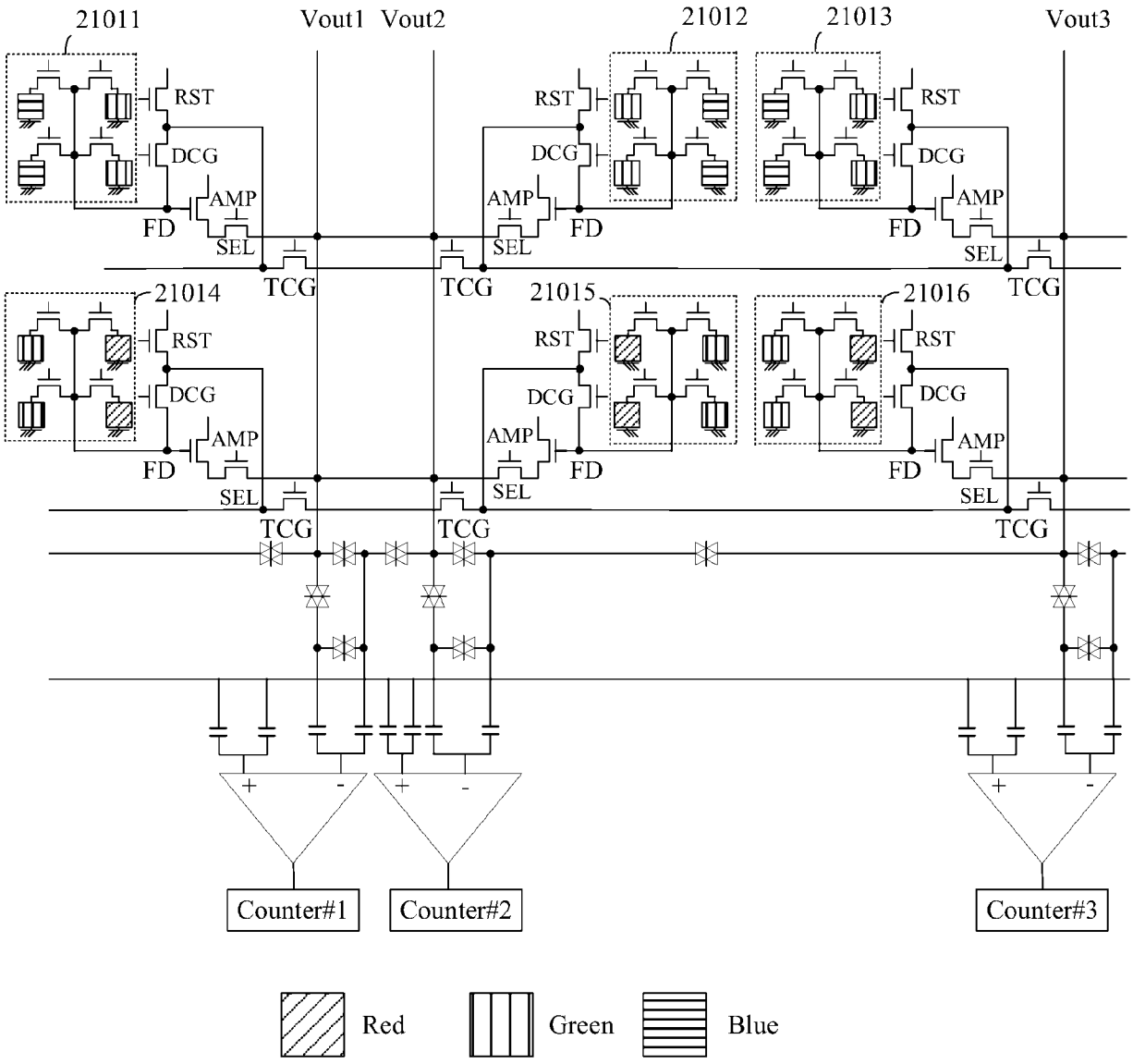
21011
Vout1
Vout2
21012
21013
Vout3
RST
DCG
AMP
FD
SEL
TCG
21014
21015
21016
Counter#1
Counter#2
Counter#3
Red
Green
Blue

FIG. 12

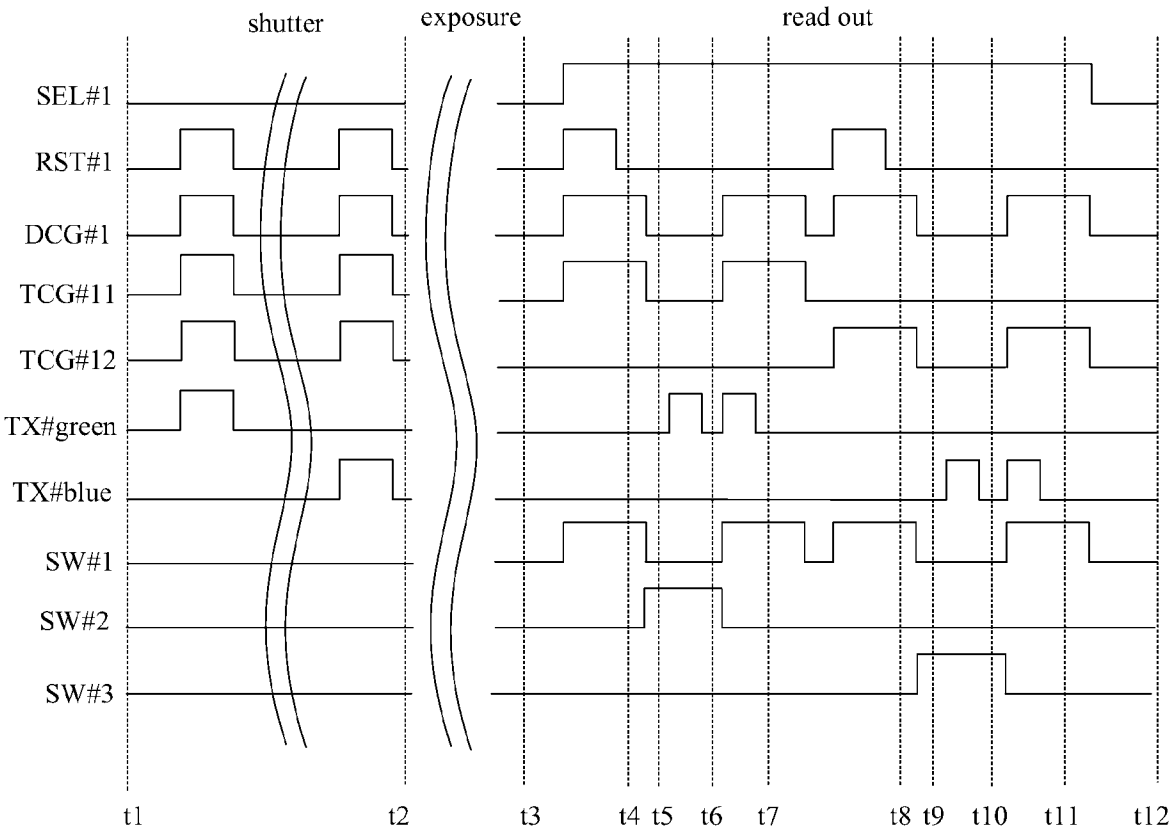
shutter
exposure
read out
SEL#1
RST#1
DCG#1
TCG#11
TCG#12
TX#green
TX#blue
SW#1
SW#2
SW#3
t1
t2
t3
t4
t5
t6
t7
t8
t9
t10
t11
t12

FIG. 13

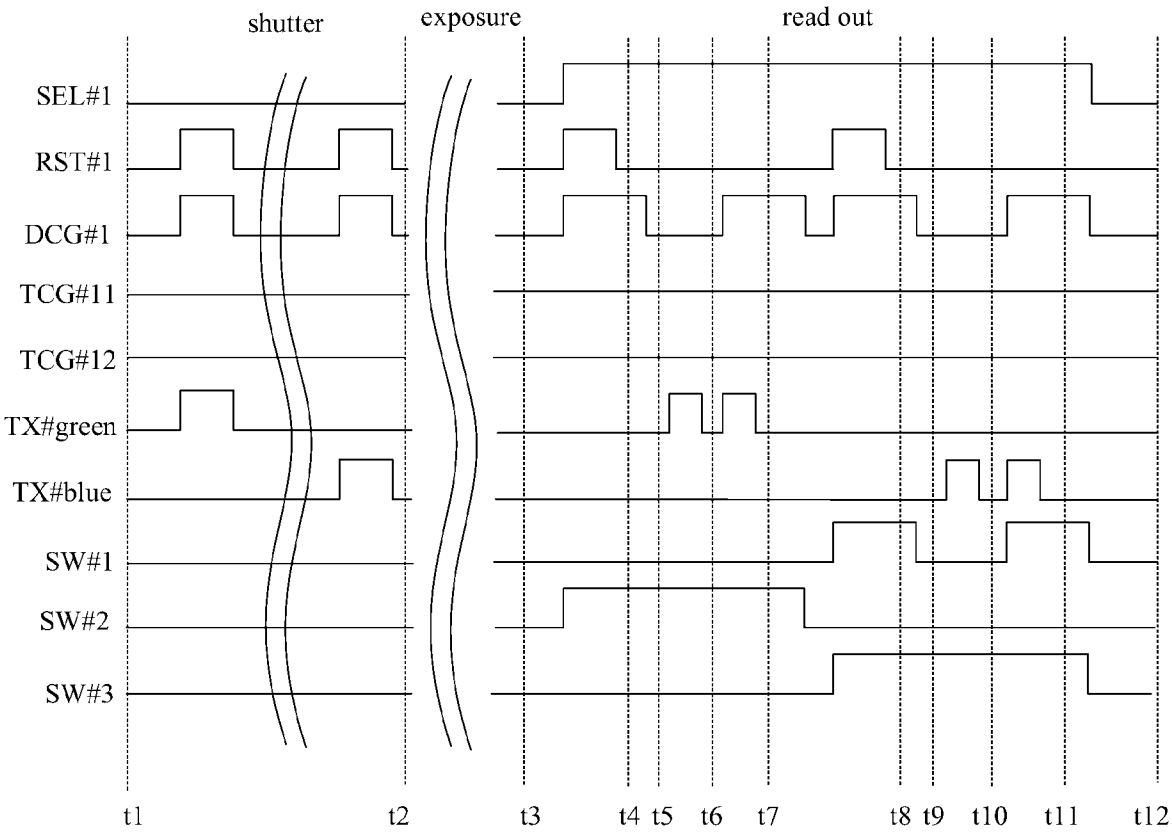
shutter
exposure
read out
SEL#1
RST#1
DCG#1
TCG#11
TCG#12
TX#green
TX#blue
SW#1
SW#2
SW#3
t1
t2
t3
t4
t5
t6
t7
t8
t9
t10
t11
t12

FIG. 14

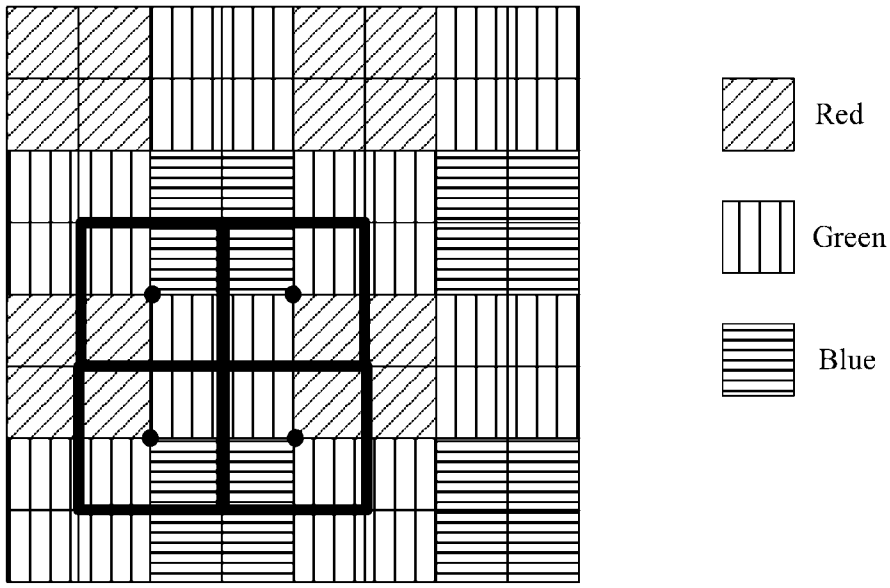
Red
Green
Blue

FIG. 15

FIG.16

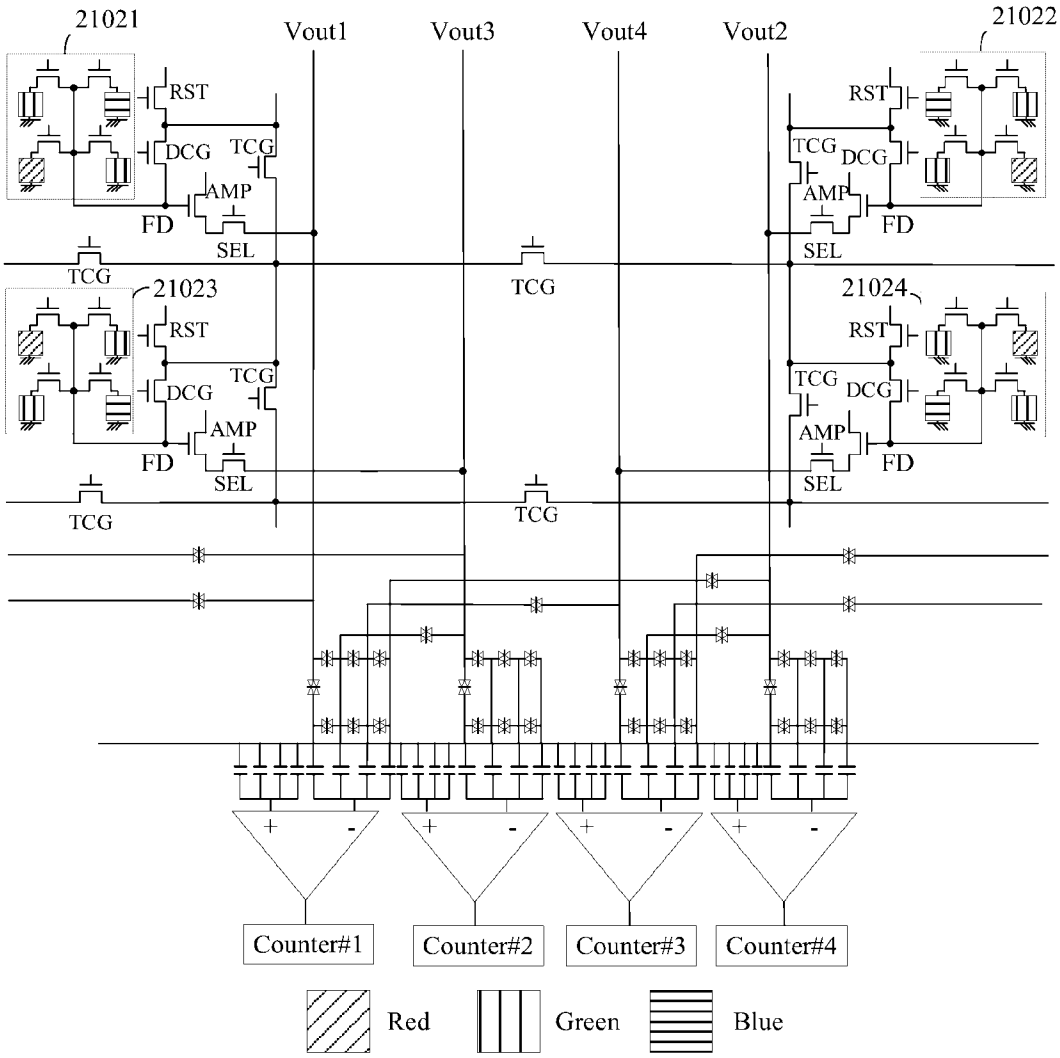
21021
Vout1
Vout3
Vout4
Vout2
21022
RST
DCG
TCG
AMP
FD
SEL
TCG
21023
21024
Counter#1
Counter#2
Counter#3
Counter#4
Red
Green
Blue

FIG. 16

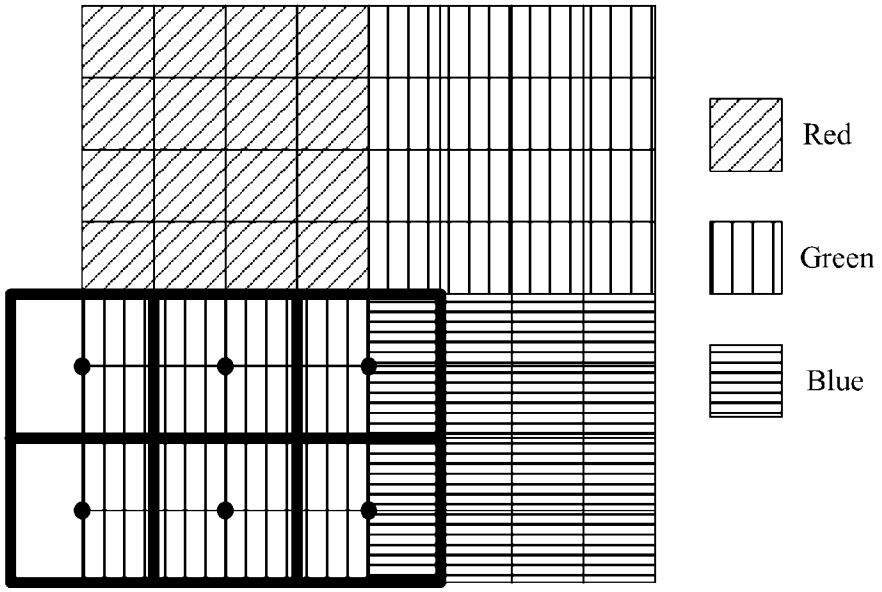

FIG. 17

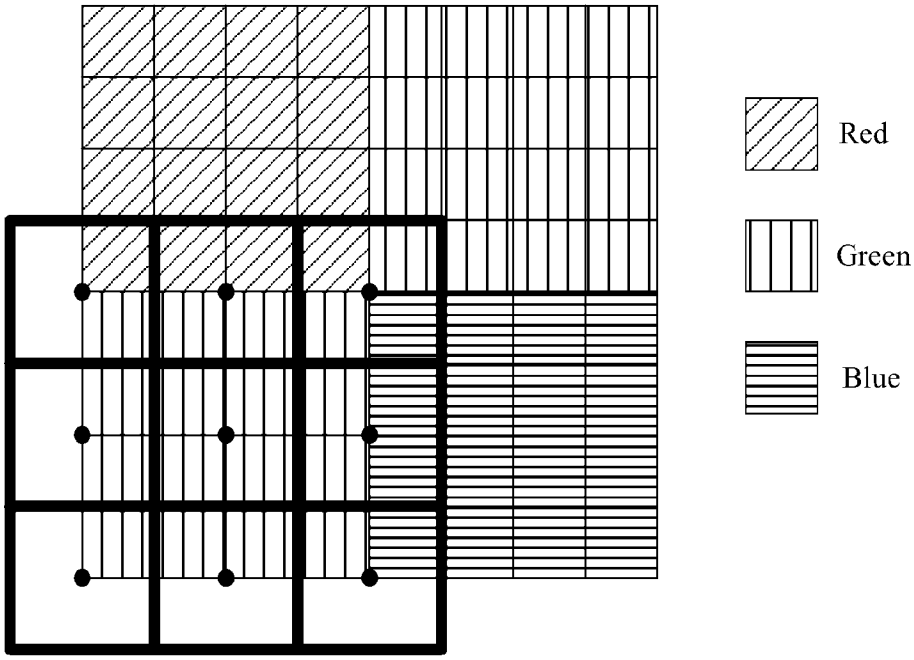

FIG. 18

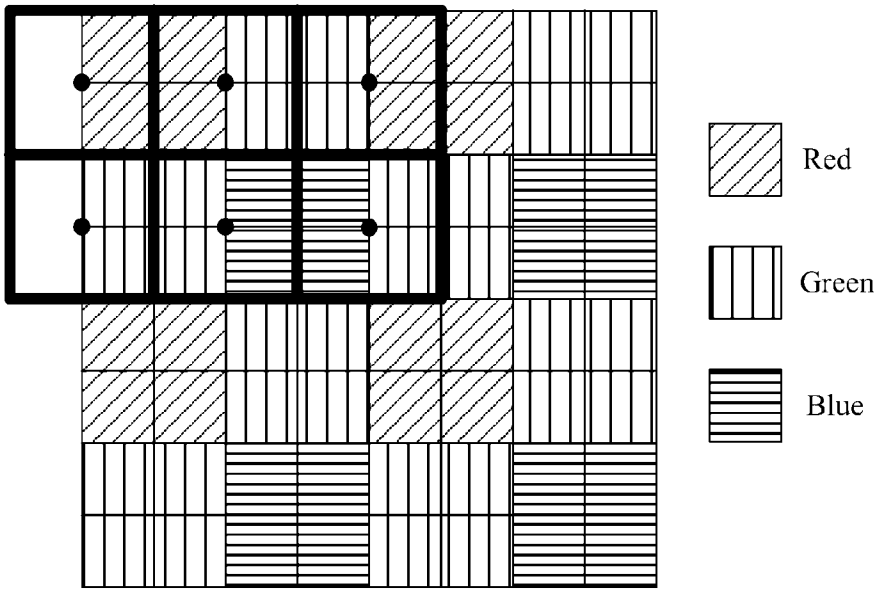

FIG. 19

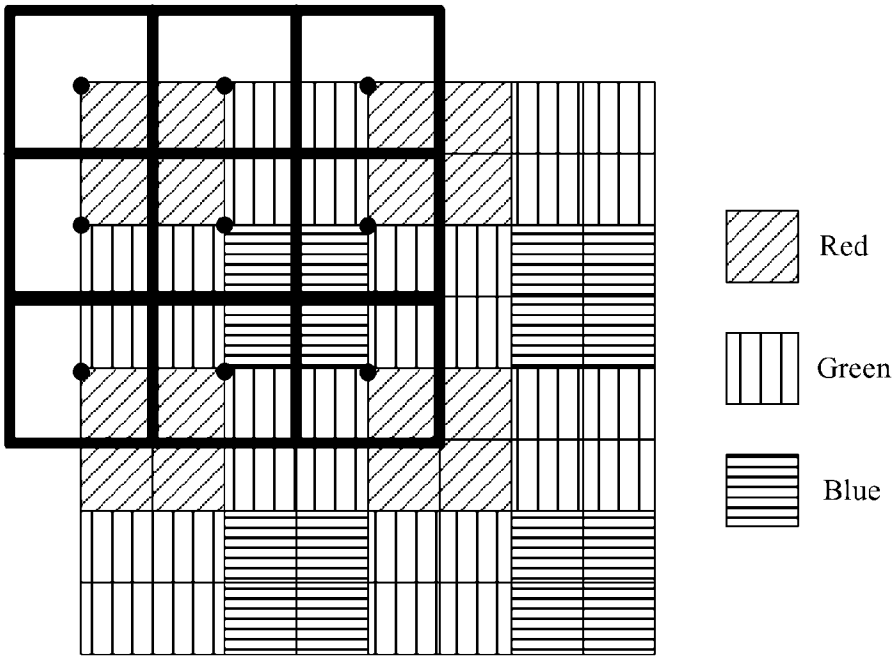

FIG. 20

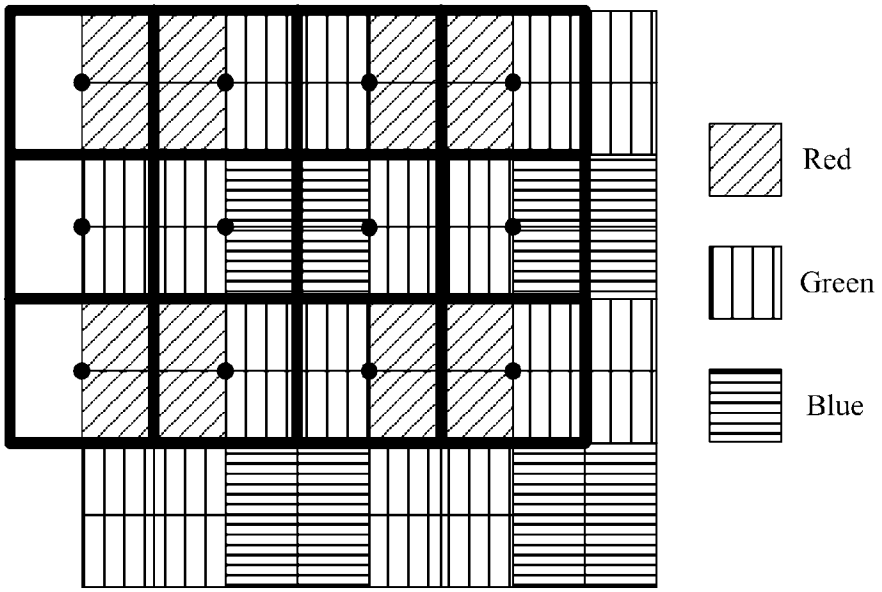

FIG. 21

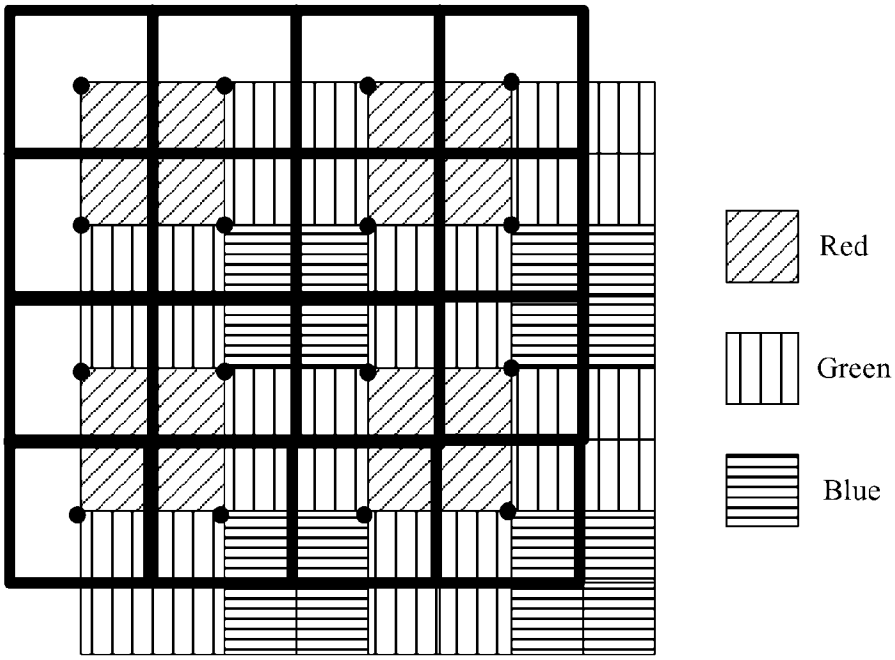

FIG. 22

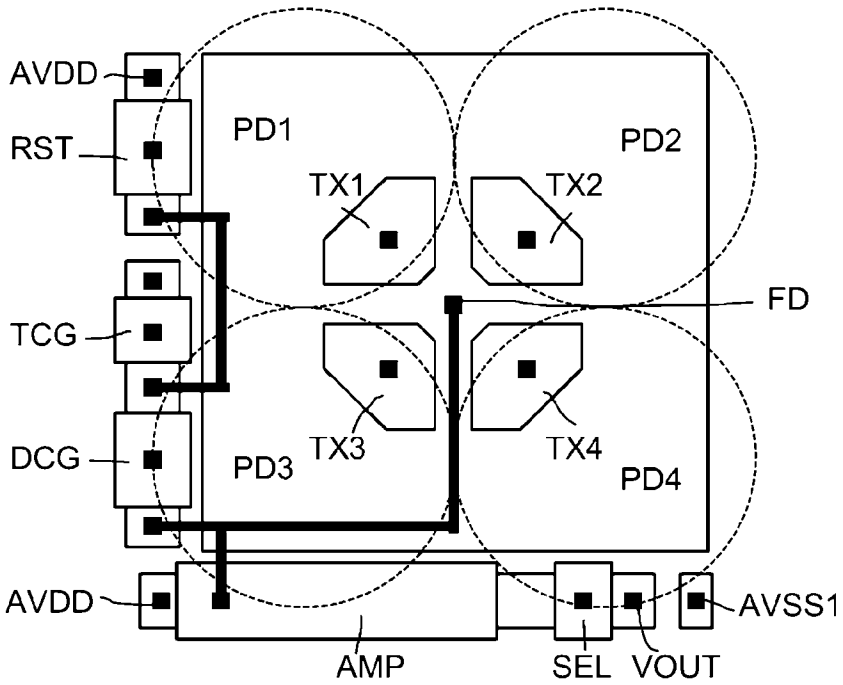
AVDD
RST
TCG
DCG
AVDD
PD1
PD2
PD3
PD4
TX1
TX2
TX3
TX4
FD
AMP
SEL
VOUT
AVSS1

FIG. 23

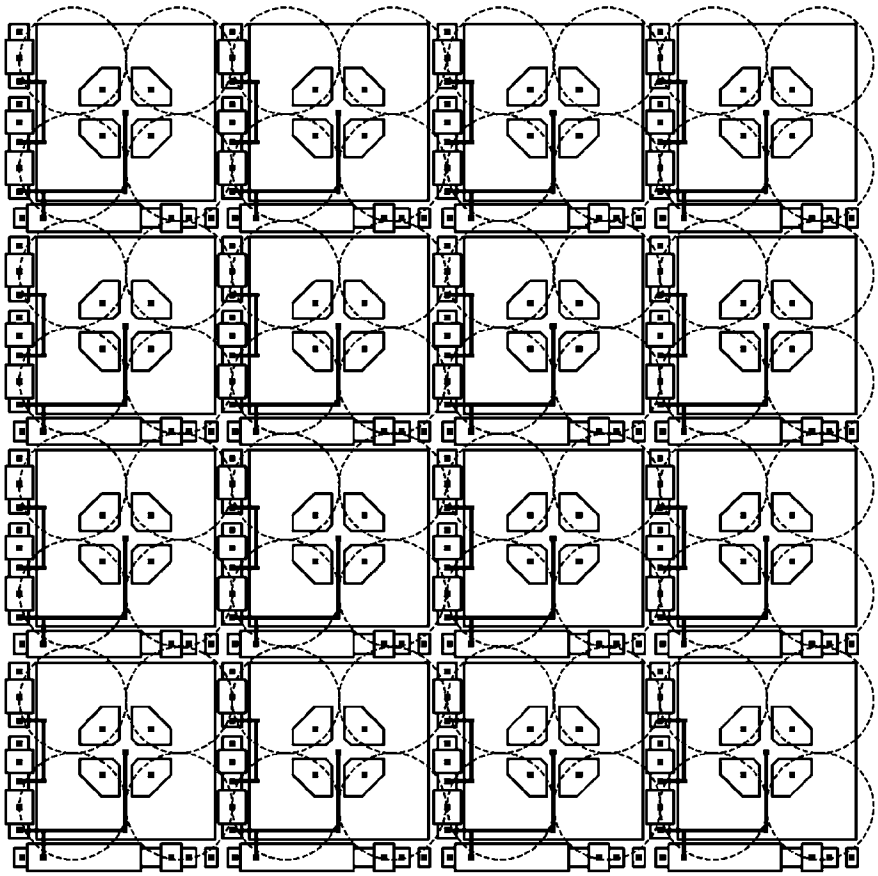

FIG. 24

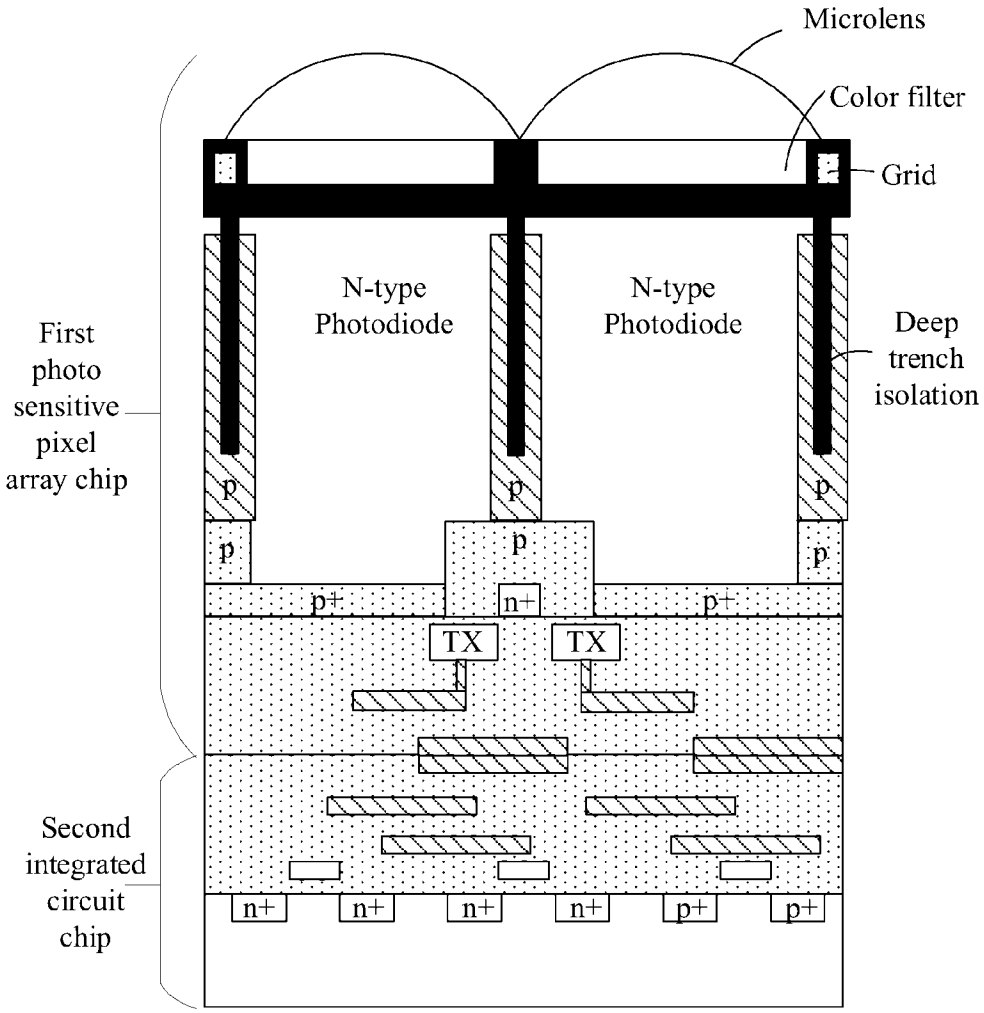
Microlens
Color filter
Grid
N-type Photodiode
N-type Photodiode
Deep trench isolation
First photo sensitive pixel array chip
Second integrated circuit chip
p
p+
n+
TX
TX

FIG. 25

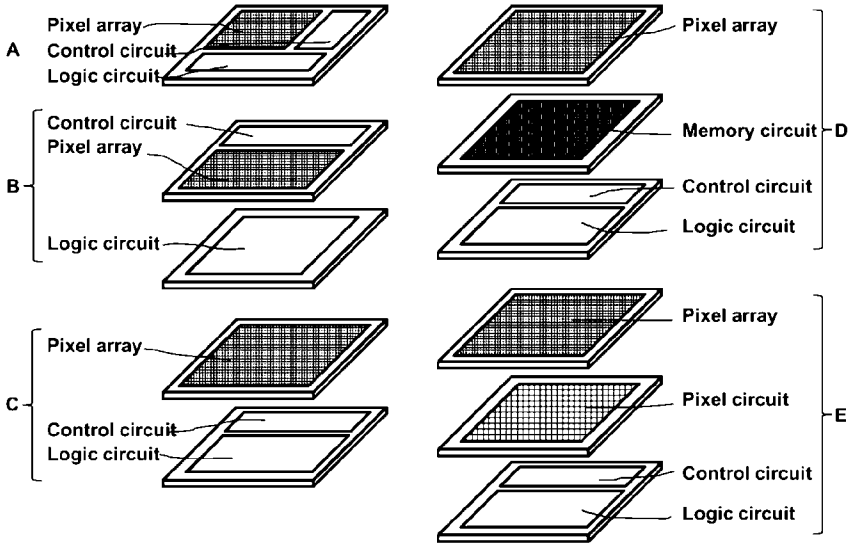
A
Pixel array
Control circuit
Logic circuit
B
Control circuit
Pixel array
Logic circuit
C
Pixel array
Control circuit
Logic circuit
Pixel array
Memory circuit
Control circuit
Logic circuit
D
Pixel array
Pixel circuit
Control circuit
Logic circuit
E

FIG. 26

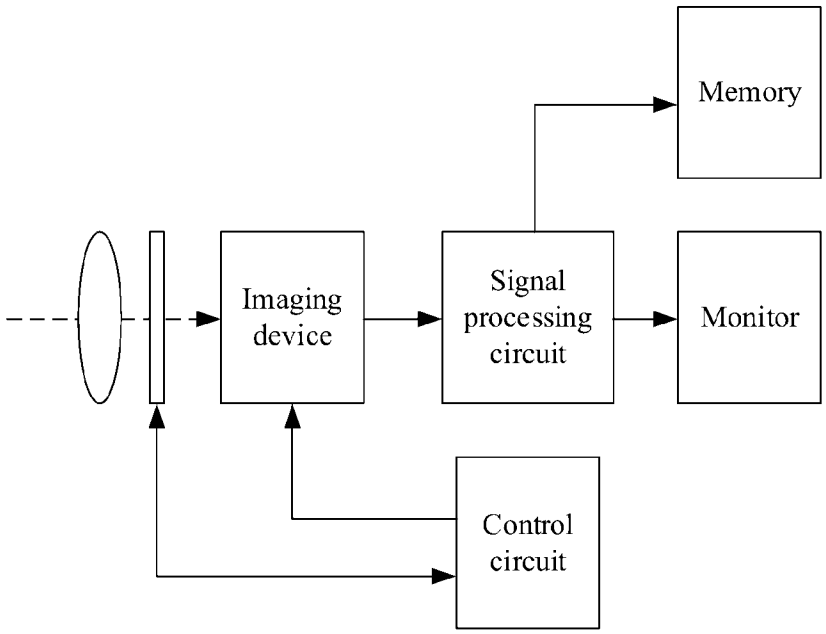
Memory
Imaging device
Signal processing circuit
Monitor
Control circuit

FIG. 27

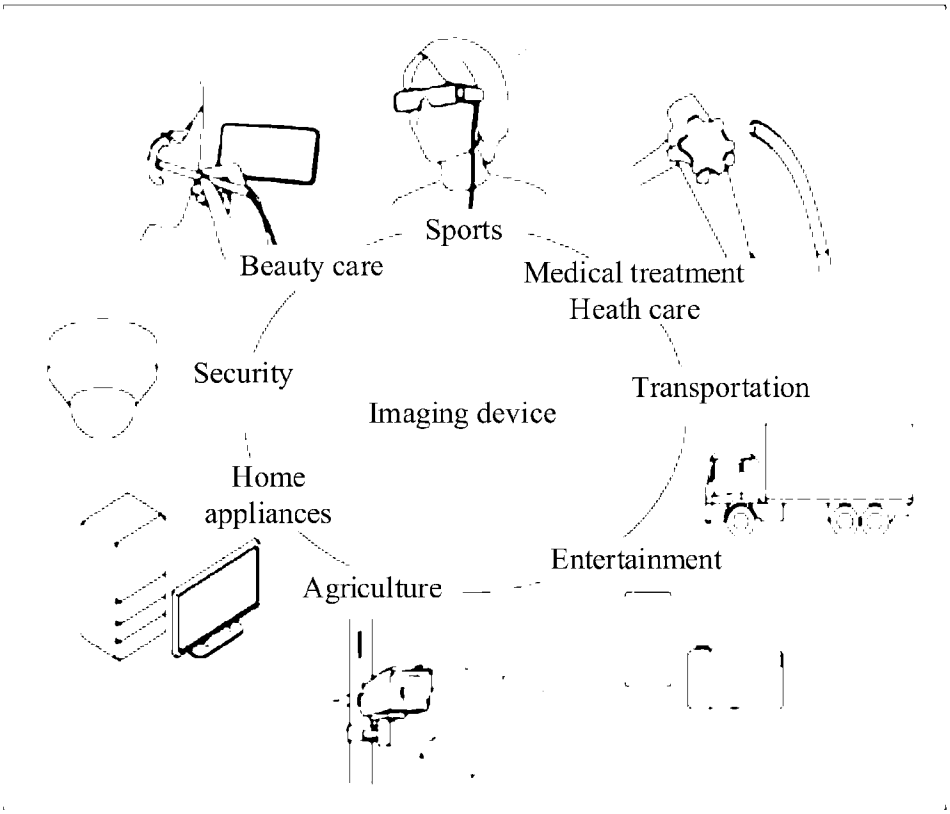
Sports
Beauty care
Medical treatment
Heath care
Security
Imaging device
Transportation
Home
appliances
Entertainment
Agriculture

FIG. 28

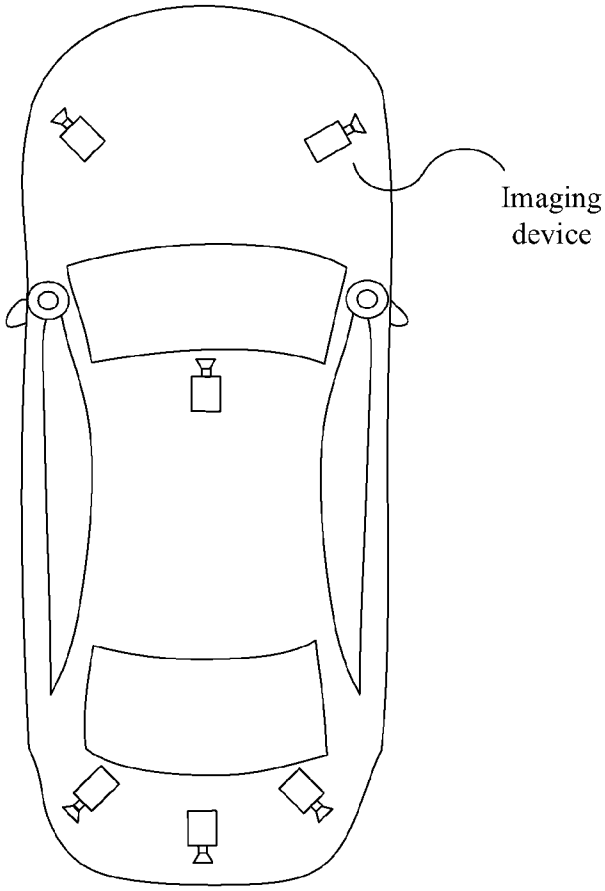

FIG. 29

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2023/078453

A. CLASSIFICATION OF SUBJECT MATTER

H04N 5/268(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNABS, CNTXT, CNKI, DWPI, VEN, USTXT, WOTXT, EPTXT: image, imaging, sensor, CCD, CMOS, FD, pixel, merge, array, group, floating, diffusion, conversion, amplify, charge, input, output

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CN 113707680 A (SK HYNIX INC.) 26 November 2021 (2021-11-26) the whole document	1-12
A	CN 113676625 A (OPPO GUANGDONG MOBILE TELECOMMUNICATION CO., LTD.) 19 November 2021 (2021-11-19) the whole document	1-12
A	CN 113242344 A (OPPO GUANGDONG MOBILE TELECOMMUNICATION CO., LTD.) 10 August 2021 (2021-08-10) the whole document	1-12
A	CN 103384999 A (PIXIM INC.) 06 November 2013 (2013-11-06) the whole document	1-12
A	CN 111885316 A (SHENZHEN AOCHEN PHOTOELECTRIC TECHNOLOGY CO., LTD.) 03 November 2020 (2020-11-03) the whole document	1-12
A	US 2022132068 A1 (CANON KK.) 28 April 2022 (2022-04-28) the whole document	1-12

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"D" document cited by the applicant in the international application
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 November 2023	**17 November 2023**
Name and mailing address of the ISA/CN **CHINA NATIONAL INTELLECTUAL PROPERTY ADMINISTRATION** **6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088, China**	Authorized officer **YANG,Hao** Telephone No. **(+86) 010-62411449**

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2023/078453

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
CN	113707680	A	26 November 2021	KR	20210144429	A	30 November 2021
				US	2021368127	A1	25 November 2021
				US	11330217	B2	10 May 2022
CN	113676625	A	19 November 2021		None		
CN	113242344	A	10 August 2021		None		
CN	103384999	A	06 November 2013	US	2013020466	A1	24 January 2013
				US	8847136	B2	30 September 2014
				US	2014368680	A1	18 December 2014
				US	10129487	B2	13 November 2018
				WO	2012092194	A1	05 July 2012
CN	111885316	A	03 November 2020		None		
US	2022132068	A1	28 April 2022	WO	2020045278	A1	05 March 2020
				US	11463644	B2	04 October 2022