United States Patent [19]

Ito et al.

[11] **3,825,684**

[45] **July 23, 1974**

[54] **VARIABLE MATRIX DECODER FOR USE IN 4-2-4 MATRIX PLAYBACK SYSTEM**

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[73] Assignee: **Sansui Electric Co., Ltd.,** Tokyo, Japan

[22] Filed: **Oct. 19, 1972**

[21] Appl. No.: **298,933**

[30] **Foreign Application Priority Data**

Oct. 25, 1971	Japan	46-84484
Oct. 30, 1971	Japan	46-86521
Nov. 4, 1971	Japan	46-87832
Nov. 10, 1971	Japan	46-89678
Dec. 29, 1971	Japan	46-2145
Mar. 23, 1972	Japan	47-29332
Apr. 17, 1972	Japan	47-38407

[52] **U.S. Cl. 179/1 GQ,** 179/100.4 ST, 179/100.1 TD

[51] **Int. Cl.** **H04r 5/00**

[58] **Field of Search** 179/1 GQ, 1 GP, 1 G, 100.4 ST, 179/100.1 TD, 15 BT

[56] **References Cited**

UNITED STATES PATENTS

3,786,193	1/1974	Tsurushima	179/1 GQ

Primary Examiner—Kathleen H. Claffy
Assistant Examiner—Thomas D'Amico
Attorney, Agent, or Firm—Harris, Kern, Wallen & Tinsley

[57] **ABSTRACT**

A decoder for use in a four channel playback system includes a control unit and a variable matrix. The control unit produces first and second control outputs which vary in opposite directions in accordance with the phase relationship between two channel signals. The variable matrix includes a first variable matrix circuit for producing two outputs related to the front channels and having matrix coefficients controlled by the first control output from the control unit and a second variable matrix circuit for producing two outputs related to the rear channels and having matrix coefficients controlled by the second control output from the control unit. The control outputs are used to improve the separation between front channels and to degrade the separation between rear channels, and vice versa, thereby enhancing the sense of presence of listeners in a reproduced sound field. The present invention discloses another decoder which comprises a first control unit for front-rear control and a second control unit for left-right control whereby front-left and right channels and rear-left and right channels are independently controlled.

34 Claims, 26 Drawing Figures

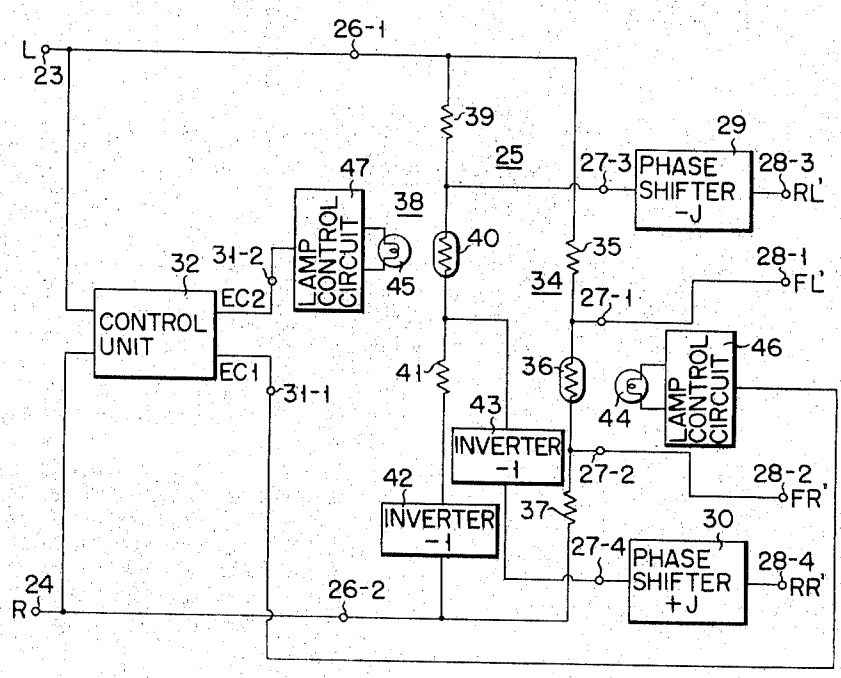


FIG. 1

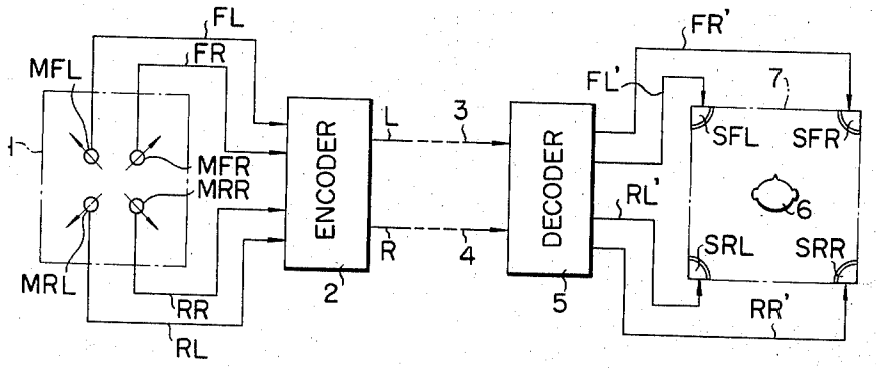

FL
FR
MFL
MFR
MRR
MRL
RR
RL
1
ENCODER
2
L
R
3
4
DECODER
5
FL'
FR'
RL'
RR'
7
SFL
SFR
SRL
SRR
6

FIG. 2

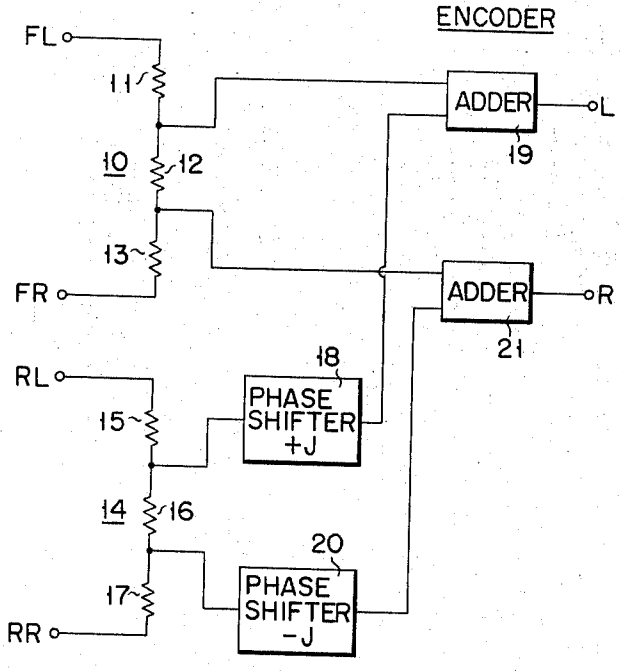

ENCODER
FL
FR
RL
RR
11
10
12
13
15
14
16
17
ADDER
19
ADDER
21
L
R
18
PHASE SHIFTER +J
20
PHASE SHIFTER -J

FIG. 3

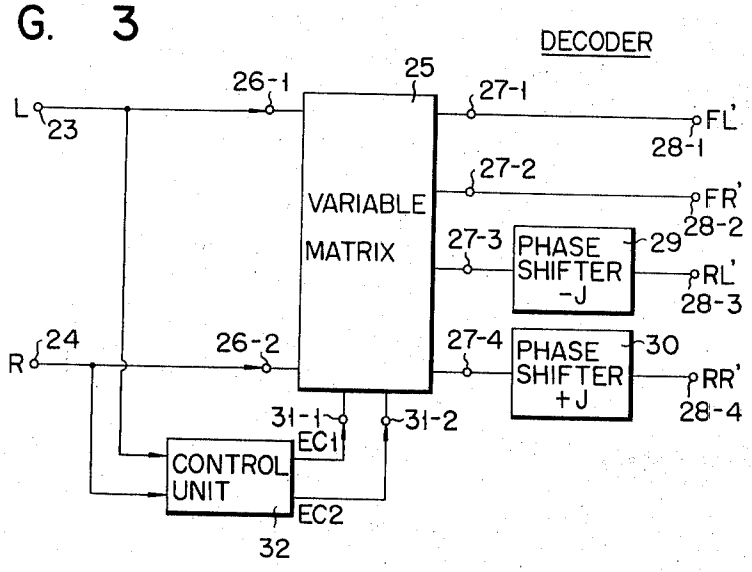

DECODER
L
23
26-1
25
27-1
FL'
28-1
27-2
FR'
28-2
VARIABLE
MATRIX
27-3
PHASE
SHIFTER
-J
29
RL'
28-3
R
24
26-2
27-4
PHASE
SHIFTER
+J
30
RR'
28-4
31-1
EC1
31-2
CONTROL
UNIT
EC2
32

FIG. 4

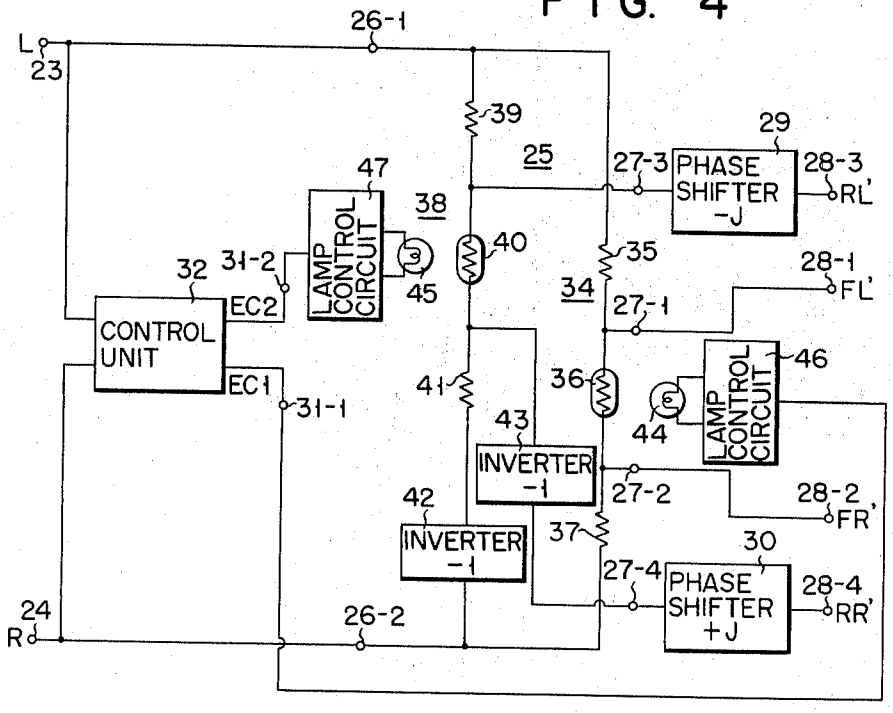

L
23
26-1
39
25
29
27-3
PHASE
SHIFTER
-J
28-3
RL'
47
LAMP
CONTROL
CIRCUIT
38
40
35
28-1
FL'
32
31-2
EC2
45
34
27-1
CONTROL
UNIT
EC1
31-1
41
36
46
44
LAMP
CONTROL
CIRCUIT
43
INVERTER
-1
27-2
28-2
FR'
42
INVERTER
-1
37
30
27-4
PHASE
SHIFTER
+J
28-4
RR'
24
R
26-2

FIG. 5

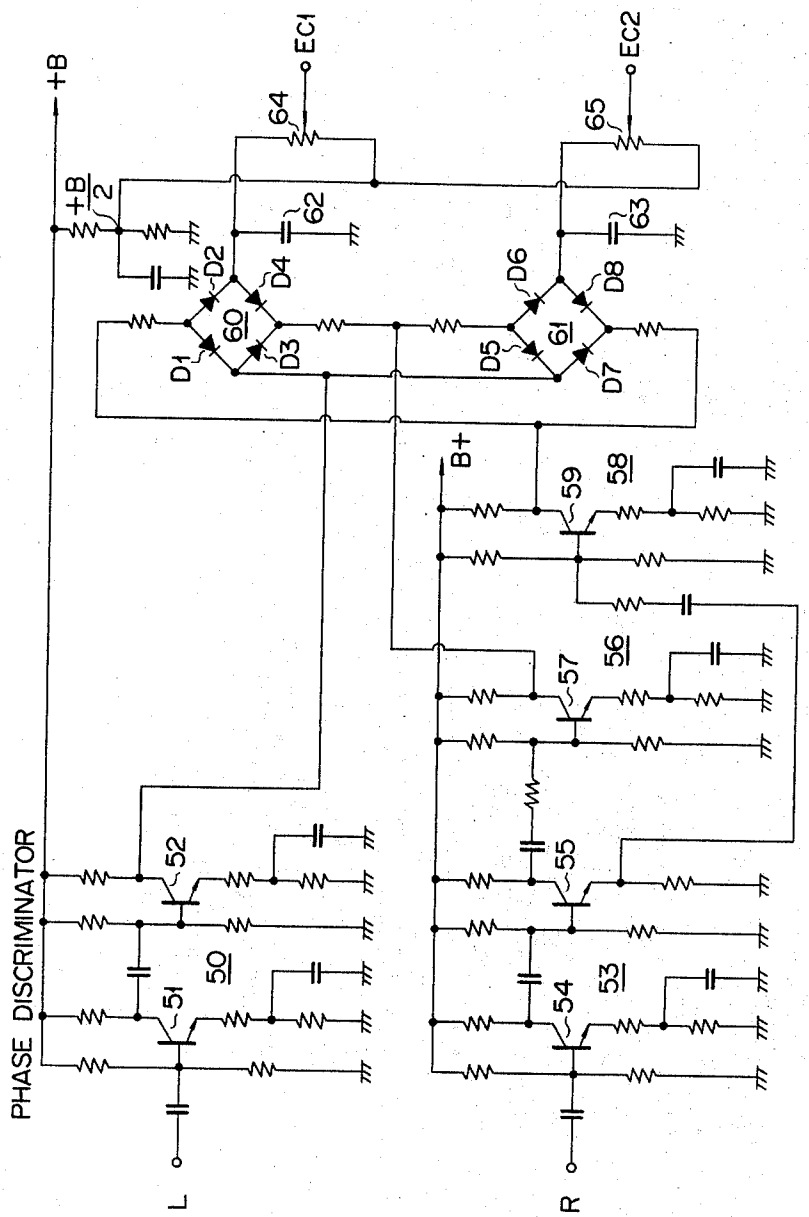

+B
EC1
EC2
64
65
+B
2
62
63
D2
D4
D6
D8
60
61
D1
D3
D5
D7
B+
59
58
57
56
55
52
50
51
53
54
PHASE DISCRIMINATOR
L
R

FIG. 6

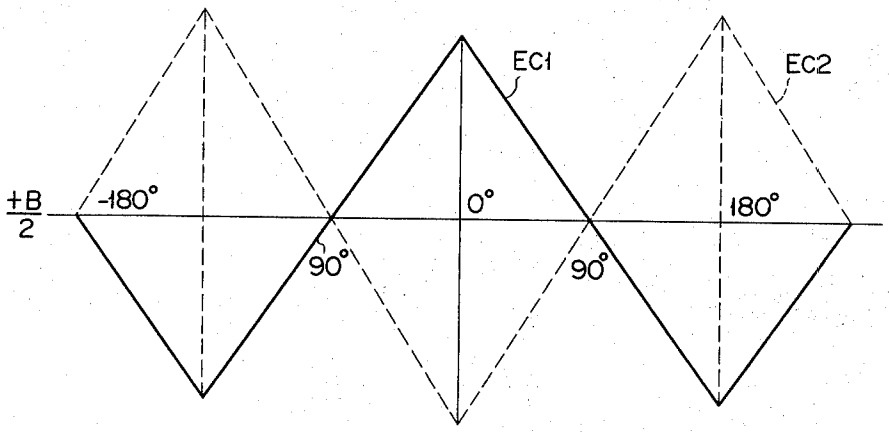


FIG. 7

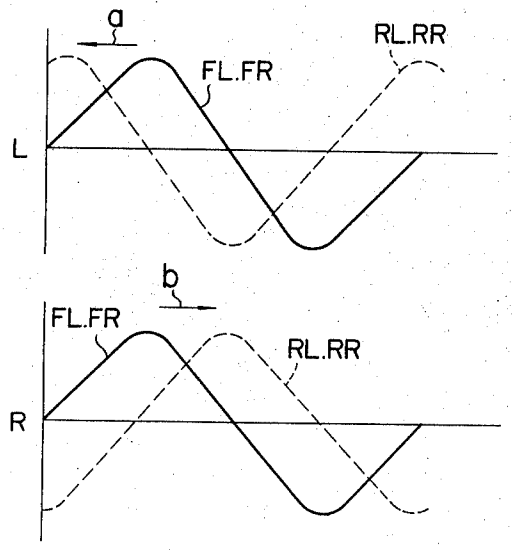


FIG. 8

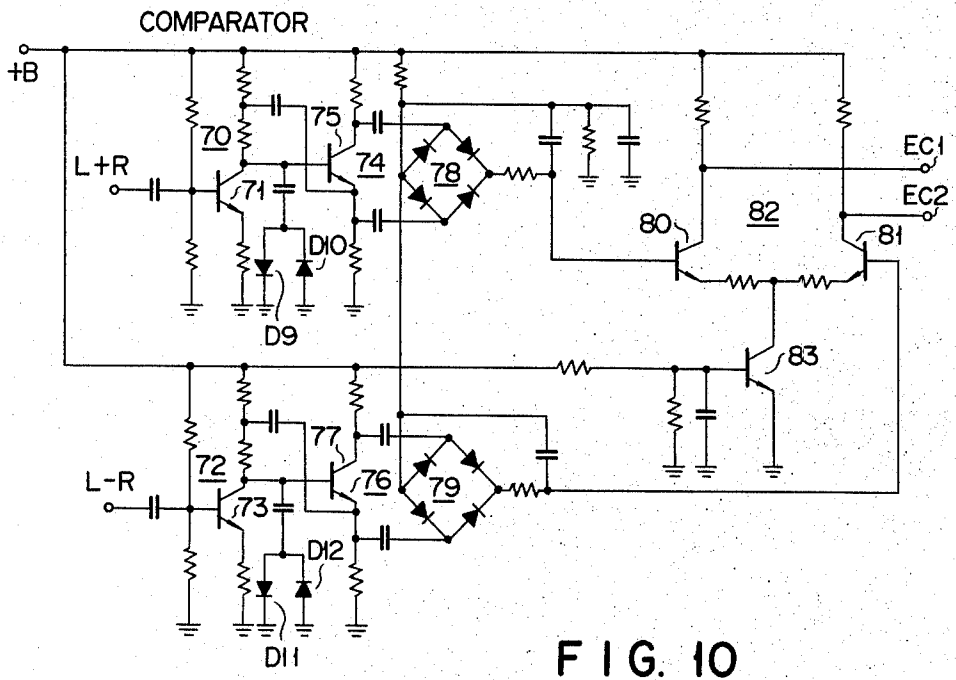
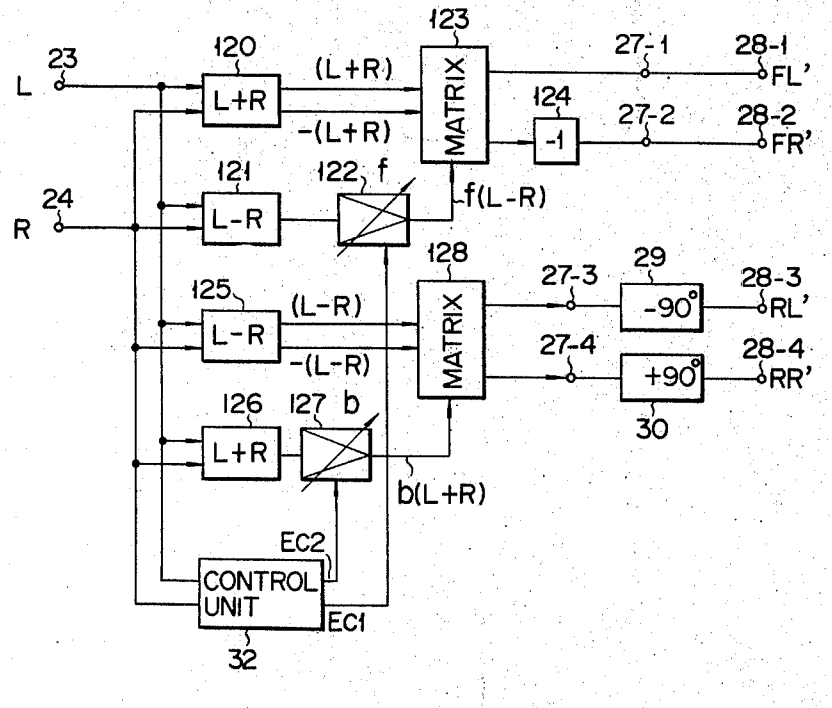

COMPARATOR
+B
L+R
70
71
75
74
78
D10
D9
EC1
EC2
80
82
81
83
L-R
72
73
77
76
79
D12
D11

FIG. 10


L
23
R
24
120
L+R
121
L-R
122
f
123
MATRIX
(L+R)
-(L+R)
f(L-R)
124
-1
27-1
28-1
FL'
27-2
28-2
FR'
125
L-R
(L-R)
-(L-R)
126
L+R
127
b
128
MATRIX
b(L+R)
27-3
29
-90°
28-3
RL'
27-4
+90°
28-4
RR'
30
EC2
CONTROL UNIT
EC1
32

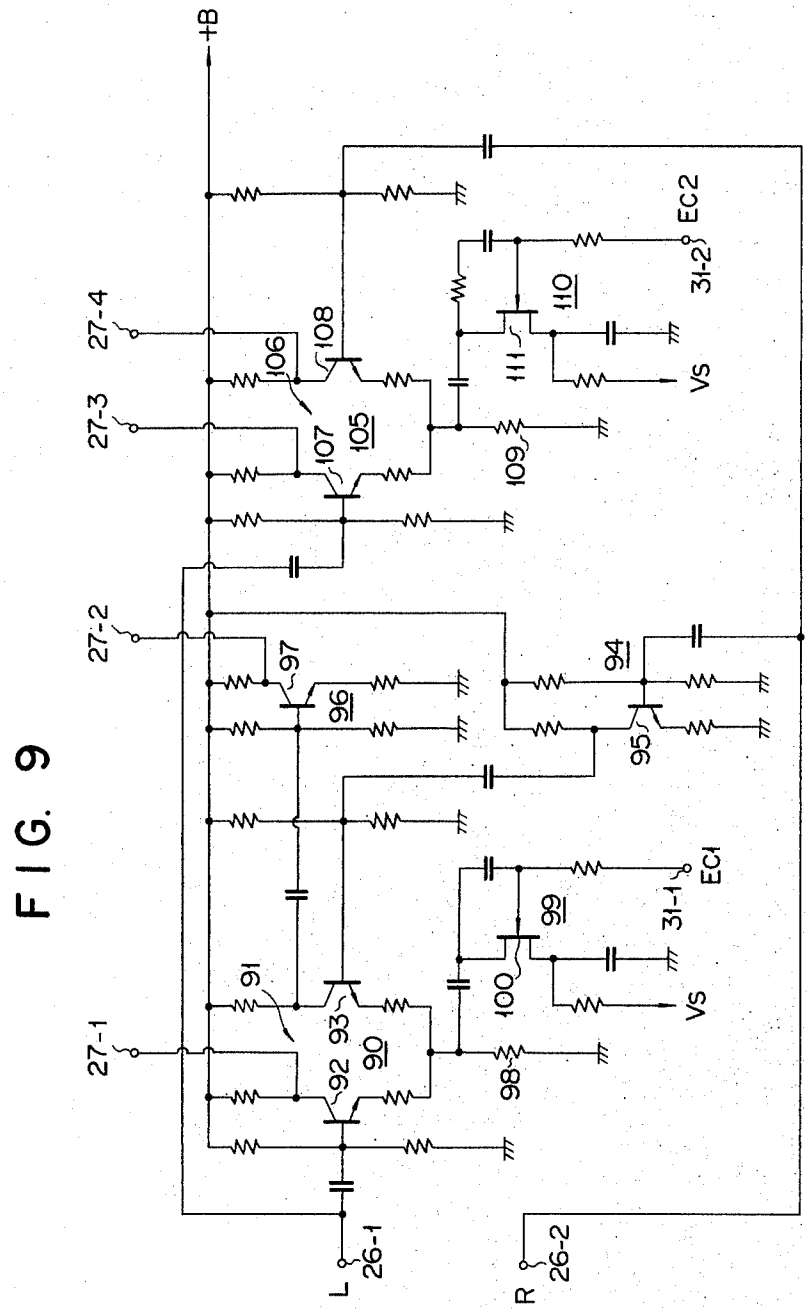
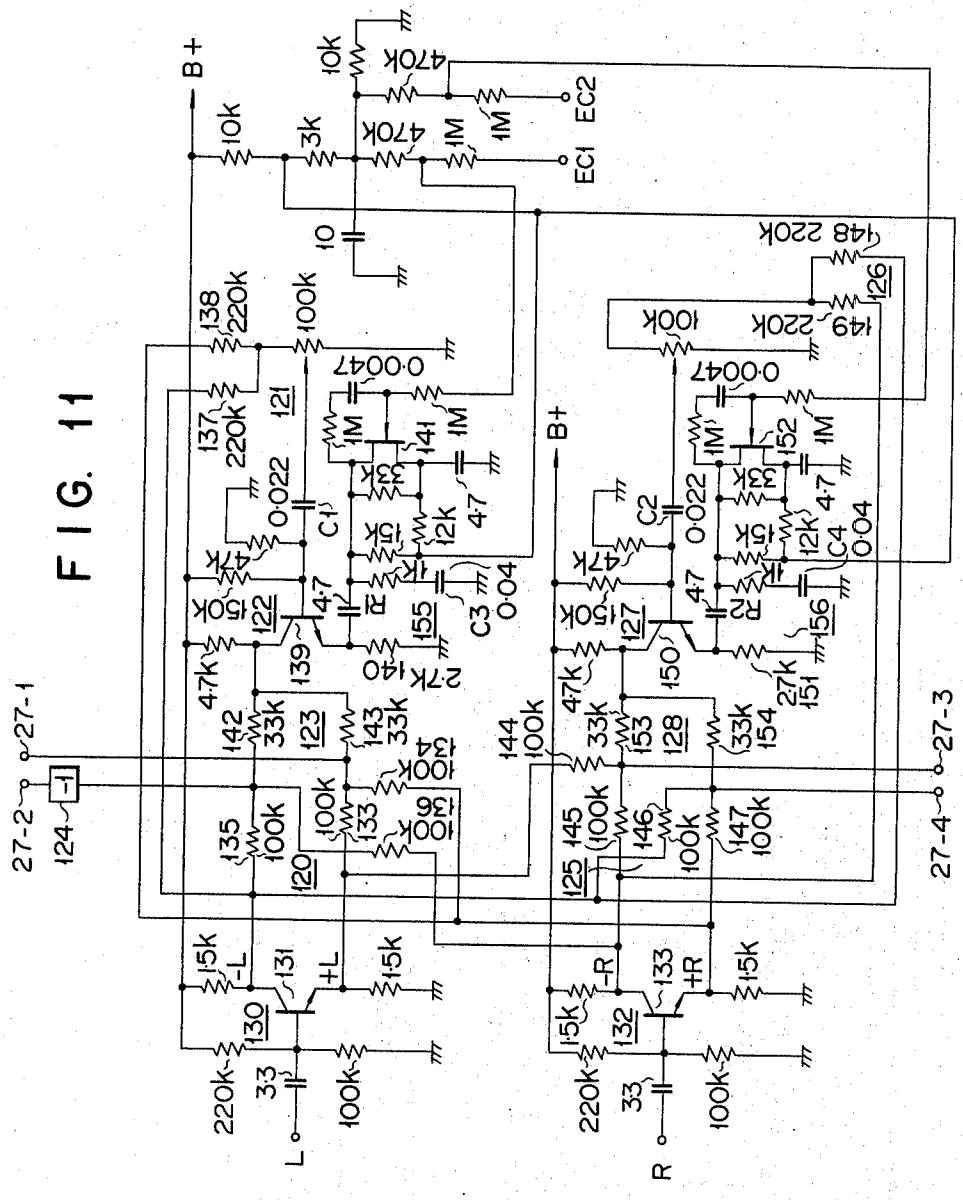

+B
27-4
27-3
27-2
27-1
106
108
107
105
109
110
111
EC2
31-2
Vs
97
96
94
95
91
93
92
90
98
99
100
EC1
31-1
L
26-1
R
26-2

FIG. 9

FIG. 11


B+
10k
470k
EC2
EC1
1M
3k
10
138
220k
100k
137
121
0.0047
0.022
C1
47k
150k
122
47
139
155
C3
0.04
2.7k
140
47k
142
33k
123
143
33k
300k
27-1
27-2
124
-1
135
100k
120
100k
133
56k
15k
-L
131
+L
130
220k
33
L
148
220k
126
149
220k
100k
C2
127
150
144
100k
153
128
154
27-3
27-4
145
146
147
125
-R
+R
132
R

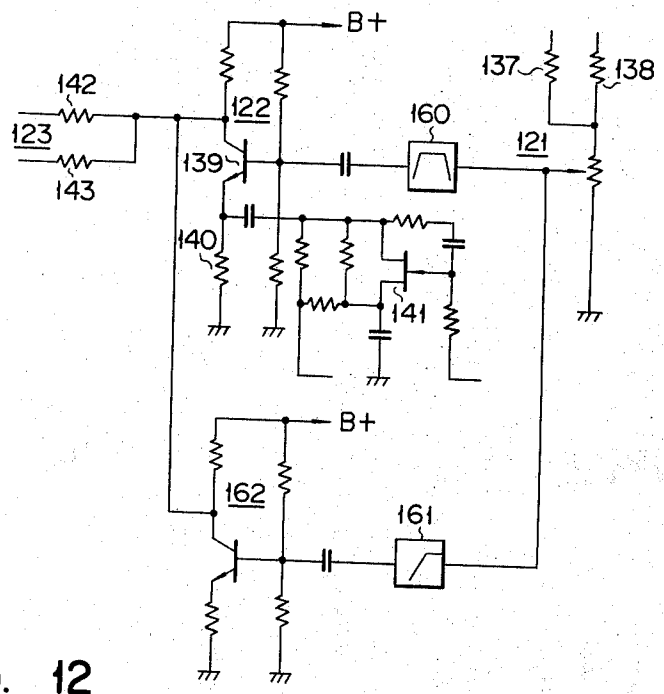

B+
142
123
143
122
139
140
141
160
121
137
138
B+
162
161

FIG. 12

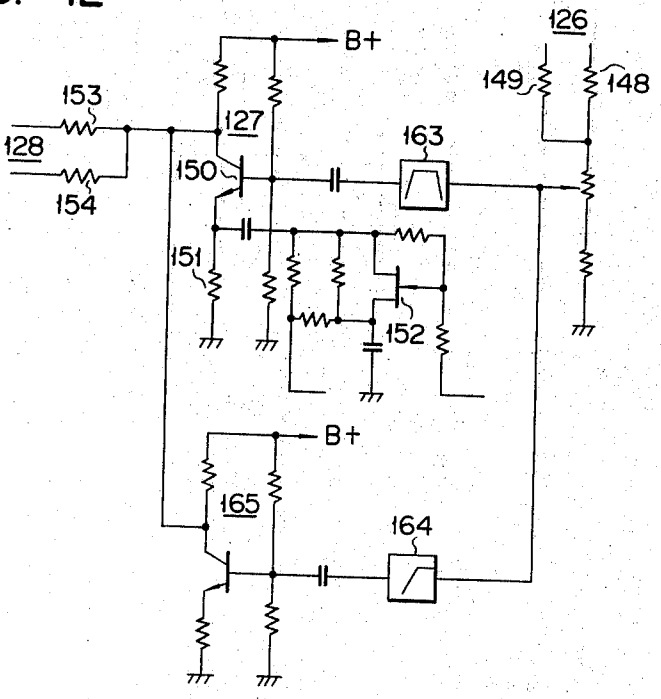

B+
153
128
154
127
150
151
152
163
126
149
148
B+
165
164

FIG. 13

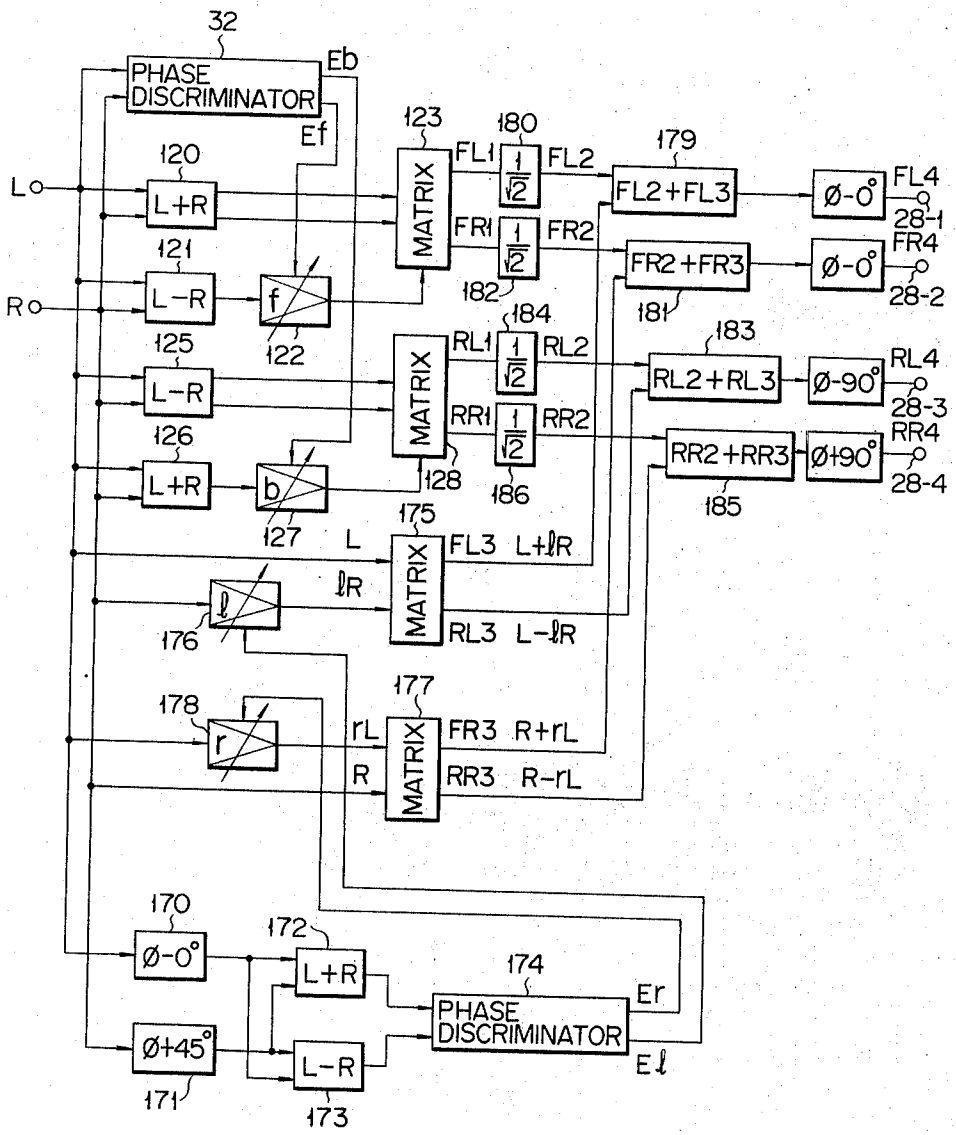

32
PHASE DISCRIMINATOR
Eb
Ef
120
L+R
121
L−R
122
f
125
L−R
126
L+R
b
127
128
123
MATRIX
FL1
FR1
180
1/√2
182
FL2
FR2
179
FL2+FL3
FR2+FR3
181
Ø-0°
Ø-0°
FL4
28-1
FR4
28-2
184
RL1
RR1
1/√2
186
RL2
RR2
183
RL2+RL3
RR2+RR3
185
Ø-90°
Ø+90°
RL4
28-3
RR4
28-4
175
MATRIX
L
ℓR
FL3 L+ℓR
RL3 L−ℓR
176
ℓ
177
MATRIX
rL
R
FR3 R+rL
RR3 R−rL
178
r
170
Ø-0°
Ø+45°
171
172
L+R
L−R
173
174
PHASE DISCRIMINATOR
Er
Eℓ

FIG. 14

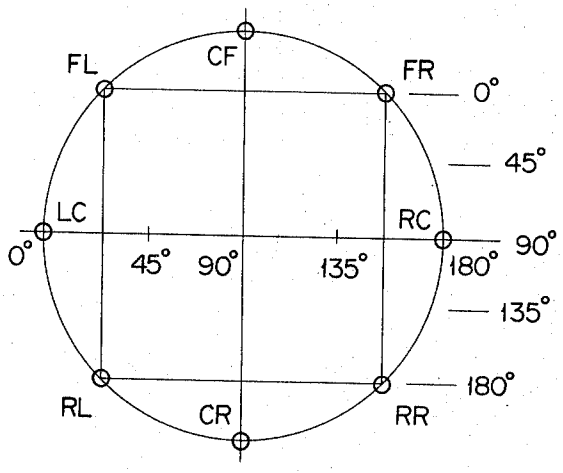

FL
CF
FR
0°
45°
LC
RC
0°
45°
90°
135°
180°
90°
135°
180°
RL
CR
RR

FIG. 15

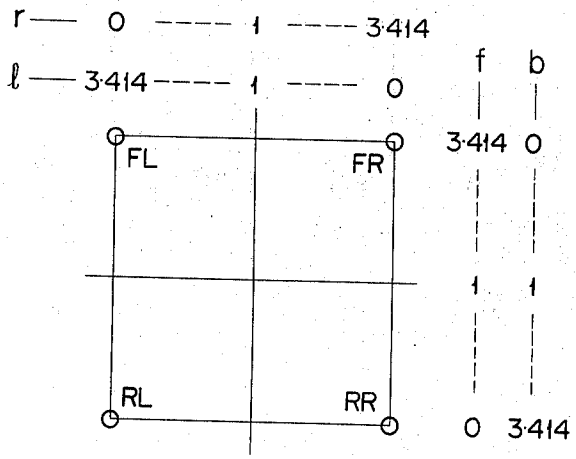

r
0
1
3·414
l
3·414
1
0
f
b
FL
FR
3·414
0
1
1
RL
RR
0
3·414

FIG. 16

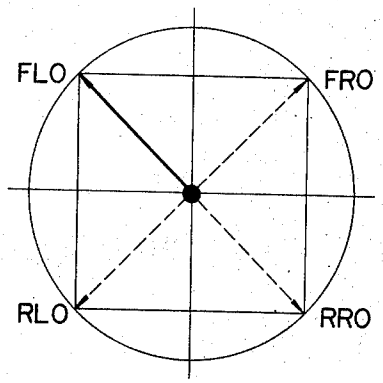


FIG. 17

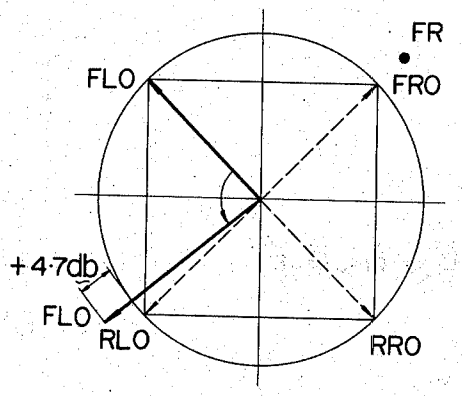


FIG. 18

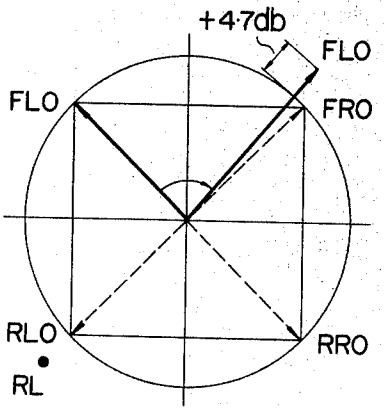


FIG. 19

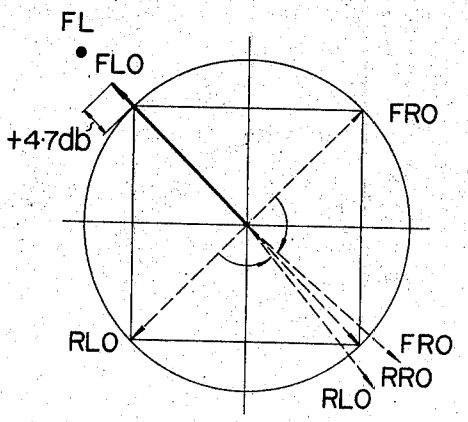


FIG. 20

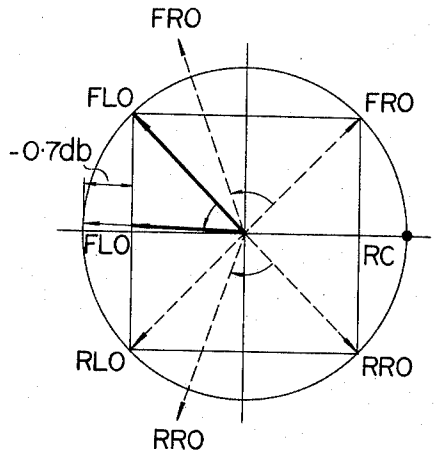


FIG. 21

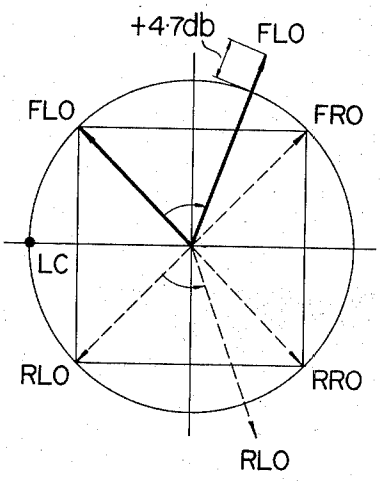


FIG. 22

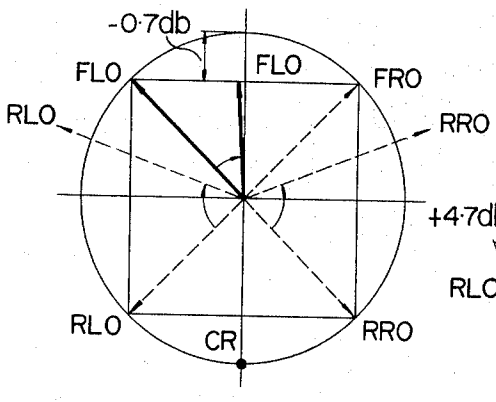


FIG. 23

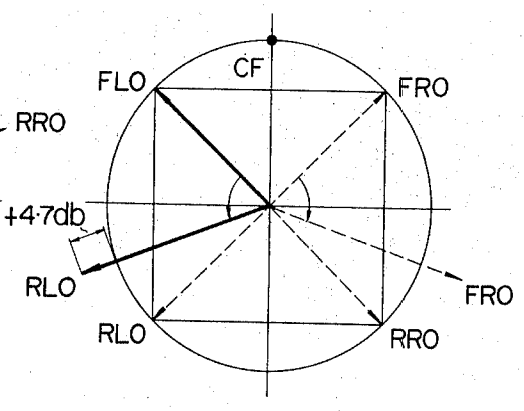


FIG. 24A

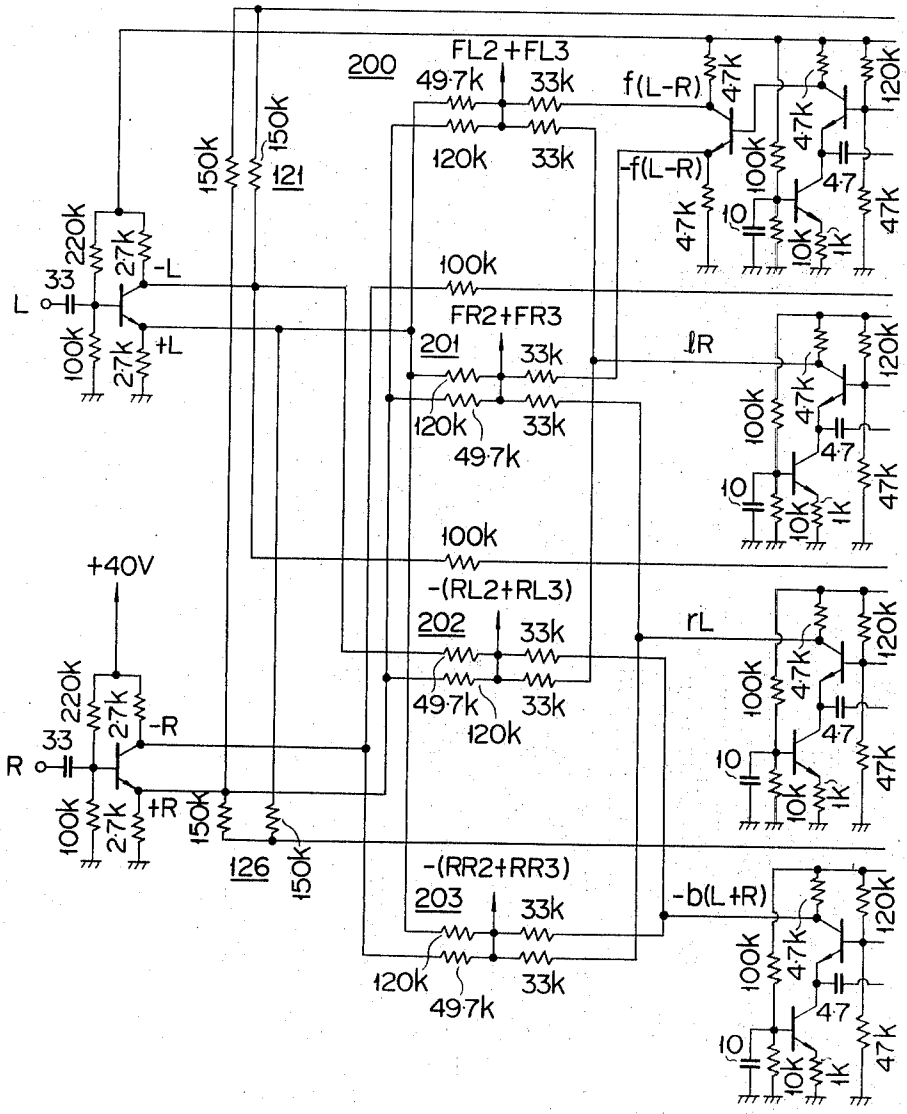

200
FL2+FL3
49·7k
33k
120k
33k
f(L-R)
-f(L-R)
150k
150k
121
100k
FR2+FR3
201
33k
120k
33k
49·7k
lR
100k
-(RL2+RL3)
202
33k
49·7k
33k
120k
rL
+40V
126
150k
-(RR2+RR3)
203
33k
120k
33k
49·7k
-b(L+R)
L
R
220k
27k
-L
+L
-R
+R
33
100k
27k
47k
4·7
10k
1k
10
120k

FIG. 24B

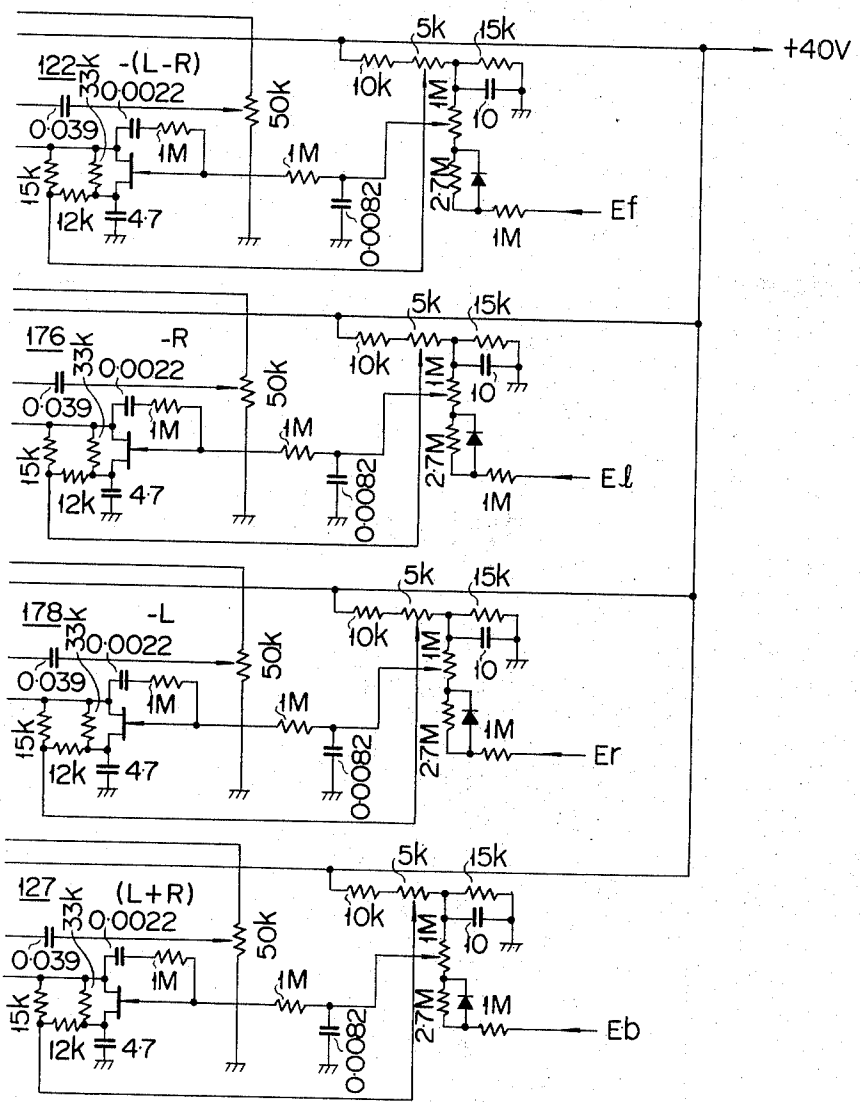
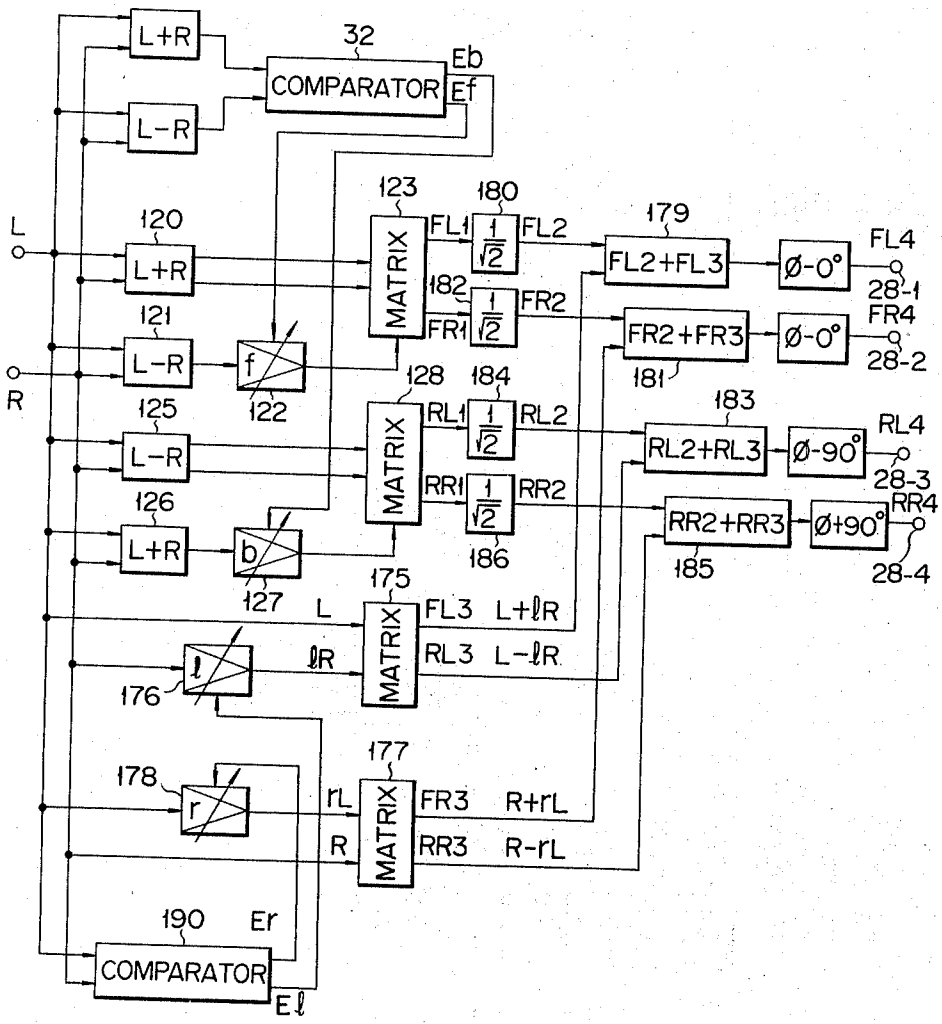

122
-(L-R)
176
-R
178
-L
127
(L+R)
33k
0·0022
0·039
1M
15k
12k
4·7
50k
5k
15k
10k
10
27M
0·0082
+40V
Ef
El
Er
Eb

FIG. 25


L+R
32
COMPARATOR
Eb
Ef
L-R
123
180
179
L
120
L+R
MATRIX
FL1
1/√2
FL2
FL2+FL3
Ø-0°
FL4
28-1
182
FR2
FR1
FR2+FR3
FR4
28-2
181
R
121
L-R
f
122
128
184
183
125
L-R
RL1
RL2
RL2+RL3
Ø-90°
RL4
28-3
RR1
RR2
126
L+R
b
127
186
RR2+RR3
Ø+90°
RR4
28-4
185
175
L
FL3
L+ℓR
ℓR
RL3
L-ℓR
176
177
178
r
rL
FR3
R+rL
R
RR3
R-rL
190
Er
COMPARATOR
Eℓ

VARIABLE MATRIX DECODER FOR USE IN 4-2-4 MATRIX PLAYBACK SYSTEM

This invention relates to a directional sound system wherein at least four directional audio input signals are encoded into two channel signals and the two channel signals are decoded into at least four audio signals corresponding to the directional audio input signals.

Recently, so-called "**4-2-4**" matrix playback systems have been used commercially. In such systems four channel directional audio input signals produced in an original sound field are transformed by an encoder into two channel signals to be recorded on such recording media as stereo phonograph records, magnetic tapes and the like, and the two channel signals reproduced from the recording media are transformed by means of a decoder into four channel audio signals approximating said four directional audio input signals which are applied to four speakers disposed about listeners in the reproduced sound field through suitable amplifiers. As above described, in this type of the "**4-2-4**" matrix playback system since the four directional audio input signals are transformed into two channel signals by the encoder it is impossible for the decoder to reproduce signals perfectly identical to the original four directional audio input signals. As a result, the cross-talk between adjacent channels in the reproduced sound signal increases greatly so that it is impossible to obtain a directional effect quite identical to that in the original sound field and an optimum listening area in a listening room is restricted to a very small area.

It is an object of this invention to provide an improved "**4-2-4**" matrix playback system decoder capable of greatly improving the separations between respective reproduced signals, between front and rear channels and between left and right channels in the forward or rearward.

Another object of this invention is to provide an improved decoder capable of eliminating cross-talks between respective channels thereby improving the quality of the sound field and greatly widening the listening area.

According to this invention, there is provided a decoder for use in a directional sound system wherein at least four directional audio input signals are encoded into two channel signals and the two channel signals are decoded into at least four audio signals corresponding to the audio input signals, characterized in that the decoder comprises a control unit responsive to the phase relationship between the two channel signals for producing first and second control signals, first matrix means connected to receive the two channel signals for producing at least two audio output signals corresponding to at least two directional audio input signals, said matrix means having variable matrix coefficients which are controlled by the first control signals, and second matrix means connected to receive the two channel signals for producing at least two audio output signals corresponding to two remaining audio input signals, the second matrix means having variable matrix coefficients controlled by the second control signals.

The present invention can be more fully understood from the following detailed description when taken in connection with reference to the accompanying drawings, in which:

FIG. **1** is a block diagram useful to explain the principle of the "**4-2-4**" matrix system;

FIG. **2** shows a connection diagram of an encoder;

FIG. **3** shows a block diagram of a decoder embodying the invention;

FIG. **4** shows a block diagram of a modified decoder;

FIG. **5** shows a circuit of a phase discriminator utilized as a control unit;

FIG. **6** is a diagram showing output characteristics of the phase discriminator shown in FIG. **5**;

FIG. **7** is a plot showing a phase relationship between **2**-channel signals;

FIG. **8** is a circuit diagram of a comparator utilized as a control unit;

FIG. **9** shows a circuit diagram of a modified decoder;

FIG. **10** shows a block diagram of another modification of the decoder;

FIG. **11** is a circuit diagram of the modified decoder shown in FIG. **10**;

FIG. **12** shows a modification of a portion of the decoder shown in FIG. **11**;

FIG. **13** shows a block diagram of a modified decoder capable of independently controlling the signals in the front-left and right channels and in the rear-left and right channels;

FIG. **14** shows the relationship between the phase angle between signals and the location of the sound source;

FIG. **15** is a graph showing the manner of varying the gains of various variable gain amplifiers utilized in the circuit shown in FIG. **13**;

FIGS. **16** to **23** are diagrams showing the shifts of demodulation vector for a specified channel under various operating conditions of the decoder shown in FIG. **13**;

FIGS. **24**A and **24**B show a circuit diagram of the variable matrix circuit shown in FIG. **13**; and

FIG. **25** shows a modification of the decoder shown in FIG. **13**.

To have a better understanding of the invention the principles of the "**4-2-4**" matrix playback system and an encoder will first be described with reference to FIGS. **1** and **2** of the accompanying drawings.

In the system shown in FIG. **1**, four microphones MFL, MFR, MRL and MRR are installed in an original sound field **1** in order to produce four channel directional audio signals FL (front-left), FR (front-right), RL (rear-left) and RR (rear-right). These four channel signals are supplied to an encoder **2** to be transformed into two signals L and R. The outputs L and R from the encoder **2** are applied through two channel paths **3** and **4** to a decoder **5** to be transformed into reproduced four channel signals FL′, FR′, RR′ and RL′ approximating original four channel signals FL, FR, RR and RL. The reproduced four channel signals are applied through amplifiers (not shown) to four loud speakers SFL, SFR, SRL and SRR located about a listener **6** in a listening room **7** to provide a stereo reproduction with a greater sense of presence than the prior art two channel stereo reproducing system.

There are many types of two channel systems which couple the outputs L and R from the encoder **2** to the decoder **5**. According to one system the two outputs L and R from the encoder **2** are recorded on a recording medium such as a stereo phonographic record or a magnetic tape and the outputs from the recording medium are applied to the decoder **5**. According to the

other system, the two outputs from the encoder **2** or the outputs reproduced from the recording medium are transmitted to the decoder **5** over an FM stereophonic broadcasting system.

The encoder **2** shown in FIG. **1** has a construction illustrated in FIG. **2.** More particularly, directional audio signals FL and FR produced by the microphones MFL and MFR disposed at the front side of the original sound field **1** are supplied to a first resistive matrix circuit **10** comprising serially connected resistors **11, 12** and **13.** The directional audio signals RL and RR in the rear side of the original sound field **1** are applied to a second resistive matrix circuit **14** comprising serially connected resistors **15, 16** and **17.** A signal from the upper terminal of the center resistor **12** of the first matrix circuit **10** and a signal derived out from the upper terminal of the center resistor **16** of the second matrix circuit **14** and phase shifted by a $+90°$ $(+j)$ phase shifter **18** are combined by an adder **19** to produce a first channel or left signal L. A signal derived out from the lower terminal of the center resistor **12** of the first matrix circuit **10** and a signal derived out from the lower terminal of the center resistor **16** of the second matrix circuit **14** and phase shifted by a $-90°$ $(-j)$ phase shifter **20** are combined by an adder **21** to produce a second channel or right signal R. It is to be understood that phase shifters **18** and **20** are constructed to provide substantially the same phase shift over the entire audible frequency band.

Thus, the L and R signals are expressed as follows:

$$L = FL + \Delta FR + jRL + J\Delta RR$$
$$R = FR + \Delta FL - jRR - j\Delta RL$$

where Δ denotes a transformation constant or a matrix constant generally having a value of approximately 0.414. The reproduced four channel signals FL′, FR′, RL′ and RR′ are produced in the following manner by an ordinary decoder having the same fixed matrix constant Δ:

$$FL' = L + \Delta R = FL(1+\Delta^2) + FR(2\Delta) + jRL(1-\Delta^2)$$
$$FR' = R + \Delta L = FR(1+\Delta^2) + FL(2\Delta) - jRR(1-\Delta^2)$$
$$RL' = -j(L-\Delta R) = RL(1+\Delta^2) + RR(2\Delta) - jFL(1-\Delta^2)$$
$$RR' = +j(R-\Delta L) = RR(1+\Delta^2) + RL(2\Delta) + jFR(1-\Delta^2)$$

Let us now consider the separation between respective channels in the reproduced sound field.

Let us assume that only the signal FL from the microphone MFL is present in the original sound field **1.** Then, the reproduced four channel signals in the reproduced sound field will be expressed as follows:

$$FL' = FL(1+\Delta^2)$$
$$FR' = FL(2\Delta)$$
$$RL' = -jFL(1-\Delta^2)$$
$$RR' = 0$$

Since $\Delta = 0.414$, the separations between channel FL′ and adjacent channels FR′ and RL′ are respectively equal to -3dB and the separation between the channels FL′ and RR′ in a diagonal direction equals $-\infty$dB as can be readily understood by those skilled in the art. As above described, since the separation between adjacent channels equals -3dB it is impossible to enjoy the stereo playback of four channels with a sufficiently large directional resolution.

FIG. **3** shows a block diagram of an improved decoder embodying the invention including a variable matrix circuit having a matrix coefficient whose magnitude is controlled in accordance with the phase difference between two channel signals L and R.

In the decoder shown in FIG. **3,** the two channel signals L and R are applied to the input terminals **23** and **24** of the decoder through two-channel media and hence to the input terminals **26-1** and **26-2** of the variable matrix circuit **25** which operates to decode or dematrix the two channel signals L and R to produce four channel signals on its output terminals **27-1, 27-2, 27-3** and **27-4.** The output terminals **27-1** and **27-2** of the variable matrix circuit **25** are coupled to the output terminals **28-1** and **28-2** of the decoder, whereas output terminals **27-3** and **27-4** of the variable matrix circuit **25** are coupled to the output terminals **28-3** and **28-4** of the decoder respectively through $\pm 90°$ phase shifters **29** and **30.** Further, the variable matrix circuit **25** is provided with control input terminals **31-1** and **31-2** to which are applied the control outputs EC1 and EC2 of a control unit **32.** The control unit **32** provides these control outputs EC1 and EC2 in accordance with the phase difference between two-channel signals L and R. The magnitudes of the first and second control outputs EC1 and EC2 from the control unit **32** vary in the opposite directions in proportion to the phase difference between signals L and R. The first control output EC1 is used to control the matrix coefficient related to the front channels, whereas the second control output EC2 is used to control the matrix coefficient related to the rear channels. Where the phase difference between signals L and R is near zero, for instance, the first control output EC1 operates to decrease the matrix coefficient related to the front channels thus enhancing the separation between front channels. On the other hand, the second control output EC2 operates to increase the matrix coefficient related to the rear channels thus reducing the separation between rear channels. Concurrently therewith the signal levels of the front channels are increased and those of the rear channels are decreased thus improving the separation between the front and rear channels.

The control unit **32** may be constituted by a phase discriminator which detects directly the phase difference between signals L and R or a comparator which detects the phase relationship between signals L and R in terms of the difference in the levels of a sum signal (L+R) and a difference signal (L−R). In this invention, the reason for controlling the matrix coefficient associated with the front and rear channels by detecting the phase relationship between signals L and R is as follows: Although a man has a keen ability to detecting the direction of a large sound but this sensitivity for a small sound coexisting with the large sound is very poor. For this reason, in the reproduction of four channel signals, where there is a large sound in the front side and a small sound in the rear side it would be possible to mroe efficiently enjoy the four channel playback by enhancing the separation between the front channels and lowering the separation between the rear channels. On the contrary, where a small sound exists in the front side and a large sound in the rear side the four channel playback could be enjoyed more efficiently by enhanc-

ing the separation between the rear channels and lowering the separation between front channels.

Where a large sound is present in the front and a small sound is present in the rear, that is, where FL, FR >> RL, RR, signals L and R have substantially the same phase. This means that the level of a sum signal (L + R) is higher than that of a difference signal (L − R).

Conversely, where a large sound is present in the rear while a small sound is present in the front, that is, where FL, FR << RL, RR, signals L and R have opposite phase. In such a case, the level of the sum signal (L + R) is lower than the level of the difference signal (L − R). For this reason, it is possible to detect the phase relationship between signals L and R by either a phase discriminator or a comparator.

FIG. **4** is a connection diagram of one example of a decoder embodying the invention. The variable matrix circuit **25** is connected between input terminals **26-1** and **26-2** and comprises a first resistive matrix circuit **34** including serially connected resistors **35, 36** and **37** and a second resistive matrix circuit **38** including serially connected resistors **39, 40** and **41** and an inverter **42.** The first matrix circuit **34** is associated with the front channels and its center resistor **36** comprises a photoconductive element such as a CdS element and the opposite terminals thereof are connected to output terminals **27-1** and **27-2.** The second matrix circuit **38** is associated with the rear channels and its center resistor **40** also comprises a photoconductive element such as a CdS element. The upper terminal of resistor **40** is connected to an output terminal **27-3** while the lower terminal to an output terminal **27-4** through an inverter **43.** Incandescent lamps **44** and **45** for illuminating resistors **36** and **40,** and lamp control circuits **46** and **47** for controlling the brightness of the lamps in accordance with the control outputs EC1 and EC2 are connected to control input terminals **31-1** and **31-2** of the variable matrix circuit **25.**

Before describing the operation of the decoder shown in FIG. **4,** the construction of the control unit **32,** an important component of this invention, will be described hereunder.

FIG. **5** shows a circuit diagram of a phase discriminator which comprises a first limiter **50** including transistors **51** and **52** connected to receive the L signal and a second limiter **53** including transistors **54** and **55** connected to receive the R signal. The first and second limiters **50** and **53** have large amplification gains and operate to transform the signals L and R into rectangular wave signals. Two output signals of opposite polarities produced by the second limiter **53** are amplified by first and second amplifiers **56** and **58** including transistors **57** and **59** respectively. The outputs from the first and second amplifiers **56** and **58** are supplied to a first switching circuit **60** and a second switching circuit **61** respectively including bridge connected diodes D_1 to D_4 and diodes D_5 to D_8, thereby causing these switching circuits ON and OFF alternately. The output from the first limiter **50** is coupled to the common input of the first and second switching circuits **60** and **61,** while the output terminals of these switching circuits **60** and **61** are grounded through capacitors **62** and **63** respectively, and are connected to a point of reference voltage (in this case, +B/2 volts) through potentiometers **64** and **65,** respectively. The slidable arms of the potentiometers **64** and **65** supplies the first and second control outputs EC1 and EC2.

The phase discriminator constructed as above described operates to switch the left signal L by alternately rendering ON and OFF the first and second switching circuits **60** and **61** in response to the right signal R thereby discriminating the phase difference between the right and left signals R and L. FIG. **6** shows the operating characteristic of the phase discriminator showing that the first and second control outputs EC1 and EC2 vary symmetrically but in opposite directions about the reference level, which is equal to about +B/2 volts in the phase discriminator shown in FIG. **5.** The case wherein the phase difference between the left and right signals L and R equals zero degree corresponds to a case wherein the sound is present only in the front, that is L = FL + ΔFR and R = FR + ΔFL. The case wherein the phase difference between the left and right signals L and R equals 180° corresponds to a case wherein the sound is present only in the rear, that is L = $+j$RL + jΔRR and R = $-j$RR − jΔRL, and the case wherein the phase difference between the signals L and R equals 90° corresponds to a case wherein sounds of the same level are present on the left hand and right hand sides in the front as well as on the left hand and right hand sides in the rear, that is L = 1 + j and R = 1 − j. FIG. **7** shows the relationship between the left signal L and the right signal R. Solid lines show the case wherein signals FL and FR alone are present and thus the signals L and R are in phase. Dotted lines show the case wherein signals RL and RR alone are present and thus the signals L and R are 180° out-of-phase. As the signals RL and RR are impressed the phase relationship between two channel signals L and R vary as shown by arrows *a* and *b*.

FIG. **8** shows a circuit diagram of a comparator which is a modified embodiment of the control unit. In this embodiment, the two channel signals L and R are added and subtracted before they enter the comparator so as to form a sum signal (L + R) and a difference signal (L − R). The sum signal (L + R) is applied to a logarithmic amplifier **70** including a transistor **71** and diodes D_9 and D_{10}, whereas the difference signal (L − R) is applied to a logarithmic amplifier **72** including a transistor **73** and diodes D_{11} and D_{12}. The output from the amplifier **70** proportional to log (L + R) is coupled to a boot strap circuit **74** comprising a transistor **75,** the outputs thereof having opposite phases being applied across a rectifier circuit **78.** Similarly, the output from the amplifier **72** which is proportional to log (L − R) is supplied to a second boot strap circuit **76** including a transistor **77** and the outputs of the boot strap circuit **76** having opposite polarities are applied to a rectifier circuit **79.** The output of rectifier **78** which is proportional to log |L+R| and the output of rectifier **79** which is proportional to log |L−R| are applied to the base electrodes of transistors **80** and **81** constituting a differential amplifier **82.** A transistor **83** is connected to the emitter electrodes of transistors **80** and **81** to cause the amplifier **82** to act properly. The differential amplifier **82** acts to operate values log |L+R|/|L−R| and log |L−R|/|L+R|. The first control output EC1 derived out from the collector electrode of transistor **80** corresponds to log |L+R|/|L−R| whereas the second control output EC2 derived out from the collector electrode of transistor **81** corresponds to log |L−R|/|L+R| and these outputs EC1 and EC2 vary schematically with op-

posite directions about the reference value in substantially the same manner as the outputs of the phase discriminator as shown in FIG. 6.

Returning back to FIG. 4, the operation of this decoder will now be described. Where the phase difference between left and right signals L and R is about zero degree, that is where a large sound is present in the front and a small sound in the rear, the first control output EC1 from the control unit 32 is large, whereas the second control output EC2 is small. As a result, the lamp control circuits 46 and 47 operate to pass a large current through the lamp 45 but a small current through the lamp 44 with the result that photosensitive element 40 manifests a small resistance value whereas the photosensitive element 36 a large resistance value. Accordingly, the level of the left signal L contained in the decoder output FL′ is increased but the level of the right signal R contributing to the cross-talk is decreased. On the other hand, the level of the right signal R contained in the output FR′ is increased whereas the level of the left signal L contributing to the cross-talk is decreased. This means an improvement of the separation between the front channels. The level of the left signal L contained in the decoder output RL′ associated with the rear channels is decreased whereas the level of the right signal R contributing to the cross-talk is increased. On the other hand, the level of the right signal R contained in the output RR′ is decreased while the level of the left signal L contributing to the cross-talk is increased. This means a degradation of the separation between rear channels. Concurrently therewith, as the level of the signals of the front channels is increased and the level of the signals of the rear channels decreases, the separation between front and rear channels will also be improved.

Where the phase difference between the left and right signals L and R is equal to approximately 180°, the separation between the rear channels will be improved and that between the front channels will be degraded which is just opposite to those described above.

Where the phase difference between the left and right signals L and R is nearly equal to 90°, that is where sounds of the same level present in the forward as well as in the rearward the control outputs EC1 and EC2 of the control unit will have the same level, it may be considered that the variable matrix circuit operates in the same manner as an ordinary fixed matrix circuit.

As above described, the decoder outputs FL′, FR′, RL′ and RR′ can be expressed as follows:

$$FL' = mL + nR$$
$$FR' = nL + mR$$
$$RL' = -j\,(pL - qR)$$
$$RR' = +j\,(qL - pR)$$

where m, n, p and q represent the variable matrix coefficients which are controlled by the control outputs EC1 and EC2 from the control unit in such a manner that the magnitudes of the coefficients m and n are controlled in the opposite directions as well as the coefficients p and q.

FIG. 9 illustrates a variable matrix circuit according to another embodiment of the invention wherein a first matrix circuit 90 associated with the front channels comprises a first differential amplifier 91 including transistors 92 and 93. The left signal L is coupled to the base electrode of transistor 92 while the right signal R is coupled to the base electrode of transistor 93 through an inverter 94 including a transistor 95. The collector electrode of transistor 92 is connected to the first output terminal 27-1 of the matrix circuit while the collector electrode of transistor 93 is connected to the second output terminal 27-2 of the matrix circuit through an inverter 96 comprising a transistor 97. A first control circuit 99 including a field effect transistor 100 is capacitively connected in parallel with a common emitter resistor 98 of transistors 92 and 93 which constitute the differential amplifier 91. The gate electrode of the field effect transistor 100 is connected to a control input terminal 31-1 so that it acts as a variable resistor. The first control circuit 99 operates to vary the AC impedance of the emitter circuits of transistors 92 and 93 in accordance with the magnitude of the control input EC1 so as to control the gain of the differential amplifier 91.

The second matrix circuit 105 associated with the rear channels comprises a second differential amplifier 106 including transistors 107 and 108. The left signal L is coupled to the base electrode of transistor 107, whereas the right signal R is coupled to the base electrode of transistor 108. The collector electrodes of transistors 107 and 108 are connected to the third and fourth output terminals 27-3 and 27-4, respectively, of the matrix circuit. A second control circuit 110 including a field-effect transistor 111 is capacitively connected in parallel with a common emitter resistor 109 for transistors 107 and 108. The gate electrode of field-effect transistor 111 is connected to a control input terminal 31-2. The second control circuit 110 operates in the same manner as the first control circuit 99 so as to control the gain of the second differential amplifier in accordance with the magnitude of the control input EC2.

The operation of the variable matrix circuit shown in FIG. 9 will be briefly described as follows: Where the left and right signals L and R are substantially in phase, the control input EC1 is large and the control input EC2 is small. Consequently, the AC impedance of the emitter circuits of transistors 92 and 93 is decreased whereby the gain of the first differential amplifier 90 is increased, whereas that of the second differential amplifier 106 is decreased. Increase in the gain of the first differential amplifier 91 results in the increase in the level of the left signal L which is derived out from the collector electrode of transistor 92 and in the decrease in the level of the right signal R contributing to increasing the cross-talk. On the other hand, the level of the right signal R derived out from the collector electrode of transistor 93 is increased and the level of the left signal L contributing to increasing the cross-talk is decreased. Accordingly, the separation between the front channels is improved with the increase in the signal level. In the rear channels, as the gain of the second differential amplifier 106 decreases, the separation degrades with the decrease in the signal level.

The reproduced four channel outputs FL′, FR′, RL′ and RR′ of this modified decoder can also be expressed by substantially the same equations used in the first embodiment of the decoder shown in FIG. 4.

FIG. 10 is a block diagram of a decoder according to another embodiment of the invention. With reference first to the front channels, there are provided a first matrix circuit 120 adapted to produce sum signals (L + R) and −(L+R) of opposite polarities, and a second matrix

circuit **121** adapted to produce a difference signal (L −R). The difference signal (L −R) is applied to a third matrix circuit **123** via a variable gain amplifier **122** to be added therein to the outputs from the first matrix circuit **120.** The first variable gain amplifier **122** is controlled by the first control output EC1 from the control unit **32** and has an amplification gain *f* which varies from 0 to 2.41 with respect to the gain of the first matrix circuit **120.** The third matrix circuit **123** functions to produce a first output expressed by (1+*f*)L + (1−*f*)R which is coupled to a terminal **27-1** and a second output expressed by −(1−*f*)L − (1+*f*)R which is coupled to a terminal **27-2** through an inverter **124.**

Associated with the rear channels there are provided a fourth matrix circuit **125** adapted to produce difference signals (L − R) and −(L − R) of the opposite polarities and a fifth matrix circuit **126** adapted to produce a sum signal (L + R). The sum signal (L + R) is applied through a second variable gain amplifier **127** to a sixth matrix circuit **128** where it is added to the outputs (L − R) and −(L R) from the fourth matrix circuit **125.**

The second variable gain amplifier **127** has an amplification gain *b* which varies from 0 to 2.41 with respect to the gain of the fourth matrix circuit **125.** Accordingly, the sixth matrix circuit **128** produces a third output expressed by (1+*b*)L − (1−*b*)R and a fourth output expressed by (1+*b*)R − (1−*b*)L. The gains of the first and second variable gain amplifiers **122** and **127** are varied in the opposite directions by the control outputs EC1 and EC2 from the control unit **32.**

FIG. **11** shows a circuit diagram of the variable matrix circuit shown in FIG. **10.** The left signal L is supplied to a first phase splitter **130** including a transistor **131** and the right signal R is applied to a second phase splitter **132** including a transistor **133.** The output +L from the first phase splitter **131** and the output +R from the second phase splitter **132** are added to each other by resistors **133** and **134** whereas the output −L from the first phase shifter **130** and the output −R from the second phase splitter **132** are added to each other by resistors **135** and **136.** Resistors **133, 134, 135** and **136** are connected to form the first matrix circuit **120.** The outputs −L and +R from the first and second phase splitters **130** and **132** are added to each other by resistors **137** and **138** which form the second matrix circuit **121.** The output (R − L) from the matrix circuit **121** is coupled to the variable gain amplifier **122** including a transistor **139** through a capacitor **C1.** In order to vary the gain of transistor **139** there is provided a field-effect transistor **141,** the conductivity between the source and drain electrodes thereof is controlled by the first control output EC1 from the control unit **32** which is impressed upon the gate electrode thereof, the field-effect transistor **141** being capacitively connected with an emitter resistor **140** of transistor **139.** The output from the variable gain amplifier **122** is added to the two outputs from the first matrix circuit **120** through the third matrix circuit **123** including resistors **142** and **143.** One output from the third matrix circuit **123** is applied to the first output terminal **27-1** and the other output to the second output terminal **27-2** through the inverter **124.**

The output +L from the first phase splitter **130** and the output −R from the second phase splitter **132** are added to each other by resistors **144** and **145,** and the output −L from the first splitter **130** and the output +R from the second phase splitter **132** are added to each other by resistors **146** and **147.** These resistors **144, 145, 146** and **147** are connected to constitute the fourth matrix circuit **125.** The outputs −L and −R from the first and second phase splitters **130** and **132** are added to each other by the fifth matrix circuit **126** including resistors **148** and **149.** The resulting sum output is coupled to the base electrode of a transistor **150** constituting the second variable gain amplifier **127** through a capacitor **C2.** For the purpose of varying the gain of transistor **150,** a field-effect transistor **152** is capacitively connected in parallel with an emitter resistor **151,** the conductivity between the source and drain electrodes of the field-effect transistor being controlled by the second control output EC2 of the control unit **32** which is impressed upon the gate electrode. The output from the second variable gain amplifier **127** is added to the two outputs from the fourth matrix circuit **125** by the action of the sixth matrix circuit **128** including resistors **153** and **154.** Two outputs from the sixth matrix circuit **128** are applied to the third and fourth output terminals **27-3** and **27-4,** respectively, of the variable matrix circuit. The values for all the capacitors shown in FIG. **11** are represented by microfarads.

The outputs FL′, FR′, FL′ and RR′ appearing at the output terminals **28-1, 28-2, 28-3** and **28-4** of the decoder shown in FIG. **10** are respectively expressed by the following equations.

$$FL' = (L+R) + f(L-R) = (1+f)L + (1-f)R = (1+\Delta)FL + (1+\Delta)FR + j(1-\Delta)RL - j(1-\Delta)RR + f((1-\Delta)FL - (1-\Delta)FR + j(1+\Delta)FL + j(1+\Delta)RR)$$

$$FR' = -(-(L+R) + f(L-R)) = (1-f)L + (1+f)R = (1+\Delta)FL + (1+\Delta)FR + j(1-\Delta)RL - j(1-\Delta)RR + f(-(1-\Delta)FL + (1+\Delta)FR - j(1+\Delta)RL - j(1+\Delta)RR)$$

$$RL' = -j((L-R) + b(L+R)) = -j((1+b)L - (1-b)R) = -j(1-\Delta)FL + j(1-\Delta)FR + (1+\Delta)RL + (1+\Delta)RR + b(-j(1+\Delta)FL - j(1+\Delta)FR + (1-\Delta)RL - (1-\Delta)RR)$$

$$RR' = j(-(L-R) + b(L+R)) = j((1+b)R - (1-b)L) = -j(1-\Delta)FL + j(1-\Delta)FR + (1+\Delta)RL + (1+\Delta)RR + b(j(1+\Delta)FR - (1-\Delta)RL + (1-\Delta)RR)$$

When the phase difference between left and right signals L and R equals zero degree, the first control output EC1 from control unit **32** is at a maximum, whereas the second control output EC2 at a minimum. Under these conditions, the gain *f* of the first variable amplifier **122** will have a maximum value of about 2.41 and the gain *b* of the second variable gain amplifier **127** will have a minimum value of about zero. Accordingly, the above described reproduced four channel signals are expressed as follows:

$$FL' = (L+R) + 2.41(L-R) = 3.41L - 1.41R = 2.83FL + j3.99RL + j2.82RR$$

$$FR' = -(-(L+R) + 2.41(L-R)) = 3.41R - 1.41L = 2.83FR - j2.82RL - j3.99RR$$

$$RL' = -j(L-R) = -j0.58FL + j0.58FR + 1.41RL + 1.41RR$$

$$RR' = j(-(L-R)) = -j0.58FL + j0.58FR + 1.41RL + 1.41RR$$

Accordingly, where left and right signals L and R are in phase the unwanted cross-talk between signals FL′ and FR′ of the front channels is reduced to substantially zero and the signal level is increased. On the other hand, the cross-talk between signals RL′ and RR′ of the

rear channels is increased and the signal level is decreased.

Where the phase difference between left and right signals L and R is equal to 180° the first control ouput EC1 of the control unit **32** is at a minimum and the second control output EC2 is at a maximum. Under these conditions, the gain *f* of the first variable gain amplifier **122** will have a minimum value of about zero and the gain *b* of the second variable amplifier **127** will have a maximum value of about 2.41. Accordingly, above described reproduced four channel signals are expressed as follows:

$$FL' = L+R = 1.41FL + 1.41FR + j0.58RL - j0.58RR$$

$$FR' = -(-(L+R)) = 1.41FL + 1.41FR + j0.58RL - j0.58RR$$

$$RL' = j((L-R) + 2.41(L+R)) = -j(3.41L+1.41R) = -j(+j2.83RL + 3.99FL + 2.82FR)$$

$$RR' = j(-(L-R) + 2.41\ (L+R)) = j(3.41R+1.41L) = j(-j2.83RR + 2.82FL + 3.99FR)$$

Accordingly, when the phases of the left and right signals L and R are opposite, it is possible to reduce the unwanted cross-talk btween signals RL' and RR' of the rear channels to substantially zero and to increase the signal level. On the contrary, the cross-talk between the signals FL' and FR' of the front channels is increased and the signal level is decreased.

Where the first and second variable gain amplifiers **122** and **127** of the variable matrix circuits shown in FIGS. **10** and **11** have a flat characteristic over the entire audio frequency range there arises the following problem. More particularly, the ears of a man have a sharp sensitivity for the sound directionality of higher frequencies but have a poor sensitivity for the sound directionality of lower frequencies. With the above described variable matrix circuits, where the sound of higher frequencies is located on the side of the rear channels the sound of the higher frequencies may be shifted to the side of the front channels by a sound of intermediate frequencies which might be located on the side of the front channels. Thus, for example, the shifting of high frequency noises between the front and rear channels will give extremely uncomfortable feeling to the listeners having sound sensitivities described above. In certain cases, low frequency sound which is to be located on the side of the front channels might be shifted to the side of the rear channels by the high frequency sound appearing on the side of the rear channels. For example, the sounds of low frequency musical instruments (for example, a bass or drum) which are to be located in the front are caused to shift to the side of the rear by the sounds of high frequency musical instruments (for example, a trumpet) and vice versa. This problem can be solved by giving to the variable gain amplifiers **122** and **127** a frequency characteristic which sets the low frequency signal components at the center of the front or rear channels and sets the high frequency signal components to the left and right of the front or rear channels. To this end, the variable gain amplifiers **122** and **127** are designed to have a low gain for signals having frequencies lower than a predetermined frequency, for example 200 Hz, and a high gain for signals having frequencies higher than a predetermined frequency, for example 5 KHz, and to control the gain for signals of an intermediate frequency band ranging from 200Hz to 5KHz. To accomplish this object, the coupling capacitors C1 and C2 each having a capacitance value, 0.022 microfarad for example, thereby mainfesting a relatively high impedance for low frequency signals, are connected between first and second variable gain amplifiers **122** and **127** and the second and fifth matrix circuits **121** and **126,** as shown in FIG. **11.** This decreases the gain of the variable gain amplifiers **122** and **127** for the low frequency signals. Further, for the purpose of increasing the gains of the variable gain amplifiers **122** and **127** for high frequency signals, impedance circuits **155** and **156** respectively including a resistor R1 and a capacitor C3 and a resistor R2 and a capacitor C4 and mainfesting low impedances for high frequencies above 5 KHz are capacitively connected in parallel with emitter resistors **140** and **151** respectively of transistors **139** and **150.**

With the variable matrix circuit constructed as above described, the low frequency blocking capacitors C1 and C2 decrease the low frequency outputs from the variable gain amplifiers **122** and **127** to substantially zero. Since the low frequency signal is not controlled by the control unit **32** the separation between the low frequency signals in the front and rear channels will be degraded. In other words, the low tone sounds are located at the centers of the front or rear channels. On the other hand, since the variable gain amplifiers **122** and **127** have a high gain for high frequency signals by the impedance circuits **155** and **156** the separations between the signals in the front channels and between the signals in the rear channels are improved for high frequency signals. Accordingly, the high tone sounds are located on the left and right sides of the front or rear channels. Because the gains of the variable gain amplifiers **122** and **127** for signals of intermediate frequencies are controlled by the control outputs EC1 and EC2, respectively, of the control unit **32,** the separations for intermediate frequency signals are controlled according to the phase relationship between the left and right signals L and R.

FIG. **12** shows a modification of the variable gain amplifier shown in FIG. **11.** With reference first to the front channels, the variable gain amplifier **122** is connected to receive the signal from the third matrix circuit **121** through a bandpass filter **160** which passes only the signals in a predetermined intermediate frequency band whereby the variable gain amplifier **122** operates on only the intermediate frequency signals. Further, a series circuit including a high-pass filter **161** and a fixed gain amplifier **162** is connected in parallel with the bandpass filter **160** and the variable gain amplifier **122.** Similarly, associated with the rear channels are bandpass filter **163,** a high-pass filter **164** and a fixed gain amplifier **165.** It will be clear that this modification can also attain the same object as the previous embodiment.

Although in the foregoing embodiments the front and rear channels have been controlled, it is also possible to independently control the front-left and right channels and the rear-left and right channels. FIG. **13** shows a block diagram of a modified decoder for this purpose. FIG. **13** is different from FIG. **10** in that it is incorporated with the following circuit components. More particularly, there are provided a 0° phase shifter **170** and a 45° phase shifter **171** which introduce a phase difference of 45° between the left signal L and the right signal R. Responsive to the outputs from phase shifters **170** and **171** an adder **172** provides an output (L+R $< +45°$), whereas a subtractor **173** provides an output

(L−R < +45°). A phase discriminator **174** for controlling the left and right channels operates to detect the phase difference between the output signals (L+R < +45°) and (L−R < +45°) to produce control outputs Er and E*l*. A matrix circuit **175** is connected to receive the left signal L and the right signal R through a variable gain amplifier **176** to produce outputs FL3(=L+*l*R) and RL3(=L−*l*R). Similarly, a matrix circuit **177** is connected to receive the left signal L through a variable gain amplifier **178,** and the right signal R to produce outputs FR3(=R+rL) and RR3(=R−*r*L) where *l* and *r* represent the gains of the variable gain amplifiers **176** and **178** respectively. These gains are controlled in the opposite directions in a range of from 0 to 3.414 by the outputs Er and E*l* from the phase discriminator **174.** The gains of the variable gain amplifiers **122** and **127** are controlled in the opposite directions in a range of from 0 to 3.414 by the outputs E*f* and E*b* of phase discriminator as the control unit **32** for controlling rear and front channels by detecting the phase difference between the left and right signals L and R. The output FL1 from the matrix circuit **123** is coupled to one input of an adder **179** via a $1/\sqrt{2}$ attenuator **180** and the output FL3 from the matrix circuit **175** is applied to the other input of adder **179.** Similarly, the output FR1 from the matrix circuit **123** is applied to one input of an adder **181** through a $1/\sqrt{2}$ attenuator **182** whereas the output FR3 from the matrix circuit **177** is coupled to the other input of adder **181.** Likewise, the output RL1 of matrix circuit **128** is applied to one input of an adder **183** through a $1/\sqrt{2}$ attenuator **184** while the output RL3 of matrix circuit **175** is applied to the other input of adder **183.** The output RR1 of matrix circuit **128** is coupled to one input of adder **185** through a $1/\sqrt{2}$ attenuator **186** and the output RR3 of the matrix circuit **177** is applied to the other input of adder **185.**

As shown by FIG. **14,** the phase difference between left and right signals L and R varies from 0° to 180° as the sound source shifts from forward to rearward, whereas the phase difference between the sum signal (L+R < +45°) and the difference signal (L−R < +45°) continuously varies from 0° to 180° as the sound source shifts from left to right. Consequently, the gains *f*, *b*, *l* and *r* of the variable gain amplifiers **122, 127, 176** and **178** vary as shown in FIG. **15.**

Turning back to FIG. **13** it will be clear that the four channel signals FL**4,** FR**4,** RL**4** and RR**4** appearing at the output terminals **28-1, 28-2, 28-3** and **28-4** of the decoder are expressed by the following equations.

$$FL4 = FL2+FL3 = 1/\sqrt{2}((1+f+\sqrt{2})L + (1-f+\sqrt{2}l)R) = 1/\sqrt{2}((1+\sqrt{2})L + R + f(L-R) + \sqrt{2}lR)$$

$$FR4 = FR2 + FR3 = 1/\sqrt{2}((1+f+\sqrt{2})R + (1-f+\sqrt{2}r)L) = 1/\sqrt{2}((1+\sqrt{2})R + L - f(L-R) + \sqrt{2}rL)$$

$$RL4 = -j(RL2+RL3) = -j1/\sqrt{2}((1+b+\sqrt{2})L - (1-b+\sqrt{2}l)R) = -j1/\sqrt{2}((1+\sqrt{2})L - R + b(L+R) - \sqrt{2}lR)$$

$$RR4 = j(RR2+RR3) = j1/\sqrt{2}((1+b+\sqrt{2})R - (1-b+\sqrt{2}r)L) = j1/\sqrt{2}((1+\sqrt{2})R - L + b(R+L) - \sqrt{2}rL)$$

The variable matrix circuit shown in FIG. **13** operates as follows: As an example, the operation of the front-left channel FL will be described. To simplify the description, the output FL4 of the decoder is expressed by the following equation:

$$FL4 = (1+\sqrt{2}+f)L + (1-f+\sqrt{2}l)R$$

Where all channels have equal inputs, respective coefficients *f*, *b*, *l* and *r* are set to be unity respectively. The signal FL4 is thus expressed by the following equation:

$$FL4 = 3.414(L+0.414R)$$

FIG. **16** shows a demodulation vector diagram of the matrix circuit. Here it is assumed that the value 3.414(L+0.414R) represents a reference level of **0** *d*B. Where the inputs are equal, the same consideration is applied also to the other three channels. Accordingly, in the case where all inputs are equal, the demodulation vectors for respective channels are directed to the respective channels.

Where signal FR is impressed upon the front-right channel FR**0,** the first phase discriminator **32** operates in phase whereas the second discriminator **174** operates in the opposite phase (180°). That is to say, the signals L and R are in phase whereas the signals (L+R<+45°) and (L−R<+45°) are 180° out-of-phase. Accordingly, respective variable coefficients are: $f = 3.414$, $b = 0$, $l = 0$ and $r = 3.414$. Thus, the signal FL**4** is given by

$$FL4 = (1+\sqrt{2}+3.414)L + (1-3.414)R = 5.828(L-0.414R)$$

Where the front-right signal FR is applied, the direction of the demodulation vector for signal FL**4** in the front-left channel FL**0** adjacent to channel FR**0** will be shifted from the front-left channel FL**0** to the side of rear-left channel RL**0** which is displaced diagonally from the channel FR**0,** and does not contain any FR signal component as cross-talk, as shown in FIG. **17.** Consequently, the signal component FR to be introduced into the adajcent channel FL**0** as cross-talk component is greatly decreased. The level of the front-left channel signal FL**4** is raised by about **4** *d*B in order to prevent the signal level lowering (in this case, about −3 *d*B) of this channel due to shifting of direction of the demodulation vector for front-left channel FL**0.**

In the presence of the rear-left signal RL the first phase discriminator **32** operates in the opposite phase whereas the second phase discriminator **174** operates in phase. Accordingly, various variable coefficients are: $f = 0$, $b = 3.414$, $l = 3.414$ and $r = 0$.

Thus FL**4** = 5.828(0.414L+R). Under these conditions. as shown in FIG. **18,** the direction of the demodulation vector for the front-left signal FL**4** is shifted to the side of front-right channel FR**0,** and the gain for the front-left channel FL**0** is raised.

In the presence of the front-left signal FL, both first and second phase discriminators **32** and **174** operate in phase so that various variable coefficients are: $f = 3.414$, $b = 0$, $l = 3.414$ and $r = 0$. Thus FL**4** = 5.828(L+0.414R).

As shown in FIG. **19,** under these conditions, the demodulation vector of the signal FL**4** does not vary but the directions of the demodulation vectors of the signals in the adjacent channels FR**0** and RL**0** shift to the side of the rear-right channel RR**0.** Under these conditions, the gains for adjacent channels as well as the gain for the channel FL**0** are increased.

In the case of the front-right signal FR and the rear-right signal RR of the same level, that is where the right-center signal RC is applied, the first phase dis-

criminator **32** operates in **90°** out-of-phase; whereas the second phase discriminator **174** operates in 180° out-of-phase. Accordingly, various coefficients become $f = 1$, $b = 1$, $l = 0$, $r = 3.414$, and thus FL4 = 3.414L.

As shown in FIG. **20,** the direction of the demodulation vector for the front-left signal FL4 shifts to the direction in which the right-center signal RC is not contained as the cross-talk, that is to the side of the left-center. Under these conditions, the gain for the front-left signal FL4 is decreased by about −0.7 dB for performing right-front and rear stereo reproduction.

Where the left center signal LC is applied, the first phase discriminator **32** performs in 90° out-of-phase operation whereas the second phase discriminator **174** performs in-phase operation. Accordingly, various variable coefficients become: $f = 1$, $b = 1$, $l = 3.414$, $r = 0$ and the FL4 = 4.828 (0.707L+R) = 5.914(Lsin35.2°+**R**cos35.2°). Under these conditions, as shown in FIG. **21,** the gain for the signal FL4 is increased for performing the left-front and rear stereo reproduction.

In the case where the rear-center signal CR is applied, the first discriminator **32** operates in phase whereas the second descriminator **172** operates in 90° out-of-phase. As a consequence, various variable coefficients become: $f = 0$, $b = 3.414$, $l = 1$ and $r = 1$ and thus FL4 = 2.414(L+R) = 3.414(Lsin45°+Rcos45°).

Under these conditions, as shown in FIG. **22,** the direction of the demodulation vector of the signal FL4 shifts to the side of the front-center channel, and for the purpose of performing the rear-left and right stereo reproductions the gains for the rear channels RL0 and RR0 are increased whereas the gain for the signal FL4 is decreased.

Where the front-center signal CF is applied, the first phase discriminator operates in phase whereas the second phase discriminator operates in 90° out-of-phase. Accordingly, various variable coefficients become: $f = 3.414$, $b = 0$, $l = 1$, $r = 1$ and thus FL4 = 5.838(L−R) = 5.914(Lcos 9.7°-Rsin9.7°).

As shown in FIG. **23,** for the purpose of performing the front-left and right stereo reproduction, the gains for front-channels FL0 and FR0 are increased.

Although above description was made with reference to only the front-left channel FL0, the operations of the other channels can be readily understood from the foregoing description.

FIGS. **24A** and **24B** show a circuit diagram of the variable matrix circuit shown in FIG. **13.** In FIG. **24A,** a first resistive matrix **200** acts as the matrices **120, 123** and **175,** and the adder **179** shown in FIG. **13** and a second resistive matrix **201** as the matrices **120, 123** and **177,** and the adder **181.** A third resistive matrix **202** acts as the matrices **125, 128** and **175,** and the adder **183** and a fourth matrix **203** as the matrices **125, 128** and **177,** and the adder **185.** For example, the matrix **200** combines the signals +L, +R, f(L−R) and lR with a relative amplitude ratio $(1+\sqrt{2}) : 1 : 1 : \sqrt{2}$.

The signals +L and +R are caused to have the relative amplitude ratio of $1+\sqrt{2} : 1$ by resistors of 49.7 kiloohms and **120** kiloohms. On the other hand, the signals f(L−R) and lR are caused to have the relative amplitude ratio of $1 : \sqrt{2}$ by input signal level settings of the variable gain amplifiers **122** and **176.** Since this circuit is similar to that shown in FIG. **10** it is believed unnecessary to repeat similar description.

FIG. **25** shows a block diagram of a modification of the decoder shown in FIG. **13.** In FIG. **25,** variable gain amplifiers **122** and **127** are controlled respectively by the outputs Ef and Eb from a comparator as the first control unit **32** for the front-rear control which detects the difference in the levels of the sum signal (L + R) and the difference signal (L − R), and variable gain amplifiers **176** and **178** are controlled respectively by the outputs El and Er from a comparator **190** as the second control unit for the left and right control which detects the difference in the levels of the left signal L and the right signal R. In this manner, it is possible to obtain the same effect as the decoder shown in FIG. **13** by detecting the difference in the signal levels.

As above described, according to this invention it is possible to greatly improve the separation between respective channels and to independently reproduce sounds from respective channels without impairing the necessary information contained therein. Moreover, as it is impossible to substantially eliminate undesirable cross-talk signals which in most cases have different phases from the main signal, the quality of the reproduced sound field is greatly improved and the optimum audible area is widened greatly.

Although the invention has been shown and described in terms of some preferred embodiments thereof, it will be clear that many changes and modifications will be obvious to one skilled in the art without departing from the true spirit and scope of the invention as defined in the appended claims. For example, the two channel signals may be respectively divided into a plurality of frequency bands, and thus control signals are produced for the respective frequency bands to control variable matrices associated with two channel signals in the corresponding frequency bands.

What we claim is:

1. A decoder for use in a directional sound system wherein at least four directional audio input signals are encoded into two channel signals and the two channel signals are decoded into at least four audio output signals corresponding to said audio input signals, said two channel signals having an amplitude ratio and a phase relationship, said decoder comprising:

at least one control unit responsive to the phase relationship between said two channel signals for producing first and second control signals;

first matrix means connected to receive said two channel signals for combining said two channel signals to produce two audio output signals corresponding to two directional audio input signals, said first matrix means including means responsive to said first control signal for varying at least the amplitude ratio of said two channel signals contained in each of said output signals; and

second matrix means connected to receive said two channel signals for combining said two channel signals to produce two audio output signals corresponding to two remaining directional audio input signals, said second matrix means including means responsive to said second control signal for varying at least the amplitude ratio of said two channel signals contained in each of said output signals.

2. A decoder according to claim **1** wherein each of said first and second matrix means comprises a resistive matrix circuit including at least one variable resistor, said two audio output signals are derived out from the opposite terminals of said variable resistor and the variable resistors of said first and second matrix means are

controlled by said first and second control signals to vary the amplitude ratios of said two channel signals contained in said output signals.

3. A decoder according to claim **2** wherein said variable resistors included in said first and second matrix means comprise photoconductive elements and wherein there are provided first and second light sources for illuminating said photoconductive elements and first and second control circuits responsive to said first and second control signals for controlling the brightness of said first and second light sources.

4. A decoder according to claim **1** wherein said first matrix means comprises a first differential amplifier having first and second input terminals, said first input terminal being connected to receive one channel signal; means for reversing the phase of the other channel signal; means for coupling the output from said phase reversing means to the second input terminal of said first differential amplifier; and means responsive to said first control signal for controlling the gain of said first differential amplifier, and wherein said second matrix means comprises a second differential amplifier having first and second input terminals connected to receive said two channel signals respectively and means responsive to said second control signal for controlling the gain of said second differential amplifier.

5. A decoder according to claim **1** further comprising:

first means for producing a sum output of said two channel signals;

second means for producing a sum output of said two channel signals having the opposite polarity to that of the output of said first means;

third means for producing a difference output of said two channel signals; and

fourth means for producing a difference output of said two channel signals having the opposite polarity to that of said third means;

wherein said first matrix means includes first variable gain amplifier means connected to receive the output of said third means, said variable gain amplifier means being controlled in its gain in response to said first control signal;

fifth means for combining the output from said first variable gain amplifier means and the output from said first means; and

sixth means for combining the output from said first variable gain amplifier means and the output from said second means; and

wherein said second matrix means includes second variable gain amplifier means connected to receive the output from said first means, said variable gain amplifier means being controlled in its gain in response to said second control signal;

seventh means for combining the output from said second variable gain amplifier means and the output from said third means; and

eighth means for combining the output from said second variable gain amplifier means and the output from said fourth means.

6. A decoder according to claim **5** wherein said two channel signals are expressed by $L = FL + \Delta FR + jRL + j\Delta RR$ and $R = FR + \Delta FL - jRR - j\Delta RL$ where FL, FR, RL and RR represent directive audio input signals and Δ represents a constant equal to about 0.414; the gain of said first variable gain amplifier means varies between substantially 0 and 2.41 in response to said first control signal; and wherein the gain of said second variable gain amplifier means varies between substantially 0 and 2.41 in the opposite direction to said gain of said first variable gain amplifier means in response to said second control signal.

7. A decoder according to claim **1** wherein said control unit includes a phase discriminator for detecting the phase difference between said two channel signals.

8. A decoder according to claim **7** wherein said phase discriminator comprises first means connected to receive one channel signal for producing a rectangular wave output; second means connected to receive the other channel signal for producing a rectangular wave output; third and fourth means which are connected to receive the output from said first means for producing outputs of opposite polarities; and first and second switching means which are alternately rendered ON and OFF in response to the outputs from said third and fourth means, the input sides of said first and second switching means being connected to receive the output of said second means to thereby produce first and second control signals from the output sides of said first and second switching means, the magnitudes of said first and second control signals varying in opposite directions in accordance with the phase difference between said two channel signals.

9. A decoder according to claim **1** wherein said control unit includes a comparator for detecting the phase relationship between said two channel signals in accordance with level difference between sum and difference signals of said two channel signals.

10. A decoder as claimed in claim **9** wherein said comparator comprises a first logarithmic amplifier connected to receive a sum signal of said two channel signals; a second logarithmic amplifier connected to receive a difference signal of said two channel signals; first means to rectify the output of said first logarithmic amplifier; second means for rectifying the output of said second logarithmic amplifier; and a differential amplifier connected to receive the outputs from said first and second means for producing first and second outputs, the magnitudes of which vary in the opposite directions in accordance with the phase relationship between said two channel signals.

11. A decoder according to claim **5** wherein each of said first and second variable gain amplifier means has a frequency characteristic such that it manifests a relatively low gain for signals having frequencies less than a first predetermined frequency and a relatively high gain for signals having frequencies less than a second predetermined frequency regardless of the magnitudes of said first and second control signals.

12. A decoder according to claim **11** wherein said first predetermined frequency is about 200 Hz and said second predetermined frequency is about 5000 Hz.

13. A decoder according to claim **5** wherein each of said first and second variable gain amplifier means includes means for substantially preventing signals contained in the input signal and having frequencies lower than a first predetermined frequency from being applied to said amplifier means and means for operating said amplifier means at a high gain for signals contained in the input signal and having frequencies higher than a second predetermined frequency which is higher than said first predetermined frequency regardless of the magnitudes of said first and second control signals.

14. A decoder according to claim 5 wherein each of said first and second variable gain amplifier means comprises a variable gain amplifier connected to mainly receive input signals having intermediate frequencies in the entire audible frequency band and a fixed gain amplifier connected to mainly receive input signals having higher frequencies than said intermediate frequencies.

15. A decoder according to claim 14 which further comprises a bandpass filter connected to the input of said variable gain amplifier and a high-pass filter connected to the input of said fixed gain amplifier.

16. A decoder according to claim 5 further comprising

a second control unit for producing third and fourth control signals in response to said two channel signals;

third variable gain amplifier means connected to receive a first channel signal, said variable gain amplifier means being controlled in its gain by said third control signal;

ninth means for producing a sum output of the output of said third variable gain amplifier means and a second channel signal;

10th means for producing a difference output of the output said third variable gain amplifier and the second channel signal;

fourth variable gain amplifier means connected to receive the second channel signal, said fourth variable gain amplifier means being controlled in its gain by said fourth control signal;

11th means for producing a sum output of the output of said fourth variable gain amplifier end the first channel signal;

12th means for producing a difference output of the output of said fourth variable gain amplifier and the first channel signal;

13th means for combining the output of said fifth means and the output of said ninth means at a predetermined amplitude ratio;

14th means for combining the output of said sixth means and the output of said eleventh means with a predetermined amplitude ratio;

15th means for combining the output of said seventh means and the output of said tenth means at a predetermined amplitude ratio; and

16th means for combining the output of said eighth means and the output of said twelfth means with a predetermined amplitude ratio.

17. A decoder according to claim 16 further comprising first and second phase shifters for introducing a predetermined phase difference between said two channel signals; adder means for adding the outputs of said first and second phase shifters; and subtractor means for producing a difference output of the outputs of said first and second phase shifters; and wherein said second control unit includes a phase discriminator for detecting the phase difference between the outputs of said adder means and subtractor means.

18. A decoder according to claim 16 wherein said second control unit includes a comparator for detecting level difference between said first and second channel signals.

19. A decoder according to claim 1 wherein said control unit produces said first control signal of the maximum level and said second control signal of the minimum level when the phase difference between said two channel signals is about 0°; said first and second control signals having the identical level when the phase difference is about 90°, and said first control signal of the minimum level and second control signal of the maximum level when the phase difference is about 180°.

20. A decoder adapted to decode two channel signals L and R each containing at least three of four directional audio signals FR, FL, RL and RR, into reproduced four channel signals FR′, FL′, RL′ and RR′ respectively corresponding to said directional audio signals FR, FL, RL and RR, said decoder comprising: a control unit responsive to the phase relationship between said two channel signals L and R for producing first and second control outputs which vary in opposite directions with reference to a predetermined reference level; first matrix means connected to receive said two channel signals L and R for producing said reproduced signals FL′ and FR′ which are expressed by $mL + nR$ and $nL + mR$, respectively, where m and n represent variable matrix coefficients which vary in the opposite directions in accordance with said first control output; and second matrix means connected to receive said two channel signals L and R for producing reproduced signals RL′ and RR′ which are expressed by $pL - qR$ and $qL - pR$, respectively, where p and q represent variable matrix coefficients which vary in the opposite directions in accordance with said second control output and said coefficients m and p vary in the opposite directions by said first and second control outputs.

21. A decoder adapted to decode two channel signals L and R, each containing at least three of four directional audio signals FR, FL, RL and RR into reproduced four channel signals FR′, FL′, RL′ and RR′ respectively corresponding to said directional audio signals FR, FL, RL and RR, said decoder comprising: a control unit responsive to the phase relationship between said two channel signals L and R for producing first and second control outputs which vary in the opposite directions with reference to a predetermined reference level; first matrix means connected to receive said two channel signals L and R for forming said reproduced signals FL′ and FR′ which are expressed by $(1+f)L + (1-f)R$ and $(1+f)R + (1-f)L$, respectively, where f represents a variable matrix coefficient which is controlled by said first control output; second matrix means connected to receive said two channel signals L and R for forming said reproduced signals RL′ and RR′ which are expressed by $(1+b)L - (1-b)R$ and $(1+b)R - (1-b)L$, respectively, where b represents a variable matrix coefficient which is controlled by said second control output, said coefficients b and f varying in the opposite directions.

22. A decoder according to claim 21 wherein said two channel signals L and R are expressed respectively by $FL + \Delta FR + jRL + j\Delta RR$ and $FR + \Delta FL - jRR - j\Delta RL$ where Δ equals substantially 0.414 and wherein said variable matrix coefficients f and b vary in opposite directions between substantially 0 and 2.41 in response to said first and second control outputs.

23. A decoder adapted to decode two channel signals L and R, each containing at least three of four directional audio input signals FL and FR associated with front left and right channels, RL and RR associated with rear-left and right channels, into reproduced four channel output signals, said decoder comprising:

a first control unit responsive to the level ratio between the front and rear audio input signals con-

tained in the two channel signals for producing first and second control signals, the magnitudes of which vary in opposite directions;

a second control unit responsive to the level ratio between the left and right audio input signals contained in the two channel signals for producing third and fourth control signals, the magnitudes of which vary in opposite directions;

first means connected to receive said two channel signals L and R for producing an output proportional to a signal $(1+f+\sqrt{2})L + (1-f+\sqrt{2}l)R$, where f and l represent coefficients which vary over a predetermined range;

second means connected to receive said two channel signals L and R for producing an output proportional to a signal $(1+f+\sqrt{2})R + (1-f+\sqrt{2}r)L$, where f and r represent coefficient which vary over a predetermined range;

third means connected to receive said two channel signals L and R for producing an output proportional to a signal $(1+b+\sqrt{2})L - (1-b+\sqrt{2}l)R$, where b and l represent coefficients which vary over a predetermined range;

fourth means connected to receive said two channel signals L and R for producing an output proportional to a signal $(1+b+\sqrt{2})R - (1-b+\sqrt{2}r)L$, where b and r represent coefficients which vary over a predetermined range;

fifth means responsive to said first control signal for varying said coefficient f;

sixth means responsive to said second control signal for varying said coefficient b;

seventh means responsive to said third control signal for varying said coefficient r; and

eigth means responsive to said fourth control signal for varying said coefficient l.

24. A decoder according to claim **23** wherein said two channel signals L and R are expressed respectively by $FL + \Delta FR + jRL + j\Delta RR$ and $FR + \Delta FL - jRR - j\Delta RL$ where Δ equals substantially 0.414 and said coefficients f, b, r and l vary respectively between substantially 0 and 3.414.

25. A decoder adapted to decode first and second channel signals, each containing at least three of four audio signals associated with front-left and right channels and rear-left and right channels, into four channel signals, said decoder comprising:

first means responsive to the level ratio between the front and rear audio input signals contained in the two channel signals for producing first and second control signals; the magnitudes of which vary in opposite directions;

second means responsive to the level ratio between the left and right audio input signals contained in the two channel signals for producing third and fourth control signals the magnitudes of which vary in opposite directions;

third means for producing a difference signal of the first and second channel signals;

fourth means responsive to said first control signal for varying the amplitude of the output signal from said third means;

fifth means for producing a sum signal of the first and second channel signals;

sixth means responsive to said second control signal for varying the amplitude of the output signal from said fifth means;

seventh means responsive to said third control signal for varying the amplitude of the first channel signal;

eighth means responsive to said fourth control signal for varying the amplitude of the second channel signal;

ninth means for combining the first and second channel signals, the output signal from said fourth means, and the output signal from said eighth means with the same polarities and a first predetermined relative amplitude ratio;

10th means for combining the first and second channel signals, the output signal from said fourth means, and the output from said seventh means with a relationship wherein the output signal from said fourth means is opposite in polarity to the remaining three signals, and a second predetermined relative amplitude ratio;

eleventh means for combining the first and second channel signals, the output signal from said sixth means, and the output signal from said eighth means with a relationship wherein the first channel signal and the output signal from said sixth means are opposite in polarity to the remaining two signals, and a third predetermined relative amplitude ratio; and

12th means for combining the first and second channel signals, the output signal from said sixth means and the output signal from said seventh means with a relationship wherein the second channel signal and the output signal from said sixth means are opposite in polarity to the remaining two signals, and a fourth predetermined relative amplitude ratio.

26. A decoder according to claim **25** wherein said first amplitude ratio is substantially $(1+\sqrt{2}) : 1 : 1 : \sqrt{2}$, said second amplitude ratio substantially $1 : (1+\sqrt{2}) : 1 : \sqrt{2}$, said third amplitude ratio substantially $(1+\sqrt{2}) : 1 : 1 : \sqrt{2}$, and said fourth amplitude ratio substantially $1 : 1 (1+\sqrt{2}) : 1 : \sqrt{2}$.

27. A decoder according to claim **25** wherein said fourth and sixth means vary in opposite directions the amplitudes of the input signals therefor over a range between substantially 0 and 3.414, and said seventh and eighth means vary in opposite directions the amplitudes of the input signals therefor over a range between substantially 0 and 3.414.

28. A decoder adapted to decode first and second channel signals, each containing at least three of four audio signals associated with front-left and right channels and rear-left and right channels, into four channel signals, said decoder comprising:

first means responsive to phase relationship between the front and rear channels for producing first and second control signals, the magnitudes of which vary in opposite directions;

second means for producing a difference signal of the first and second channel signals;

third means responsive to said first control signal for varying the amplitude of the output signal from said second means;

fourth means for producing a sum signal of the first and second channel signals;

fifth means responsive to said second control signal for varying the amplitude of the output signal from said fourth means;

sixth means for combining the first and second channel signals, and the output signal from said third means with the same polarities;

seventh means for combining the first and second channel signals, and the output signal from said third means with a relationship wherein the first and second channel signals are opposite in polarity to the output signal from said third means;

eighth means for combining the first and second channel signals and the output signal from said fifth means with a relationship wherein the second channel signal is opposite in polarity to the remaining two signals; and

ninth means for combining the first and second channel signals and the output signal from said fifth means with a relationship wherein the first channel signal is opposite in polarity to the remaining two signals.

29. A decoder according to claim **28** wherein said third and fifth means vary in opposite directions the amplitudes of the input signals therefor over a range from about 0 to 2.414.

30. A decoder according to claim **16** wherein each of said variable gain amplifier means has a frequency characteristic such that is manifests a relatively low gain for signals having frequencies less than a first predetermined frequency and a relatively high gain for signals have frequencies less than a second predetermined frequency regardless of the magnitudes of said first and second control signals.

31. A decoder according to claim **30** wherein said first predetermined frequency is about 200 Hz and said second predetermined frequency is about 5000 Hz.

32. A decoder according to claim **16** wherein each of said variable gain amplifier means includes means for substantially preventing signals contained in the input signal and having frequencies lower than a first predetermined frequency from being applied to said amplifier means and means for operating said amplifier means at a high gain for signals contained in the input signal and having frequencies higher than a second predetermined frequency which is higher than said first predetermined frequency regardless of the magnitudes of said first and second control signals.

33. A decoder according to claim **16** wherein each of said variable gain amplifier means comprises a variable gain amplifier connected to mainly receive input signals having intermediate frequencies in the entire audible frequency band and a fixed gain amplifier connected to mainly receive input signals having higher frequencies than said intermediate frequencies.

34. A decoder according to claim **33** which further comprises a bandpass filter connected to the input of said variable gain amplifier and a high-pass filter connected to the input of said fixed gain amplifier.

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