# United States Patent

[11] **3,624,634**


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[73] Assignee **RCA Corporation**


[54] **COLOR DISPLAY**
**11 Claims, 8 Drawing Figs.**


[52] **U.S. Cl.** ..... **340/324 A,** 178/5.2 R, 178/5.4 CD
[51] **Int. Cl.** ..... **G06f 3/14**
[50] **Field of Search** ..... 340/324 A; 178/5.4 CD, 5.4 R, 5.2 R



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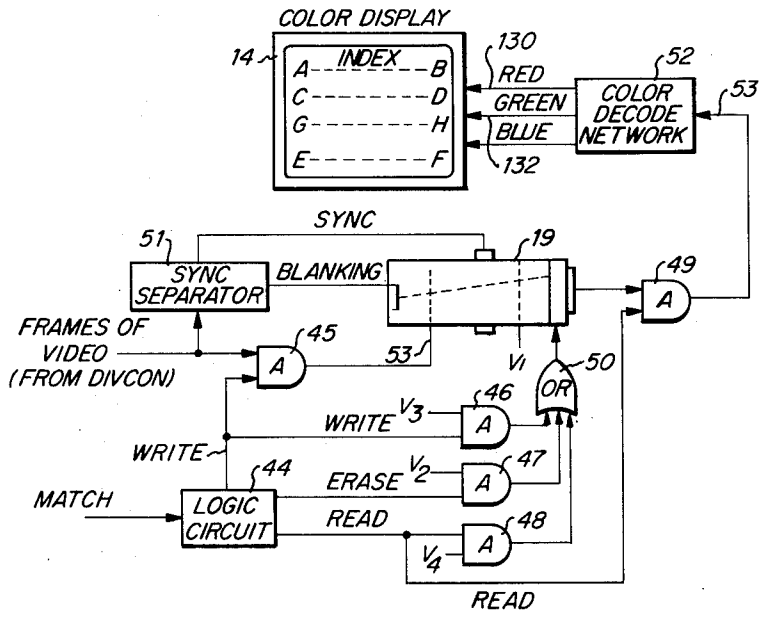
**ABSTRACT:** A data source transmits data signals, which represent information to be displayed and the colors in which it is to be displayed, to a display means such as a kinescope. The color-indicating data signals are stored for one line time and the stored signals are employed to cause the display means to display the remaining data signals of the line in the color called for by the stored signal.

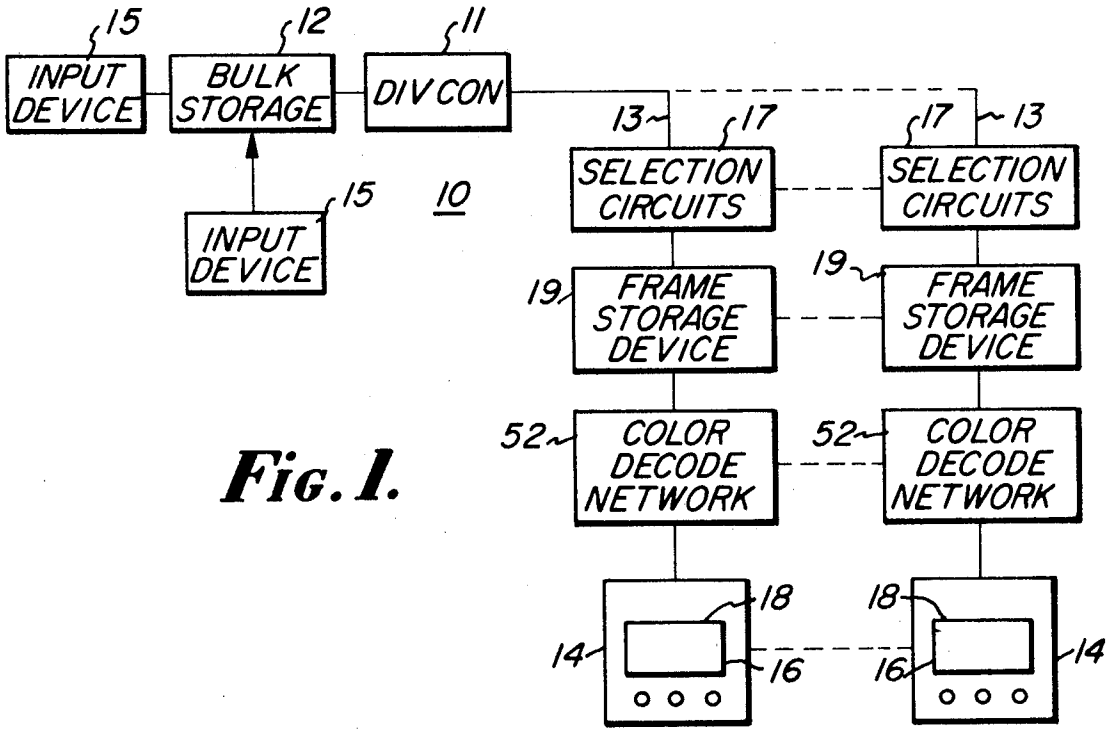



Fig. 1.

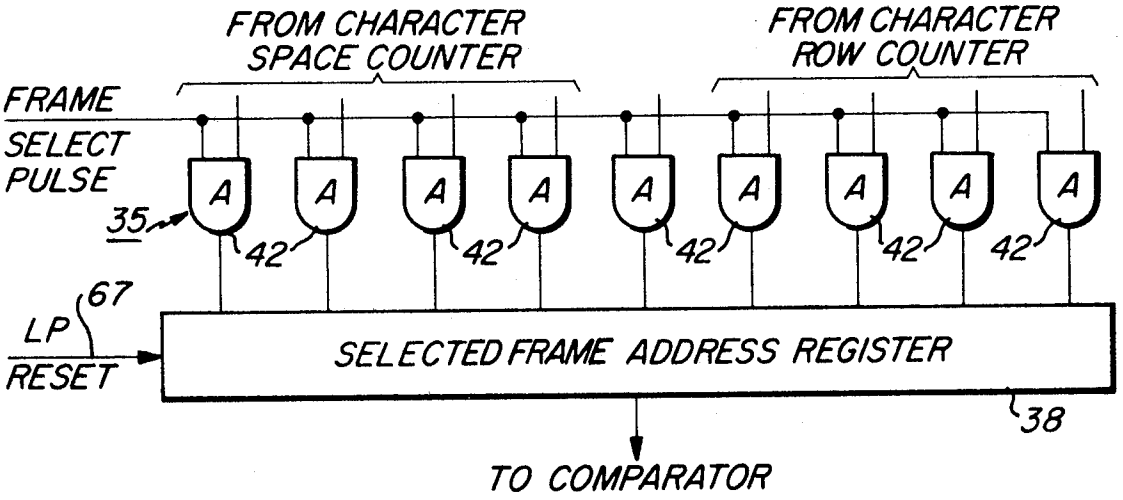



Fig. 5.

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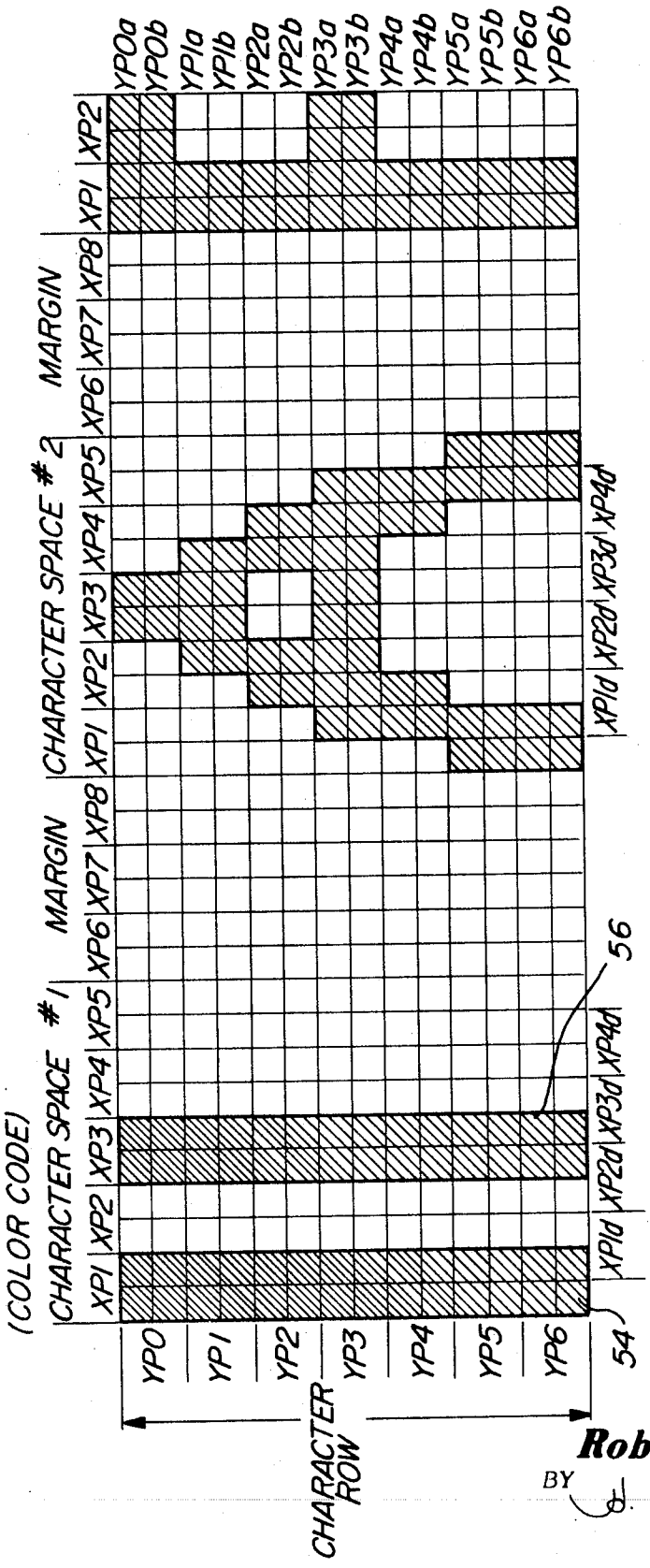


Fig. 2.

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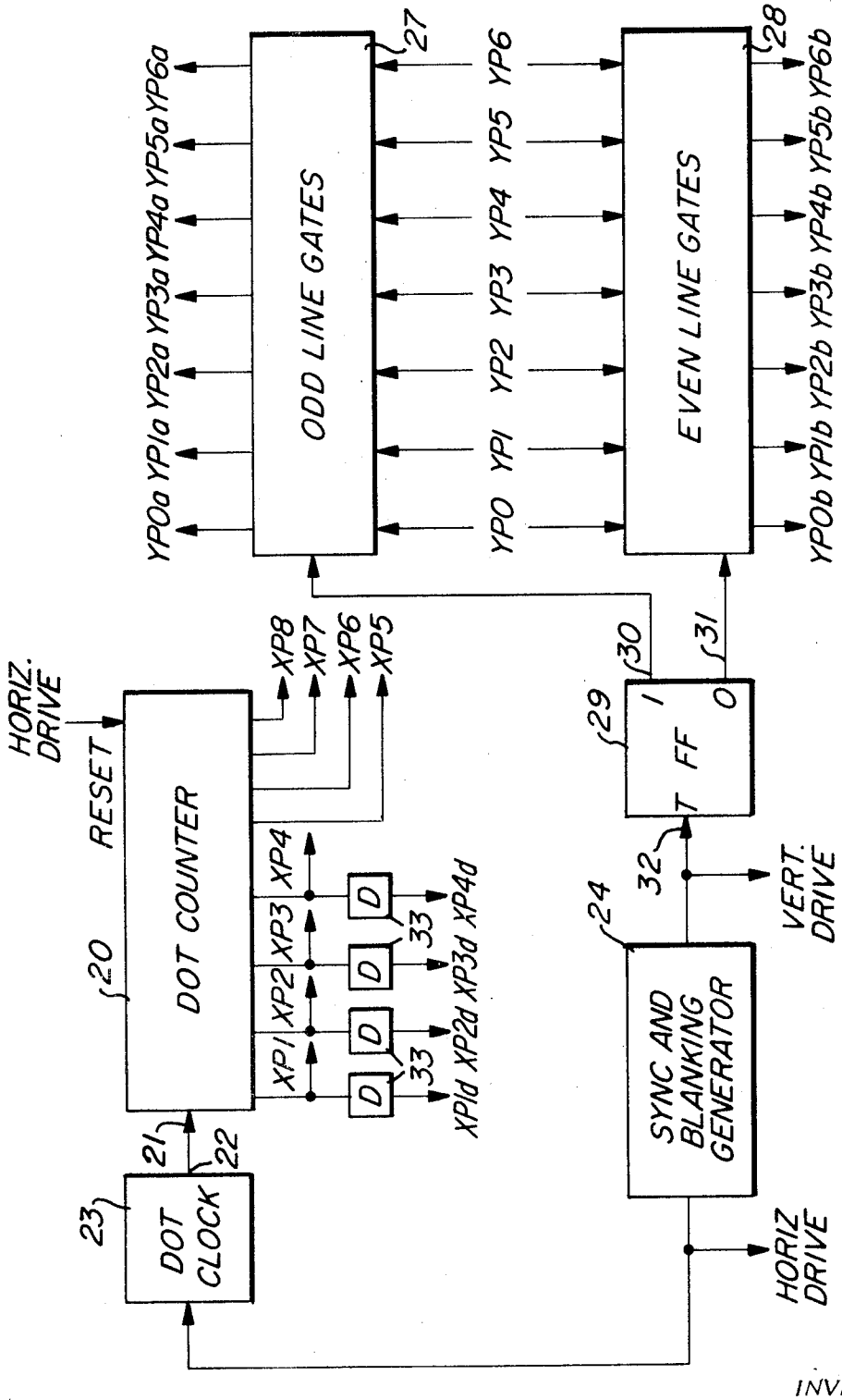


Fig. 3.

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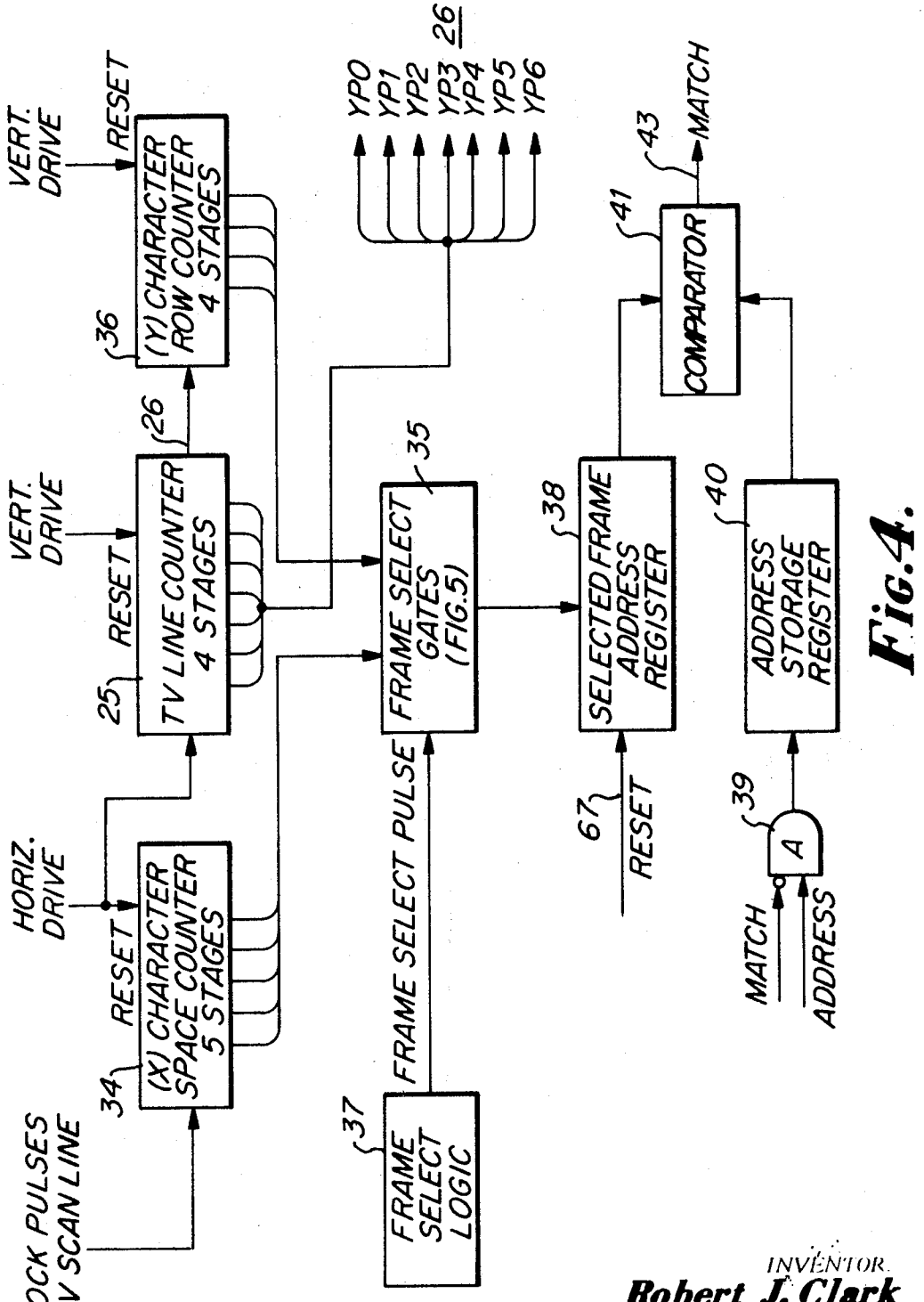


Fig.4.

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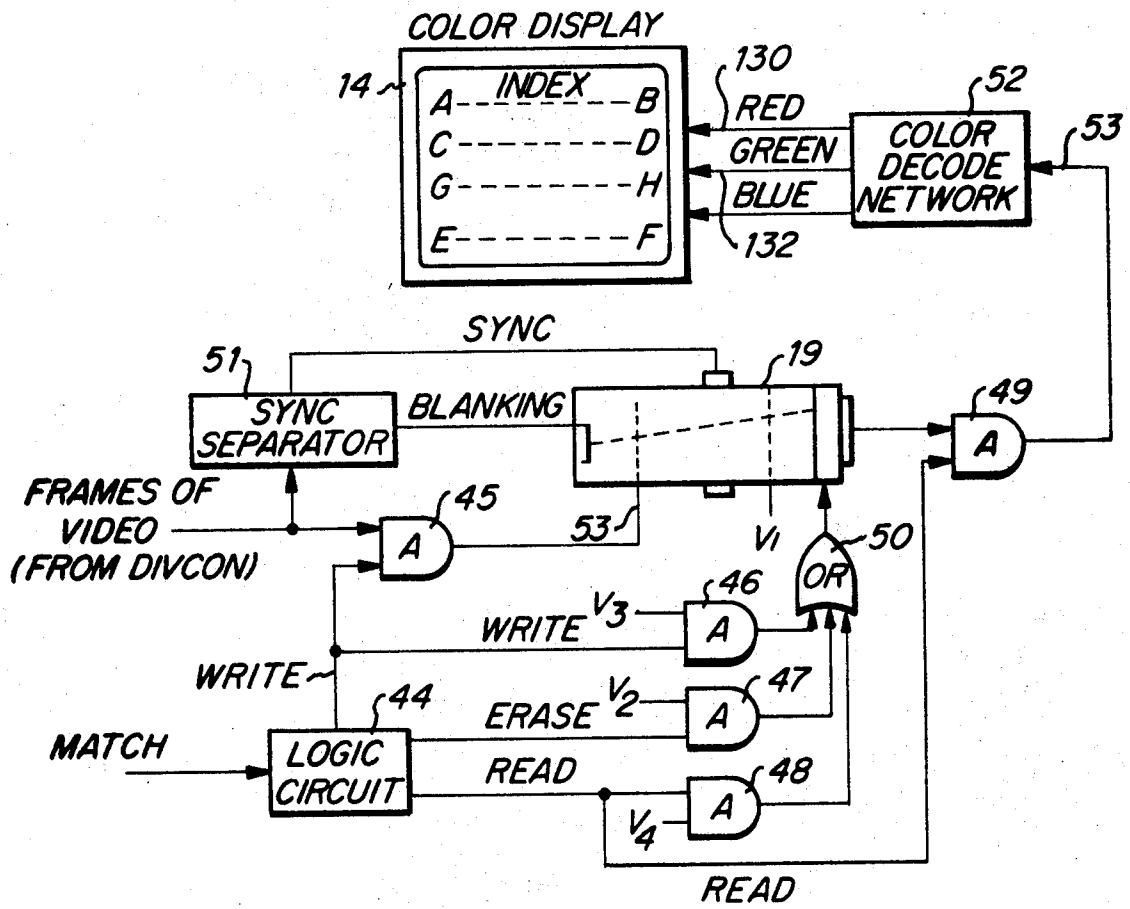


*Fig. 6.*

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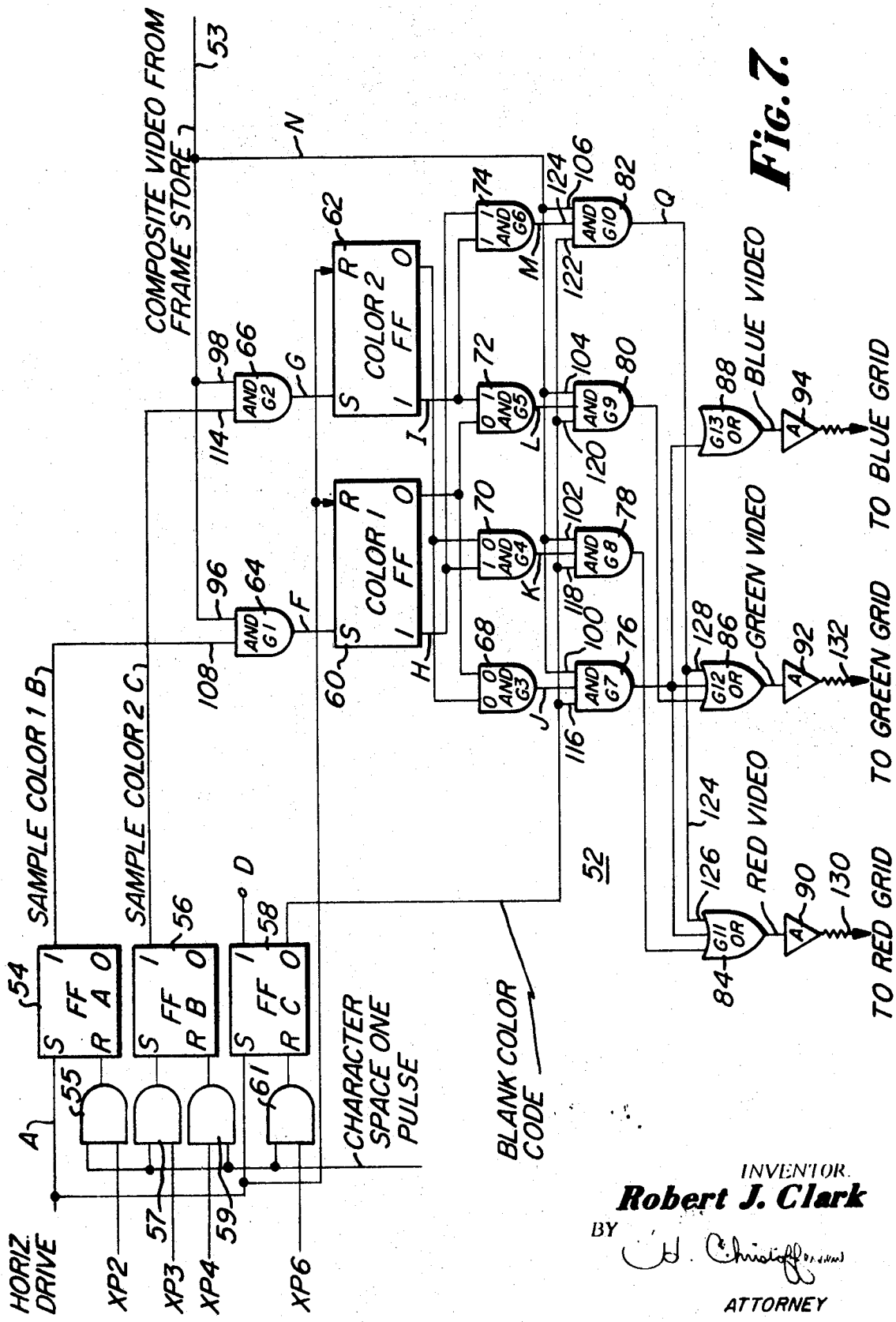


Fig. 7.

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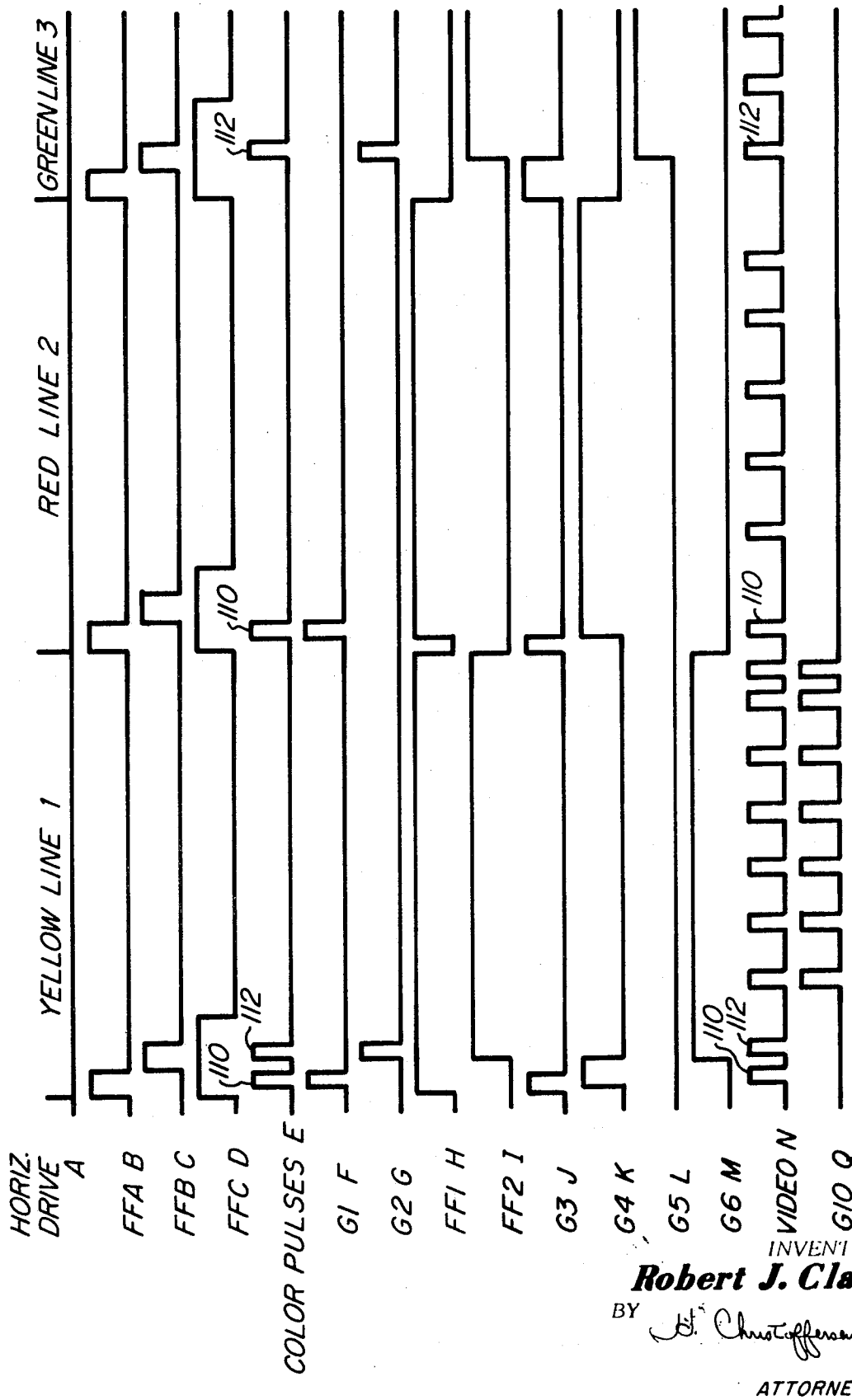


Fig. 8.

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# COLOR DISPLAY

## BACKGROUND OF THE INVENTION

Data terminal displays are becoming increasingly popular in computer and data processing applications. Such displays not only are pleasing to the eye but they permit emphasis to be placed on certain data on the display screen. One method of emphasizing data is to display different lines or rows of data in different colors.

It is the object of this invention to provide a relatively simple and inexpensive system for displaying lines or rows of data in different colors on a data display terminal.

## SUMMARY OF THE INVENTION

A color display means which includes means responsive to input data signals for displaying the signals and means responsive to color-controlling signals for causing the displayed data to be displayed in the colors called for by the color-controlling signals. Means are included for producing for each line of information to be displayed, data signals including a color-indicating manifestation for indicating the color in which the data signals in that line are to be displayed. Means responsive to the color-indicating manifestation store the color-indicating signal for one line time, and in response to the stored signal, applies a color-controlling signal to the means responsive to the color-controlling signals of the color display means, for that line time, and in response to the stored signal, applies a color-controlling signal to the means responsive to the color-controlling signals of the color display means, for that line time. The remaining data signals for that same line time are concurrently applied to the means responsive to data signals of the color display means.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is an overall block diagram of a display system which may embody the invention;

FIG. 2 is a graphical illustration of the formation of individual characters including the color select pulses and the manner in which they may be displayed on the display device;

FIG. 3 is a logic diagram useful in the understanding of the basic timing of the system;

FIG. 4 is a logic diagram of a system which may employ the frame selection process of the system;

FIG. 5 is a detailed logic diagram of the frame select gates shown in FIG. 4;

FIG. 6 is a diagram illustrating how a frame of selected video may be processed for display on the display device;

FIG. 7 is a color decode network which embodies the invention; and

FIG. 8 is a group of waveforms which are helpful in understanding the operation of the color decode network of FIG. 7.

## DETAILED DESCRIPTION

For purposes of the present invention, the color display system which embodies the invention is described as operating with the information retrieval and display system of application Ser. No. 667,543, now, abandoned filed Sept. 13, 1967 by the present inventor and assigned to the same assignee of this application. It is to be understood, however, that this use is merely illustrative as the invention is equally suitable for use in many other applications.

FIG. 1 is an overall block diagram of the information retrieval and display system 10 of the aforementioned reference, that retrieves informational data stored in a bulk storage device 12 and transmits the data to any of a plurality of display networks 13. Each display network 13 includes one color display device 14 for displaying the data. The bulk storage device 12 may, for example, comprise a magnetic storage system such as a magnetic core memory, magnetic drum or a magnetic disk. A plurality of input devices 15, such as keyboards, insert the informational data in the storage



device 12 to be stored therein. The keyboard entries to the storage device 12 are in the form of binary characters. The color display devices 14 include conventional, commercially available, color television picture tubes 16, for displaying the characters. In accordance with the present invention, a color decode network 52 is included for decoding the data in the rows of video received from the frame storage device 19, to permit the individual rows of information to be displayed in a color called for by a color control signal in that row of data. Details are given later.

In order to display the informational data stored in binary character form in the storage device 12 on a television picture tube 16, it is necessary to convert the binary characters into corresponding video signals in a digital-to-video converter (DIVCON) unit 11. The converter unit 11 decodes the binary characters from the storage device 12 and produces the selective blank and unblank signals necessary to display the characters, such as shown in part in FIG. 2, on the faces 18 of the color picture tubes 16.

Conventional television picture tubes exhibit a frame of pictorial images each 1/30 of a second to provide 30 frames per second. Each frame of images is composed of two interlaced fields of scan lines and each field corresponds to a complete scanning of the face 18 of a picture tube 16 from top to bottom. The data to be displayed is, therefore, organized in the storage device 12 in blocks of data arranged to correspond to frames of video signals when converted to video signals in the converter unit 11.

Each successive block of data is converted into a frame of video signals and the fields comprising the frames are transmitted in series to the plurality of display networks 13. Each user or viewer selects a desired frame by actuating selection circuits 17 to extract the desired frame from the other serially occurring frames. One of the serially occurring frames is a master index by means of which, and with the aid of light probe or keyboard, any one of the other frames of stored video may be selected.

The selection is accomplished by incorporating a frame address in each field of video and actuating the selection circuits 17 when the desired frame arrives. For example, a frame address may provide the field video data signals and appear at the top margin of each field. Alternatively, the frame address may be located in one of the first 18 scan lines in a field. These scan lines are not usable for transmitting video data signals since they are generated during the vertical retrace interval occurring between the end of one field and the beginning of the next field. The advantage of utilizing one of these scan lines for this purpose is that the frame address is not displayed on the face 18 of the picture tube 16.

A frame that is actually selected for viewing in any display network 13 is stored in frame storage device 19 for the network and is periodically read out for display on the color picture tube 16 of the network. The frame storage device 19 effectively provides each television color picture tube 16 with a refresh memory and thereby permits a single frame of informational data to be viewed as if the frame were stationary. The frame storage device 19 may comprise a recirculating delay line, a recirculating shift register or any other storage device capable of being read out cyclically. A preferred form of storage device 19 is a nondestructive read out charge storage tube. Such a tube may be scanned in unison with the television color picture tube 16, thereby simplifying read out. Furthermore, analog information such as graphical or pictorial data readily may be stored in such a tube.

It is to be noted that any viewer in any of the display networks 13 may select any frame desired and two or more viewers may view the same or different frames.

FIG. 2 shows the manner in which character patterns may be formed and displayed on a display device, such as a conventional picture tube and shows also how the color coding signals would look, if displayed. In such a tube, the scanning beam that generates the display traverses the face of the tube from left to right and from top to bottom. Each character pat-

tern is composed of a plurality of contiguous dots that are produced by the selective blanking and unblanking of the scanning beam as the beam laterally traverses the display device.

In the black-and-white television picture tube itself, the dots are, of course, white with the background dark, whereas the dots are shown dark on a white background in FIG. 2 for illustrative purposes. It is understood that when a color picture tube is used, these dots may be white or may be in any one of a plurality of colors. The characters shown in character space 1 at dot spaces XP1 and XP3 are the color-indicating signal. While for purposes of this discussion the signals are shown to produce a visible indication, in practice, the screen is blanked for the entire interval corresponding to XP1—XP5 of character space 1, inclusive. All of this is discussed later in connection with FIG. 7. A character such as character A, illustrated at character space 2, may, for example, be five dot spaces wide, regions XP1 through XP5, and may be spaced by a margin of three dot spaces, regions XP6 through XP8, from the next character.

The dots spaces, regions XP1 through XP8, correspond in duration to dot signals XP1 through XP8, respectively, which are generated by a dot counter 20, FIG. 3. The dot signal XP6 may be termed an end-of-character pulse and the dot signal XP8 may be termed the start-of-character pulse The input terminal 21 of the dot counter 20 is connected to an output terminal 22 of a dot clock 23. The dot clock 23 has a pulse repetition rate of 5.12 pulses per microsecond, which produces a scan line having a useful duration of 50 microseconds. This produces 32 character space regions per scan line. The dot clock 23 is synchronized with a sync and blanking generator 24 by means of a horizontal drive pulse. The horizontal drive pulse also resets the dot counter 20. The dot counter, dot clock, and sync and blanking generator are part of the DIVCON unit 11 (FIG. 1).

Each character may also be seven scan lines in height, region YPO through YP6, (FIG. 2). In an interlaced system, the height is formed by two pairs of interlaced scan lines, as shown by the scan lines labeled YPO*a* through YP6*a* and YPO*b* through YP6*b*, respectively, (FIG. 2). Hence, the two interlaced scan lines YPO*a* and YPO*b* are equal in height to one noninterlaced scan line YPO, etc. The alphabetic notations *a* and *b* are appended to the scan line designations to denote, respectively, the odd and even interlaced fields of scan lines. A field of scan lines in an interlace system is a single scan of a display device and two interlaced fields of such scan lines comprise a frame.

The height regions YPO–YP6 (FIG. 2) correspond in duration to line signals YPO–YP6 which are generated by a television (TV) line counter 25 (FIG. 4). The counter 25 which comprises four stages, counts horizontal drive pulses. There are 262 horizontal drive pulses per frame of video. There is, therefore, at the output terminal 26 of the counter 25, one pulse for every 16 input pulses, that is, one pulse each 16 scan lines. The line counter 25 generates the line signals 26, YPO–YP6 denoting the scan line positions, corresponding respectively to counts 1–7, as well as scan line signals denoting positions or margins between character rows. There may be, for example, 16 character rows formed, each row containing 32 characters.

The odd and even interlaced scan lines YPO*a*–YP6*a* therefore, changes state every YPO*b* –YP6*b* are generated by odd and even line gates 27 and 28, respectively, (FIG. 3). These gates, for example, may be AND gates. The input signals to the odd line gates are the line signals YPO–YP6 and the output signal from the "1" terminal 30 of a flip-flop 29. The input signals to the even line gates are the line signals YPO–YP6 and the output signal from the "O" terminal of the flip-flop 29. The input terminal 32 of the flip-flop is connected to the generator 24 which applies the vertical drive pulse to the input terminal 32. The flip-flop 29, therefore, changes state every field period, whereby the odd line gates 27 are enabled during the odd field times and the even line gates 28 are enabled during the even field times. The gates 27 and 28 and the flip-flop 29 are part of the DIVCON unit 11 (FIG. 2).

Each character pattern is formed in a character space array be selectively blanking and unblanking the scanning beam in each scan line. The retentivity of vision of the human eye is relied upon to build up the impression of completely static characters from the separate character slices that are produced each scan line, similar to the manner in which a picture is built up in television. To form the character A (FIG. 2), the scanning beam in the first odd interlaced scan line YPO*a* is blanked during the dot spaces, regions XP1, XP2; unblanked during the dot space, region XP3; and then blanked again during the dot spaces, regions XP4 and XP5. During the remaining scan lines, similar blanking and unblanking occurs until the entire character pattern is formed. To form characters which are more pleasing to the eye, the dot signals XP1 through XP4 are delayed in delay circuits 33 (FIG. 3) to form delayed dot signals XP1*d* through XP4*d*. The delayed dot spaces, regions XP1*d*–XP4*d* (FIG. 2), correspond in duration to the delayed dot signals XP1*d*–*XP4d*. The delayed dot signals may be utilized to bridge over the dot signals XP1–XP5 to prevent any gaps from appearing between dot spaces.

The number of character rows and character spaces is a design choice made on the basis of the size and number of characters desired.

FIG. 4 illustrates portions of the DIVCON unit 11 and the selection circuits 17 which function to select the frame of video to be displayed on the face of the color display device 14 (FIG. 1). A character space counter 34 is connected to a plurality of frame select gates 21 which are shown in greater detail in FIG. 5. The TV line counter 25 is connected to the odd and even line gates 27 and 28 (FIG. 3) and to a character row counter 36, which is connected to the frame select gates 35. A frame select logic network 37 is connected to the gates 35, which in turn are connected to a selected frame address register 38. The system also includes and AND gate 39 which is connected to an address storage register 40. The selected frame address register 38 and the address storage register 40 are connected to a comparator 41.

The character space counter 34 comprises a five-stage counter which counts 32 clock pulses per TV scan line. These clock pulses, for example, may be XP8 pulses, which were earlier termed as start-of-character pulses. The space counter 34 is reset by a horizontal drive pulse which originates in the sync and blanking generator 24 (FIG. 3). There are, therefore, 32 separate counts generated, each of which is indicative of one of the 32 character spaces per TV line. The horizontal drive pulses are connected to the input terminal of the TV line counter 25 which comprises four stages. The counter 25, as was explained earlier, counts the horizontal drive pulses, the first seven counts of the counter generating the line signals YPO–YP6. There is, therefore, at the output terminal 26 of the counter 25, one pulse for every 16 input pulses, that is one pulse each 16 scan lines. The counter 25 is reset at the end of each field period by the vertical drive pulse which is generated by the sync and blanking generator 24 (FIG. 3).

The pulse produced by the counter 25 are applied to the input terminal of the character row counter 36 which comprises four stages. Accordingly, counter 36 counts from 1 to 16 and is reset by the above-mentioned vertical drive pulse. Each count, therefore, is indicative of one of the 16 character rows generated per field.

The output lines of the character space counter 34 and the character row counter 36 are connected in parallel to the input terminals of frame selected gates 35. The signals on these lines (five from 34 and four from 36) comprise a nine-bit word which is indicative of the address, row and character space on the screen of a display. This address is indicative of a frame of video which is stored in the bulk storage device 12 (FIG. 1). For example, refer to FIG. 6, the character A is indicative of the address of one frame of video and the character F is indicative of the address of another frame of video. A frame select pulse, which is generated by the frame select

logic circuit 37 is also applied to the frame select gate 35 when the light probe is pointed at a displayed symbol.

Referring briefly to FIG. 5, it may be seen that the plurality of AND gates 42 which comprise the frame select gates 35 are primed in response to a frame select pulse representing binary "1." The gates 42 each receive also a second signal from the character space counter 34 or the character counter row counter 36. When both signals applied to a gate 42 represent binary "1," the gate becomes enabled. The convention is adopted that a relatively positive signal represents a binary "1" and a relatively negative signal represents a binary "0".

Assume that the master index frame of video is displayed and the viewer wishes to view the frame of video having the address indicative of the character F. The nine-bit word for the character F is 000010000, which is the space-row position of the character F (FIG. 2). If a viewer wishes to view the frame of video which has this particular address, the light probe is pointed at the character F and the frame select logic circuit 37 (FIG. 4) generates a binary "1" signal, which enables and AND gates 42, which are primed, thereby applying the nine-bit word 000010000, in parallel, to the selected frame address register 38. The register 38 stores this particular address until reset by a reset signal generated by the light probe circuit or keyboard, depending upon which is used in the selection circuit. This address is then applied to the comparator circuit 41 (FIG. 4).

Returning to FIG. 4, a match signal is generated at the output terminal 43 of the comparator 41. This signal is a binary "1" when the addresses in the respective registers 38 and 40 are the same and is a binary "0" when the address in register 40 is not the same as the address in register 41. The match signal is applied to a first input terminal of the AND 39, priming the gate when the match signal is a binary "0." Applied to the second input terminal of the AND gate 39 are the serially arriving addresses of the stored frames of video from the DIVCON unit 11 (FIG. 1). As was explained earlier, the frame address may be located in one of the first 18 scan lines in a field. Since two fields comprise a frame of video, there is one frame time between each different address arriving at the second input terminal of the AND gate 39. When the addresses stored in registers 38 and 40 correspond, the comparator generates the match signal, which is a binary "1" This signal then disables the AND gate 39 causing address storage register 40 to retain the last stored address maintaining the match signal at a binary "1" level.

FIG. 6 illustrates one of the color display devices 14, the frame storage device 19 and pertinent portions of the selection circuits 17. The circuit also includes a logic circuit 44, first, second, third, fourth and fifth AND gates 45, 46, 47, 48 and 49, respectively, and OR gate 50, sync separator 51, and a color decode network 52.

The sync separator 51 is synchronized with the synchronization systems of both the DIVCON unit 11 and the color display device 14, whereby the video signals stored in the storage device 19 are read out in proper time sequence for display on the color display device 14, as the sync separator provides sync and blanking signals for the storage device 19. Frames of video signals, each frame comprising two fields, are applied to the sync separator 51 and to a first input terminal of the AND gate 45. Applied to the second input terminal of the AND gate 45 is a "write" signal from the logic circuit 44. The match signal, which was previously described, is applied to an input terminal of the logic circuit 44, whereby the logic circuit 44 successively generates an "erase," a "write" and a "read" signal in response to the match signal being a binary "1." The logic circuit 44 is described in detail in the aforementioned referenced application, and corresponds to the flip-flop 94, OR gate 114, AND gate 116 and counter 118 illustrated at FIG. 3*b* of the reference application.

Assuming the match signal is a binary "1, " the logic circuit first generates an "erase" signal, which is a binary "1," and which is applied to a first input terminal of and AND gate 47. Applied to the second input terminal of the AND gate 47. Applied to the second input terminal of the gate 47 is a voltage V2 which is of a level required for erasing the video information which was stored in the frame storage device 19. The output signal from gate 47 is at a level V2 and is applied to a first input terminal of the OR gate 50. The output signal from the gate 50 is at a level V2 and is applied to the storage device 19.

It requires two interlaced fields of scan lines to be generated to complete the erase cycle, since the storage device 19 scans in synchronism with the display device 14. It may be seen, therefore, that the address of the frame of video which is to be written on the storage device 19 must be contained in the preceding frame of video. For example, if the frame of video which has the address corresponding to the character F (FIG. 6) is selected for viewing, the address for F must be contained in the frame of video preceding the frame containing video identified by F. If this preceding frame happens to be for the character A (FIG. 6), it may be seen, therefore, that the frame of video, two fields, which is indicative of A is arriving serially at the input terminal of the sync separator and the first input terminal of the AND gate 45 at the same time the match signal is a binary "1" in response to the address corresponding to F being stored in the registers 38 and 40 (FIG. 4). Therefore, during the time interval the erase cycle is being generated, the frame of video corresponding to the address for character A is arriving serially at a first input terminal of the gate 45. This gate, however, is disabled since the write signal at the second input terminal is a binary "0."

At the end of these two field periods, the "write" signal is then generated by the logic circuit 44, as the frame of video, two fields, which is indicative of F is arriving serially at the first input terminal of the gate 45, whereby the two fields of video comprising the frame indicative of the F are applied to the control grid 53 of the storage device 19. Accordingly, the erase signal returns to a binary "0" disabling gate 47. Concurrently, the write signal, which is now a binary "1" is applied to a first input terminal of the AND gate 46. Applied to the second input terminal of the gate 46 is a voltage V3 which is of a level required to write into the storage device 19. The output signal which is now at a level V3 is then applied via OR gate 50 to the storage device 19.

The "write" cycle requires two field times to complete since it requires two interlaced scan periods to generate a frame of video. The "write" cycle is completed, therefore, at the same time the frame of video indicative of F has passed through gate 45. The "write" signal then returns to binary "0" disabling gate 45, whereby succeeding frames of video may not be written into the storage device 19.

The logic circuit 44 then generates a "read" signal which is at a binary "1" level and which is concurrently applied to first input terminals of AND gates 48 and 49, respectively. Applied to the second input terminal of the gate 48 is a voltage V4 which is of a level required to read from the storage device 19. The output signal from gate 48 is applied via OR gate 50 to storage device 19 to initiate the read cycle. Applied to the second input terminal of the AND gate 49 is the output signal from the storage device 19, which in this instance is the frame of video indicative of F. The output signal from gate 49, therefore, is this frame of video and is applied to the input terminal of the color decode network 52 and in turn is applied to the deflection circuits of display device 14, whereby the frame of video may be displayed.

FIG. 7 illustrates the color decode network 52 and FIG. 8 illustrates waveforms present in the network of FIG. 7. A frame of black-and-white composite video is transmitted via the line 53 to the color decode network 52. The frame of video is comprised of a plurality of lines of data, each line including a color code or color indicating manifestation which specifies the color in which the data in the particular line is to be displayed on the color display 14 (FIG. 6). Referring briefly to FIG. 2, there is illustrated a portion of one row of data in the frame of video. This row of data is comprised of seven scan lines YP0–YP6, as was explained earlier. The color-indicating manifestation, that is, two pulse signals, either one of or both

of which may be present or absent, for each line of the row of data occurs in the time interval of character space one. The color-1 pulse, when present, occurs at a time corresponding to the XP1 dot regions and the color-2 pulse, when present, occurs at a time corresponding to the XP3 dot regions. By the use of two color code pulses, $2^2$ or four different colors may be indicated for display. Table 1, below illustrates how the four colors are derived.

TABLE I

| Color-1 pulse | Color-2 pulse | Red video amp. | Green video amp. | Blue video amp. | Color on TV monitor |
|---|---|---|---|---|---|
| Absent | Absent | ON | ON | ON | White. |
| Present | Absent | ON | OFF | OFF | Red. |
| Absent | Present | OFF | ON | OFF | Green. |
| Present | Present | ON | ON | OFF | Yellow. |

It is to be understood, of course, that the invention is not limited to the use of two color pulses. More such pulses may be employed to permit more colors to be displayed. For example, a third color pulse may be made to occur at a time corresponding to the dot space region XP5 to permit $2^3$ or eight different colors to be indicated for display and so on. The number of color pulses utilized is merely a design choice.

The circuit of FIG. 7 also includes five storage devices such as flip-flops, three, **54**, **56** and **58**, are connected to store signals indicative of specific time intervals during the character space one interval For example, flip-flop **54** is set by the horizontal drive pulse and is reset by the XP2 pulse during character space one interval. The flip-flop **54**, therefore, is in a set condition during the XP1 time interval which coincides with the time interval during which the color-1 pulse is generated. Flip-flop **56** is set by the XP3 pulse and reset by the XP4 pulse during character space one interval. The flip-flop **56**, therefore, is in a set condition during the XP3 time interval which coincides with the time interval during which the color-2 pulse is generated. Flip-flop **58** is set by the horizontal drive pulse and is reset by the XP6 pulse during character space one interval and is in a set condition, therefore, during the entire character space one time interval.

The remaining flip-flops **60** and **62** are reset by the horizontal drive pulse. Flip-flop **60** is set whenever flip-flop **54** is set and a color-1 pulse concurrently occurs, and flip-flop **62** is set whenever flip-flop **56** is set and a color-2 pulse concurrently occurs. AND gates **64** and **66**, respectively, control the setting of flip-flops **60** and **62**.

AND gates **68**, **70**, **72** and **74** are connected to receive output signals from flip-flops **60** and **62**. The specific conditions shall be discussed in detail later.

AND gates **76**, **78**, **80** and **82** are connected to receive at their first input terminals the signals from gates **68**, **70**, **72** and **74**, respectively. A composite video signal is coupled via line **53** to input terminals **100**, **102**, **104** and **106** of the gates **68**, **70**, **72** and **74**, respectively. The third input terminals **116**, **118**, **120** and **122**, respectively, are connected to the "**0**" output terminal of flip-flop **58**.

Included are OR gates **84**, **86** and **88** which are connected to one or more of the output terminals of the gates **76**, **78**, **80** and **82**. These connections are discussed in detail later. The output terminals of the gates **84**, **86** and **88** are connected to the input terminals, respectively, of red, green and blue video amplifiers **90**, **92** and **94**, respectively.

Referring to FIG. **8**, the horizontal drive pulse is illustrated at A and the output signal from the flip-flop **54** is illustrated at B. As was stated earlier, the flip-flop **54** is set by the horizontal drive pulse and is reset by the XP2 pulse during the character space one interval as the XP2 pulse and character space one pulse enable AND gate **55**. During the time interval flip-flop **54** is set, the signal present at the input terminal **108** of gate **64** is at a relatively positive potential representing a binary "1." If a color-1 pulse **110** (wave E, FIG. **8**) occurs during this set interval, the signal at input terminal **96** of gate **64** goes relatively positive representing binary "1." In this instance, the output signal from the gate **64**, as illustrated at F, is positive (the binary "1" level) and sets the flip-flop **60** to the one state.

As was stated earlier, flip-flop **56** is set by the XP3 pulse and is reset by the XP4 pulse during the character space one interval, as first gate **57** and then gate **59** is enabled. THis flip-flop is in the one state, therefore, only during the time at which the color-2 pulse (**112** in FIG. **8**), if present, occurs. Accordingly, if the color-2 pulse is present on line **53**, AND gate **66** becomes enabled (see G, FIG. **8**) and sets flip-flop **62**.

As was stated earlier, the flip-flop **58** is set to the one state by the horizontal drive pulse and is reset by the XP6 or end-of-character pulse during the character space one interval as gate **61** is enabled. The "**0**" output terminal of this flip-flop is connected to input terminals **116**, **118**, **120** and **122** of gates **76**, **78**, **80** and **82**, respectively. The signal present on this terminal inhibits the respective gates during the character space-1 time interval so that the color code signals are not transmitted to the color display device **14** of FIG. **6** and are not displayed.

When color-1 and color-2 pulses **110** and **112**, respectively, are present in a particular character row of data, the data in that particular row is generated in the color yellow, as may be seen by referring to table I. When both pulses are present, both flip-flops **60** and **62** become set and AND gate **74** connected to the **1** output terminals of these flip-flops becomes enabled. This is illustrated at M of FIG. **8**.

The output signal from gate **74** is applied to the input terminal **124** of gate **82**. Gate **82** is inhibited during the character space one time interval by the set flip-flop **58** (see wave D, FIG. **8**). However, thereafter flip-flop **58** becomes reset priming gate **82** and the latter passes the composite video present on line **53** to OR gates **84** and **86**. The video or data signals on line **53** are illustrated at N in FIG. **8** and the output signals from gate **82** are illustrated at Q. Note that the color-1 and -2 pulses **110** and **112**, as illustrated at N, are not present at Q for the reason already discussed.

As already mentioned, during the line interval after character space **1**, the composite video on line **53** is applied through gate **82** to OR gates **84** and **86**, respectively. The output signals from these gates are coupled to the input terminals of red video amplifier **90** and green video amplifier **92**. These amplifiers translate the data to the form suitable for intensity modulating the red and green control grids of the color display **14** (FIG. **6**). The output signals from these amplifiers, in turn, are coupled to the red and green input terminals **130** and **132** of the color display device **14** (FIG. **6**). As may be seen from table I, when the red video amplifier **90** and the green video amplifier **92** are concurrently on, the data is displayed on the display device **14** in the color yellow.

The data illustrated at line **2** and line **3** time of FIG. **8** illustrates the signals present in the color decode network **52** when the data in a particular line is to be displayed in red (line **2**) or green (line **3**), respectively. Reference to table I, FIG. **7** and FIG. **8** readily illustrates how the colors white, red and green are generated.

In brief, when only the color-1 signal is present, flip-flop **60** becomes set and flip-flop **62** remains reset. AND gate **70** becomes primed and, at the appropriate time, AND gate **78** applies the composite video via OR gate **84** and amplifier **90** to the red grid. When only the color-2 signal is present, the composite video is applied via AND gate **80** and OR gate **86** to the green grid. When neither color-1 nor color-2 signals are present, AND gate **76** applies the composite video via OR gates **84**, **86** and **88** to all three control grids.

The operation of a standard red, green, blue television receiver is well known in the art and will not be discussed in the specification. The operation of such a device is explained in "Color Television Fundamentals," second edition, by Milton S. Kiver.

What has been described is a color display system in which frames of video are selectively displayed on a color display device and the rows of characters in the frame of video may be

displayed in one color only, which is determined by the color signals appearing in the first character space in a particular row of characters.

What is claimed is:

1. In combination:

a color display means including means responsive to input video data signals for displaying data corresponding to said signals and means responsive to color-controlling signals for causing the displayed data to be displayed in the colors called for by said color-controlling signals;

means for producing for each line of information to be displayed video data signals which include a video color-indicating manifestation for indicating the color in which the data signals in that line are to be displayed;

means responsive to said video color-indicating manifestation for storing a color-indicating signal for one line time, and in response to the stored signal, for applying a color-controlling signal to the means responsive to said color-controlling signals of said color display means, for that line time; and

means for concurrently applying the remaining data signals for that same line to the means responsive to data signals of said color display means.

2. In combination:

a color display system including means responsive to input video data display signals for displaying data corresponding to said signals and means responsive to input data color-indicating signals for causing the displayed data to be displayed in the colors called for by said color-indicating signals;

means for producing for each line of information to be displayed video data signals which include both data display signals and a data color-indicating signal for indicating the color in which the data for that line is to be displayed;

means coupled to said means responsive to input video data color-indicating signals and responsive to said data color-indicating signal for storing said color-indicating signal for one line time, and for controlling the color displayed during said line time in response to the stored signal; and

means for concurrently applying the data display signals for that same line to the means responsive to data display signals of said color display means.

3. In combination:

color display means responsive to input video data signals for displaying said signals in colors called for by ones of said data signals;

means for supplying for each line of information to be displayed video data signals, including video color signals for indicating the color in which the data signals in that line are to be displayed;

means responsive to the color signals for storing each color signal for one line time; and

means responsive to said stored color signals for causing the data signals to be displayed in the color called for by said color signals.

4. The combination claimed in claim 3, said color signals occurring during the first data signal space item interval in a line of information.

5. The combination claimed in claim 4, including means for blanking the color signals during the first data signal space time interval, prior to the line of information being displayed.

6. The combination claimed in claim 3, said means responsive to the color signals for storing each color signal for one line time comprising for each color signal means capable of assuming one of two states, said last-named means assuming the first state if a color signal is present and assuming the second state at the end of a line of information.

7. The combination claimed in claim 3, said means responsive to said stored color signals including a plurality of gates and color amplifiers.

8. In a color display system the combination comprising:

a color display device having three input terminals, namely red, green and blue video input terminals;

a source of input video data signals, including video color signals for indicating the color in which the data signals are to be displayed;

means responsive to the video color signals for storing a color-indicating signal for one line time;

three amplifiers, namely a red, green and blue video amplifier;

gate means responsive to said color indicating signal and input video data signals for gating the input data signals to selected ones of said three amplifiers as called for by said color indicating signal; and

means for coupling the red, green and blue video amplifiers to the red, green and blue video input terminals, respectively, of said color display device.

9. A color display apparatus comprising, in combination:

a source of binary data signals representing information to be displayed and including binary data signals denoting the color in which said information is to be displayed;

means for storing a frame of video information to be displayed and for storing, for each line of video information in said frame to be displayed, video signals for indicating the color of that line;

digital-to-video converter means responsive to said binary data signals for supplying to said frame storing means corresponding video data signals;

means responsive to the video data signals indicative of the color of a line for producing color signals corresponding thereto and for storing said signals for the duration of said line; and

color display means responsive to said frame of video data for displaying information corresponding thereto and responsive to said color signals for displaying said data in the color chosen.

10. A color display system comprising, in combination:

a source of binary data signals representing display information and also representing the color in which said information is displayed;

a single digital-to-video converter means responsive to said binary data for producing a plurality of frames of video data corresponding thereto including, for each line of video data, video signals for indicating the color in which that line of data will be displayed;

a plurality of means, each for selecting and storing one of said plurality of frames to be displayed;

a plurality of color display means, each responsive to the video data signals in its said frame storage means for displaying lines of information and responsive to color signals for displaying each line in the color indicated by said color signals; and

a plurality of means, each responsive to the video signals for indicating color in its said frame store means, for producing and storing for one line time, color signals corresponding to the color in which said line of information is to be displayed.

11. The combination as set forth in claim 10 wherein said video signals for indicating color for each line stored in each of said frame store means occurs in a fixed position relative to the information in that line and wherein there is further included means for blanking the video signals for indicating color where that indication would otherwise be displayed in said lines of information.

* * * * *

# UNITED STATES PATENT OFFICE

# CERTIFICATE OF CORRECTION

Patent No. 3,624,634 Dated November 30, 1971

Inventor(s) Robert John Clark

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 1, lines 27 to 30, cancel beginning with "for that line time" to and including "of the color display means,". Column 3, line 30, "useful duration" should read ---useful (visible) duration---; lines 63 and 64, "YP0a-YP6a therefore, changes state every YP0b-YP6b" should read ---YP0a-YP6a and YP0b-YP6b---. Column 4, line 59, "pulse" should read ---pulses---. Column 5, line 21, "and" should read ---the---; line 74, "and" should read ---the---; line 75, cancel "Applied to the second input terminal of the AND gate 47.". Column 8, line 6, "THis" should read ---This---. Column 9, line 6, "a color display" should read ---color display---; line 58, "item" should read ---time---.

Signed and sealed this 19th day of September 1972.

(SEAL)
Attest:

EDWARD M.FLETCHER,JR.
Attesting Officer

ROBERT GOTTSCHALK
Commissioner of Patents

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