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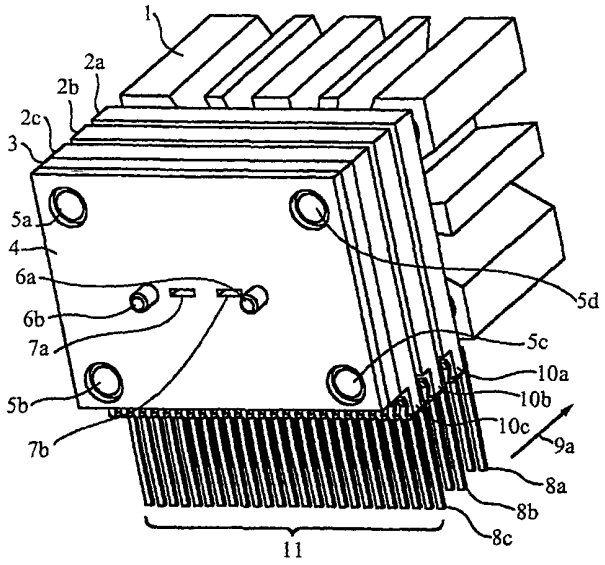
(54) Title: METHOD AND APPARATUS FOR COMBINED ALIGNMENT AND HEAT DRAIN OF STACKED PROCESSING STAGES



(57) Abstract: A method and apparatus for cooling and simultaneously aligning processing devices consisting of stacked processing stages (PS). The invention utilizes heat drain profiles (5a-d) that are held in position and parallel orientation by a heat sink base (1). The heat drain profiles (5a-d) protrude through soldering holes (14) of each processing stage. The soldering holes (14) have a heat bridge characteristic (HTC) defined mainly by their surface material, their surface area, and their fitting precision. The heat drain profiles (5a-d) are of number, size and material such that they drain a minimal thermal energy at the lowest temperature difference between heat sink base (1) and PS for a given HTC. The minimal thermal energy is higher than the maximum thermal energy created within a PS.

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Patent Application of

For

Method and Apparatus for Combined Alignment and Heat Drain of Stacked Processing Stages

Field of Invention

The present invention relates to a method and an apparatus for combined alignment and heat drain of stacked processing stages and in particular to a method and apparatus for combined alignment and heat drain of individual modules of an optical multiplex transceiver.

Background of the Invention

The demand for speed of signal processing in a computer and for capacity in signal communication between several computers is ever increasing. A technique to meet the

demand for high signal transmission is optical multiplexing such as wavelength division multiplexing (WDM) and time division multiplexing (TDM). In the WDM technique, the spectrum of a light beam transmitted in an optical fiber is divided into a number of wavelength divisions, which represent independent signal strings for transmitting information. Each wavelength division is an independent signal carrier. Hence, the advantage of optical multiplexing is its ability to transmit simultaneously in a single optical fiber a high number of information.

In a number of optoelectronic processing stages (OPS) optical signals of distinct wavelength are either collinear emitted or collinear received. These OPS are typically monolithically grown structures with a planar bottom and top surface. The optical signals are emitted or received perpendicular to the planar top surface.

US. Pat. No. 5,487,124 discloses a bi-directional wavelength division multiplex transceiver module, wherein a semi-translucent mirror is used to separate wavelength division multiplexed signals and redirect them to individual OPS's.

Recent research achievements allow the fabrication of semi-translucent OPS's with distinct translucent/opaque properties such that they work simultaneously as an optical bandwidth filter and an optoelectronic converter. These OPS's are made opaque only for the spectrum of their predetermined wavelength division and are sufficiently

translucent for the remaining light spectrum. In case of a receiver, a number of stacked OPS's with distinct absorption spectra are sequentially arranged and absorb the wavelength divisions of a through passing light beam. In case of an emitter each OPS adds its signal in the distinct wavelength division to the passing light beam. As a result, the effort of multiplex transceivers to combine/separate the individual wavelength divisions and direct them from/to the corresponding OPS is significantly reduced such that the number of OPS in a single multiplex transceiver can be increased.

Optical multiplex systems are superior to electrical transmission systems, because they are noise free and enable a much longer transmission distance. These advantages are not only utilized for communication between computers or individual circuit boards but also within a stacked multichip circuit.

US. Pat. No. 5,568,574 discloses modulator-based photonic chip-to-chip interconnections for dense three-dimensional multichip module integration. In this invention, a number of OPS's are embedded within individually manufactured semiconductor structures that perform logical operations and are placed in tightly stacked processing stages (PS) above each other. The OPS's are placed in corresponding alignment in each of the semiconductor structures such that the optical signal beams travel vertically through the semiconductor stack. Thus, circuit boards with their two-

dimensional conductive connections between the individual chips are replaced by a three-dimensional structure.

Semi-translucent OPS open up new possibilities for highly compact, tightly stacked PS. The high processing capacity in such PS produces heat. In conventional two-dimensional arrayed circuits and optoelectronic devices heat dissipation is relatively simple to achieve, since sufficient air contact surface is available for heat exchange. A heat absorbing air stream is thereby either thermally stimulated or provided by a fan.

US. Pat. No. 5,280,191 discloses a packaging for pairs of optical devices having thermal dissipation means. The invention discloses a design of a duplex transceiver with secondary circuitry and a heat sink for cooling. The heat sink is a sheet metal part, which provides flat areas with low thermal convection.

US. Pat. No. 5,513,073 discloses an optical device heat spreader and thermal isolation apparatus. In this invention of a duplex transceiver, the optoelectronic devices are connected to a heat spreader card, which is thermally isolated from the transceiver board. The heat spreading card is a flat sheet metal piece kept in a insolating distance to the transceiver board.

In tightly stacked PS the ratio between air contact surface and generated heat decreases unfavorably. In addition to that, alignment features surrounding the central circuitry

interrupt the heat flow to the remaining air contact surfaces at the sides of the PS.

US. Pat. No. 4,985,805 discloses a device for the cooling of optoelectronic components and a flange joint used therefor. A number of processing stages are stacked above a heat drain base plate. The vertical alignment and heat drain from the processing stages to the base plate is accomplished by vertical metal plates that are laterally attached to the processing stages with screws. The vertical metal plates have no designated alignment features, such that the achievable precision is not sufficient for stacked multiplexing PS. The metal plates have a certain elasticity such that the screw attachment does not provide sufficient contact over the lengths and widths of the PS. Because of their bulkiness, screw connections are generally unfavorable for microelectronic assemblies.

Therefore, there exists a need for a method and apparatus to align a number of processing stages and simultaneously drain their processing heat. The current invention addresses this problem.

High capacity electrical circuitry is generally very sensitive to electromagnetic fields. Therefore, there exists a need for stacked processing stages to shield them against peripheral electromagnetic fields. The current invention addresses this need.

Typically, solid leads and solder pins are used to provide solid electrical ground. In stacked processing stages the available area is limited. Therefore, there exists a need to utilized existing features for a stable electrical ground. The current invention addresses this need.

Objects and Advantages

Accordingly, it is a primary object of the present invention to provide a method and apparatus to simultaneously align a number of tightly stacked processing stages, drain their processing heat and keep them below a predetermined temperature.

It is a further object of the present invention to provide a stable voltage ground for stacked processing stages.

It is a further object of the present invention to provide a faraday shield for stacked processing stages.

Summary of the Invention

The invention achieves alignment and simultaneous cooling of stacked processing stages (PS) with a number of parallel heat drain profiles (HDP) that protrude through soldering holes of each PS establishing mechanical and thermal connections. The contour lengths and the heights of the soldering holes define bridging areas between PS and HDP.

The HDP's are held in position within a heat sink base, which is typically placed on one end of the PS stack. The heat sink base has ribs to increase its air contact surface. The alignment profiles are made of a thermally conductive material like for instance aluminum or copper based alloys.

Each PS has a central processing area (CPA) where the optoelectronic and electronic circuitry is placed. A surrounding ring structure (SRS) captures the radially travelling thermal energy that is produced in the CPA and drains it in the bridging areas to the HDP. The draining capacity is directly proportional to the size of the bridging area, the average temperature difference between the PS's and the HDP's at the bridging area and the quality of the snug fit.

The HDP's are placed in sufficient proximity on the SRS to drain the captured thermal energy such that the temperature difference within the SRS and subsequently within the CPA remains within a predetermined temperature range. The thermal energy travels inside the HDP towards the heat sink base where it is dissipated into the surrounding atmosphere.

Thermal energy flows from a thermal source with a high temperature level to a thermal drain with a low temperature level resulting in a temperature gradient along the thermal path. Materials with good thermal conductivity like

aluminum and copper are a first factor for helping to obtain the flat temperature gradients. The second factor is the size of the section area of the thermal path, which affects directly the slope of the temperature gradient for a given thermal energy flow. In the current invention, each processing stage drains a certain thermal energy at a maximum allowable temperature to the HDP's, raising its temperature level and adding a step in the temperature gradient. The HDP has to have a minimum section area such that the average temperature in the HDP at the most distant PS remains sufficiently below the PS temperature such that enough thermal energy can bridge over.

The preferred application of the invention is an optical multiplex transceiver mainly consisting of several optoelectronic PS's (OPS's). The HDP's are arranged along the direction of the signal light beam. The heat sink base is typically an extrusion profile with cooling ribs and straight holes where the HDP's are soldered in. It is positioned preferably opposite of the cable connecting side. The HDP's have a preferably circular contour, which allows a high fabrication precision with relatively little machining effort. The OPS are stacked next to the heat sink base leaving a certain gap for air circulation. A number of functional stages are placed between the OPS or at the end of the stack as they are known for optical transceiver devices.

Solder ball connections are arrayed on the OPS to provide electrical signal transmission between them.

Each OPS may have on a side an array of laterally extending solder pins that connect the multiplex transceiver mechanically and electrical with a printed circuit board. The solder pins are preferably surface mount an edge of the OPS. The connection with the printed circuit board is optionally provided by edge castellations as they are known to those skilled in the art. The heat sink remains thermally insulated within a certain insulating distance to the printed circuitry board.

The HDP's provide an electrical ground for the OPS by connecting them to the heat sink. The circular arrangement of the HDP's provides thereby a favorable faradic shield effect against peripheral electromagnetic noise.

Brief Description of the Figures

Fig. 1 shows a first perspective view of the preferred embodiment of the invention with the adapter side of the multiplex transceiver being visible.

Fig. 2 shows a second perspective view of the preferred embodiment of the invention with the heat sink side of the multiplex transceiver being visible.

Fig. 3 shows a side view of the preferred embodiment of the invention and a corresponding graph visualizing the temperature distribution in the heat drain profiles.

Fig. 4 shows a front view of an example of a single optoelectronic processing stage with superimposed isothermal curves.

Detailed Description

Although the following detailed description contains many specifics for the purposes of illustration, anyone of ordinary skill in the art will appreciate that many variations and alterations to the following details are within the scope of the invention. Accordingly, the following preferred embodiment of the invention is set forth without any loss of generality to, and without imposing limitations upon, the claimed invention.

The invention performs four main tasks: first to align the processing stages; second to drain sufficient thermal energy from the processing stages; third to keep the stage peak temperature sufficiently below a critical level for a most unfavorable surrounding air temperature and hampering influences like dust on the heat sink; and fourth to provide a stable electrical ground to all stages. In the following, the four main tasks are described in detail.

Fig. 1 shows a perspective view of a preferred application of the invention for an optical multiplex transceiver. It is appreciated that the method and apparatus of the invention may be applied to any processing device, which at least partially consists out of stacked processing stages as they are known to those skilled in the art.

An exemplary number of processing stages **2a**, **2b**, **2c** are stacked together with a first functional stage **3** and a

second functional stage **4** on the heat drain profiles **5a-d**. The heat drain profiles **5a-d** drain the heat created during the functional operation of the processing stages **2a**, **2b**, **2c** in the heat drain direction **9a** into a heat sink base **1**. Each of the processing stages **2a**, **2b**, **2c** has a solder pin array **8a**, **8b**, **8c**, which consist of surface mounted solder pins that extend laterally from socket shoulders **10a**, **10b**, **10c** as it is known to those skilled in the art. The solder pin arrays **8a**, **8b**, **8c** form a solder pin matrix **11**, which provides a two dimensional mechanical connection and a number of electrical contacts in a final assembly position on a printed circuit board (not shown). It is appreciated that the solder pins may be edge castellations as they are known to those skilled in the art. The solder pin arrays **8a**, **8b**, **8c** may also drain some heat.

The heat drain profiles **5a-d** are pressed into base holes **12a-d** (see **Fig. 2**) of the heat sink base **1**. The heat sink base **1** is preferably an extruded profile made of aluminum or copper based material with an extrusion direction parallel to the main heat drain direction **9a**. Design features of extruded fabricated profiles are generally parallel, which allows a precise alignment of the heat drain profiles **5a-d**. In an optional reaming operation the precision of the dimension and parallel orientation of the base holes **12a-d** can be additionally increased.

The heat drain profiles **5a-d** are made of a core material with a high thermal conductivity and have a preferably circular section, which allows them to be manufactured with

the requisite precision. The core material is preferably an aluminum based material or a copper based material. Optional surface coatings like for instance gold or silver coating prevent oxidation and raise the thermal contact conductivity of the heat drain profiles **5a, 5b, 5c, 5d.**

The processing stages **2a, 2b, 2c** carry in a central processing area the processing circuitry and are stacked on the heat drain profiles **5a-d** with their soldering holes **14** (see **Fig. 2**). The soldering holes **14** have sufficient tolerance in shape, orientation and position to the heat drain profiles **5a-d** to avoid strain on the assembled processing stages **2a, 2b, 2c.** To fixate the processing stages **2a, 2b, 2c** and to establish thermal and electrical conductivity the heat drain profiles **5a-d** are soldered in the soldering holes **14.**

Thermal energy is generated as a by-product of the operational function of the processing circuitry in the central processing area of the processing stages **2a, 2b, 2c.** This radial energy is radially transmitted to the periphery where the soldering holes are located. Each processing stage **2a, 2b, 2c** has a maximum thermal processing energy (MTPE) that is generated during full stage operation and during a given time unit (TU). The thermal energy causes a rise of the stage temperature, which has to remain with a safety distance **60** (see **Fig.3**) below a critical level **61** (see **Fig.3**) under worst conditions. The worst conditions are defined by a high surrounding air temperature **45** and eventual reduction of

the cooling capacity of the heat sink base **1** because of deposited dust that may clog the ribs **16**.

The soldering holes **14** are of a hole material with high thermal contact conductivity (TCC) and define with their section length and their height a bridging area. The TCC and the size of the bridging area define a maximum thermal bridging energy (MTBE) that can bridge from one of the processing stages **2a, 2b, 2c** onto the heat drain profiles **5a-d** during TU and at a given bridging temperature difference (BTD) between the stage hole temperatures **41a-c** (see Fig.3) and a local profile temperature. The MTPE together with a safety margin energy is MTBE. The safety margin energy covers eventual corrosion in the bridging areas, which may reduce the TCC.

The first functional stage **3** may carry the lens system as it is known for optical transceivers. The second functional stage **4** features the design elements required for aligning and accessing a cable plug of a fiber optic cable as known to those skilled in the art. Exemplary alignment features for such a cable plug are the alignment pins **6a, 6b**. Exemplary access features are the plug slots **7a, 7b** where receiving and emitting light beams pass through.

Fig. 2 shows a perspective view of the optical multiplex transceiver as described above with its heat sink base **1** being visible. The heat sink base **1** has a preferably rectangular section hull contour with a number of cooling

ribs **16** being placed between the corner bases **17** that hold the heat drain profiles **5a-d** with their base holes **12a-d.**

The corner bases **17** have a corner base width **22** where the thermal energy drained from the heat drain profiles **5a-d** passes through and onto a heat sink core **18.** The heat sink core **18** in the center of the heat sink **1** receives a thermal energy that is drained from the heat drain profiles **5a-d** in the corner bases **17** and distributes it evenly to the cooling ribs **16,** which increase the air contact surface of the heat sink base **1.** The heat sink base **1** is kept in a decoupling distance **19** to the adjacent processing stage **2a** to avoid thermal shorting of the designated thermal path and to provide full air contact for the heat sink **1.**

It is noted that the cooling ribs **16** may be placed at any location of the heat sink base **1.**

The metallic materials of the heat drain profiles **5a-d** are electrically conductive to allow for electrical power delivery, electrical ground and/or electrical signal transmission between the individual stages. The heat drain profiles **5a-d** are preferably utilized to provide a ground and a faraday shield for the optical processing stages **2a, 2b, 2c.** The heat drain profiles **5a-d** ground thereby the optical processing stages **2a, 2b, 2c** the heat sink base **1.** The circular arrangement of the heat drain profiles **5a-d** provide a faraday shield effect thereby to shield the optoelectronic receiver/emitter structures **24a, 24b** (see

Fig. 4) and the supporting electronic circuitry **23** against peripheral electromagnetic noise.

The heat sink base **1** has an extrusion height **20** to provide sufficient mechanical interlocking length with the heat drain profiles **5a-d** and sufficient surface of the heat sink **1**. Extrusion profiles have a minimum wall thickness and gap width that is limited by the fabrication technique. Thus a maximum section contour length is defined, which leaves the extrusion height **20** as the only variable factor to increase the heat sink surface necessary to exchange the sum thermal energy generated by all processing stages **2a, 2b, 2c** under worst climatic conditions. As a result, the extrusion height **20** typically exceeds significantly the main thermal exchange length **32** (see **Fig. 3**) between the heat drain profiles **5a-d** and the heat sink base **1**. The reduction of the TCC caused by the optional electrical insulation layer increases the thermal exchange length **32** within the extrusion height **20** and the overall cooling performance remains unaltered.

The rectangular design typically used for electronic circuitry and subsequently the typical election of four heat drain profiles **5a-d** limits the amount of electrical transmission paths between the individual processing stages **2a, 2b, 2c.** Optional ball grid arrays **15a, 15b** correspondingly placed on all processing stages **2a, 2b, 2c** provide additional electrical transmission paths. **Fig. 2** shows the optional ball grid arrays **15** only on one side of the processing stage **2a** without contacting an adjacent

processing stage and is shown solely for purposes of visualization. It is appreciated that anybody skilled in the arts may place the optional ball grid arrays **15a, 15b** between the processing stages **2a, 2b, 2c** to establish functioning electrical path between them.

Fig. 3 shows the optical multiplex transceiver as described above in side view together with a corresponding graph that visualizes the temperature relations of the preferred application of the invention. The horizontal axis of the graph corresponds to the dimensions of the optical multiplex transceiver in the main heat drain direction **9a** and the secondary heat drain direction **9b**. The vertical axis of the graph represents temperatures. The values and relations shown in this graph are shown for the sole purpose for visualization without any claim for accuracy. Given is an surrounding air temperature **45** with a maximum level of typically 85 degrees centigrade, which results in a maximum level of the stage peak temperatures **41a-c** for a maximum thermal energy generated in the processing stages **2a-c**. Each of the processing stages **2a-c** has a stage hole temperature **42a-c** at the contact surface of the bridging area of the soldering holes **14**. For purposes of visualization circumferential variations of the stage hole temperature **42a-c** are neglected in **Fig. 3**.

The level differences between the stage peak temperatures **41a-c** and their corresponding stage hole temperatures **42a-c** are defined by the radial thermal conductivity within the processing stages **2a-c**. Optional thermally conductive

layer structures with radial orientation increase the radial conductivity. Electrical leads, which are typically made from copper based materials with good thermal conductivity properties connect the central processing area with the ball grid arrays, and hence serve simultaneously to reduce the radial thermal conductivity of the processing stages **2a-c**.

The drain profile temperature curve **43** visualizes the temperature of the heat drain profiles **5a-d** at various locations. For the purpose of visualization, radial temperature variations of the heat drain profiles **5a-d** are neglected in **Fig. 3**.

In the exemplary visualization of the graph each of the processing stages **2a-c** has the same TCC and the same average GBTD between the drain profile temperature curve **43** and the stage hole temperatures **42a-c**. As a result, the curve segments **43c**, **43e**, and right part of **43g** are shown in the graph to be parallel and having the bridging decline angle **47a-c**. The left part of curve segment **43g** is declining towards the first and second functional stages **3**, **4**, which do not generate heat and thus have a cooling influence on the heat drain profiles **5a-d**. As a result, the main heat drain direction **9a** is inverted in the peak **48** to the secondary heat drain direction **9b**.

The first functional stage **3**, which preferably carries the lenses to focus the passing light beams is close to the heat generating processing stage **2c** and has a relatively

small surface contact to surrounding air. The lowest temperature **432** of the first functional stage is therefore only insignificantly below the curve segment **43h**. The hole temperature **431** of the first functional stage is located between lowest temperature **432** and curve segment **43h** at a location dependent on the relation between internal thermal conductivity (ITC) and the thermal bridging conductivity (TBC) in the bridging area.

The second functional stage **4** has more surface exposed to the cooling air and is separated by the first functional stage **3** from the next heat producing processing stage **2c**. Hence, its lowest temperature **442** and its hole temperature **441** are significantly below the curve segment **43i**.

Having a constant TCC in all stages and having constant thermal properties of the heat drain profiles **5a-d** over their length in the example visualized in **Fig. 3**, the thermal energy bridges proportional to the bridging temperature difference BTD between the contact surface of the soldering holes **14** and the drain profile surface in the bridging areas. It is appreciated that anybody skilled in the art may vary the TCC between or within each of the processing stages **2a-c** and the heat sink base **1**. It is also appreciated that anybody skilled in the art may vary the thermal properties, geometric shapes, and numbers of the heat drain profiles **5a-d** over their length without diverting from the scope of the invention.

The curve segments **43b, 43d, 43f** show the temperature decline with the conduction decline angle **46** in the heat drain profiles **5a-d** over the traveling length of the thermal energy. The conduction decline angle **46** is dependent on the material specific thermal conductivity and the size of the section area of the heat drain profiles **5a-d** as it is known to those skilled in the art. Since thermal energy is imposed on the heat drain profiles **5a-d** at the curve segments **43c, 43e, 43g** they have the bridging decline angles **47a-c.** For the constant TCC and BTD in the bridging decline angles **47a-c** are proportional to the imposed and drained thermal energy.

At the peak **48** the thermal flow changes from the direction towards the heat sink base **1** to the direction towards the first and second functional stages **3, 4.** Reducing the TCC of the first and second functional stages moves the peak 48 towards the left end of the processing stage **2c** and results in less energy and less thermal load imposed onto the first and second functional stages **3,4.**

The heat sink base **1** has a heat sink hole temperature **44** and the heat sink core temperature **44b,** which has level discrepancies over its length dependent on the mass of the heat sink core **18.** For the purpose of visualization, the heat sink core temperature **44b** is defined as constant over the heat drain direction **9.** In the exemplary monolithic heat sink base **1** the thermal conductivity between the base holes **12a-d** and the heat sink core **18** dependents mainly on

the corner base width **22** and is represented by the third decline angle **49**.

The heat sink base **1** receives the sum thermal energy from all heat generating processing stages **2a-c**, except the thermal energy that is transmitted onto the first and second functional stages **3,4** and a certain energy amount that is transmitted to the surrounding air along the thermal path. The heat sink base **1** transmits the thermal energy mainly via convection to the surrounding air. As it is known to those skilled in the art, the thermal exchange energy at TU between heat sink base **1** and the surrounding air is dependent on the size of the air contact surface, the air flow characteristic around the heat sink base **1**, the convection temperature difference (CTD) between heat sink temperature **44b** and surrounding air temperature **45** and the TCC between surrounding air and air contact surface. It is appreciated that anybody skilled in the art may change the design of the heat sink base **1**.

The heat drain profiles **5a-d** drain the sum thermal energy over the main thermal exchange length **32**. The curve segment **43a** approaches asymptotically the hole temperature **44** such that the temperature difference in the secondary thermal exchange length **33** is at low level insignificant for thermal energy exchange is.

In the following, the heat transfer of the invention is described against the main heat drain direction **9a** since the surrounding air temperature **45** at the very end of the

thermal path defines the profile peak temperature **48** and consequently the stage peak temperatures **41a-c**. The base hole temperature **44** is a result of the given surrounding air temperature **45** and depends on it as described above.

Between thermal path point **50** and **51** the temperature rises in the heat drain profiles **5a-d** according to the curve segment **43a**. The higher the temperature difference to the base hole temperature **44**, the more thermal energy is drained from the heat drain profiles **5a-d** and the steeper the curve segment **43a** becomes. Between thermal path point **51** and **52** the temperature rises with the thermal conductivity angle **46**, which is defined by the section size and the thermal conductivity of the material of the heat drain profiles **5a-d**.

Between thermal path point **52** and **53** the temperature rises with the thermal conductivity angle **47a**, which is defined by the thermal energy generated in the processing stage **2a** at TU and is imposed over the hole heights **21a** on the heat drain profiles **5a-d** within. The stage hole temperature **42a** and consequently the stage peak temperature **41a** rise above the level of curve segment **43c** to the point where the BTD is sufficient to drain the generated thermal energy to the heat drain profiles **5a-d**.

Between thermal path point **53** and **54** the temperature raises with the thermal conductivity angle **46**.

Between thermal path point **54** and **55** the temperature rises with the thermal conductivity angle **47b**, which is defined by the thermal energy generated in the processing stage **2b** at TU and is imposed over the hole heights **21b** on the heat drain profiles **5a-d** within. The stage hole temperature **42b** and consequently the stage peak temperature **41b** rise above the level of curve segment **43c** to the point where the BTD is sufficient to drain the generated thermal energy to the heat drain profiles **5a-d**.

Between thermal path point **55** and **56** the temperature rises with the thermal conductivity angle **46**.

Between thermal path point **56** and **57** the temperature rises with the thermal conductivity angle **47c**, which is defined by the thermal energy generated in the processing stage **2c** at TU and is imposed over the hole heights **21c** on the heat drain profiles **5a-d** within. The stage hole temperature **42c** and consequently the stage peak temperature **41c** rise above the level of curve segment **43g** to the point where the BTD is sufficient to drain the generated thermal energy onto the heat drain profiles **5a-d**. At the profile peak temperature **48** the heat drain direction **9a** inverts and flows in secondary heat drain direction **9b** towards first and second functional stages **3**, **4** and is drained as described above.

Hence, the temperature increase over the thermal path as described above results in a maximum level of the stage peak temperature **41c**. For a most unfavorable high level of the surrounding air temperature **45**, the sum thermal

conductivity of the thermal path is at a level to have the maximum level of the stage peak temperature **41c** with a minimal safety temperature margin **60** below the a maximum operation temperature **61**.

Fig.4 shows the front view of one of the processing stages **2a-c** with superimposed isothermal temperature lines visualizing the lateral temperature distribution. The exemplary processing stage **2** has in its central area an optoelectronic receiver structure **24a**, an optoelectronic emitter structure **24b** and supporting electronic circuitry **23** in immediate surrounding. Electrical conductive leads **25** emanate in radial direction from the supporting electronic circuitry **23** and connect with the ball grid arrays **15a, 15b**. The processing heat generated by the circuitry results in the shown stage peak temperature **41**. The thermal energy that is produced flows radially away and is captured at peripheral ring structure **26** and redirected towards the soldering holes **14**. Over the thermal path in the processing stage **2** the temperature declines according to the local thermal conductivity. The temperature decline is visualized by the isothermal temperature lines **41I-III** and **42I-III** with constant temperature differences. Since the thermal conductivity of the central processing area is low the isothermal temperature lines are closer together. The radial conductive leads **25** increase the thermal conductivity. The peripheral ring structure **26** has a good thermal conductivity, which results in a larger distance between the isothermal temperature lines. The peripheral ring structure **26** has sufficient mass around the soldering

holes **14** such that the circumference temperature discrepancies along the circumference are kept below a maximum level.

The circumferential temperature discrepancies result in thermal expansion differences of the heat drain profiles **5a-d**, which alter their straightness and impose radial mechanical tensions onto the processing stages **2a-c**. The maximum level of the circumferential temperature difference is the level, at which the straightness of the heat drain profiles remains within a predetermined limit.

It is appreciated that the soldering holes **14** may be shaped such that they contact the heat drain profiles **5a-d** only on a portion of their circumference and that the heat drain profiles **5a-d** may have a noncircular section shape with a cooling feature like for instance cooling ribs.

It is appreciated that the heat drain profiles **5a-d** may be connected to each other at a portion or all over their length such that they may form a singular profile with preferably hollow section shape. The stages **2a-c**, **3**, and **4** may be stacked and aligned there within without diverting from the scope of the invention. Precision alignment features may be utilized between individual optoelectronic processing stages **2a**, **2b**, **2c** to position the optoelectronic processing stages **2a**, **2b**, **2c** with a higher precision than it is provided by the heat drain profiles **5a-d**.

It is appreciated that the invention may be utilized for vertical-cavity surface-emitting laser and edge-emitting laser as they are known to those skilled in the art.

Accordingly, the scope of the invention should be determined by the following claims and their legal equivalents:

What is claimed is:

1. A stack-module multiplex transceiver for transmitting signals between an optical cable end and a connector array of a circuit board, said stack-module multiplex transceiver being stack-assembled on a number of heat drain profiles in parallel orientation to a beam direction defined by said optical cable end and comprising:

A) a heat drain base holding said number of heat drain profiles;

B) at least one processing stage comprising:

1) an optical communication device;

2) a controller circuitry; and

3) a number of guiding means for receiving said heat drain profiles.

2. The stack-module multiplex transceiver of claim 1, wherein said heat drain base is a profile extending along said beam direction.

3. The stack-module multiplex transceiver of claim 1, wherein said stack-module multiplex transceiver comprises an optical stage.

4. The stack-module multiplex transceiver of claim 1, wherein said stack-module multiplex transceiver comprises a functional stage.

5. The stack-module multiplex transceiver of claim 1, wherein said stack-module multiplex transceiver comprises a cable alignment stage.

6. The stack-module multiplex transceiver of claim 1, wherein said processing stages have edge castellations.

7. The stack-module multiplex transceiver of claim 6, wherein said edge castellations are laterally placed on at least one of said processing stages.

8. The stack-module multiplex transceiver of claim 1, wherein said heat drain profiles are in thermal communication with said guiding means.

9. The stack-module multiplex transceiver of claim 1, wherein said guiding means are in electrical communication with said control circuitry.

10. The stack-module multiplex transceiver of claim 1, wherein said processing stages have leads, said leads being electrically and thermally conductive.

11. The stack-module multiplex transceiver of claim 10, wherein said leads terminate in peripheral ball grid arrays.

12. A stack-module multiplex transceiver for transmitting signals between an optical cable end and a connector array of a circuit board, said stack-module multiplex transceiver being stack-assembled on a heat drain profile in parallel orientation to a beam direction defined by said optical cable end and comprising:

A) a heat drain base holding said heat drain profile;

B) a number of processing stages, at least one of said number of processing stages comprising:

1) an optical communication device;

2) a controller circuitry; and

3) a guiding means for receiving said heat drain profile.

13. The stack-module multiplex transceiver of claim 12, wherein said heat drain profile has a cooling feature.

14. A method for simultaneous aligning and cooling of processing stages within a stack assembly, said method comprising the following steps:

A) binding and aligning heat drain profiles parallel in a heat sink base;

B) shaping and placing heat transfer areas of said processing stages correspondingly with section contours of said drain profiles;

C) thermally connecting a processing area of said processing stages with said heat transfer areas;

D) stacking said processing stages with said heat transfer areas on said heat drain profiles and contacting said heat transfer areas with said heat drain profiles; and

E) transmitting a processing heat from said processing areas to said heat transfer areas and onto said heat drain profiles, whereby said processing heat is drained from said drain profiles into said heat sink base.

15. The method of claim 14, wherein said heat drain profiles are electrically conductive.

16. The method of claim 15, wherein said heat transfer areas communicate electrically with said processing areas and said heat drain profiles.

17. The method of claim 15, wherein said heat drain profiles communicate electrically with said heat sink base.

18. The method of claim 14, wherein said processing areas process optical signals.

19. The method of claim 14, wherein said processing areas process electrical signals.

20. The method of claim 14, wherein said processing areas receive a signal light beam.

21. The method of claim 20, wherein said signal light beam has a beam direction parallel to said heat drain profiles.

22. A method for simultaneous aligning and cooling of processing stages within a stack assembly, said method comprising the following steps:

A) binding and aligning a heat drain profile parallel in a heat sink base, whereby said heat drain profile provides an alignment feature for orientation and position for said processing stage;

B) shaping and placing heat transfer areas of said processing stages correspondingly with section contours of said drain profiles;

C) thermally connecting conductive a processing area of said processing stages with said heat transfer areas;

D) stacking said processing stages with said heat transfer areas on said heat drain profiles and contacting said heat transfer areas with said heat drain profiles; and

E) transmitting a processing heat from said processing areas to said heat transfer areas and onto said heat drain profiles, whereby said processing heat is drained from said drain profiles into said heat sink base.

23. The method of claim 22, whereby said heat drain profile has a cooling feature.

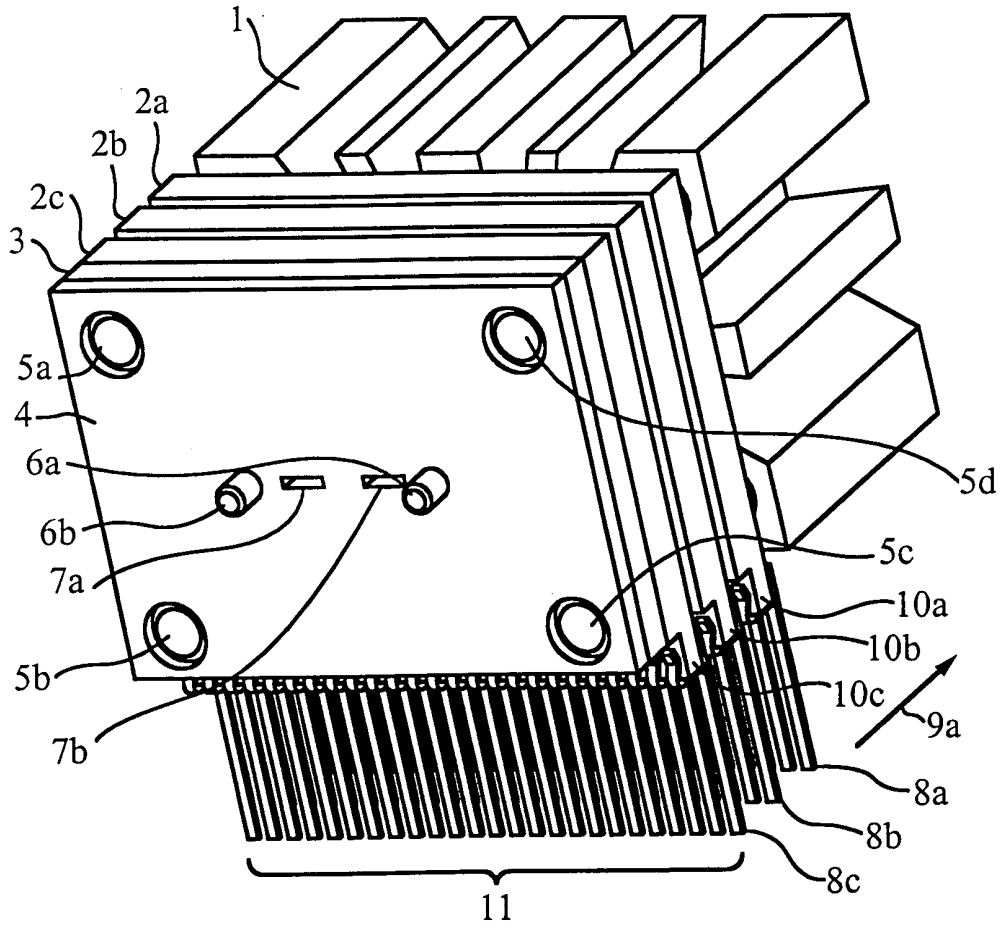
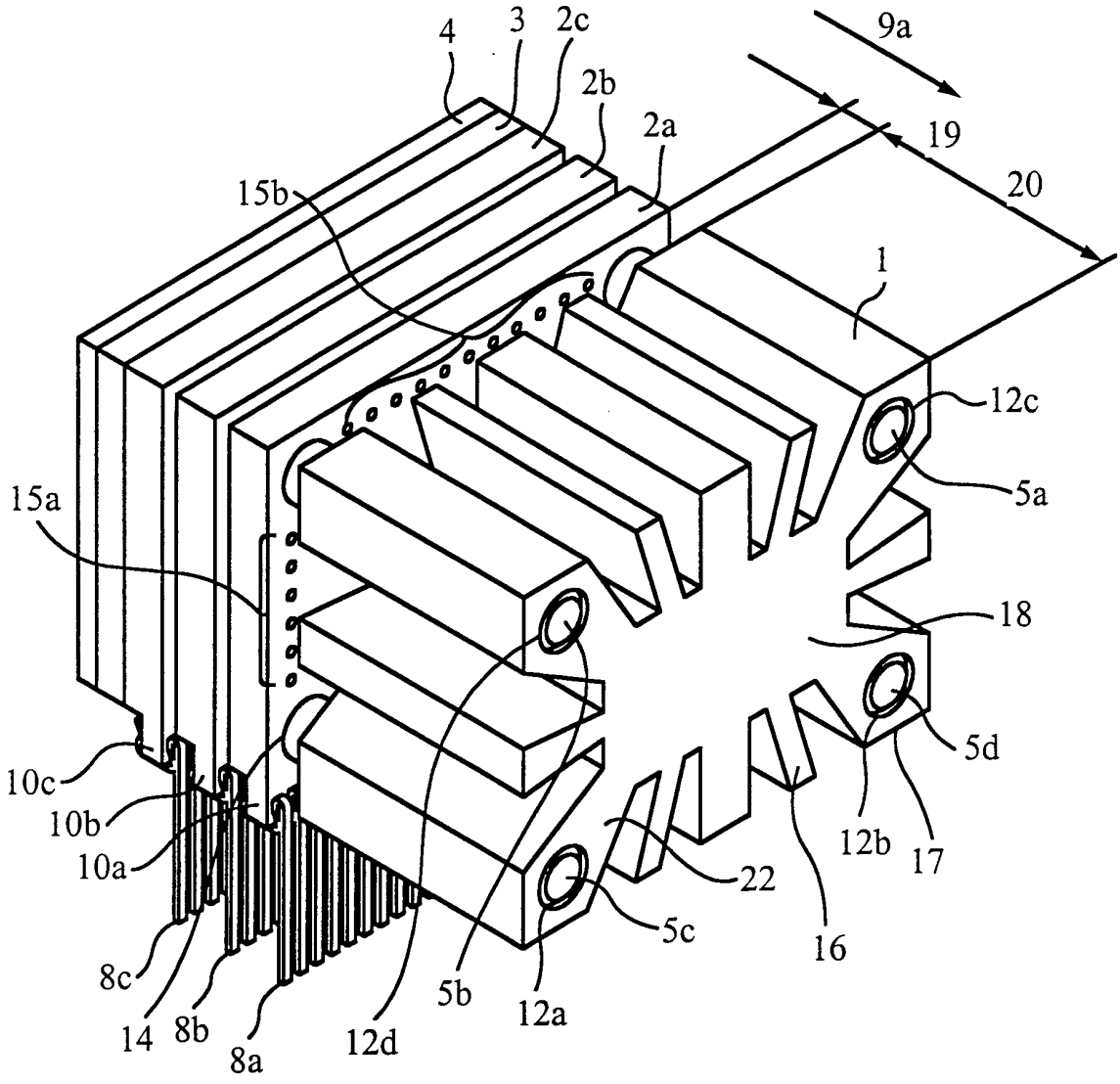


FIG. 1


4
3
2c
2b
2a
9a
19
20
15b
1
12c
5a
15a
18
5d
10c
10b
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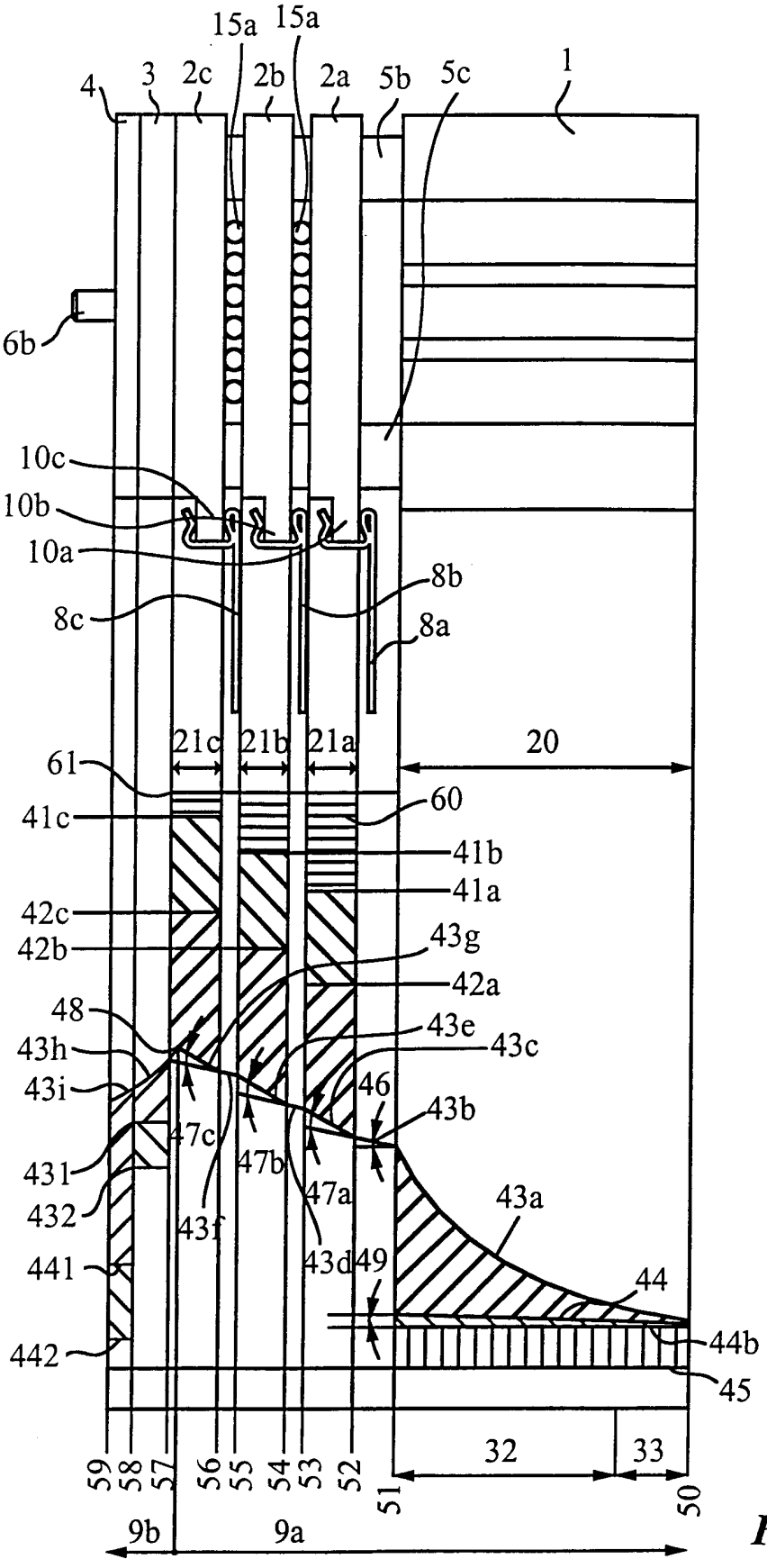
12b
17
22
5c
16
8c
5b
12a
14
8b
12d
8a

FIG. 2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15a
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3
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2b
2a
5b
5c
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6b
10c
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10a
8b
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8a
21c
21b
21a
20
61
60
41c
41b
41a
42c
42b
43g
42a
48
43e
43h
43c
43i
46
43b
47c
47b
47a
431
43a
432
43f
43d
49
441
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9b
9a

FIG. 3

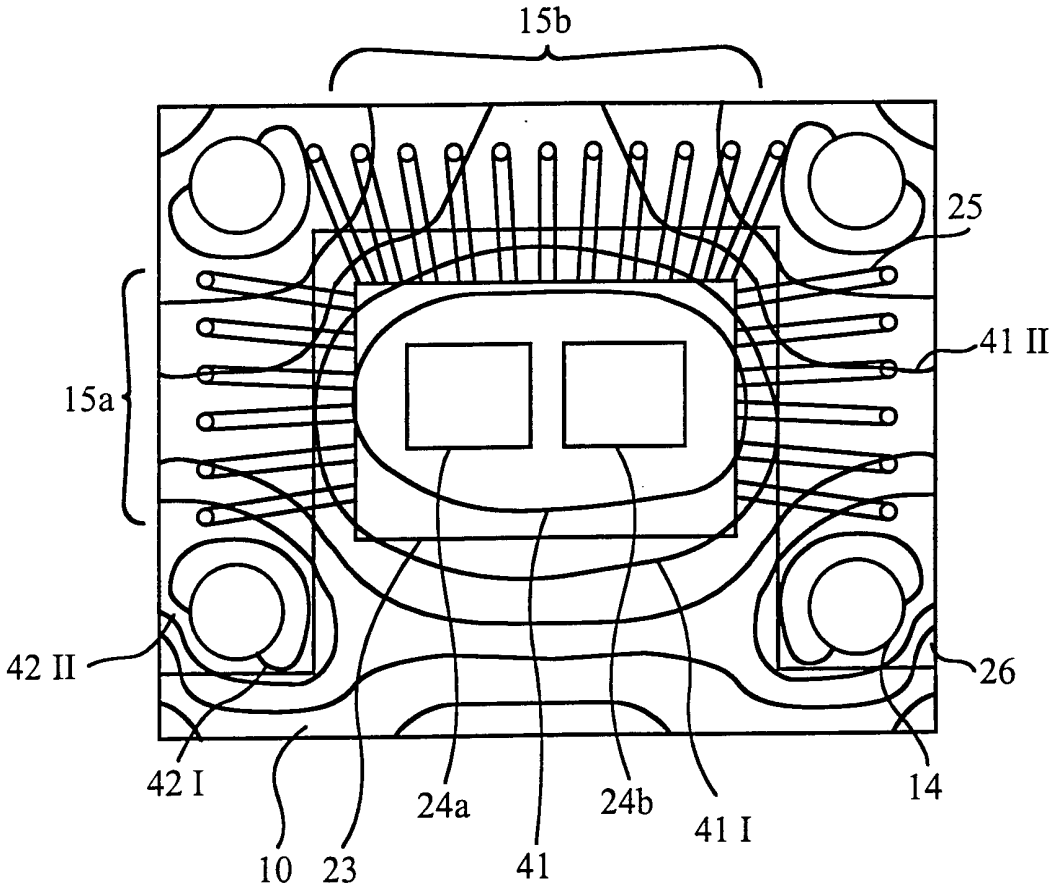

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US00/28017

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) :Please See Extra Sheet.

US CL :324/760; 359/152, 143; 361/382; 361/386; 385/92; 257/879, 80, 86

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 324/760; 359/152, 143; 361/382; 361/386; 385/92;

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

USPAT

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X,P	US 6,097,521 A (ALTHAUS et al) 01 August 2000, col. 10, lines 4-67.	1, 4, 12
X	US 5,999,295 A (VOWELL et al) 07 December 1999, col. 1, lines 39-49, col. 6, lines 64-67-col. 7, lines 1-15.	1
A,P	US 6,024,500 A (WOLF) 15 February 2000, lines 1, lines 55-67 - col. 2, lines 1-25, lines 40-67.	1-3, 5, 9, 10, 12, 15-20
X,P	US 6,072,613 A (HENNINGSSON et al) 06 June 2000, col. 1, lines 31-67 - col. 3, lines 1-67	3, 9, 18-21
A	US 5,731,709 A (PASTORE et al) 24 March 1998, col. 9, lines 10-67 - col. 10, lines 1-47.	6, 7, 11, 13, 14, 22, 23

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 08 JANUARY 2001	Date of mailing of the international search report 08MAR2001
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3988	Authorized officer LESLIE PASCAL Telephone No. (703) 305-4700

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US00/28017

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 4,706,164 A (L'HENAFF et al) 10 November 1987, col. 1, lines 61-68 - col. 1, lines 1-52.	1, 2, 8, 12-17, 21, 22, 23
A	US 4,701,829 A (BRICAUD et al) 20 October 1987, abstract.	8, 10, 14, 17, 22
X,P	US 5,994,720 A (SNYMAN et al) 30 November 1999, col. 10, lines 14-50, Fig. 15	1, 3, 4, 9, 10, 19
X,P	US 6,111, 271 A (SNYMAN et al) 29 August 200, col. 1, lines 15-24, abstract.	1, 3, 4, 9, 10, 19
X	US 5,808,336 A (MIYAWAKI) 15 September 1998, col. 18, lines 31-58	2, 10, 12, 13, 15, 16, 19

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US00/28017

A. CLASSIFICATION OF SUBJECT MATTER:
IPC (7):

G01R 31/02; H04B 10/02, 10/00; H02B 1/00; H05K 7/20; G02B 6/36; HO1L 29/788, 33/00