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Sugimoto et al.

[11] **3,885,469**

[45] **May 27, 1975**

[54] **MAGNET OPERATING TIME COMPENSATION SYSTEM**

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[73] Assignee: **Fujitsu Limited**, Japan

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[30] **Foreign Application Priority Data**

July 28, 1972 Japan 47-75766

[52] **U.S. Cl.** **101/93.48**

[51] **Int. Cl.** **B41j 9/26**

[58] **Field of Search** ..... 340/172.5; 101/93 C, 93.48

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Assistant Examiner—Paul R. Woods
Attorney, Agent, or Firm—Staas & Halsey

[57] **ABSTRACT**

A magnet operating time compensation system is disclosed for line printers, in which fluctuation of a printing magnet drive voltage due to a load change in the printing magnet exciting period is predicted by operating the content of a buffer memory having stored therein printing information and a time period corresponding to the predicted result is used as a compensation time period thereby to prevent irregularities in the arrangement of the characters resulting from the fluctuation of the printing magnet drive voltage.

8 Claims, 6 Drawing Figures

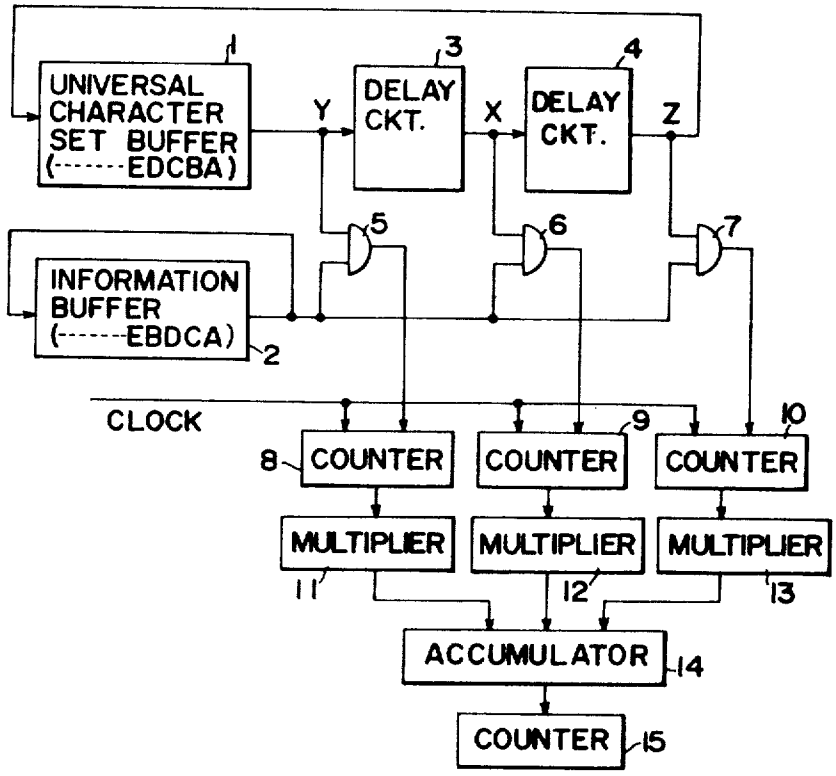


FIG. 1

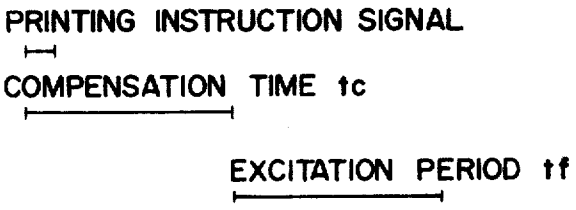

PRINTING INSTRUCTION SIGNAL
COMPENSATION TIME tc
EXCITATION PERIOD tf

FIG. 2

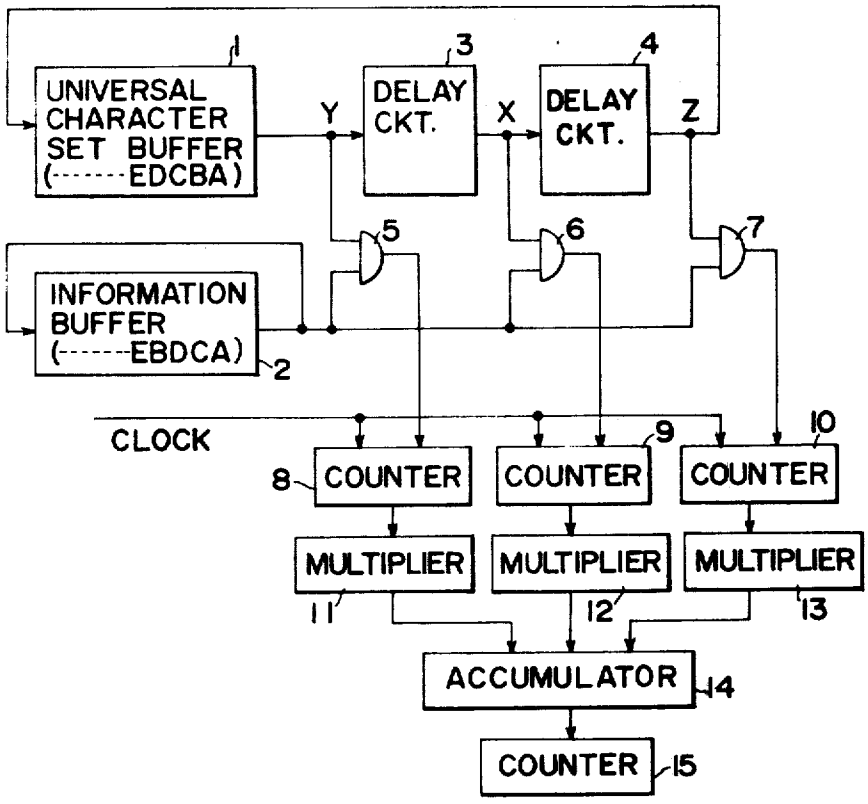

UNIVERSAL CHARACTER SET BUFFER (------EDCBA)
1
DELAY CKT.
3
DELAY CKT.
4
Y
X
Z
5
6
7
INFORMATION BUFFER (------EBDCA)
2
CLOCK
8
COUNTER
9
COUNTER
10
COUNTER
MULTIPLIER
11
MULTIPLIER
12
MULTIPLIER
13
ACCUMULATOR
14
COUNTER
15

FIG. 3

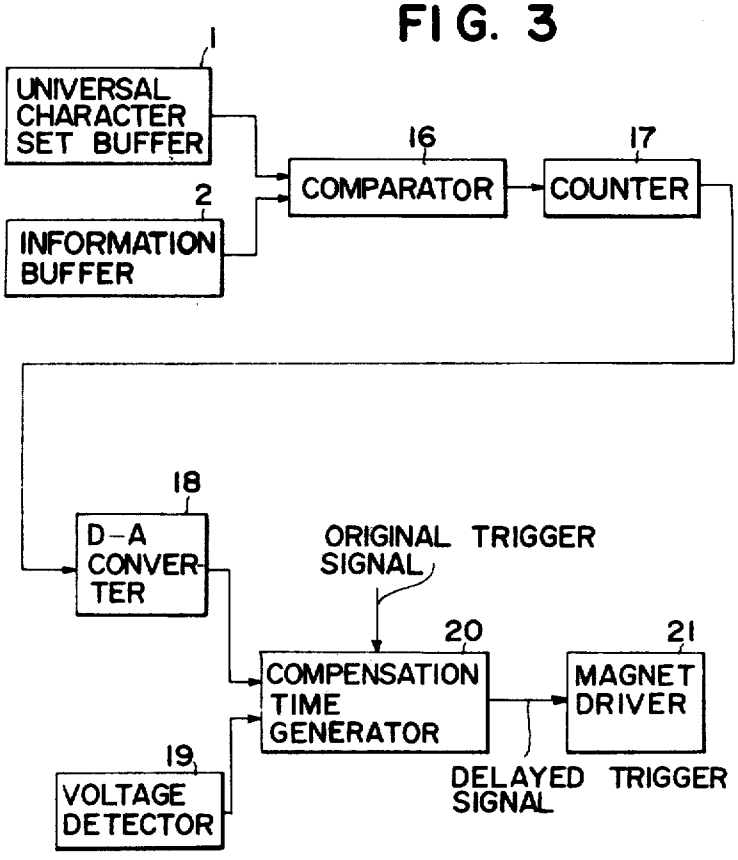
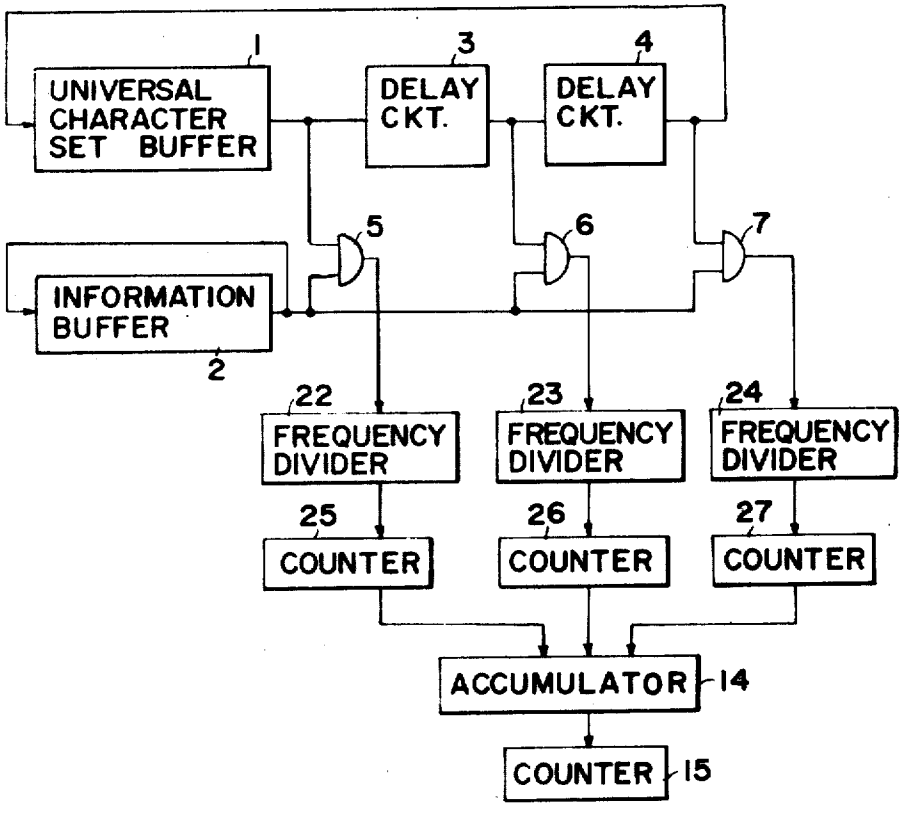

1
UNIVERSAL CHARACTER SET BUFFER
2
INFORMATION BUFFER
16
COMPARATOR
17
COUNTER
18
D-A CONVERTER
ORIGINAL TRIGGER SIGNAL
20
COMPENSATION TIME GENERATOR
21
MAGNET DRIVER
19
VOLTAGE DETECTOR
DELAYED TRIGGER SIGNAL

FIG. 4


1
UNIVERSAL CHARACTER SET BUFFER
3
DELAY CKT.
4
DELAY CKT.
5
6
7
INFORMATION BUFFER
2
22
FREQUENCY DIVIDER
23
FREQUENCY DIVIDER
24
FREQUENCY DIVIDER
25
COUNTER
26
COUNTER
27
COUNTER
ACCUMULATOR
14
COUNTER
15

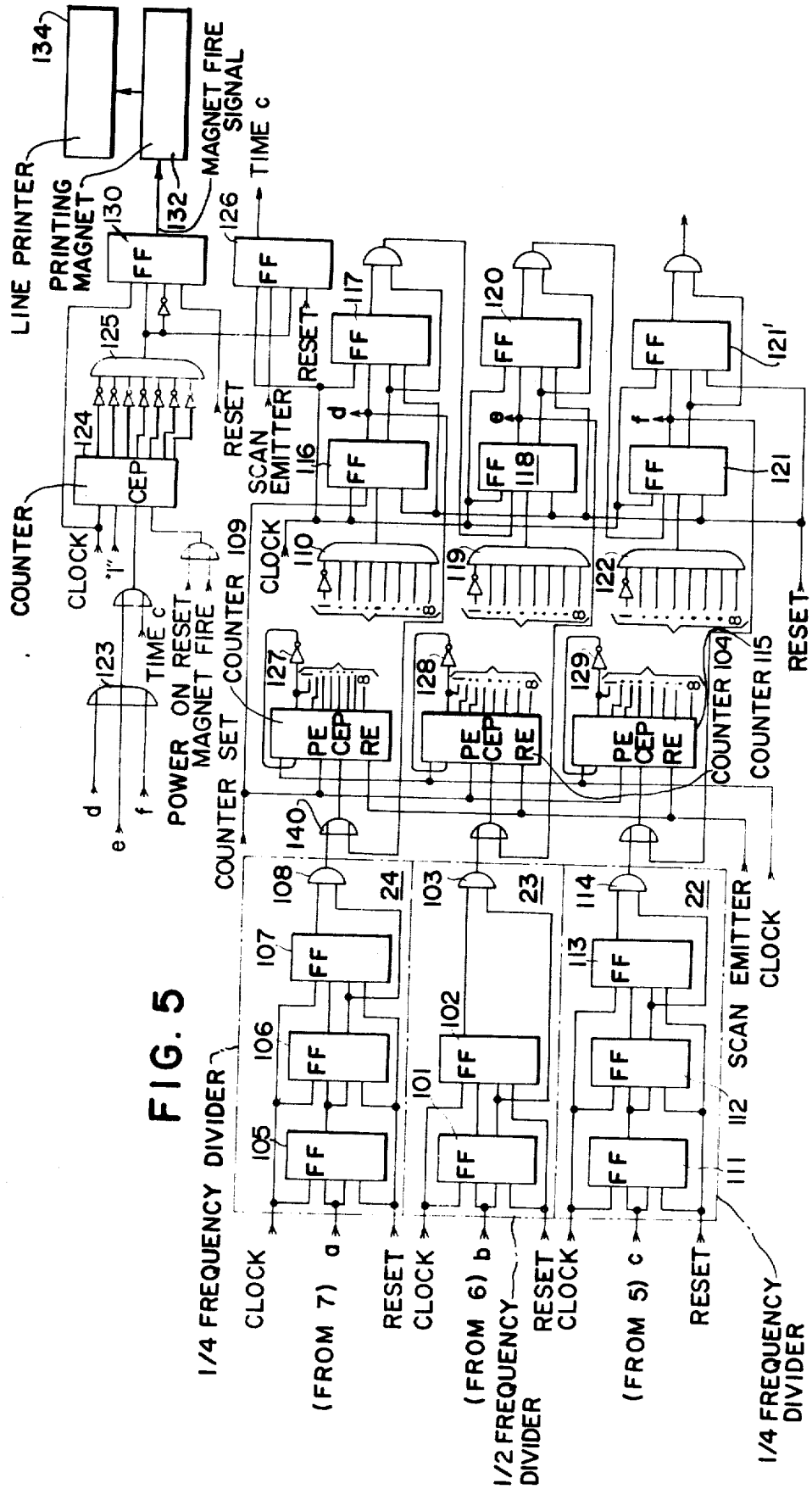
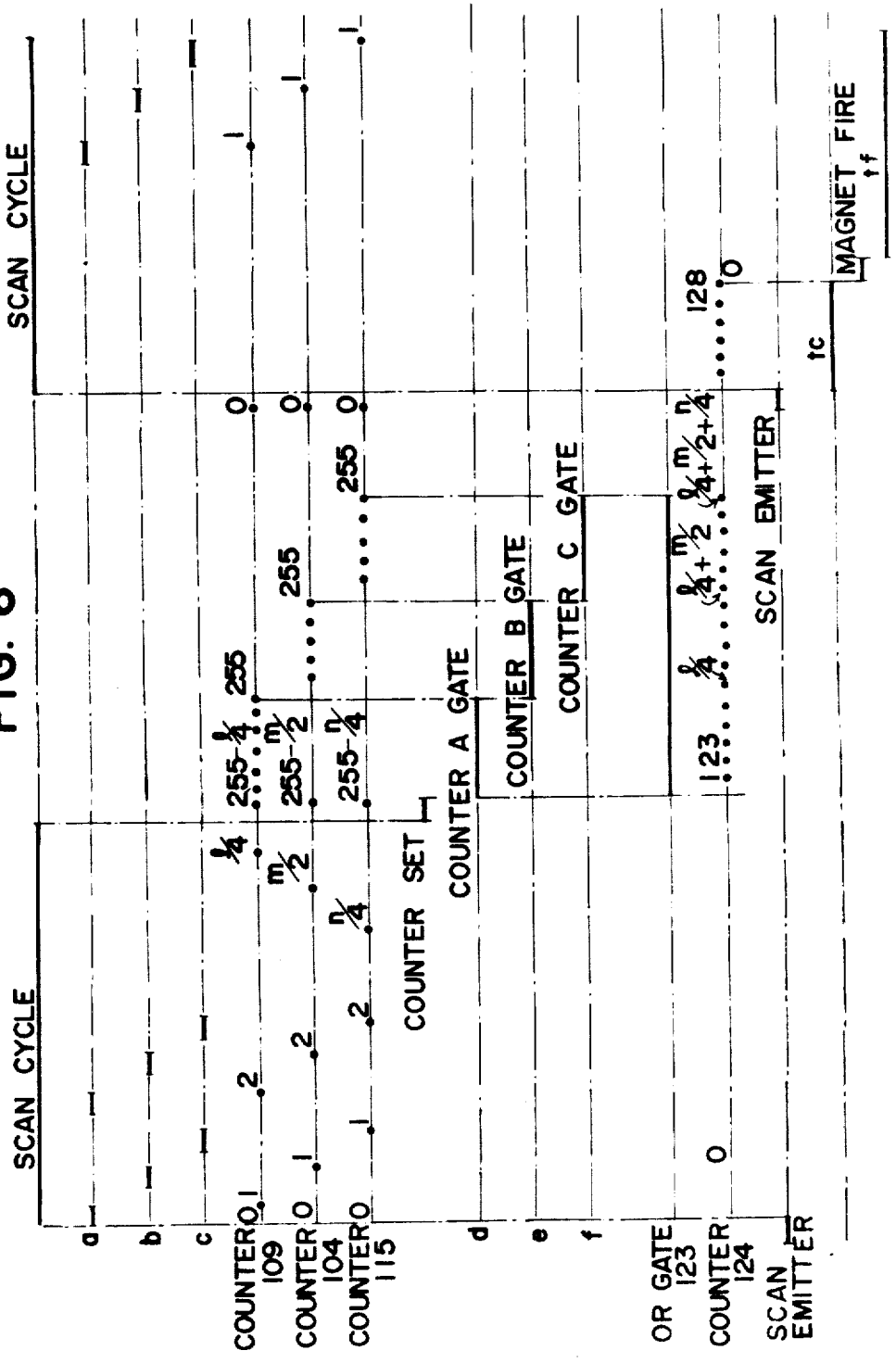

LINE PRINTER
PRINTING MAGNET
MAGNET FIRE SIGNAL
TIME c
COUNTER
CLOCK
"1"
TIME c
POWER ON RESET
MAGNET FIRE
COUNTER SET
COUNTER 109
SCAN EMITTER
RESET
CLOCK
COUNTER 104
COUNTER 115
1/4 FREQUENCY DIVIDER
(FROM 7) a
(FROM 6) b
1/2 FREQUENCY DIVIDER
(FROM 5) c
1/4 FREQUENCY DIVIDER
SCAN EMITTER
CLOCK
RESET
FF
CEP
PE
RE

FIG. 5

FIG. 6


SCAN CYCLE
SCAN CYCLE
a
b
c
d
e
f
COUNTER 109
COUNTER 104
COUNTER 115
OR GATE 123
COUNTER 124
SCAN EMITTER
COUNTER SET
COUNTER A GATE
COUNTER B GATE
COUNTER C GATE
SCAN EMITTER
MAGNET FIRE
tc
tf
0
1
2
255
128
123

MAGNET OPERATING TIME COMPENSATION SYSTEM

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a magnet operating time compensation system, and more particularly to a magnet operating time compensation system for line printers in which a change in a printing magnet drive voltage during a supply of an exciting current to a printing magnet is predicted to thereby ensure printing impact at a desired time.

2. Description of the Prior Art

Generally, line printers have a type transfer member of high speed revolution such as a type drum or the like, and achieve printing by a printing hammer element at the time when a type on a type transfer member reaches a predetermined position. The printing hammer is driven by supplying an exciting current to a printing magnet. Accordingly, a change in the drive current to the printing magnet causes a time lag in printing impact to introduce irregularities in the array of characters.

To avoid this, in the prior art, the magnet drive voltage is detected at the time of application of a printing instruction signal and a compensation time *tc* is prepared corresponding to the detected voltage; in other words, the compensation time is selected short or long dependent on whether the magnet drive voltage is low or high, thereby effecting the printing impact at the desired time.

However, the adjustment of the compensation time is merely achieved by detecting a voltage before the supply of the exciting current to the printing magnet. Consequently, where the number of the same character to be printed in the same line is large, printing magnets of respective digits, i.e., print positions, are excited in parallel at the same time, which causes a great decrease in the magnet drive voltage at the instant of excitation making it impossible to prevent irregularities at the instant of printing impact. Further, with increased revolving speed of the type drum, for example, where types A, B, C, . . . are arranged on the type drum, when a printing magnet for printing the type B is excited, those printing magnets for printing the types before and after it, that is, A and C are also excited and the influence of this excitation appears in the form of a fluctuation of the drive voltage which causes a change in the instant of printing impact of the type B.

SUMMARY OF THE INVENTION

It is an object of this invention to provide a magnet operating time compensation system for line printers which overcomes the above-described defects and in which fluctuation of the magnetic drive voltage in the printing magnet exciting period is predicted from the content of a buffer memory having stored therein printing information and the compensation time is adjusted or corrected correspondingly.

Thus, the magnet operating time compensation system of this invention is characterized in that, in line printers adapted to achieve the printing impact at the desired instant by providing a compensation time corresponding to the fluctuation of the printing magnet drive voltage, the fluctuation of the printing magnet drive voltage in the period of supplying the exciting current to the printing magnet is predicted by detecting the content of the buffer memory having stored therein the printing information to adjust the compensation time correspondingly.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a diagram, for explaining a compensation time *tc* for printing in line printers;

FIG. **2** is a block diagram showing one example of this invention;

FIG. **3** is a block diagram illustrating another example of this invention;

FIG. **4** is a block diagram showing another example of this invention;

FIG. **5** is a circuit diagram of the principal part of the example of FIG. **4**; and

FIG. **6** is a time chart, for explaining the operation of the part depicted in FIG. **5**.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

As shown in FIG. **1**, where a printing instruction signal for a specified character is applied, a magnet drive voltage is detected as to its amplitude and the duration of the compensation time *tc* is controlled as a function of that detected amplitude, or magnitude of the voltage. After the compensation time *tc*, excitation of the corresponding magnet is carried out. In general, printing impact is achieved after the lapse of time a little longer than the excitation period *tf*. For the sake of brevity, let it be assumed that the printing impact takes place at the instant of completion of the excitation period *tf*.

Generally, fluctuation of the magnet drive voltage causes a change in the exciting current, which results in a change in the instant of the printing impact. This change appears in the form of an irregularity in the array of characters printed in a line. In view of this, the change in the instant of the printing impact is compensated for by providing shortened or elongated compensation time *tc* dependent upon whether the magnet drive voltage is low or high respectively. With such a conventional system, however, the compensation time *tc* is merely determined by detecting the magnet drive voltage before the exciting current is applied to the printing magnet and no consideration is given to the compensation based on the fluctuation of the drive voltage in the exciting current supply period. Namely, where the number of the same characters to be printed in the same line is large, the characters are printed at the same time, so that the respective magnets are excited in parallel and this causes variations in the drive voltage which cannot be compensated for by the prior art system. With increased revolving speed of the type drum, a time *ts* in which a type of a second character to be printed reaches its printing position after that of a first character has reached its printing position is about one-half of the excitation period *f* depicted in FIG. **1**. Consequently, printing magnets for other characters are excited in parallel in the exciting period *tf* shown in FIG. **1**, by which the voltage of the driving magnet fluctuates and causes a change in the instant of the printing impact.

FIG. **2** illustrates one example of this invention which overcomes the above defect. In FIG. **1**, reference numeral **1** indicates a universal character set buffer (hereinafter referred to as a UCSB for the sake of brevity), which stores character arrangements on the type drum

in the form of respective character codes, **2** refers to an information buffer (hereinafter referred to as an INB for the sake of brevity), which stores printing information in the form of character codes in the order of the digits of characters in the same line; **3** and **4** designate delay circuits; **5, 6** and **7** relate to comparator or collating circuits taking the form of, for example, AND circuits; **8, 9** and **10** indicate counters; **11, 12** and **13** refer to multipliers for weighting, i.e., multiplying, the counting outputs of counters **8, 9** and **10** by the constants α, β and γ respectively; **14** designates an accumulator for accumulating outputs from the multipliers **11, 12** and **13**; and **15** identifies a counter for detecting the output from the accumulator **14.**

The UCSB **1** has set therein characters A, B, C, D, E . . . in the form of character codes in the order of their arrangement on the type drum. The INB **2** has set therein characters to be printed in the same line in the form of character codes in the order of their digit, or character print positions. In the illustrated example, the characters are printed in the order of A, C, D, B and E.

Prior to actual printing, the contents of the UCSB **1** and INB **2** are sequentially sent out therefrom in accordance with clock signals and compared with each other by the comparator circuits **5, 6** and **7** respectively. Namely, when the character from the UCSB **1,** for example, B, appears at a point X in FIG. **1,** the characters C and A appear at points Y and Z respectively. At that instant, the characters A, C, D, B, E, . . . of the respective digits in the same line are read out from the INB **2.** Accordingly, each time the character B exists in the same line, the comparator circuit **6** derives therefrom an output 1 and the number m of the characters B is detected by the counter **9.** In a similar manner, the counter **8** detects the number n of the characters C in the same line which is disposed immediately after the character B on the type drum, and the counter **10** detects the number l of the characters A in the same line which is disposed immediately before the character B on the type drum.

Namely, in the present example, at the time of the actual printing of the character B, the number m of the characters B present in the same line, the number l of the characters A (disposed immediately before the characters B on the type drum) which are present in the same line and printed before the characters B, and the number n of the characters C (disposed immediately after the characters B on the type drum) which are present in the same line and printed after the characters B, are detected based on the content of the INB **2,** which serves as a buffer memory having stored therein the printing information. As a result, at the time of exciting the printing magnet for printing the character B, the degree to which the voltage for driving the printing magnet is lowered, can be predicted in accordance with the number of characters to be printed before and after the character B. Based on this predicted result, the compensation time tc shown in FIG. **1** is adjusted. The multipliers **11, 12** and **13,** the accumulator **14** and the counter **15** are provided for this purpose and they illustrate one example in which the compensation time tc is approximated according to the following expression:

$$A_c = \alpha \cdot l + \beta \cdot m + \gamma \cdot n$$

where α, β and γ are constants. Namely, the multipliers **11, 12** and **13** perform operations of $\alpha \cdot l$, $\beta \cdot m$ and $\gamma \cdot n$ respectively and the accumulator **14** accumulates $(\alpha \cdot l + \beta \cdot m + \gamma \cdot n)$. The output of the accumulator **14** is detected by the counter **15,** and the compensation time tc for printing the character B is provided based on the detected result.

The present example is adapted such that, at the time of printing the character B, the number m of the characters B and the numbers l and n of the characters A and C, respectively, immediately before and after the characters B are used in the form of $(\alpha \cdot l + \beta \cdot m + \gamma \cdot n)$. However, it is also possible to consider their functional relationships, and characters of desired numbers of digits before and after the character to be printed, i.e. characters not immediately before and after the character to be printed, may be operated upon to provide the desired compensation time. In an extreme case, the compensation time tc can be determined based on the number of the characters B only.

FIG. **3** shows another example of this invention in which the compensation time tc is determined by analog means. In FIG. **3,** reference numerals **1** and **2** correspond to those in FIG. **2,** and **16** indicates a comparator or collating circuit which corresponds to the delay circuits **3** and **4** and the comparator circuits **5, 6** and **7** in FIG. **2.** Reference numeral **17** designates a counter circuit, which corresponds to circuits **8, 9, 10, 11, 12, 13** and **14.** In the case of determining the compensation time tc based on the number of only the characters to be printed, the counter circuit **17** may be considered to correspond to the counter **9,** the multiplier **12** and the accumulator **14.** Reference numeral **18** identifies a digital-to-analog converter, **19** refers to circuit for detecting the printing magnet drive voltage at the time of application of the printing instruction signal, depicted in FIG. **1, 20** relates to a compensation time generator circuit, and **21** identifies a printing magnet driving circuit.

In FIG. **3,** the UCSB **1** and the INB **2,** the comparator circuit **16** and the counter **17** usually detect $(\alpha \cdot l + \beta \cdot m + \gamma \cdot n)$ as is the case with the example of FIG. **2,** and the detected value is converted by the digital-to-analog converter **18** into an analog value, which is then applied to the compensation time generator circuit **20.** Further, detector circuit **19** detects the drive voltage, which is supplied to the compensation time generator circuit **20.** In accordance with the outputs of both circuits **18** and **19,** the compensation time generator circuit **20** generates and applies after a delay corresponding to the compensation time tc shown in FIG. **1** an original trigger signal as the delayed trigger signal for the excitation period tf to the magnet driver circuit **21.** Namely, at this instant, a supply of the exciting current to the printing magnet is started.

As has been described in the foregoing, in the present invention, the compensation time tc is adjusted in accordance with the printing magnet drive voltage at the time of the generation of the printing instruction signal. In particular, the compensation time tc is determined by detecting the number m of printing magnets which would be excited at the same time and those numbers l and n of printing magnets for other characters which would affect the exciting current during the excitation of the printing magnet for printing the desired character, by predicting from the detected numbers of the characters that the drive voltage would be fluctuated thereby and by selecting the compensation time tc to

compensate for a change in the instant of printing impact due to the fluctuation of the drive voltage.

Namely, the fluctuation of the drive voltage during the excitation of a printing magnet for printing a character, for example, B, is foreseen and the fluctuation is taken into consideration in the determination of the compensation time *tc*. Consequently, also where the number of the same characters B to be printed in the same line at one time is large or where the influence of printing adjacent characters A, C, etc., on the type drum is exerted at the instant of the printing impact for the character B due to an increased, i.e., high revolving speed of the type drum, the printing impact can be effected at the correct instant.

In the example shown in FIG. **2**, the outputs from the comparator circuits **5, 6** and **7** (shown to be AND circuits) are respectively counted by the counters **8, 9** and **10** and the operations of multiplying the counted contents by the constants α, β and γ are achieved by the multipliers **11, 12** and **13** respectively, but it is also possible to directly multiply the outputs from the comparator circuits **5, 6** and **7** by the constants α, β and γ. For example, if the constants α, β and γ are taken as one-fourth, one-half and one-fourth respectively, it is sufficient to frequency divide the outputs from the comparator circuits **5** and **7** to one-fourth and that from the comparator circuit **6** to one-half.

FIG. **4** is a block diagram illustrating another example of this invention which is designed to obtain the compensation time *tc* by the operation described above and in which the same reference numerals as those in FIG. **2** designate the same parts. The outputs from frequency divider circuits **22, 23** and **24**, which frequency divide the outputs from the comparator circuits **5, 6** and **7** and serve as multipliers, are counted by counters **25, 26** and **27** respectively, thereby to provide $\alpha \cdot l$, $\beta \cdot m$, and $\gamma \cdot n$, as described previously. In turn, these values are accumulated by the accumulator **14**, thus obtaining $(\alpha \cdot l + \beta \cdot m + \gamma \cdot n)$. This result is detected by the counter **15** and the compensation time *tc* is determined in accordance with the detected result.

FIG. **5** shows a circuit for processing the outputs from the aforesaid comparator circuits **5, 6** and **7** to produce the compensation time *tc*, and FIG. **6** is a time chart for explaining the operation therefor.

A detecting signal of synchronization of the revolution of the type drum is generated for each line of type on the drum and, upon impression of a scan emitter pulse by the detecting signal, a scan cycle is initiated. By the scan emitter pulse, binary counters **104, 109** and **115** are reset. Upon initiation of the scan cycle, the content of the information buffer **2** and the output from the universal character set buffer **1** from which character arrangement is read out in synchronization with the scan emitter pulse, are compared with each other by the comparator circuits **5, 6** and **7** as previously described.

In FIG. **5**, the constants α, β and γ are implemented as one-fourth, one-half and one-fourth respectively. The output *a* from the comparator circuit **7** is applied to a one-fourth frequency divider circuit **24** which comprises J-K flip-flops **105** to **107** and an AND gate **108**; the output *b* from the comparator circuit **6** is applied to a one-half frequency divider circuit **23** which is composed of J-K flip-flops **101** and **102** and an AND gate **103**; and the output *c* from the comparator circuit **5** is applied to a one-fourth frequency divider circuit **22** which is comprised of J-K flip-flops **111** to **113** and an AND gate **114.**

The J-K flip-flops herein used are master-slave type ones, which are supplied at their J and K terminals with input signals upon application of a clock pulse to their T terminal. These J-K flip-flops operate in a manner that, in the former period of the rising of the clock pulse, a gate between the master and slave is closed; in the latter period of the rising, and input gate is opened to permit the application of the input signal to the master; in the former period of the falling of the clock pulse, the input gate is closed; and in the latter period, the gate between the master and slave is opened to apply the signal stored in the master to the slave to derive therefrom an output.

The binary counters **104, 109** and **115** are, for example, 8-bit counters, which indicate **255** when all the bits are 1. The binary counters count the outputs from the frequency divider circuits **22** to **24** respectively, providing $\alpha l = \frac{1}{4} l$, $\beta m = \frac{1}{2} m$ and $\gamma n = \frac{1}{4} n$. Each of the counters **104, 109** and **115** produces eight parallel outputs shown in FIG. **5** in a schematic manner and designated **1 . . . 8.** As will later become apparent, these eight parallel outputs are supplied to respectively associated eight parallel inputs of the respectively corresponding gates **110, 119** and **122.** It will be noted that the bit 1 output of each of the counters **109, 104** and **115** is also supplied through an inverter **127, 128** and **129,** respectively, in a return loop to a corresponding input of the respective counters. In addition, each of the bit 1 outputs is supplied through an inverter to its corresponding gate **110, 119** or **122.** In a similar fashion, it will be seen that the plural bit outputs of a binary counter **124,** to be described, are connected through parallel circuits and associated inverters to the inputs of a gate **125.**

Upon completion of the scan cycle, a counter set signal is produced and the binary counters **104, 109** and **115** are set with their count contents being inverted by inverters **127, 128** and **129.** For example, if the counted content is 01011010, the counter is set at 10100101. Accordingly, the set outputs from the binary counters **104, 109** and **115** are **255-**$\frac{1}{4} l$, **255-**$\frac{1}{2} m$ and **255-**$\frac{1}{4} n$ respectively.

By the counter set signal, a J-K flip-flop **116,** the set output of which produces the counter A gate (FIG. **6**), is set and its set output *d* (i.e., the counter A gate) is applied through an OR gate **140** to a count gate CEP of the binary counter **109** to open the gate CEP, whereby the binary count **109** starts to count a main clock. When the counted content of the binary counter **109** has become **254,** it is detected by a gate **110** to reset the J-K flip-flop **116.** With such operation, if the pulse interval of the main clock is taken as τ, the length of time of the counter A gate output is $\frac{1}{4} \cdot l \cdot \tau$.

When the J-K flip-flop **116** has been set and reset by the output from the gate **110,** a J-K flip-flop **118,** which produces the counter B gate, (FIG. **6**) is set by a counter A gate end signal derived from a J-K flip-flop **117** and, by the set output *e* (i.e., the counter B gate), the count gate CEP of the binary counter **104** is opened and counter **104** thus starts counting of the main clock. When its count content has reached **254,** the J-K flip-flop **118** is set by the output from a gate **119.** Consequently the length of time of the counter B gate is $\frac{1}{2} \cdot m \cdot \tau$.

Then, when the J-K flip-flop **118** has been reset after set, a J-K flip-flop **121** which produces the counter C

gate is set by a counter B end signal derived from a flip-flop **120** and, by its set output *f* (i.e., the counter C gate), the count gate CEP of the binary counter **115** is opened and this counter starts to count the main clock. When the count content has reached **254,** a J-K flip-flop **121** is set by the output from a gate **122.** Consequently, the length of time of the counter C gate is $¼ \cdot n \cdot \tau$.

Since the set outputs *d*, *e* and *f* from the J-K flip-flops **116, 118** and **121** are applied to an OR gate **123,** the length of the output from the OR gate **123** is $¼ \cdot l + ½ \cdot m + ¼ \cdot n$. A binary counter **124** counts the length of the output from the OR gate **123.**

Under such condition, the circuit waits for the next scan emitter signal. Upon application of the scan emitter signal, a J-K flip-flop **126** is set and, by its output time *c*, the count gate CEP of the binary counter **124** is opened and the binary counter **124** starts to count the main clock. Each bit output from the counter **124** is applied to a gate **125** through an inverter, so that when the count content of the counter **124** has become **128,** the J-K flip-flop **126** is set and, at the same time, a J-K flip-flop **130** is set to provide a magnet fire signal, by which a magnet **132** for printing impact is excited, and the binary counter **124** is reset. The magnet **132** in conventional fashion actuates the printing elements of a conventional line printer **134,** for each excitation thereof in response to the magnet fire signal from flip-flop **130.** Suitable line printers for use as printer **134** are sold commercially by International Business Machines Corporation, Model designations 1403 and 3211 and are described in U.S. Pat. Nos. 3,513,774 and 3,516,764.

In this manner, the compensation time *tc* of $[128 - (¼ \cdot l + ½ \cdot m + ¼ \cdot n)] \cdot \tau$ is obtained.

The present invention is not limited specifically to the foregoing examples but may be variously modified and varied within the scope defined by the appended claims.

What is claimed is:

1. A time compensation control system for use in a line printer wherein for each successive line of characters to be printed in accordance with printing information supplied to the system, the line printer presents, in common, at each character print position of the print line and in each print interval of a cycle of plural time sequential print intervals, a corresponding one of plural character types available for printing, and wherein printing of a common type character at print positions of a line selected in accordance with said printing information is effected by a drive voltage generated for each such print interval, the generation of the drive voltage and thus the instant of printing in response to the drive voltage in a given print interval being controlled in accordance with the duration of a compensation time, comprising:

means for storing printing information signals corresponding to the characters to be printed in a line, for each of successive lines,

means for detecting from the printing information signals of said storing means each character of a given, common type to be printed on a line simultaneously and during a corresponding print interval,

means responsive to the number of common type characters detected by said detecting means for predicting a resultant change in the drive voltage during the said corresponding print interval, and

means for adjusting the duration of the compensation time in accordance with the said predicted resultant change in the drive voltage, thereby to control the timing of the drive voltage and thereby the instant of printing impact during the said corresponding print interval.

2. A time compensation control system as recited in claim **1** wherein:

said detecting means comprises a counter for counting the said number of characters of a common type to be printed during a print interval, and

said predicting means comprises a multiplier for multiplying the count content of said counter by a preselected constant.

3. A time compensation control system as recited in claim **1** wherein:

said detecting means comprises:

first means for counting the number of characters of a first common type to be printed simultaneously during a given print interval,

second means for counting the number of characters of a second common type corresponding to a preceding print interval, and

third means for counting the number of characters of a third, common type corresponding to a succeeding print interval, and

said predicting means comprises first, second and third multipliers for multiplying the count content of said first, second and third counting means by respectively corresponding first, second and third preselected constants, and means for accumulating the multiplication outputs of said first, second and third multiplying means.

4. A time compensation control system as recited in claim **1** wherein:

said detecting means produces an output signal for each said character of said common type to be printed simultaneously on a line during a corresponding print interval, and

said predicting means comprises a divider circuit for receiving the output signals produced by said detecting means and dividing the number thereof by a pre-established constant, and means for accumulating the divided outputs of said multiplying means.

5. A time compensation control system as recited in claim **1** wherein:

said detecting means produces an output signal for each said character of said common type to be printed simultaneously on a line during a corresponding print interval, and

said predicting means comprises means for receiving and counting the output signals from said detecting means for each print interval, and means for converting the count accumulated by said counting means in each said print interval to an analog value, and

said adjusting means delays the output therefrom of a trigger signal for producing the drive voltage in accordance with said analog value, thereby to control the timing of the drive voltage.

6. A time compensation control system as recited in claim **1** wherein there is further provided

means for storing signals identifying each said character type available for printing in the sequence of said corresponding time sequential print intervals, and

said detecting means comprises means for comparing each said stored character type signal with each of the signals stored in said printing information storing means corresponding to characters to be printed in a line, in sequence for said corresponding, time sequential print intervals.

7. A time compensation control system as recited in claim 6 wherein said detecting means further comprises:

first and second delay circuits, each producing a delay corresponding to a print interval, and connected in series to receive the output of said character type signal storing means, the output of said first delay circuit comprising a signal defining the character type corresponding to a current print interval, the output of said second delay circuit comprising a signal defining the character type corresponding to the next preceding print interval, and the output of said storing means comprising a signal defining the character type corresponding to the next succeeding print interval of said time sequential print intervals of a cycle,

first, second and third comparing means respectively receiving the character type signal output of said storing means and the character type signal outputs of said first and second delay circuits,

said second comparing means thereby supplying an output signal for each character in the line of printing information corresponding to the common character type and said first and third comparing means respectively producing output signals for each character in the said line of the said common types of the respectively corresponding, next succeeding and next preceding print intervals of said cycle, and

said predicting means includes first, second and third means receiving the output signals of said first, second and third comparing means, respectively, for weighting the respective said output signals by respectively corresponding first, second and third preselected weighting constants, and means for accumulating the weighted outputs of said weighting means, the accumulated output thereof comprising the said predicted resultant change in the drive voltage to which said adjusting means responds for adjusting the duration of the compensation time.

8. A time compensation control system for use in a line printer wherein for each successive line of characters to be printed in accordance with printing information supplied to the system, the line printer presents, at each character print position of the print line and in sequential print intervals of a cycle of plural time sequential print intervals, respectively corresponding plural character types available for printing, and wherein printing of characters, selected in accordance with said printing information, is effected by a drive voltage generated for each such print interval, the generation of the drive voltage and thus the instant of printing in response to the drive voltage in a given print interval being controlled in accordance with the duration of a compensation time, comprising:

means for storing printing information signals corresponding to characters to be printed,

means for detecting from the stored printing information signals of said storing means each character to be printed on a line during a corresponding print interval,

means responsive to the number of characters detected by said detecting means for predicting a resultant change in the drive voltage during the said corresponding print interval, and

means for adjusting the duration of the compensation time in accordance with the said predicted resultant change in the drive voltage, thereby to control the timing of the drive voltage and thereby the instant of printing impact during the said corresponding print interval.

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