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(54) Gain control circuit

(57) In a gain control circuit of the "eight transistors gain cell" type comprising amplification means 40, 44; 42, 46 disposed in each log-antilog transmission path 16, 20; 18, 22 of the cell of the gain control circuit for providing in each path signal gain as a function of the input signal to the circuit means 60, 62, 68, 70; 64, 66, 72, 74 is provided for reducing the distortion component in the output signal due to the inherent parasitic base resistances of the transistors of the gain cell. The circuit is separated in a Class AB amplifier. In a further embodiment the transistors 68, 70, 72, 74 are replaced by cross coupling resistors (90, 92; 94, 96 Fig. 3).

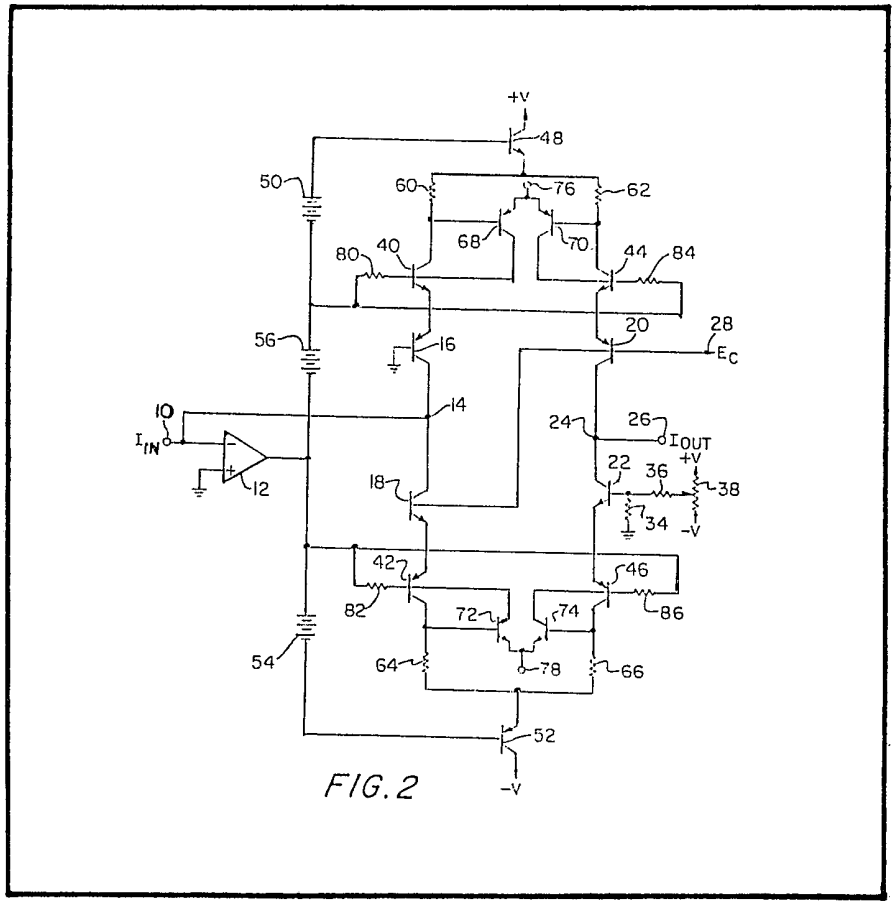

FIG. 2

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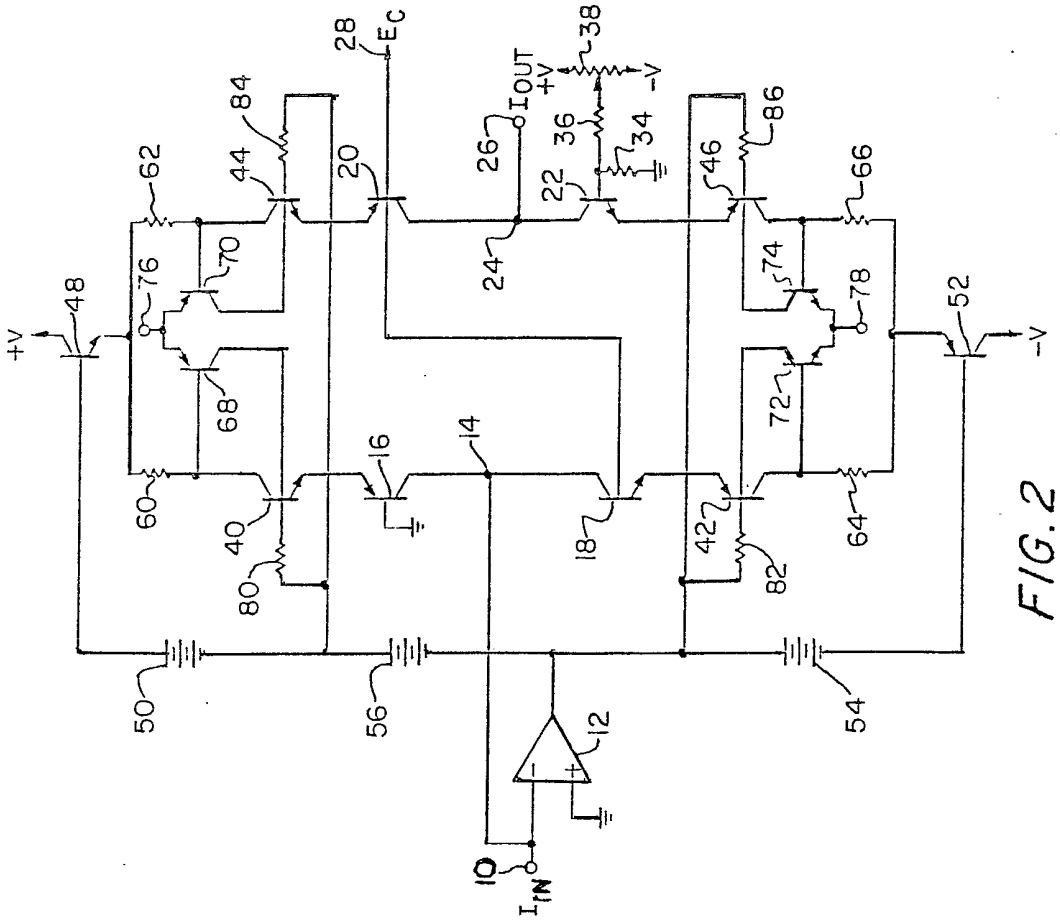

FIG. 2

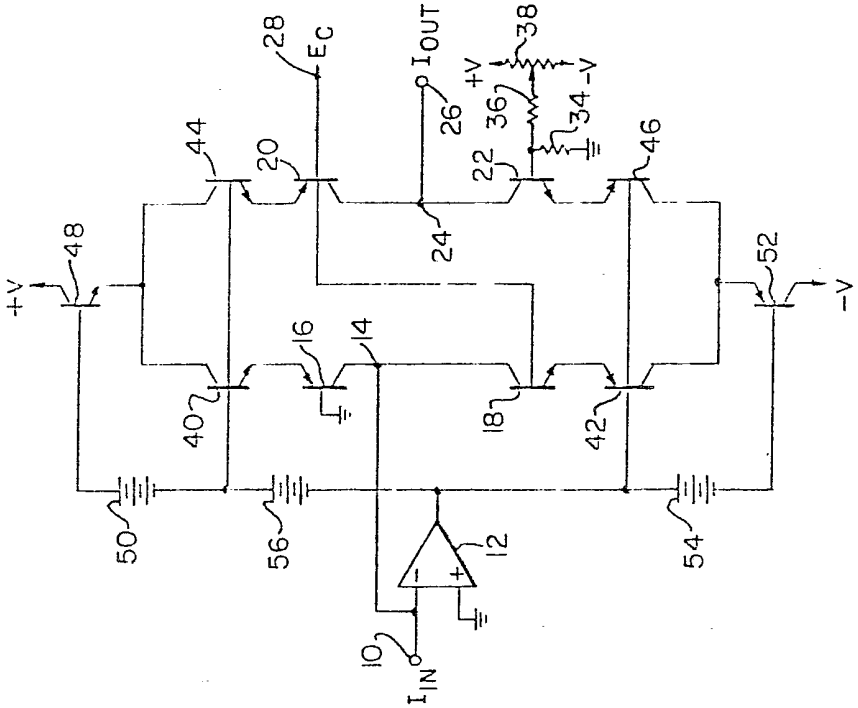

FIG. 1

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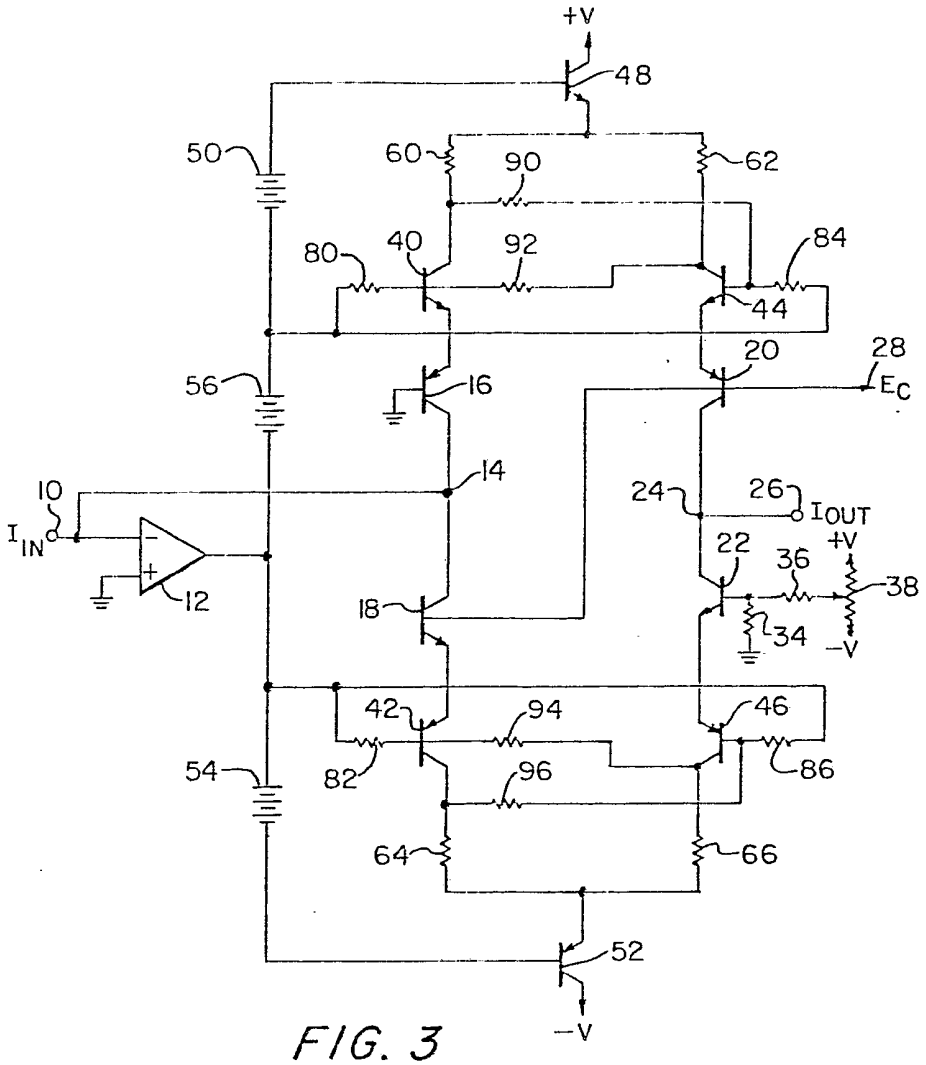

FIG. 3

SPECIFICATION

Gain control systems

This invention relates to electronic multipliers or gain control circuits, and more particularly to analog multipliers with logarithmic control responses, and this application has been divided out of U.K. Patent Application No. 8028910.

Many systems, especially those used for audio and video signals, include signal gain circuits controlled in response to an electrical command or gain control signal. One such gain control circuit, also referred to as a "voltage control amplifier" or "VCA", is described and claimed in U.S. Patent 3,714,462 issued to David E. Blackmer on January 30, 1973 (the claimed circuits hereinafter being collectively referred to as the "Blackmer circuit"). The Blackmer circuit has been commercially successful, particularly for use in audio noise reduction systems, commonly referred to as "companders".

The Blackmer circuit is an analog device providing a logarithmic control response. The circuit generally includes first signal converting means for providing a first signal which is logarithmically related to the input signal, and second signal converting means. The latter is connected to the first signal converting means so as to provide an output signal which is an anti-logarithmic function of the sum of the first signal and the gain control signal. More specifically, the Blackmer circuit comprises an input operational amplifier having a pair of feedback paths, one being conductive when the input signal is of a positive polarity, the other being conductive when the input signals is of a negative polarity. In the preferred form of the Blackmer circuit, each feedback path includes a log device for converting the input signal of the correct polarity into a log form. Each log device in each path has connected to it an antilog device for converting the log signal together with the gain control signal into an antilog form. For want of a better expression the signal path defined between the input of each log device and the output of the corresponding antilog device to which the log device is coupled shall hereinafter be referred to as the "log-antilog transmission path". The log devices are preferably collector-emitter circuits of transistors of opposite conductivity type, i.e. PNP and NPN transistors, since such circuits exhibit log-linear transfer characteristics. Similarly, the anti-log devices are typically emitter-collector circuits of transistors of opposite conductivity types, since such circuits exhibit antilog-linear transfer characteristics. A control signal is summed with the log signal of each path by applying the voltage to the bases of the log and the antilog transistors, thereby controlling the gain of the circuit.

Although the Blackmer circuit, employing the four transistors as log and antilog devices (hereinafter referred to for convenience as the "primary" transistors) theoretically provides substantially zero distortion, as a practical matter commercially available transistors are not perfect. Thus, the output of the circuit may include some detectable distortion, although in the case of audio applications, it may not be readily discernable to the average listener. This distortion can be attributed, at least in part, to two inherent characteristics of the primary transistors: (1) each transistor has a finite current gain and (2) each transistor exhibits an inherent non zero or parasitic base resistance. As a result of finite gain, when any base current is provided through the base of the transistor a base voltage error results and a distortion component will be generated due to the voltage drop across the parasitic base resistance. Where the log converting and antilog converting transistors of each signal path are matched, at unity gain the distortion contributed by the log and antilog transistors of each signal path are equal and opposite and will cancel one another. However, as the gain shifts from unity gain, the amount of signal in the log converting transistors differs from that in the anti-log converting transistors and the distortions are not equal and thus will not cancel each other.

This distortion component typically will show up in standard SMPTE IM (intermodulation) distortion tests. The error voltage at the bases of these devices can be thought of as another control voltage signal which varies the gain of the circuit as the signal is changing, so that as the gain shifts from unity gain the amount of distortion tends to increase.

Various techniques have been proposed to correct for this distortion. One suggested technique described in U.S. Patent Application 943,859 filed by Gary Bergstrom on September 19, 1978 and assigned to the present assignee (Attorney's Docket No. DBX-23) modifies the Blackmer circuit by incorporating means for generating an error correction signal derived from a comparison of the output and input signals of the Blackmer circuit and means for suming the error correction signal with the control signal and the log signal. By adding in the error correction signal, the distortion component in the output is reduced.

Another suggested technique now being commercially exploited incorporates into the emitter path of each primary transistor of the Blackmer circuit a diode element so as to form four compound log and antilog devices. For convenience this circuit shall be referred to hereinafter as the "four-transistor, four-diode, cell VCA". To form the four-transistor, four-diode cell VCA, the emitter of each primary transistor of the Blackmer circuit is connected to a secondary transistor, the latter being connected so as to operate in a diode mode. The secondary diode-connected transistors are of an opposite conductivity as the corresponding primary transistors to which they are connected so that the emitters of the log and antilog NPN primary transistors of log-antilog transmission path are connected to the corresponding emitters of PNP secondary diode-connected transistors, and the emitters of the log and antilog PNP primary

transistors of the other log-antilog transmission path are connected to the corresponding emitters of NPN secondary diode-connected transistors. The PNP secondary diode-connected transistors are connected with their bases and collectors tied together and to a first current source. The NPN secondary diode-connected transistors are connected with their bases and collectors tied together and to a second current source. The first and second current sources are connected to receive the output of an input operational amplifier of the circuit, the inverting input of which receives the current signal input of the circuit and the positive input of which is connected to ground. As the input signal varies the relative magnitude of the current provided by one current source to the pair of secondary diode-connected transistors to which it is connected varies with respect to the magnitude of the current provided by the other current source connected to the other pair of secondary diode-connected transistors such that the sum of the currents provided by the current sources to the secondary diode-connected transistors always remain substantially constant.

The quiescent biasing currents provided by the current sources through the respective diode transistors to the emitters of the corresponding primary transistors are set to provide a Class A push-pull device which has the advantage over the Blackmer circuit in that distortion due to the inherent base resistance of the log and antilog transistors will be substantially reduced due to the cancellation by complementary errors in the corresponding set of base resistances of the second transistors of the same transmission path. Further, there is a slight difference in the voltage per decade current change in NPN and PNP transistors. The four-transistor, four-diode VCA cancels this error since a NPN and PNP transistor forms each log converter and each antilog converter of each path.

An improvement over the four-transistor, four-diode cell VCA is described in co-pending U.K. Patent Application 8023488 (which hereinafter referred to as the "companion application"). The companion application describes and claims a gain control circuit comprising amplification means (1) disposed in each log-antilog transmission path and (2) providing in each path signal gain as a function of the input signal to the circuit. Providing signal gain in each transmission path reduces the requirements of the input amplifier and increases the gain bandwidth product over that provided by the four-transistor, four-diode cell VCA.

The embodiment described in the companion application is Class A push-pull eight transistor gain cell VCA. More specifically, four secondary transistors are connected to the corresponding emitters of the primary transistors in a manner so as to provide signal gain greater than unity in each log-antilog transmission path the gain being a function of the input signal to the circuit. Each secondary transistor is of a conductivity type opposite to that of the primary transistor to which it is paired. The bases of the secondary transistors of one transmission path are tied together connected to system ground through a capacitor and a series resistor, as well as to the output of the input operational amplifier. The remaining secondary transistors, i.e., those of the other transmission path, have their collectors connected together and to the input of a differential current gain stage and their bases connected together and to the output of the gain stage. As described in the companion application, as long as the quiescent levels remain at least twice the maximum expected current level in response to the maximum input level, the sum of the biasing currents through the emitters of the primary transistors remain substantially constant.

Although the class A push-pull eight transistor gain cell VCA disclosed in the companion application is an improvement over the four-transistor, four-diode cell VCA, there are applications when the use of a Class AB amplifier is more desirable. These include circuits requiring low and gain-independent input bias currents and circuits in which noise levels must be kept as an absolute minimum.

Accordingly, one object of the present invention is to reduce the IM and harmonic distortion provided in the eight transistor gain cell.

According to ther present invention there is provided a gain control circuit for controlling the signal gain of an input signal in response to a control signal, said circuit comprising a pair of log-antilog transmission paths, one path for the signal portion of each representation of said input signal, each of said paths including: (a) first signal converting means for providing a first signal as a logarithm function of the respective portion of said input signal. (b) second signal converting means for providing an output signal as an antilogarithmic function of the sum of the first signal and the control signal; and (c) signal modification means disposed in each path for modifying said first signal and said output signal as a function of the input and output signals so as to reduce distortion in said output signal said signal modification means including means for generating as a function of the input signal and the output signal, a correction signal through each of said first signal and second signal converting means.

Other objects of the invention will in part be obvious and will in part appear hereinafter. The invention accordingly comprises the apparatus possessing the construction, combination of elements, and arrangement of parts which are exemplified in the following detailed disclosure, and the scope of the application of which will be indicated in the claims.

For a fuller understanding of the nature and objects of the present invention, reference should be had to the following detailed description taken in connection with the accompanying drawings, wherein:—

Fig. 1 shows a gain control circuit operable as

a Class AB amplifier in accordance with parent Patent Application No. 8028910;

Fig. 2 shows a modification to the Fig. 1 circuit to provide compensation for reducing distortion due to the inherent parasitic base resistance of the primary and secondary transistors of the gain cell in accordance with the present invention; and

Fig. 3 shows an alternative embodiment to the embodiment shown in Fig. 2.

Referring to the drawings, like numerals are used to describe like parts throughout the Figures.

In Fig. 1, the input signal current is applied to current input terminal 10 of the gain control circuit shown. Terminal 10 is shown connected to the negative input terminal of operational amplifier 12, the latter having its positive input connected to ground and its negative input connected to the input junction 14 which forms the input to the gain cell defining the two log-antilog transmission paths of the circuit. Input junction 14 is formed by the connection of the two collectors of the primary log transistors 16 and 18, the first being PNP transistor while the latter being an NPN transistor. The collectors of the primary antilog transistors 20 and 22 are joined at output junction 24 so as to form the current output terminal 26. As will be more evident hereinafter log transistor 16 and antilog transistor 20 in part define one log-antilog transmission path, while log transistor 18 and antilog transistor 22 in part define the other log-antilog transmission path. The gain control signal Ec is applied to the control signal input terminal 28. The latter is connected to the bases of a log transistor of one log-antilog transmission path and an antilog transistor of the other path. As shown the connection is made to the bases of primary transistors 18 and 20.

In order to provide symmetry among the primary transistors 16, 18, 20 and 22, the base of the antilog transistor which does not receive the control voltage, i.e. transistor 22, is conntected through resistor 34 to ground, and through resistor 36 to a variably adjustable DC voltage source 38; while the base of the remaining log transistor, i.e. transistor 16, is grounded. As well known adjustment of source 38 provides the desired symmetry to correct for the sum of the transistor device V_{be} mismatches in one log-antilog transmission path as compared with the transistor device mismatches in the other log-antilog transmission path.

To the extent described, the emitters of transistors 16 and 20 and the emitters of transistors 18 and 22, would be coupled together to form the Blackmer circuit. However, in accordance with the invention described and claimed in the companion application, the Blackmer circuit is modified such that amplification means, in the form of secondary transistors 40, 42, 44 and 46 are each connected to a corresponding emitter of a primary transistor and connected within the circuit so as to provide signal gain in each log-antilog transmission path.

More particularly, the emitter of each primary log transistor 16 and 18 is connected to the emitter of the respective secondary log transistor 40 and 42 with each secondary log transistor being of a conductivity type opposite to that of the primary log transistor to which it is paired. Similarly, the emitter of each primary antilog transistor 20 and 22 is connected to the emitter of the respective secondary antilog transistor being of a conductivity type opposite to that of the primary antilog transistor to which it is paired. The secondary transistors of each log-antilog transmission path have their collectors tied together and their bases connected together. This results in what has been referred to and is described in the companion application as an "eight transistor gain cell VCA". The embodiment of the eight transistor gain cell described in the companion application operates as a Class A amplifier. Biasing currents, the sum of which remains substantially constant, are provided through the emitters of the primary transistors with the quiescent levels of the biasing current being at least twice the maximum expected levels of the transmitted signals in response to the maximum input level. In this manner current flows through the transistors through the entire input cycle and no distortion due to cross-over is produced.

In the parent application No. 8028910, a Class AB gain control circuit is provided having advantages of the Class A device shown in the companion application. Referring to Fig. 1, in order to provide Class AB operation, the junction of the collectors of the secondary transistors 40 and 44 and the junction of the collectors of the secondary transistors 42 and 46 are each connected to a low impedance voltage source which is derived from transistors operated to maintain the source voltage to provide the respective desired biasing current. As shown, the junction of the collectors of secondary transistors 40 and 44 are connected to the emitter of NPN transistor 48, the latter having its collector connected to a positive voltage potential and its base connected to the positive side of a DC voltage source 50. Similarly, the tied collectors of transistors 42 and 46 are connected to the emitter of PNP transistor 52, the latter having its collector connected to a negative voltage potential and its base connected to the negative side of a DC voltage source 54. The positive side of source 54 is connected to the output of the input operational amplifier 12, which in turn is connected to the negative side of DC source 56. The negative side of source 50 and the positive side of source 56 are connected to the bases of secondary transistors 40 and 44, while the bases of secondary transistors are connected to the positive side of source 54 and the negative side of source 56. Sources 50 and 54 provide sufficient bias to operate transistor 48 and 52 to maintain the collector voltages of transistors 40, 42, 44 and 46 near their base voltage to minimize junction heating in the latter set of transistors as the resultant thermal gradients may cause significant gain error and distortion.

Preferably, the DC voltage sources 50, 54 and 56 are transistors connected in a diode mode, matched for their V_{be} transfer characteristics with those of the primary transistors 40, 42, 44 and 46 and suitably connected to a suitable current drive (not shown) in order to produce the desired voltage drop across each of the diode-connected transistors. The voltage potential provided by sources 50, 54 and 56 are such that the base of each of the secondary transistors 40, 42, 44 and 46 is provided with a bias voltage so as to produce a quiescent current (i.e. when the input current at input terminal 10 is zero) through the collector-emitter paths of the primary transistors 16, 18, 20 and 22. So long as the input current at terminal 10 is zero and the bias current of amplifier 12 is zero, an equal quiescent current flows through each of the transistors 16 and 18 and each of the transistors 20 and 22 and the current output at terminal 26 is zero. The amplitude level of the quiescent current is set well below that of the expected maximum input current in order to provide Class AB operation.

In operation, when the input signal current at input terminal 10 is of a first representation, e.g. of a positive polarity, the positive input current is applied to junction 14. As the input current at terminal 10 goes positive, the input at the negative input terminal of the input operational amplifier 12 goes positive resulting in the output of the amplifier to go negative. As the output of amplifier 12 goes negative the secondary transistors 42 and 46 become more conductive since a negatively increasing output of amplifier 12 results in a negatively increasing voltage on the base of transistors 42 and 46 and therefore an increase in the base-emitter voltage applied to the secondary transistors 42 and 46. Thus, more current flows through transistors 18, 22, 42 and 46. Simultaneously, the output of the operational amplifier 12 results in the secondary transistors 40 and 44 to become less conductive resulting in less current flowing through transistors 16 and 20. As the input current at terminal 10 increases, and other output of operational amplifier 12 becomes more negative, the transistors 42 and 46 become fully conductive and transistors 40 and 44 become completely non-conductive. Thus, the log-antilog transmission path defined by transistors 18, 42, 22 and 46 provides a signal at the output terminal 26 which is an antilogarithm function of the sum of the DC control signal Ec applied to terminal 28 and a signal which is a logarithmic function of the input signal.

Conversely, when the input signal current at the input terminal 10 is of an inverted representation, i.e., a negative polarity, the negative input current is applied to the junction 14. As the input current at terminal 10 goes negative, the input to the input operational amplifier 12 goes negative, resulting in the output of the amplifier going positive. As the output of the amplifier 12 goes positive the secondary transistors 40 and 44 become more conductive since a positively increasing output of amplifier 12 results in a positively increasing voltage on the base of transistors 40 and 44 and therefore an increase in the base-emitter voltage applied to the secondary transistors 40 and 44. Thus, more current flows through transistors 16, 20, 40 and 44. Simultaneously, the output of the operational amplifier 12 results in the secondary transistors 42 and 46 becoming less conductive and consequently less current flowing through transistors 18 and 22. As the negative input current at terminal 10 becomes more negative and the output of operational amplifier 12 becomes more positive, the transistors 40 and 44 become fully conductive and transistors 42 and 46 become completely nonconductive. Consequently, the log-antilog transmission path defined by transistors 16, 40, 20 and 44 provide a signal at the output terminal 26 which is in anti-logarithmic function of the sum of the DC control signal Ec applied to terminal 28 and a signal which is a logarithmic function of the input signal. The device as described thus provides Class AB operation.

Referring now to Figs. 2 and 3, these show the Fig. 1 circuit additionally including means for providing compensation derived from a comparison of the input and output signals so as to substantially reduce or cancel the distortion components in the output signal attributable to the inherent parasitic base resistances of the transistors in each of the log-antilog transmission paths in accordance with the present invention.

Referring to Figs. 2, resistors 60 and 62 of identical values are respectively connected between the collector of secondary transistor 40 and the emitter of transistor 48 and between the latter and the collector of secondary transistor 44. Similarly, identical resistors 64 and 66 are respectively connected between secondary transistor 64 and the emitter of transistor 52 and between the latter and resistor 66. The current generated through each of the resistors 60, 62, 64 and 66, will respectively be substantially equal to the biasing current plus the input current I_{in} when the latter is of a negative polarity, substantially equal to the biasing current plus the input current I_{in} when the latter is positive and substantially equal to the biasing current plus the output current I_{in} when the latter is positive and substantially equal to the biasing current plus the output current I_{out} when the latter is positive. Consequently, the voltage differential generated between (1) the collectors of secondary transistors 40 and 44 will be proportional to the difference between the input and output signals, when the latter are of a negative polarity and (2) the collectors of secondary transistors 42 and 46 will be proportional to the difference between the input and output signals when the latter are of a positive polarity. Thus, at unity gain when the input and output currents are equal the voltage generated across resistors 60 and 62 or across resistors 64 and 66 are equal and the voltage differentials will be zero.

Means are provided for measuring the

potential difference between the collectors of transistors 40 and 44 (i.e. across resistors 60 and 62) and between the collectors of transistors 42 and 46 (i.e. across resistors 64 and 66) and for providing compensation as a function of the potential differences so as to substantially reduce or cancel the distortion component in the output attributable to the inherent parasitic base resistances of transistors 16, 18, 20, 22, 40, 42, 44 and 46. The means for measuring the potential difference and providing the necessary compensation in Fig. 2 includes a pair of transistors 68 and 70 and a pair of transistors 72 and 74, each pair being connected as a differential pair. Specifically, the transistors 68 and 70 are PNP type transistors preferably matched with transistors 16, 20, 40 and 44, having their bases respectively connected to the collectors of secondary transistors 40 and 44, their emitters connected together and to current source 76 and their collectors respectively connected to the bases of secondary transistors 40 and 44. Similarly, the transistors 72 and 74 are NPN type transistors preferably matched with transistors 18, 22, 42 and 46, having their bases respectively connected to the collectors of secondary transistors 42 and 46, their emitters connected together and to current source 78 and their collectors respectively connected to the bases of secondary transistors 42 and 46. Resistors shown at 80, 82, 84 and 86 are inserted between the corresponding base of secondary transistors 40, 42, 44 and 46 and the corresponding point to which the bases are connected in the Fig. 1 embodiment.

Where the circuit operates at unity gain, the input signal equals the output signal. As a consequence for negative input signals the currents through resistors 60 and 62 will be equal and the voltage potential between the collectors of transistors 40 and 44 will be equal to zero. Thus the base voltage on transistor 68 equals the base voltage on transitor 70 and equal currents are provided from transistors 68 and 70 to the respective bases of transistors 40 and 44. Similarly, for positive input signals the currents through resistors 64 and 66 are equal and the voltage potential between the collectors of transistors 42 and 46 will be zero. Thus, the base voltages on transistors 72 and 74 are equal and the currents provided from transistors 72 and 74 are equal.

When the gain shifts from unity gain a greater armount of current will flow through one of the resistors 60 and 62 with respect to the current flowing through the other since its current flowing through resistor 60 equals the input current plus the biasing current from transistor 48, the current flowing through resistor 62 equals the output current plus the same biasing current from transistor 78 and at nonunity gain the output current does not equal the input current. Thus, a voltage potential differential exists between the collector of transistor 40 and the collector of transistor 44. As a function of the difference between the input and output currents. This voltage potential differential produces a current differential output of transistor 68 and 70 to the bases of transistors 40 and 44. This current differential is converted to a voltage across resistor 80 or 84 which is added to the log signal to substantially reduce or cancel the voltage error provided by the inherent parasitic base resistances of the transistors 16, 20, 40 and 44. A similar result occurs for positive input signals at nonunity gain in the other log-antilog transmission path defined by transistors 18, 22, 42 and 46. The currents from sources 76 and 78 are each adjusted to provide precisely the gain between the voltage signals from the collectors of transistors 40 and 44 and the collectors of transistors 42 and 46 to impress exactly the correction voltage required across resistors 80, 82, 84 and 86. This is especially useful in integrated circuits where the correcting currents can be connected to external currents so as to permit adjustment.

In the alternative arrangement shown in Fig. 3, the differential pair of transistors 68 and 70 and current source 76 can be replaced with a pair of cross resistors 90 and 92. Cross resistor 90 is connected between the collector of transistor 40 and the base of transistor 44. Cross resistor 92 is connected between the base of transistor 40 and the collector of transistor 44. Similarly, the differential pair of transistors 72 and 74 and current source 78 is replaced by cross resistors 94 and 96. Cross resistor 94 is connected between the base of secondary transistor 42 and the collector of transistor 46, and cross resistor 96 is connected between the base of secondary transistor 46 and the collector of transistor 42.

At unity gain equal currents flow through resistor 60 and 62 or resistors 64 and 66 and the base voltages on transistors 40 and 44 or transistors 42 and 46 will be the same. Accordingly, the potential across resistor 90 will substantially equal that across resistor 92 and the potential across resistor 94 will substantially equal the potential across resistor 96. As the gain changes from unity gain, and the input and output current are different. Depending on the polarity of the input signal, the voltage drop across resistor 90 will be different from the voltage drop across resistor 92 and the voltage drop across resistor 94 will be different from that across resistor 96 due to the respective voltage differential between the collectors of transistors 40 and 44 and between the collectors of transistors 42 and 46. Since the currents through resistors 60 and 64 are always equal to the input signal plus the biasing current (depending on the polarity of the input signal) and similarly the currents through resistors 62 and 66 are always equal to the output signal plus the biasing signal the difference of the currents flowing through resistors 90 and 92 and through resistors 94 and 96 are a function of the difference between the input and output signals. The current differential is again converted to a voltage on the base of the appropriate

secondary transistor where it is added to the log signal so as to cancel or substantially reduce the distortion component due to the inherent resistances of transistors, 16, 18, 20, 22, 40, 42, 44 and 46. The Fig. 3 embodiment has the further advantage over the Fig. 2 embodiment in that any mismatching between transistors 40 and 44 and between transistors 42 and 46 can respectively be compensated for by adjusting the relative values of resistors 90 and 92 and the relative values of resistors 94 and 96.

The present invention provides an improved gain control circuit suitable for Class AB operation and for correcting for the distortion component in the output signal attributable to the inherent parasitic base resistors of the transistor components in the log-antilog transmission paths.

Since certain changes may be made in the above apparatus without departing from the scope of the invention herein involved, it is intended that all matter contained in the above description or shown in the accompanying drawing shall be interpreted in an illustrative and not in a limiting sense.

In our copending U.K. patent application No. 8028910 there is described and claimed a gain control circuit for controlling the signal gain of an input signal in response to a control signal, said circuit comprising:

A pair of logarithmic-antilogarithmic transmission paths, one path for the signal portion of each representation of said input signal, each of said paths including

(A) first signal converting means including first and second transistors for providing a first output signal as a logarithmic function of the respective portion of said input signal

(B) second signal converting means including primary and secondary transistors for providing a second output signal as an anti-logarithmic function of the sum of said first output signal and said gain control signal;

means for generating a quiescent biasing current through said first and second signal converting means of each of said paths at levels below the maximum expected levels of the input signal and said second output signal of each of said paths; and

means connected to said second and secondary transistors of each path for setting said biasing currents through the first and second signal converting means of each of said paths so that said circuit operates as a class AB amplifier.

Claims

1. A gain control circuit for controlling the signal gain of an input signal in response to a control signal, said circuit comprising: a pair of log-antilog transmission paths, one path for the signal portion of each representation of said input signal, each of said paths including:

(a) first signal converting means for providing a first signal as a logarithm function of the respective portion of said input signal;

(b) second signal converting means for providing an output signal as an anti-logarithmic function of the sum of the first signal and the control signal; and

(c) signal modification means disposed in each path for modifying said first signal and said output signal as a function of the input and output signals so as to reduce distortion in said output signal said signal modification means including means for generating, as a function of the input signal and the output signal, a correction signal through each of said first signal and second signal converting means.

2. A circuit according to claim 1, wherein each of said first signal converting means comprises a primary and a secondary transistor, and each of said second signal converting means comprises first and second transistors, wherein the collector current of the secondary transistor of each of said first signal converting means of each path is a function of the respective portion of said input signal, and the collector current of the second transistor of each of the second signal converting means is a function of the output signal.

3. A circuit according to claim 2, wherein a correction signal is generated through each of said primary and secondary transistors of said first signal converting means as a function of said input signal, and through each of said first and second transistors of said second signal converting means as a function of said output signal.

4. A circuit according to claim 3, wherein said signal modification means includes a pair of transistors for each of said paths, said pair of transistors being connected to provide a correction signal to the base of one of said first, second, primary and secondary transistors of each of said signal converting means in response to the detected signal level of the corresponding collector current of the second or secondary transistors of the same signal converting means.

5. A circuit according to claim 4 wherein each said pair of transistors is adapted to be driven by a common voltage source.

6. A circuit according to claim 2, wherein a correction signal is generated through each of said primary and secondary transistors of each first signal converting means and the first and second transistors of each second signal conversion means as a function of the difference between the collector current of the secondary transistor of the first signal converting means and the collector current of the second transistor of the corresponding second signal converting means of the same path.

7. A circuit according to claim 6, wherein said signal modification means includes a pair of transistors for each of said paths, said pair of transistors being connected to provide the correction signal to the base of one of said first, second, primary and secondary transistors of each of the first and second signal converting means in response to the difference in voltage levels of the

collectors of the second and secondary transistors of the same path.

8. A circuit according to claim 7 wherein each pair of transistors is adapted to be connected to a common current source.

9. A circuit according to claim 6, wherein said signal modification means includes means for cross-coupling the base of each of the second and secondary transistors of the same path respectively with the corresponding collectors of the secondary and second transistors of that path so that the signal correction provided is a function of the difference between the voltages on the collectors of the second and secondary transistors of the same path.

10. A circuit according to claim 2, further including a resistor coupled to the collector of each of said second and secondary transistors, and the value of each said resistor is a function of any mismatching in the VBE/IC characteristics of the primary and secondary transistors of the first signal converting means with that of the VBE/IC characteristics of the first and second transistors of the second signal converting means of the same path.

11. A circuit according to claim 2, further including means for generating a biasing current through each of said first, second, primary and secondary transistors so that said circuit operates substantially as a class AB device.

Superseded claims 10 and 11

New or amended claims:—

10. A circuit according to claim 2, further including a resistor coupled to the collector of each of said second and secondary transistors, and the value of each said resistor is a function of any mismatching in the VBE/IC characteristics of the primary and secondary transistors of the first signal converting means with that of the VBE/IC characteristics of the first and second transistors of the second signal converting means of the same path.

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