Sept. 18, 1962 D. N. LEE 3,054,905

LOAD-DRIVING CIRCUIT

Filed Nov. 21, 1960

2 Sheets-Sheet 1

FIG. 1.

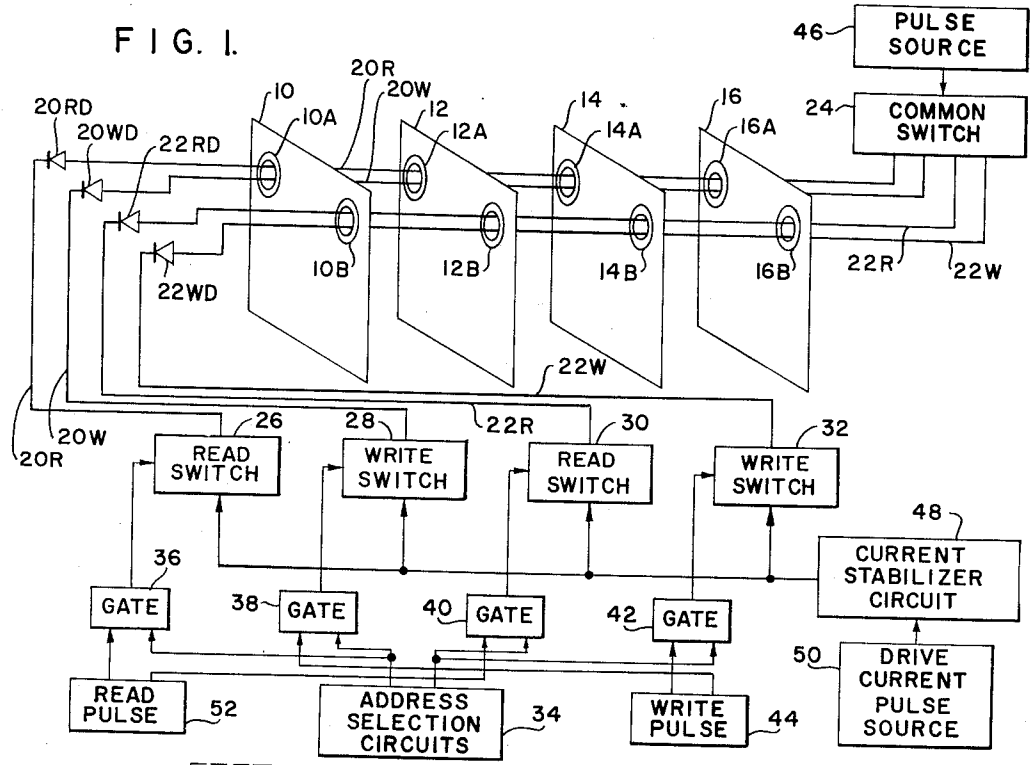
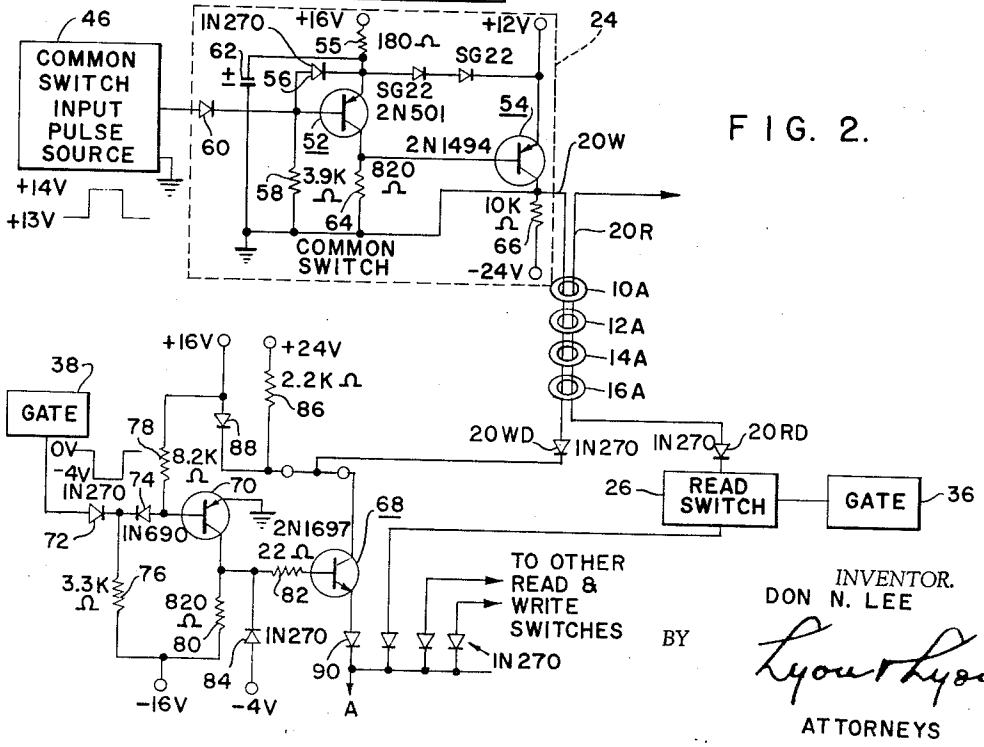



FIG. 2.

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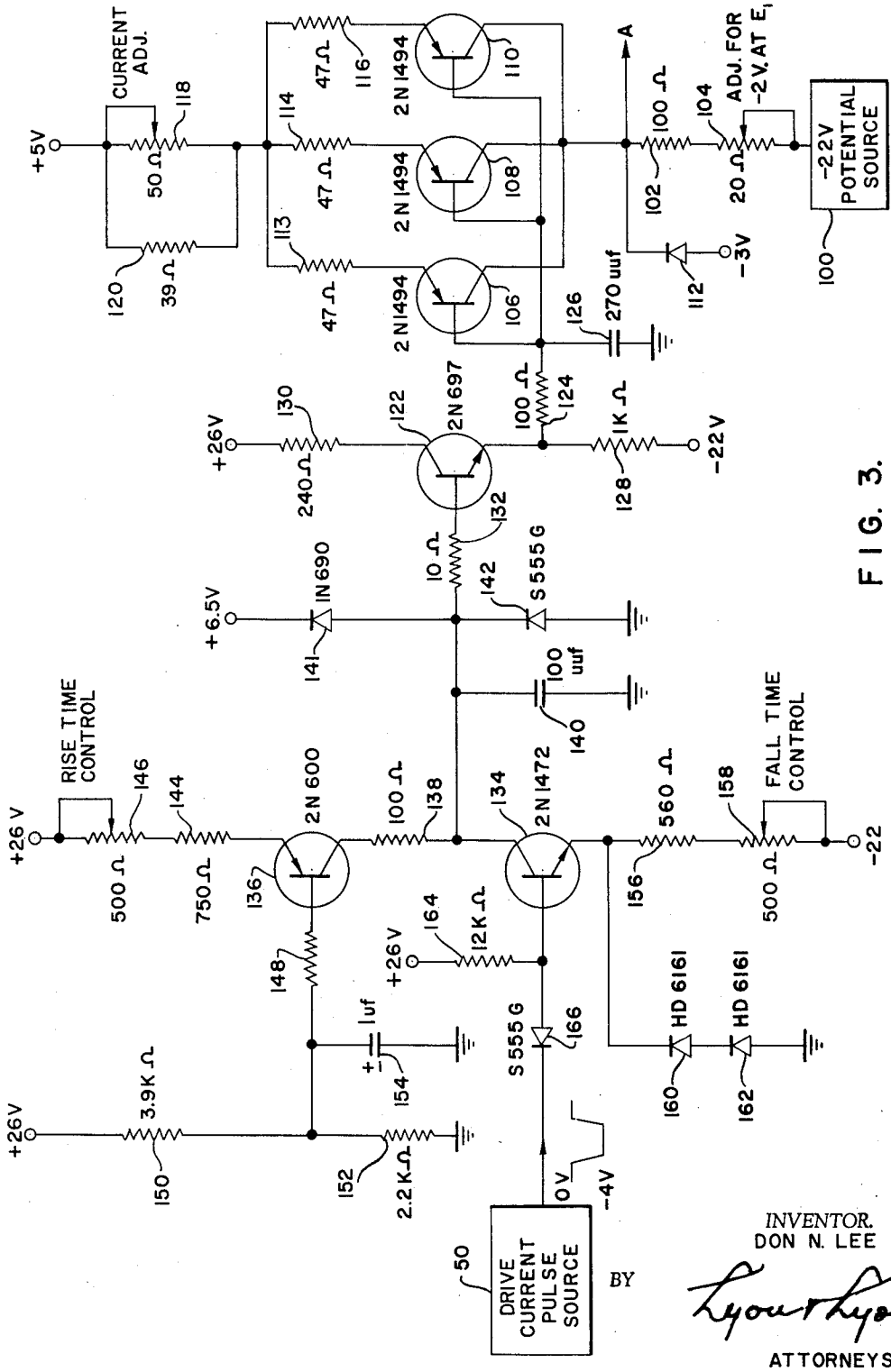


FIG. 3.

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3,054,905

# LOAD-DRIVING CIRCUIT

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7 Claims. (Cl. 307—88)

This invention relates to circuitry which is employed for driving loads of the type having a diode in series with an inductance and, more particularly, to improvements therein.

Memory systems of the type employing a large number of magnetic cores, each of which has a substantially toroidal shape as well as a substantially rectangular hysteresis characteristic, have found extensive employment in present-day computer systems. There are various different arrangements employed for the wiring of the magnetic memory, but these all substantially reduce to an arrangement for applying current through one or more windings inductively coupled to a core for the purpose of driving that core from saturation at one polarity to saturation at the opposite polarity. One popular memory system is known as the "word-organized" system. In a "word-organized" memory system, there are provided a plurality of core planes, the number being determined by the number of bits desired for a word. Each core plane has a number of cores arranged in columns and rows, the number being determined by the word-storage capacity for the memory. These core planes are usually arranged in a manner so that one core in each core plane can be driven, for either reading or writing, simultaneously with one core in each of the other core planes. Thus, by properly addressing or selecting the driving windings, a word at a time may be read into or out of the word-organized memory.

The usual winding arrangement is to have one winding coupled to a different core in each one of the core planes. These cores are associated for the purpose of storing a single word. Two other windings are provided for each one of the core planes. Each of these windings is coupled to every one of the cores in the associated core plane. These two other windings are usually called the digit-plane winding and the sense winding. A drive winding has current applied thereto, so that the associated single core in the core planes is driven to saturation at a given polarity. If it is desired to read out the word previously stored in these cores, then the sense winding for each digit plane detects whether or not an output is derived in response to the applied drive.

In the fabrication of a word-organized memory, in order to insure that currents will flow through the drive windings in only one direction, a diode is connected in series with each one of the drive windings. This precaution is taken, not only to avoid the effects of induced currents in these windings, but also, and more particularly, to prevent currents from flowing due to "sneak current paths" which can occur when one end of each one of the drive windings is connected to a common return terminal. In the operation of a word-organized memory, particular care must be paid to the consistency and stability of the rate of rise and fall, as well as to the amplitude of the current in the drive windings. At higher rates of operation, the diode in each drive winding presents complications for obtaining linear current rise and minimum cycle time, since diodes which can operate at sufficiently high currents have appreciable delays, both in achieving forward conduction and in turning off.

An object of this invention is to provide a drive circuit which minimizes the effect of a diode in a load of the type described.



Another object of this invention is the provision of a novel drive circuit for a load of the type described.

Still another object of the present invention is the provision of an improved drive circuit.

These and other objects of the invention are achieved in an arrangement wherein current for driving a load, which comprises effectively any inductance in series with a diode, is applied in a manner so that, first, the diode is primed, and, thereafter, the required load current is provided. In this manner, the required linearity of the driving waveform for the load is maintained, since the priming current for the diode is extremely small, when compared to the current for driving the load, and, thus, as far as the load is concerned, is negligible. The forward conduction and turnoff time of the diode, which heretofore presented a problem, effectively is no longer a handicap. The arrangement employed is to provide current from a constant-current source to a selected driving winding and to a dummy load. Because of the presence of the dummy load, the selected drive-winding current is small, just sufficient to prime the diodes. As soon as this is accomplished, the dummy load is removed or opened, whereby the full-load current is applied to the drive winding.

The novel features that are considered characteristic of this invention are set forth with particularity in the appended claims. The invention itself, both as to its organization and method of operation, as well as additional objects and advantages thereof, will best be understood from the following description when read in connection with the accompanying drawings, in which:

FIGURE 1 is a block diagram illustrating a driving arrangement for a word-organized memory in accordance with this invention; and

FIGURES 2 and 3, taken together, comprise the circuit diagram of an embodiment of this invention.

Reference is now made to FIGURE 1, which is a block diagram illustrating how an embodiment of this invention may be employed for driving a magnetic-core word-organized memory. Such memory will include a plurality of digit-core planes **10**, **12**, **14**, **16**. Each one of these core planes contains a plurality of magnetic cores which, in each core plane, are exemplified, respectively, by **10A**, **10B**, **12A**, **12B**, **14A**, **14B**, **16A** and **16B**. There are as many cores in each digit plane as the number of words desired to be stored. The only windings which are represented in FIGURE 1 are the drive windings for reading and writing. In an embodiment of the invention which was constructed, two of these windings were employed for each group of cores assigned to a word. One of these windings **20R** was employed when it was desired to read, and the other of these windings **20W** was employed when it was desired to write. These are the windings which are shown inductively coupled to the cores **10A**, **12A**, **14A**, **16A**. The other set of drive windings **22R**, **22W** are employed for storing or reading from the cores **10B**, **12B**, **14B**, **16B**.

One end of all the windings in the memory is connected to a common switch **24**. The other end of the read winding **20R** is connected to a read switch **26**. The other end of the write winding **20W** is connected to a write switch **28**. The other end of the read winding **22R** is connected to a read switch **30**. The other end of the write winding **22W** is connected to the write switch **32**.

When it is desired to write into a certain section of the memory first, the address-selection circuits **34** are activated to apply an enabling pulse to one of the plurality of gates **36**, **38**, **40**, **42**. A different one of these gates is assigned to each read switch, and, likewise, a different one of these gates is assigned to each write switch. The address-selection circuits **34** comprise a circuit ar-

rangement, well known in the art, for directing an enabling pulse to the one of the gates, the output from which is connected to either the write switch or read switch, which will drive the line coupled to the cores in the section of the memory wherein either reading or writing is to occur.

Thus, assume that the address-selection circuits 34 have enabled gate 38. A write-pulse source 44 applies a pulse to all the gates which are connected to the write switches. However, only the enabled gate 38 will provide an output. This output is applied to the write switch 28. Another pulse source 46 applies a pulse to the common switch. As a result of the pulses to the common switch 24 and the write switch 28, current is applied by a current-stabilizer circuit 48, which flows through the write switch, the line 20W, and the diode 20WD, to the common switch 24. The value of this current, however, is insufficient to drive the cores 10A through 16A, but is sufficient to prime the diode 20WD or to place it in a condition such that the rise time and fall time of the drive pulse is substantially unaffected by the presence of the diode in the line, and the wave shape of the drive pulse is substantially unaffected thereby, as well. Substantially, as soon as the priming current is established, a pulse is provided to the current-stabilizer circuit by the drive-current pulse source 50, which enables the current-stabilizer circuit to provide the required drive current to the cores 10A, 12A, 14A, and 16A.

It will be appreciated that a number of other necessary windings to the core plane, such as the digit-plane winding and the sense winding, have been omitted in the interest of simplicity in the drawings. It is believed that the function of these is sufficiently well understood so that an explanation of these in connection with this invention is not necessary. From the description of the block diagram in FIGURE 1, it will be appreciated how, whenever it is desired to drive any of the groups of cores which are employed for storing a word, the address-selection circuits are enabled to select that core group; then a read-pulse source 52 or write-pulse source 44 provides a pulse through the selected gate to select a read switch or write switch, which is connected to the drive winding coupled to the cores desired to be written into or read from. The pulse source 46 then provides an enabling pulse to the common switch 24, whereby a priming current is provided to the selected drive line. Almost instantaneously thereafter the drive-current pulse source 50 enables the current-stabilizing circuit 48 to provide a drive current to the selected drive line.

Reference is now made to FIGURES 2 and 3, which show a circuit diagram of the embodiment of the invention.

FIGURE 2 shows the circuit diagram of the common switch and read or write switch circuit, and FIGURE 3 shows the circuit diagram of the current-stabilizer circuit. Similar reference numerals are applied to structures shown in FIGURES 2 and 3 which are identical to those shown in FIGURE 1. Thus, by way of example, only the cores 10A, 12A, 14A, and 16A are shown in FIGURE 2. These cores are inductively coupled to a write winding 20W and to a read winding 20R. In series with these windings are the diodes 20WD and 20RD, respectively. The common-switch input-pulse source 46 drives the common switch, which includes two transistors 52, 54. The common-switch input-pulse source 46 is connected to the base of transistor 52 through a diode 60. The emitter of the transistor 52 is connected through a resistor 55 to a source of operating potential, which, by way of example, is shown as 16 volts. A diode 56 is connected between the emitter and base of transistor 52. A resistor 58 is connected between the base and ground of the transistor 52. A capacitor 62 is connected from the emitter of transistor 50 to ground.

The emitter of transistor 54 is connected to a source of operating potential, shown by way of example as 12 volts. The collector of transistor 52 is connected to the base of transistor 54 and also to ground through a resistor 64. The collector of transistor 54 is connected to a —24-volt source through a resistor 66. The collector of transistor 54 is also connected to ground. One end of the windings passing through all the cores is connected to the collector of transistor 54. The other end of winding 20W is connected through a diode 20WD to the collector of a transistor 68 in the write switch. This write switch besides transistor 68 also includes a transistor 70.

The gate 38 applies an output to the base of transistor 70 through two diodes, respectively 72, 74, which are connected in series opposition. The junction of these two diodes is connected through a resistor 76 to a negative-potential source. Thus, a negative-input pulse from the gate 38 allows the junction of the two diodes to go negative, thereby blocking diode 74 and making the base of transistor 70 positive. The base of transistor 70 is connected to a positive potential source through a resistor 78. The emitter of transistor 70 is connected to ground; the collector is connected to a negative-potential source through a resistor 80 and is also connected to the base of transistor 68 through a resistor 82. The collector of transistor 70 is also connected to a negative-potential source through a clamping diode 84. The collector of transistor 68 is connected to the diode 20WD and also through a positive-potential source through a resistor 86. It is also connected to the potential source used for biasing the base of transistor 70 through a clamping diode 88. The emitter of transistor 68 is connected through a diode 90 to the current stabilizer circuit shown in FIGURE 3. All the read and write switches are connected through diodes to the current stabilizer. The points of connection are respectively designated by the letter "A" in FIGURES 2 and 3.

The current-stabilizer circuit includes a source of potential 100 from which the drive current is derived. In series therewith, there is a fixed resistor 102 and a variable resistor 104. The values of these resistors are selected so that a constant-current source is provided for the low-impedance load which is being driven. In series with the constant-current source or resistors and potential source there is provided a "dummy load." This dummy load comprises as many transistors as are required to handle the current required for driving. In an embodiment of the invention which was built, three transistors 106, 108, and 110 were used. These have their collectors connected in parallel and in series with the resistor 102. Also connected to this point is a clamping diode 112, which is, in turn, connected to a negative-bias-potential source. The respective emitters of the transistors 106, 108, 110 are connected through resistors 113, 114, 116 to a source of operating potential through the potentiometer 118, which is connected in parallel with a resistor 120.

The three transistors constituting the dummy load are driven by a transistor 122. The emitter of transistor 122 is connected to the bases of all of the transistors 106, 108, 110 through a resistor 124. A capacitor 126, which is connected between the bases of transistors 106, 108, and 110 and ground, serves to bypass current fluctuations. The emitter of transistor 122 is connected through a resistor 128 to a negative-potential source, and its collector is connected through resistor 130 to a positive-potential source. The base of the transistor 122 is connected through a resistor 132 to the collector of a transistor 134. A second transistor 136 has its collector connected through a resistor 138 to the collector of transistor 134. A capacitor 140 is connected from the collector of transistor 134 to ground. A first diode 141 is connected between a source of positive bias and the collector of transistor 134. A second diode 142 is connected between the collector of transistor 134 and ground.

Transistor **136** has its emitter connected through a resistor **144** in series with a potentiometer **146** to a source of positive potential. The base of transistor **136** is connected through a resistor **148** to a voltage divider or bias potential source which includes two resistors **150**, **152**, connected between a source of potential and ground. A capacitor **154** is connected across resistor **152**. Transistor **134** has its emitter connected through resistor **156** and potentiometer **158** to a negative-bias source. Two diodes in series, respectively **160**, **162**, are connected between the emitter of transistor **134** and ground. A resistor **164** connects a positive-bias source to the base of transistor **134**. The drive-current-pulse source **50** is connected to the base of transistor **134** through a diode **166**.

In the quiescent state, which occurs when no drive is applied to the memory, the read and write switch transistors are in nonconductive states, as are also the common-switch transistors. Transistor **136** is biased to be conductive, as is also transistor **134**. Transistor **122** is also maintained conductive as a result, and this maintains the transistors **106**, **108**, and **110** conductive, also. Current from the potential source flows through resistor **102**, and through the three transistors **106**, **108**, **110**, which constitute the dummy load. Potentiometer **118** is used to adjust the value of this current.

When a reading or writing operation is desired, then a pulse is applied from the common-switch input-pulse source **46** to transistor **52** at the same time that a pulse is applied to transistor **70** from the gate **38**. The input pulse from the gate **38**, in an embodiment of the invention which was built, was a negative-going pulse which falls from zero to −4 volts. This resulted in a change of the potential at the emitter of transistor **68** from −2 volts to 0.75 volt. The pulse from the common-switch input-pulse source enables transistor **52** to turn on transistor **54** so that a priming current is permitted to flow from the current stabilizer through transistor **68**, through the diode **20WD** in series with the winding **20W**, and then through the common-switch transistor **54**. However, only a small amount of current is available in this path as long as the dummy load is maintained conductive. In an embodiment of the invention which was built, the required priming current was approximately 15 milliamperes.

The turning on of the common switch and read or write switch circuits precedes only momentarily the application of a drive-current-pulse source to the current-stabilizer circuits, on the order of a tenth of a microsecond. The application of a drive-current pulse from the source **50** turns off the transistor **134**. As a result, transistor **122** is turned off, and this, in turn, turns off dummy-load transistors **106**, **108**, and **110**. Effectively, this results in opening the dummy load, whereby current can be provided through resistor **102** to the transistor **68** and the drive winding **20W** in an amount required for driving the cores.

When transistor **134** is cut off, capacitor **140** charges up from transistor **136**. As a result, a linear rate of voltage change is applied to the base of transistor **122**, so that its cutoff and that of the three transistors **106**, **108**, **110** also occur at a linear rate. Accordingly, the current increase in the word drive line occurs at a linear rate. The rise time of the current can be adjusted from 30 millimicroseconds up to any larger value desired by means of the adjustment potentiometer **146**.

After a time interval determined by the duration of the pulses applied to the circuits, the current begins to fall. The fall time of the current is controlled by the potentiometer **158** in the emitter of transistor **134**. This determines the duration of time required to discharge capacitor **140**. The current drawn by the dummy load is determined by the setting of potentiometer **118**. Potentiometer **104** determines the voltage established at the output of the current stabilizer.

The values provided in the circuit diagram of the invention are shown by way of exemplification of an embodiment of the invention which was actually constructed and operated. These, however, are not to be construed as a limitation on the invention.



There has been shown and described herein a circuit arrangement for driving a load which includes a diode in series with an inductance, wherein delays caused by the diode in turning on and turning off large currents are rendered negligible. Further, degradation of the driving-current wave shape caused by the presence of the diode is also made negligible. The driving current wave shape now has a linear rise and fall, and, by means of this invention, independent control over the rise and fall times is made available.

I claim:

1. A circuit for driving a load comprising a plurality of magnetic cores, a winding coupled to said plurality of magnetic cores, and a diode connected in series with said winding, said circuit comprising means for applying a priming current to said series-connected diode and winding, and means for applying a driving current to said series-connected diode and winding immediately after said priming current, said priming current being small relative to said driving current.

2. A circuit for driving a load comprising a plurality of magnetic cores, a winding coupled to said plurality of magnetic cores, and a diode connected in series with said winding, said circuit comprising means for applying a priming current to said series-connected diode and winding, and means connected to said means for applying a priming current for enabling it to increase the amplitude of the current applied to a load-driving current level immediately after application of said priming current.

3. A circuit for driving a load of the type comprising a plurality of magnetic cores, a winding coupled to said magnetic cores, and a diode connected in series with said winding, said circuit comprising a first and second transistor each having base, collector, and emitter electrodes, means for connecting said series-connected diode and winding between said first transistor collector and said second transistor collector, means for rendering said first and second transistors conductive, current-source means connected to said second transistor emitter and including means for providing a value of current when in the quiesent state for said first and second transistors and said series-connected diode and winding for priming said diode, and means for providing a value of current when in the active state to said first and second transistors and said series-connected diode and winding for driving said load; and means for driving said current-source means to its active state.

4. A circuit for driving a load of the type comprising a plurality of magnetic cores, a winding coupled to said magnetic cores, and a diode connected in series with said winding, said circuit comprising a first and second transistor each having base, collector, and emitter electrodes, means for connecting said series-connected diode and winding between said first transistor collector and said second transistor collector, means for rendering said first and second transistors conductive for providing a priming current for said diode followed by a load-driving current including an auxiliary load, a source of potential, a resistor connecting said auxiliary load to said source of potential, means connecting said second transistor emitter to said resistor where it connects to said auxiliary load, and means for preventing said auxiliary load from drawing current through said resistor after said first and second transistors have been rendered conductive.

5. A circuit for driving a load of the type comprising a plurality of magnetic cores, a winding inductively coupled to said magnetic cores, and a diode connected in series with said winding, said circuit comprising a potential source, a transistor having base, emitter, and collector electrodes, a resistor connecting said collector to said potential source, means for maintaining said transistor conductive for drawing current from said potential source

through said resistor, switch means coupling said load to said collector for applying current to said load when operated, means for operating said switch means, and means for rendering said transistor nonconductive after operation of said switch means whereby said load has a driving current applied thereto.

6. A circuit for driving a load of the type comprising a plurality of magnetic cores, a winding coupled to said magnetic cores, and a diode connected in series with said winding, said circuit comprising a first and second transistor each having base, collector, and emitter electrodes, means for connecting said series-connected diode and winding between said first transistor collector and said second transistor collector, means for rendering said first and second transistors conductive, a third transistor having base, emitter, and collector electrodes, a source of operating potential, a resistor connecting said source of operating potential to said third transistor collector, means connecting said third transistor emitter to said source of operating potential, means connecting said second transistor emitter to said third transistor collector, means for applying a signal to said third transistor collector for maintaining said third transistor conductive to supply priming current to said diode when said first and second transistor are rendered conductive, and means for removing said signal from said third transistor collector for rendering said third transistor nonconductive to supply load-driving current to said load.

7. A circuit for driving a load of the type comprising a plurality of magnetic cores, a winding coupled to said magnetic cores, and a diode connected in series with said winding, said circuit comprising a first and second transistor each having base, collector, and emitter electrodes, means for connecting said series-connected diode and winding between said first transistor collector and said second transistor collector, means for rendering said first and second transistors conductive, a third transistor



having base, emitter, and collector electrodes, a source of operating potential, a resistor connecting said source of operating potential to said third transistor collector, means connecting said third transistor emitter to said source of operating potential, means connecting said second transistor emitter to said third transistor collector, means for controlling the conductive state of said third transistor including fourth, fifth, and sixth transistors each having collector, emitter, and base electrodes, means coupling said fourth transistor emitters to said third emitter base, a first operating potential source, means connecting said first operating potential source to said fourth transistor collector and emitter, means connecting said fourth transistor emitter to said third transistor base, second and third operating potential sources, means for respectively connecting said second and third operating potential sources to the fifth and sixth transistor collectors and emitters, means connecting said fifth and sixth transistor collectors together, means connecting said fifth and sixth transistor collectors to said fourth transistor base, means for applying bias potential to the bases of said fifth and sixth transistors for maintaining these transistors and said fourth and third transistors conductive, a capacitor connected in parallel with said fifth transistor, means for applying a signal to said fifth transistor to overcome the bias applied thereto and render it nonconductive whereby said capacitor will charge up from said sixth transistor and render said fourth and third transistors nonconductive to thereby provide a load-driving current to said load.

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