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(54) **Data Transmission; Clock Pulse Recovery**

(57) Circuitry capable of dealing with the problems caused by receiver clock sub-system failure leading to cycle skipping, i.e. loss of bit count integrity, for use in a digital transmission receiver system comprises both means for blocking spurious receiver clock pulses and means for supplying missing receiver clock pulses, and includes:— means including an AND gate 1 associated with a first monostable circuit Mono 1 for blocking further clock pulses after a first clock pulse for a first predetermined time slightly less that the time between two adjacent normal clock pulses; and means pulse gen 2 for supplying a clock-type pulse if a normal and unblocked clock pulse fails to be generated after a first clock pulse within a second predetermined time slightly more than the time between the adjacent normal clock pulses.

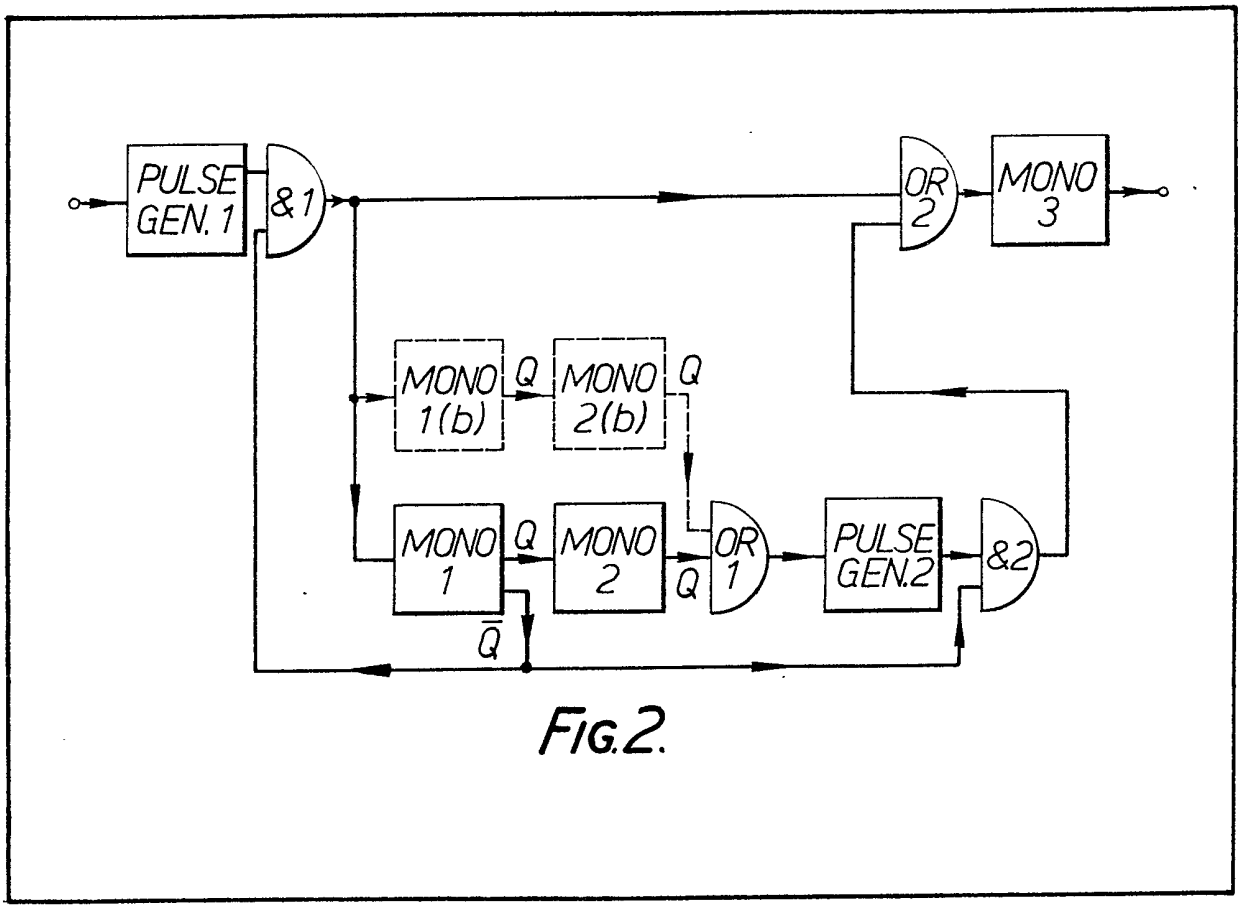

FIG.2.

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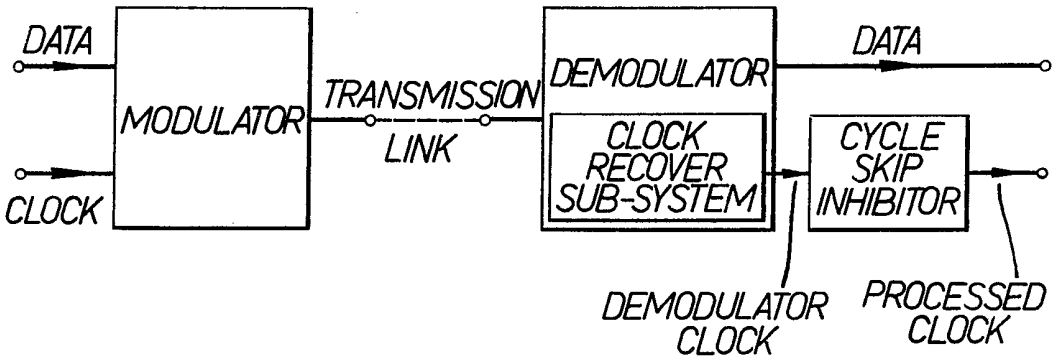
DATA
CLOCK
MODULATOR
TRANSMISSION LINK
DEMODULATOR
CLOCK RECOVER SUB-SYSTEM
DATA
CYCLE SKIP INHIBITOR
DEMODULATOR CLOCK
PROCESSED CLOCK

FIG. 1.

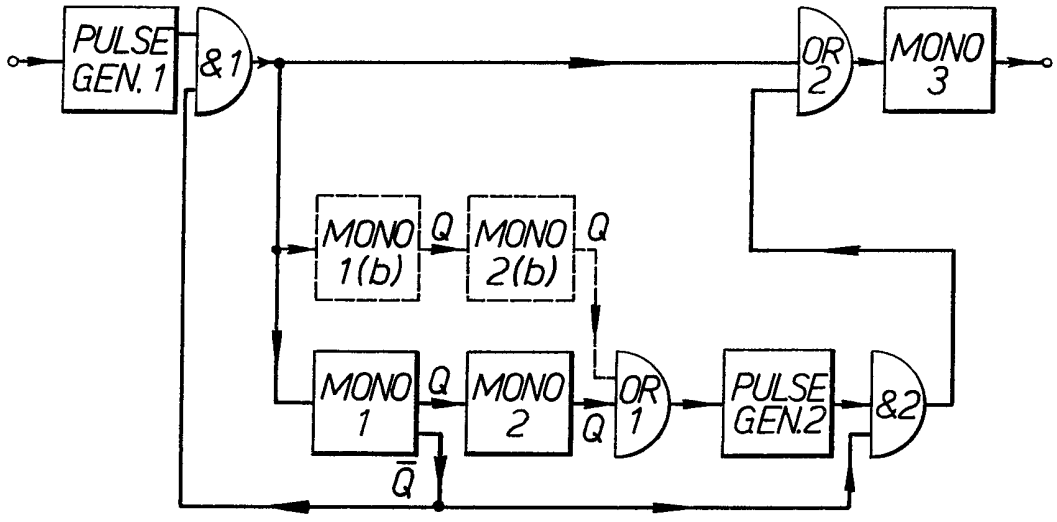
PULSE GEN. 1
&1
OR 2
MONO 3
MONO 1(b)
Q
MONO 2(b)
Q
MONO 1
Q
MONO 2
Q
OR 1
PULSE GEN.2
&2
Q̄

FIG. 2.

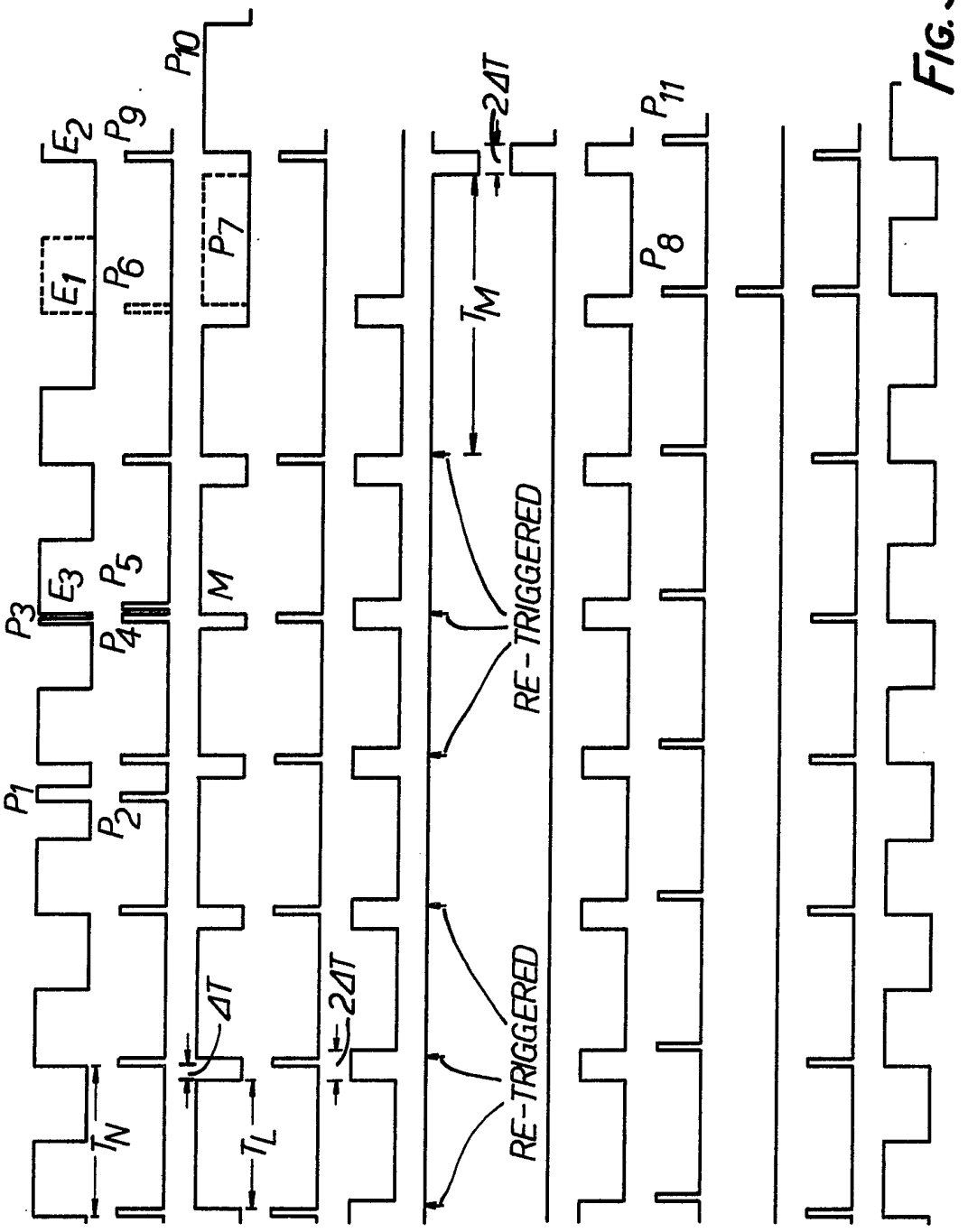
a) DEMODULATOR CLOCK OUTPUT
b) PULSE GEN 1 OUTPUT
c) MONO 1 Q OUTPUT
d) &1 OUTPUT
e) MONO 2 Q OUTPUT
f) MONO 1b Q OUTPUT
g) MONO 2b Q OUTPUT
h) OR-1 OUTPUT
j) PULSE GEN 2 OUTPUT
k) &2 OUTPUT
l) OR-2 OUTPUT
m) MONO 3 OUTPUT
P1
P2
P3
P4
P5
P6
P7
P8
P9
P10
P11
E1
E2
E3
M
TN
TL
TM
Δt
2Δt
2Δt
RE-TRIGGERED
RE-TRIGGERED

FIG. 3.

SPECIFICATION

Data Transmission

This invention relates to data transmission, and concerns in particular the maintenance of bit count integrity in the transmission of data in digital form.

There are many occasions when it is desirable to transmit data in the form of electrical or electromagnetic pulses along a wire or radio link, and these days the data is very frequently in binary digital form—that is, in the form of a series of sets of discrete on/off pulses in which each set of pulses is in essence a number defining the magnitude of some factor, the series of sets then defining how that factor's magnitude varies with some other factor (normally time)—rather than in analogue form, where the signal fluctuates continuously in magnitude in a manner analogous to the magnitude fluctuation of the factor being defined thereby. Digital data links of this general kind are now very common in long distance telephone and radio communications systems, and are practically essential in computer networks.

Digital data transmission systems have certain very significant advantages over analogue systems, and one of these is that, because, unlike an analogue signal, a digital signal being received should—at certain times defined by a regular series of clock pulses—only have one or another of a relatively few discrete values (in a binary system there are, of course, only two such values), if what is received does not in fact have one of the appropriate discrete values, but is approximate to such a value, then the receiving equipment can modify the signal so that it does have the exact value—and thus can "regenerate" exactly the transmitted signal in its original form free from all interference. For example, in a binary digital transmission signal where the data is transmitted as a series of on/off pulses, and these are assigned the respective values "1" and "0", a "1" signal which, because of interference, arrives at the receiver as "0.9" can automatically be represented as a "1" signal identical to the original signal.

Nevertheless, even digital transmission systems suffer from some problems. One of these, for example, is when the noise level—the amount of interference caused to the signal—is such as to result in a degree of distortion comparable to the magnitude of the signal itself, in which case the receiver equipment may well approximate the received signal to the wrong discrete value (thus, if a binary signal "1" is received as "0.4" the receiver will regenerate it as a "0" rather than as a "1"). This sort of bit error may occur with a probability typically within the range 10^{-3} to 10^{-9} for operational systems, and does not pose a problem for a well-designed communication link. A much more serious problem, however, is that arising from incorrect regeneration of the associated clock pulses, which is caused by noise and/or message dependency so perturbing the signal pulses that they occur at the wrong time.

As intimated above, the information-bearing pulses in a digital transmission system occur at certain specific and predetermined time intervals controlled by a master clock, and it is the presence or absence of a pulse at the clock time that constitutes the signal involved. In the receiving system a preliminary subsystem regenerates clock pulses (as can be appreciated, the master clock timing can easily be deduced from the regular spacing of the data pulses), and once the receiver's own internal clocking system is operative it "knows" when to sample the incoming signal so as to extract the signal level—representing the data—at the correct time. Unfortunately, it occasionally happens that a noise-induced distortion of the incoming signal—the apparent insertion or deletion of a pulse, for example—results in the receiver's clock sub-system failing to generate the correct number of clock pulses in any given period (it may generate too many or too few); this, in turn, means that the signal level extraction system fails to sample the incoming signal the correct number of times in the period in question (it may sample it too often or not often enough); and as a result the received signal suffers from a loss of bit count integrity.

In most digital data transmission systems—specifically those where part of the data being transceived is coded instructions to subsequent equipment concerning the handling of the rest of the data—it is essential that over a given period the number of data bits received is the same as the number transmitted. A loss of bit count integrity (also known as cycle skipping) may generally occur relatively infrequently, but when it does it may be extremely troublesome—causing, for example, lengthy frame synchronisation failure in associated multiplexer systems and forward-error-correction decoders.

The present invention seeks to provide circuitry capable of dealing with the problems caused by receiver clock sub-system failure leading to cycle skipping.

In one aspect, therefore, this invention provides a cycle-skip inhibitor electronic circuit for use in a digital transmisson receiver system in association with the receiver's clock recovery sub-system, which circuit constitutes both means for blocking spurious receiver clock pulses and means for supplying missing receiver clock pulses, and comprises:

a) means for blocking further clock pulses after a first clock pulse for a first predetermined time slightly less than the time between two adjacent normal clock pulses; and

b) means for supplying a clock-type pulse if a normal and unblocked clock pulse fails to be generated after a first clock pulse within a second predetermined time slightly more than the time between the adjacent normal clock pulses.

The circuit of the invention blocks further clock pulses for a first predetermined time after a first clock pulse, and also supplies a clock-type pulse if a normal clock pulse fails to be generated within a

second predetermined time after a first clock pulse. The two times are "slightly" less or more than the normal clock interval—and although it is not easy to say precisely what is meant by the word "slightly", nevertheless the following guidance can be given.

On the one hand it is, as might be appreciated, highly desirable that any utilised clock pulse (or clock-type pulse) occur at approximately the time the normal clock pulse should have occurred. In this way sampling of the incoming signal will be effected at what is, statistically, the best time to attain an accurate value, and there will be no odd gaps in the receiver output that might cause problems in associated equipment. Thus the difference between each predetermined time and the normal pulse time interval is desirably small. However, acceptable limits vary widely depending on the particular application or system concerned and so no definitive values can be given. Nevertheless, by way of general guidance it can be said that the difference between each predetermined time and the normal pluse interval desirably does not exceed 10% of the normal interval. On the other hand, however, it is equally undesirable to make the difference between each predetermined time and the normal time interval so small that it is comparable to the time period in which a data pulse is statistically expected to arrive (noise-induced distortion means data pulses do not always arrive exactly on time, and are statistically most likely to arrive within a certain time band the width of which depends rather upon the signal-to-noise ratio and message statistics). All in all, therefore, it is currently considered that the time difference should be within the range 2 to 10%, especially about 5%, of the normal pulse interval, so that in the preferred case the expressions "slightly less than" and "slightly more than" means "95% of" and "105% of" respectively.

The means for blocking further clock pulses is conveniently a first AND-gate having as its first input the normal clock pulses and as its second input the inverse output $\overline{Q}$ of a first monostable circuit triggered for the first predetermined time by the normal clock pulses *after* they have passed through the AND-gate, the output of the AND-gate being fed onwards to the rest of the circuitry. Both the AND-gate and the monostable circuit are quite conventional. Thus, the AND-gate allows through its first input if it is also receiving a second input, while the monostable, which has both a main output Q and an inverse output $\overline{Q}$, is triggered from a relaxed state where its main output is "0" and its inverse output is "1" (that is, it has no main output signal, but it does have an inverse output signal) to its triggered state where its main output is "1" and its inverse output is "0" (that is, it has a main output signal but no inverse output signal). It will therefore be seen that the blocking means operates as follows:

Once a normal clock pulse has been passed by the AND-gate the monostable circuit is triggered for the first predetermined time (slightly less than the normal clock pulse interval), and for that time the monostable's inverse output $\overline{Q}$—"0"—connected to the AND-gate second input closes the gate to any subsequent (spurious) clock pulse received at the gate's first input. At the end of the first predetermined time the monostable circuit spontaneously relaxes (as it is designed so to do), providing a "0" main output Q and a "1" inverse output $\overline{Q}$, so opening the AND-gate to the next clock pulse. If this next clock pulse is a spurious pulse (thus, occurring *before* the next normal clock pulse), then of course the blocking means acts in the described manner to block off that next normal clock pulse; because the time interval during which the AND-gate is open is short, the passed spurious clock pulse is a satisfactory substitute for the blocked normal clock pulse.

The means for supplying a clock-type pulse in place of a missing normal clock pulse is conveniently a clock-type pulse generator whose output is initiated immediately after the end of the second predetermined time and is the first input of a second AND-gate the second input of which is the inverse output $\overline{Q}$ of the first monostable circuit and the output of which is fed to the rest of the circuitry. Again, the second AND-gate and the pulse generator are quite conventional, and it will therefore be seen that the supplying means operates as follows:

Once a normal clock pulse has passed the first AND-gate the clock-type pulse generator produces a clock-type pulse output immediately after the second predetermined time. If the next clock pulse passes the first AND-gate within the appropriate time band then the first monostable is triggered and the resulting "0" inverse output $\overline{Q}$ closes the second AND-gate blocking the onwards transmission of the spare pulse supplied by the clock-type pulse generator. If, however, this next clock pulse fails to pass the first AND-gate within the allowed time band then the first monostable remains untriggered, and the resulting "1" inverse output $\overline{Q}$ opens the second AND-gate to the "spare" pulse produced by the clock-type pulse generator, which spare pulse is then passed to the rest of the receiver in place of the missing "normal" clock pulse.

The required delay in initiating the output of the clock-type pulse generator is advantageously achieved by a chain starting with the first monostable which triggers a second monostable with initiates "spare" pulse production. Most conveniently the relaxation of the first monostable is used to trigger the second monostable for a period equal to the difference between the first and second predetermined times, and the relaxation of the second monostable initiates "spare" pulse production.

The inventive circuit so far described can cope successfully with multiple spurious clock pulses, but cannot deal with successive multiple clock pulse losses. Though this latter eventuality is likely to be very rare, nevertheless a comparatively simple extension to the circuit can handle this problem. Preferably, therefore, the

means for supplying a clock-type pulse includes additional means whereby if a normal clock pulse has failed to be generated after a first clock pulse within the second predetermined time, then a clock-type pulse is also supplied if the following normal clock pulse also fails to be generated within a normal clock pulse interval after the end of the second predetermined time.

The additional means—the means for supplying a clock-type pulse in place of a second missing normal clock pulse—is conveniently the same clock-type pulse generator as previously described, connected in the same manner as previously described, but with an alternate output initiating means operative a full normal pulse interval after the end of the second predetermined time. Moreover, in the manner previously described the required delay in initiating the clock-type pulse generation is advantageously achieved by a similar chain in which an alternate first monostable parallels the principal first monostable, is triggered for a period equal to the first predetermined period (slightly less than the normal clock pulse interval) plus the normal clock-pulse interval, and in turn triggers an alternate second monostable paralleling the principal second monostable.

Naturally, a similar second additional supply means could be used to guard against loss of three consecutive normal clock pulses, and so on.

The inventive circuit appears to be useful in any digital data transmission system where, because of excessive noise, or for some other reason, there is a possibility of cycle skip causing loss of bit count integrity, and the invention naturally extends to such a system when employing a circuit as described and claimed herein.

Certain embodiments of the invention will now be described, though only by way of illustration, with reference to the accompanying drawings in which:

Figure 1 shows in schematic block diagram form part of a digital transception system incorporating a cycle-skip inhibitor circuit of the invention;

Figure 2 shows in schematic block diagram form the inventive cycle-skip inhibitor circuit as used in the transception system of Figure 1; and

Figure 3 shows the outputs of various components in the diagram of Figure 2.

Figure 1 generally speaks for itself—but, briefly it shows the final section of a digital data transmitter (the modulator, receiving data and clock pulses, and then suitably encoding the data for transmission) connected, via a transmission link (for example, a land line or radio channel) to a receiver of which only the demodulator (and its constituent clock-recovery sub-system) and the inventive cycle-skip inhibitor are shown.

The cycle-skip inhibitor is shown in Figure 2. The components forming the cycle-skip inhibitor—the AND-gates, the OR-gates, the monostable circuits, and the pulse generators—are conventional, and the manner in which they are connected is self evident. Their mode of operation is now explained, with reference to Figure 3, as follows:

1. General

Consistent with normal practice, the clock-recovery sub-system in the demodulator produces a clock output signal of half-width (return-to-zero) format as depicted in Figure 3a (the nominal clock period is T_N as shown), and the demodulator clock signal will trigger pulse generator 1 on each positive going edge to produce a stream of narrow pulses as shown in Figure 3b. Under normal conditions (i.e., in the absence of cycle-skipping) the narrow pulses will be routed via AND-gate 1 to trigger the monostable 1 on the negative-going edges (for the moment the existence of monostables 1b and 2b is ignored). The monostable's active period will be of duration T_L, and will give rise to a waveform at main output Q as shown in Figure 3c. The pulses at AND-gate 1 will be also routed via OR-gate 2 and monostable 3 to the circuit output port, where they are designated "processed clock."

2. Suppression of Spurious Pulses

a) During each period T_L, the inverse output $\overline{Q}$ of monostable 1 will be in the LOW condition, such that passage of pulses from pulse generator 1 via AND-gate 1 will be inhibited. Thus, should a spurious clock edge be produced by the demodulator (e.g., due to cycle-skipping), as depicted diagrammatically in Figure 3a (spurious pulse P1), this pulse in turn triggering a secondary spurious pulse (P2, Figure 3b) in pulse generator 1, this latter pulse will be prevented from reaching the output port. Accordingly, even though the demodulator has introduced an extra, unwanted clock transition, the bit count integrity at the output of the inhibitor will be preserved.

b) In the event that a spurious clock pulse is produced during a period in which a monostable 1 has relaxed (e.g., pulse P3, triggering pulse P4) this will propagate via AND-gate 1, OR-gate 2 and monostable 3 to the output port. However, it will result in early triggering of monostable 1 (waveform M, Figure 3c), and will thus prevent the normal clock edge, E3 (which produces P5), from producing an output. Thus, although a time displacement of the processed clock output signal away from the nominal position will arise, the bit count integrity will again be preserved.

3. Supply of "Missing" Pulses

The remaining circuitry in the inhibitor is provided to cover those situations in which a loss of bit count integrity at the demodulator output entails a *suppression* of the normal clock transition.

a) The negative-going edge of monostable 1 main output Q is arranged to trigger monostable 2 which produces a pulse of width $2\Delta T$; see Figures 3c/3e (note that ΔT is the interval prior to the expected arrival time of a clock transition from the demodulator for which AND-gate 1 is

'transparent' to spurious pulses; in practice ΔT is chosen to be of the order of 5% of the nominal clock period, T_N). In turn, the negative-going edge of monostable 2 triggers pulse generator 2 (via OR-gate 1) which produces a narrow pulse stream (similar to pulse generator 1) as shown in Figure 3j.

Under normal circumstances, the auxiliary pulse stream produced by pulse generator 2 is prevented from reaching the output port (via OR-gate 2) by the action of AND-gate 2; the latter is inhibited by the LOW state of monostable 1 inverse output $\overline{Q}$ for a period T_L each cycle. Suppose, now, that, due to cycle-skipping, edge E1 (Figure 3a) fails to emerge from the demodulator. Then pulse P6 (Figure 3b) will not be produced at the pulse generator 1 output, and accordingly pulse P7 will not be triggered in monostable 1. Under these conditions, pulse P8 (Figure 3j), which is produced by pulse generator 2, will be free to propagate via AND-gate 2 and OR-gate 2 to the monostable 3 input where it will act as a substitute for the suppressed clock transition (E1/P6).

Whilst P7 (for example) is suppressed, the circuit will be susceptible to unwanted additional pulses which might arrive from the demodulator. However, this constitutes a *double* cycle-skip event—which is believed to be a phenomenon arising with negligible probability. Nevertheless, it may be noted that should such an additional pulse arise it will result in early triggering of monostable 1, and will hence suppress the next clock pulse. Thus, the bit count integrity will be preserved.

The circuit will quickly revert to normal operation, monostable 1 not being subsequently retriggered until the next pulse arrives from pulse generator 1.

b) Although, as observed above, multiple consecutive cycle-skip events are believed to be extremely rare, it is to be noted that the basic circuit as described above provides automatic protection for multiple spurious pulse *insertions* (e.g., for, say, two pulses similar to P1 arising in the clock half-cycle), but that for pulse *deletions* the basic circuit as so far described cannot cope with two or more *consecutive* losses of clock transitions. However, the configuration may easily be generalised to cater for this eventuality as now explained.

Consider now that additional monostables (1b, retriggable, and 2b) are introduced as depicted in dotted outline in Figure 2. Monostable 1b will be triggered in a similar fashion to monostable 1, but will produce a pulse of longer duration (T_M), as shown in Figure 3f. Pulses from monostable 1b (assuming the latter is not continuously retriggered) will trigger monostable 2b on the trailing edge, and the output from monostable 2b will propagate via OR-gate 1, and will in turn trigger pulse generator 2.

It will be evident, on consideration of the mode of operation of the circuit, that should *two* successive clock transitions be suppressed at the demodulator output (e.g. edges E1 and E2) then two successive pulses from pulse generator 1 will be suppressed (e.g., P6 and P9), as will two consecutive outputs from monostable 1 (e.g., P7 and P10). However, monostable 2 (initiated by the last trailing edge of the monostable 1 pulse) will trigger pulse generator 2, and so restore the first suppressed edge (e.g., by substituting P8).

Similarly, monostable 1b will trigger monostable 2b (and hence pulse generator 2) and will restore the second suppressed edge (e.g. by substituting P11). Thus, the bit count integrity will be preserved.

Claims

1. A cycle-skip inhibitor electronic circuit for use in a digital transmission receiver system in association with the receiver's clock recovery sub-system, which circuit constitutes both means for blocking spurious receiver clock pulses and means for supplying missing receiver clock pulses, and comprises:

a) means for blocking further clock pulses after a first clock pulse for a first predetermined time slightly less than the time between two adjacent normal clock pulses; and

b) means for supplying a clock-type pulse if a normal and unblocked clock pulse fails to be generated after a first clock pulse within a second predetermined time slightly more than the time between the adjacent normal clock pulses.

2. A circuit as claimed in claim 1, wherein it is arranged that the two predetermined times "slightly" less or more than the normal clock interval differ from that interval by within 2 to 10% thereof.

3. A circuit as claimed in claim 2, wherein it is arranged that the time difference is about 5% of the normal pulse interval.

4. A circuit as claimed in any of the preceding claims, wherein the means for blocking further clock pulses is a first AND-gate having as its first input the normal clock pulses and as its second input the inverse output $\overline{Q}$ of a first monostable circuit triggered for the first predetermined time by the normal clock pulses after they have passed through the AND-gate, the output of the AND-gate being fed onwards to the rest of the circuitry.

5. A circuit as claimed in any of the preceding claims, wherein the means for supplying a clock-type pulse in place of a missing normal clock pulse is a clock-type pulse generator whose output is initiated immediately after the end of the second predetermined time and is the first input of a second AND-gate the second input of which is the inverse output $\overline{Q}$ of the first monostable circuit and the output of which is fed to the rest of the circuitry.

6. A circuit as claimed in claim 5, wherein the required delay in initiating the output of the clock-type pulse generator is achieved by a chain starting with the first monostable which triggers a second monostable which initiates "spare" pulse production.

7. A circuit as claimed in claim 6, wherein the relaxation of the first monostable is used to

trigger the second monostable for a period equal to the difference between the first and second predetermined times, and the relaxation of the second monostable initiates "spare" pulse production.

8. A circuit as claimed in any of the preceding claims, wherein, in order to deal with successive multiple clock pulse losses, the means for supplying a clock-type pulse includes additional means whereby if a normal clock pulse has failed to be generated after a first clock pulse within the second predetermined time, then a clock-type pulse is also supplied if the following normal clock pulse also fails to be generated within a normal clock pulse interval after the end of the second predetermined time.

9. A circuit as claimed in claim 8, wherein the additional means is the same clock-type pulse generator as previously described hereinbefore, connected in the same manner as previously described hereinbefore, but with an alternate output initiating means operative a full normal pulse interval after the end of the second predetermined time.

10. A circuit as claimed in claim 9, wherein the required delay in initiating the clock-type pulse generation is advantageously achieved by a similar chain in which an alternate first monostable parallels the principal first monostable, is triggered for a period equal to the first predetermined period (slightly less than the normal clock pulse interval) plus the normal clock-pulse interval, and in turn triggers an alternate second monostable paralleling the principal second monostable.

11. A cycle-skip inhibitor electronic circuit as claimed in any of the preceding claims and substantially as described hereinbefore.

12. A digital data transmission system incorporating a cycle-skip inhibitor electronic circuit as claimed in any of the preceding claims.

New Claims or Amendments to Claims filed on 13 Oct 1980

New or Amended Claims:—

1. A cycle-skip inhibitor electronic circuit for use in a digital transmission receiver system in association with the receiver's clock recovery sub-system, which circuit constitutes both means for blocking spurious receiver clock pulses and means for supplying missing receiver clock pulses, and comprises:—

a) means for blocking further clock pulses after a first clock pulse for a first predetermined time slightly less than the time between two adjacent normal clock pulses, this pulse-blocking means being a first AND-gate having as its first input the normal clock pulses and as its second input the inverse output $\overline{Q}$ of a first monostable circuit triggered for the first predetermined time by the normal clock pulses after they have passed through the AND-gate, the output of the AND-gate being fed onwards to the rest of the circuitry; and

b) means for supplying a clock-type pulse if a normal and unblocked clock pulse fails to be generated after a first clock pulse within a second predetermined time slightly more than the time between the adjacent normal clock pulses, this pulse-supplying means being a clock-type pulse generator whose output is initiated immediately after the end of the second predetermined time and is the first input of a second AND-gate the second input of which is the inverse output $\overline{Q}$ of the first monostable circuit and the output of which is fed to the rest of the circuitry.

2. A circuit as claimed in claim 1, wherein it is arranged that the two predetermined times "slightly" less or more than the normal clock interval differ from that interval by within 2 to 10% thereof.

3. A circuit as claimed in claim 2, wherein it is arranged that the time difference is about 5% of the normal pulse interval.

4. A circuit as claimed in any of the preceding claims, wherein the required delay in initiating the output of the clock-type pulse generator is achieved by a chain starting with the first monostable which triggers a second monostable which initiates "spare" pulse production.

5. A circuit as claimed in claim 4, wherein the relaxation of the first monostable is used to trigger the second monostable for a period equal to the difference between the first and second predetermined times, and the relaxation of the second monostable initiates "spare" pulse production.

6. A circuit as claimed in any of the preceding claims, wherein, in order to deal with successive multiple clock pulse losses, the means for supplying a clock-type pulse includes additional means whereby if a normal clock pulse has failed to be generated after a first clock pulse within the second predetermined time, then a clock-type pulse is also supplied if the following normal clock pulse also fails to be generated within a normal clock pulse interval after the end of the second predetermined time.

7. A circuit as claimed in claim 6, wherein the additional means is the same clock-type pulse generator as previously specified hereinbefore, connected in the same manner as previously specified hereinbefore, but with an alternative output initiating means operative a full normal pulse interval after the end of the second predetermined time.

8. A circuit as claimed in claim 7, wherein the required delay in initiating the clock-type pulse generation is achieved by a similar chain in which an alternate first monostable parallels the principal first monostable, is triggered for a period equal to the first predetermined period (slightly less than the normal clock pulse interval) plus the normal clock-pulse interval, and in turn triggers an alternate second monostable paralleling the principal second monostable.

9. A cycle-skip inhibitor electronic circuit as claimed in any of the preceding claims and substantially as described hereinbefore.

10. A digital data transmission system incorporating a cycle-skip inhibitor electronic circuit as claimed in any of the preceding claims.

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