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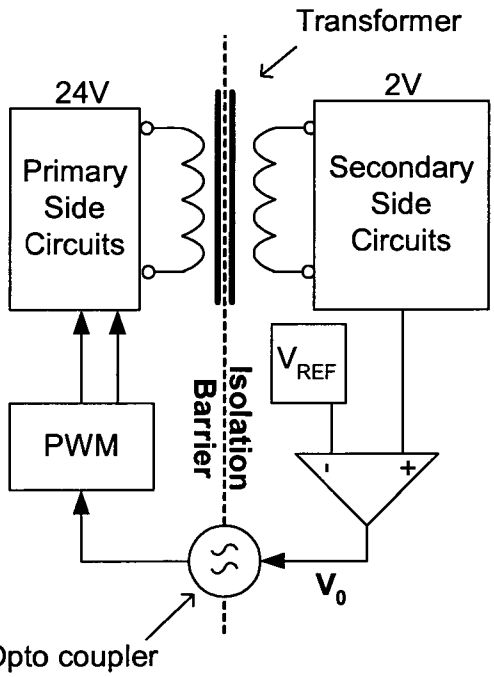
(54) Title: A DIGITALLY CONTROLLED ISOLATED POWER CONVERTER



Traditional Analog Control Isolated SMPC.

Fig. 1 (PRIOR ART)

(57) Abstract: A digital SMPC (1) comprises an SMPS primary side (2) and an SMPS secondary side (3). Opto-couplers (4) perform bi-directional communication between primary side and secondary side communication circuits (5, 6). The primary side communication circuits (5) are connected via a loop controller (7) to the primary side (2). The secondary side communication circuits 6 are connected to the secondary side 3 via an ADC (8). The analogue-to-digital converter (ADC, 8) digitises the output voltage V0 on the secondary side. The secondary side communication module (6) encodes this value and uses the data couplers (4) to transmit it over the isolation barrier. The primary side communication module (5) receives and decodes the value and provides it to the loop controller module (7). The loop controller (7) is implemented as a Digital Signal Processor (DSP) or a hardware PID-controller. A Digital Pulse Width Modulator (DPWM) generates the switching signals for the primary side power stage (2), which stabilizes the secondary side output voltage V_o.

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"A Digitally Controlled Isolated Power Converter"

INTRODUCTION

Field of the Invention

The invention relates to control of power converters.

Prior Art Discussion

In an isolated switched mode power converter there is no electrical connection between the primary and secondary side. The traditional analog control of SMPCs is shown in Fig. 1. The primary side high voltage DC or AC is converted to a low voltage DC signal across a transformer. The DC signal is compared with a reference level and an error signal V_o generated. This error signal is transmitted to the primary side through an optocoupler. The pulse width modulator (PWM) acts on this error signal generating signals that control switches on the primary side thereby regulating the secondary side voltage.

The traditional analog scheme supports the design of precise and inexpensive isolated SMPCs, and is therefore highly popular. However, despite its popularity it is recognised that it suffers from a number of serious drawbacks including the following:

- The LED of the optocoupler suffers from a significant reduction of light emission over the life of the optocoupler, this being particularly accelerated at high operating temperatures.
- Incompatibility with emerging digital SMPC control.
- High component count leading to reliability penalties, increased manufacturing cost, and material management challenges.
- Fixed output voltage (i.e. non-programmable), set through resistor network and voltage reference.
- Fixed frequency compensation, and closed-loop performance (set through passive networks), unsuitable for advanced, adaptive digital control.

- Undesirable zero in compensator gain through parasitic modulation of optocoupler LED current.
- Messy converter startup due to U2 behaviour (integrator wind-up) leading to non-monotonic Vo rise.
- Inability to detect open-loop condition (missing or mal-functioning component in feedback path).

Prodić A., Erickson R.W. and Maksimović D., "Digital Controller Chip Set For Isolated DC-DC Power Supplies", IEEE APEC 2003, February 2003, pp. 866-872, describes an arrangement in which a clock signal is fed forward to the secondary side on an extra line.

WO2003/049267 describes capacitive coupling for communication between primary and secondary sides of a power converter.

The invention is directed towards providing improved digital power converter control.

SUMMARY OF THE INVENTION

According to the invention, there is provided a digital power converter having primary and secondary power stages, primary side circuits including a loop controller, secondary side circuits including an ADC, a communications interface between the primary and secondary sides, wherein each of the primary and secondary side circuits include a transmitter and a receiver for bi-directional communication of data across the interface.

In one embodiment, the secondary side circuits comprise means for using encoded data from the primary side to adjust a reference voltage.

In one embodiment, the circuits of both sides comprise means for sending auxiliary data to the other side, including over-voltage protection safety signals.

In one embodiment, the auxiliary signals include over-temperature protection signals.

In one embodiment, the auxiliary signals include power failure signals.

In one embodiment, the auxiliary signals include user data.

In one embodiment, the transmitters and receivers register incoming and outgoing signals, and synchronise incoming asynchronous signals.

In one embodiment, the transmitters and receivers ensure correct i/o timing such as reading an ADC result back.

In one embodiment, at least one transmitter comprises a shift register for data transfer across the interface.

In one embodiment, the transmitter and receiver are combined as a transceiver on at least one side.

In one embodiment, the primary side loop controller is adapted to adjust the sample time instant of the secondary side ADC.

In one embodiment, the secondary side circuits are adapted to receive an encoded data packet and use it as an ADC sample trigger.

In one embodiment, the interface comprises two couplers for bi-directional communication

In one embodiment, the interface comprises at least one opto-coupler.

In one embodiment, the primary side circuits are adapted to generate data packages and to send them across the interface to the secondary side circuits.

In one embodiment, said packages generated by the primary side circuits include a digital representation of a nominal output voltage.

In one embodiment, said packages generated by the primary side circuits include a package number for synchronisation of packages on both sides.

In one embodiment, said primary side circuits are adapted to transmit to the secondary side circuits packages containing a package number and successive packages for a frame have a number which is incremented, and the secondary side circuits are adapted to synchronise to the package numbers to ensure the correct order and alignment of information bits, and the secondary side circuits are adapted to transmit to the primary side circuits packages which are direct responses to received packages.

In one embodiment, said packages generated by the secondary side circuits include an ADC value indicating output voltage and auxiliary data signals.

In one embodiment, the secondary side circuits comprise a clock synchronizer for extracting the primary side clock from a data stream and outputting both a recovered clock and synchronized data and for using a falling edge of the recovered clock is to send secondary side data back to the primary side and the primary side circuits are adapted to read an incoming data stream without the need of further synchronization because the clock is held synchronous to the primary side clock.

In one embodiment, the secondary side circuits are adapted to transmit data packages to the primary side circuits in synchronism with said clock.

In one embodiment, said clock synchronizer comprises a master clock which operates at a multiple N of a nominal primary side clock, and a state machine which has a number 2N+2 of intermediate states and 2 start-up states; wherein each state is represented by a received serial data bit and a bit which is the secondary side master clock; and the state machine moves between states directed by a change in either of said bits and while the state machine remains in states 0-N the recovered clock is nominally zero, and while the machine is in states N-2N-1 the state is 1.

In one embodiment, the loop controller comprises a digital pulse width modulator adapted to provide a signal that controls the primary side switches, in which rising and falling edges of this signal cause the switches to turn ON/OFF, causing a transient disturbance on the secondary side output; and the loop controller is adapted to transmit a signal to the ADC to cause the sampling instant to occur midway between the rise and fall of the DPWM signal, to allow optimal positioning of the ADC sampling instant.

In one embodiment, the loop controller is adapted to compensate for latency in communication between the primary side circuits and the secondary side circuits by advancing timing of a data packet transmission.

DETAILED DESCRIPTION OF THE INVENTION

Brief Description of the Drawings

The invention will be more clearly understood from the following description of some embodiments thereof, given by way of example only with reference to the accompanying drawings in which:-

Fig. 1 is a diagram illustrating a prior art analogue control isolated SMPC;

Fig. 2 is a block diagram of a digital SMPC of the invention, incorporating an opto-coupler for bi-directional communication between primary and secondary sides;

Fig. 3 is a block diagram showing bi-directional communication blocks of the SMPC;

Fig. 4 shows a primary side transceiver in more detail, and Fig. 5 shows a secondary side transceiver in more detail;

Fig. 6 shows control of ADC sampling; and

Fig. 7 is a diagram illustrating a mechanism for clock synchronisation across the opto-coupler.

Description of the Embodiments

Referring to Fig. 2 a digital SMPC 1 comprises an SMPS primary side 2 and an SMPS secondary side 3. Opto-couplers 4 perform bi-directional communication between primary side and secondary side communication circuits 5 and 6. The primary side communication circuits 5 are connected via a loop controller 7 to the primary side 2. The secondary side communication circuits 6 are connected to the secondary side 3 via an ADC 8.

The analogue-to-digital converter (ADC) 8 digitises the output voltage V_o on the secondary side. The secondary side communication module 6 encodes this value and uses the data couplers 4 to transmit it over the isolation barrier. The primary side communication module 5 receives and decodes the value and provides it to the loop controller module 7. The loop controller 7 is implemented as a Digital Signal Processor (DSP) or a hardware PID-controller. A Digital Pulse Width Modulator (DPWM) generates the switching signals for the primary side power stage 2, which stabilizes the secondary side output voltage V_o.

The primary side controller 7 can determine the instant when the ADC samples V_o. This allows sampling of a settled output. The start of the received data package on the secondary side triggers the ADC sampling process.

The secondary side uses the encoded data to adjust a programmable reference voltage to produce the selected V_o.

Both sides can send auxiliary data to the opposite side. This data is appended to the main data. This auxiliary data may include safety signals like over-voltage-protection (OVP), over-temperature-protection (OTP) and power failure (PF) but also arbitrary end-user data.

The following summarises some features and benefits:

- Effect of optocoupler aging on analog transmission of data is avoided.
- Support of bi-directional transmission of digital data across the isolation barrier through external optical or capacitive isolation barrier components.
- Minimum number of isolation barrier components: Only two optocouplers are required to handle multiple signals. No extra channels are required for clock information. In order to accommodate the transmission of additional information from the secondary side to the primary side, such as over voltage protection (OVP) and over temperature protection (OTP), the traditional analog approach requires an additional optocoupler for each signal transmitted.
- A broken primary-secondary link will be detected.
- Minimised bit-rate through optimized data packets/frames. Low bit-rate will reduce the cost of barrier components. Barrier components will transmit digital information only. Barrier component deterioration will not affect SMPC dynamic performance.
- Primary digital SMPC controller fully controls sampling time instant of the analog to digital converter.
- Primary side digital SMPC controller can transmit up to 16 arbitrary digital signals to the secondary side.

The communication modules 5 and 6 allow the bi-directional data link between the primary and secondary side of the SMPS, and they consist of:

- Interfaces to external modules, i.e. DSP, Vref, ADC and auxiliary signals.
- Serial Data receiver and transmitter circuits.
- Clock recovery circuit on secondary side.

These are shown in more detail in Fig. 3, and the interface modules shown in Fig. 3 have the following functions:

- Register incoming and outgoing signals.
- Synchronisation of incoming asynchronous signals (AUX Interface only).
- Ensure proper I/O timing, e.g. reading the ADC result back when it is valid.
- Serial-to-Parallel and Parallel-to-Serial conversion.

The transceiver modules contain the data transmitter and receiver. These are implemented by serial shift registers and en-/decoders and contain additional sub-modules for timing and error handling. Both Primary-to-Secondary and Secondary-to-Primary transceivers are shown in Fig. 4 and Fig. 5. They are implemented using similar circuitry but differ significantly in number and direction of interface signals.

The primary side transceiver is clocked by the primary side clock. The secondary side has to recover this clock from the incoming data and provide this clock to the secondary side transceiver. This is shown in Fig. 5. The outgoing secondary-to-primary packages are sent synchronously to the primary side clock. This allows the primary side receiver to sample secondary data without need for synchronisation.

Description of blocks

Output Shift Register	Serial shift register. Performs Parallel to Serial Conversion. Shifting and loading is controlled by the timing controller.
Input Shift Register	Serial shift register. Performs Serial to Parallel Conversions. Shifting is controlled by the timing controller.
Encoder	Encodes data signals into the form needed for transmission. Forward error correction bits are added for data integrity.
Decoder	Decodes data back to original form and corrects/detects errors using the forward error correction bits.
Packet Detector	Detect the start of a new incoming data packet.
Timing Controller	Central logic which controls the timing of all other modules. This can be implemented as a state machine or as combinational logic.
Packet Counter	Stores current packet number.
Error Register	Stores reported data errors and indicates which data (Vout, Vref, Aux) is in error.
Clock recovery	Recovers the clock signal from the incoming data. This can be implemented either as state machine or as digital phase-locked loop.

Data Packages

The data packages sent contain the following information in encoded form together with forward error correction and protocol bits.

Primary-to-secondary side package

- Sampling time instant i.e. controls when ADC samples the output voltage V_{out} (see information below).
- Digital representation of the reference voltage value V_{ref}, which determines the nominal output voltage.
- Package number, to synchronise package frames on both sides.
- Auxiliary data signals (e.g. "power loss detected").

Secondary-to-Primary side package

- ADC value, i.e. output voltage $V_{out.}$
- Auxiliary data signals (e.g. "over voltage detected", "over temperature detected").

Encoding of Sampling Instant.

Control of the sampling instant of the ADC is very important for digitally controlled SMPCs. The primary side loop controller contains a DPWM which produces a signal that controls the primary side switches (Fig. 6). The rising and falling edges of this signal cause the switches to turn ON/OFF. This produces a transient disturbance on the secondary side output V_0. The ADC sampling instant should be controlled to avoid sampling during a transient disturbance. The optimal sampling instant occurs midway between the rise and fall of the DPWM signal. This information is known a priori by the primary side loop controller. An advantageous aspect is transmission of this information from the primary side to the secondary side to allow optimal positioning of the ADC sampling instant.

The ADC sample timing information cannot be encoded within the data packets as digital data. The transmission latency to receive and decode a digital value representing the ADC sample time information is too long for cycle-by-cycle control of the ADC sampling time on the secondary side. The ADC sampling time instant is

determined by receipt of the primary-to-secondary data package on the secondary side. The sequence of operations is:

- The primary side transmitter sends a new primary-to-secondary package when instructed to by the primary side loop controller.
- The receipt of a new package on the secondary side is determined by the packet detector (Fig. 4).
- The packet detector recognises a new packet by the presence of a packet start code.
- The packet detector immediately outputs a signal to trigger the ADC sampling.

This scheme allows the ADC sample instant to be adjusted individually for each switching phase of the power converter. The loop controller preferentially sets the sample time instant to be during the positive duty cycle of the primary side switches. Also, because the packets contain redundant information, their length can be adjusted without destroying critical primary-to-secondary data.

The latency between transmitter and receiver is mostly due to the coupler latency with some smaller delays for the triggering and detection. The loop controller can compensate this latency by advancing timing of the data packet.

Package frames and package numbers

While the main information, V_{out}, is sent in full with each package. The additional, less time critical information, i.e. V_{ref} and the auxiliary signals, is only sent bit-wise with each package. This reduces the package length and allows for higher speeds.

All packages containing bits for the same data value compose a package frame. Each primary-to-secondary package contains a package number that is zero at begin of every frame and gets continuously incremented with every package. The secondary side can synchronise itself to this package number to ensure the correct order and alignment of all information bits. Because the secondary-to-primary side packages are direct responses to the primary-to-secondary they don't need to include an own package number.

Prototype board

A prototype board has been developed which includes the full SMPS, the ADC with programmable reference voltage and the data coupler. The digital communication modules are implemented on Field Programmable Gate Array (FPGA) development boards, which are connected to the prototype board.

Clock Synchronization

A master clock operates at a multiple N of the nominal primary side clock. A state machine has a number of states 2N+2 intermediate states and 2 start-up states. Each state is represented by 2 bits, containing a bit (a) which is the received serial data bit and a bit (b) which is the secondary side Master clock. The machine moves between states directed by a change in either (a) or (b). While the state machine remains in states 0-N the recovered clock is nominally zero. While the machine is in states N-2N-1 the state is 1.

In more detail, and referring to Fig. 7 the primary and secondary communication sides do not share a common clock. In order to synchronize the incoming primary data the secondary side contains a clock synchronizer which extracts the primary side clock from the data stream and outputs both the recovered clock and the synchronized data. The falling edge of the recovered clock is then used to send the secondary data back to the primary side. Because this clock is held synchronous to the primary side clock the primary side can simply read the incoming data stream without the need of further synchronization.

The secondary side clock synchronizer is implemented as follows:

- A master clock which operates at four times the nominal primary side clock is used to clock the clock synchronizer.
- A state machine is used which has five states (0-3, B) for the low (0) and five states (4-6, F) for the high level (1) of the input data.
- The input to the state machine is the input data stream, which is read at the rising and falling edge of the master clock.
- For every input bit with the nominal bit period time the state machine is

through four of the associated states either 0-3 (if input bit is zero) or 4-6 (if input bit is one).

- Maintaining Synchronisation between primary and secondary is achieved by:
  - A slower-then-nominal primary side clock is compensated by using a fifth state (F or B) i.e. extending the bit length by 25% for the current input bit.
  - A faster-then-nominal primary side clock is compensated by skipping the fourth state (0 or 4), i.e. shortening the bit length by 25% for the current input bit.
- The outputs of the state machine are the recovered clock and data signals which are defined only by the state encoding of the current state, as shown in the figure below.
- Two initialization states (C and D) are used after reset to ensure proper start.

The invention is not limited to the embodiments described but may be varied in construction and detail.

Claims

1. A digital power converter having primary and secondary power stages, primary side circuits including a loop controller, secondary side circuits including an ADC, a communications interface between the primary and secondary sides, wherein each of the primary and secondary side circuits include a transmitter and a receiver for bi-directional communication of data across the interface.

2. A digital power converter as claimed in claim 1, wherein the secondary side circuits comprises means for using encoded data from the primary side to adjust a reference voltage.

3. A digital power converter as claimed in claims 1 or 2, wherein the circuits of both sides comprise means for sending auxiliary data to the other side, including over-voltage protection safety signals.

4. A digital power converter as claimed in claim 3, wherein the auxiliary signals include over-temperature protection signals.

5. A digital power converter as claimed in claims 3 or 4, wherein the auxiliary signals include power failure signals.

6. A digital power converter as claimed in any of claims 3 to 5, wherein the auxiliary signals include user data.

7. A digital power converter as claimed in any preceding claim, wherein the transmitters and receivers register incoming and outgoing signals, and synchronise incoming asynchronous signals.

8. A digital power converter as claimed in any preceding claim, wherein the transmitters and receivers ensure correct i/o timing such as reading an ADC result back.

9. A digital power converter as claimed in any preceding claim, wherein at least one transmitter comprises a shift register for data transfer across the interface.

10. A digital power converter as claimed in any preceding claim, wherein the transmitter and receiver are combined as a transceiver on at least one side.

11. A digital power converter as claimed in any preceding claim, wherein the primary side loop controller is adapted to adjust the sample time instant of the secondary side ADC.

12. A digital power converter as claimed in any preceding claim, wherein the secondary side circuits are adapted to receive an encoded data packet and use it as an ADC sample trigger.

13. A digital power converter as claimed in any preceding claim, wherein the interface comprises two couplers for bi-directional communication

14. A digital power converter as claimed in any preceding claim, wherein the interface comprises at least one opto-coupler.

15. A digital power converter as claimed in any preceding claim, wherein the primary side circuits are adapted to generate data packages and to send them across the interface to the secondary side circuits.

16. A digital power converter as claimed in claim 15, wherein said packages generated by the primary side circuits include a digital representation of a nominal output voltage.

17. A digital power converter as claimed in either of claims 15 or 16, wherein said packages generated by the primary side circuits include a package number for synchronisation of packages on both sides.

18. A digital power converter as claimed in any of claims 15 to 17, wherein said primary side circuits are adapted to transmit to the secondary side circuits packages containing a package number and successive packages for a frame have a number which is incremented, and the secondary side circuits are adapted to synchronise to the package numbers to ensure the correct order and alignment of information bits, and the secondary side circuits are adapted to transmit to the primary side circuits packages which are direct responses to received packages.

19. A digital power converter as claimed in any of claims 15 to 18, wherein said packages generated by the secondary side circuits include an ADC value indicating output voltage and auxiliary data signals.

20. A digital power converter as claimed in either of claims 18 or 19, wherein the secondary side circuits comprise a clock synchronizer for extracting the primary side clock from a data stream and outputting both a recovered clock and synchronized data and for using a falling edge of the recovered clock is to send secondary side data back to the primary side and the primary side circuits are adapted to read an incoming data stream without the need of further synchronization because the clock is held synchronous to the primary side clock.

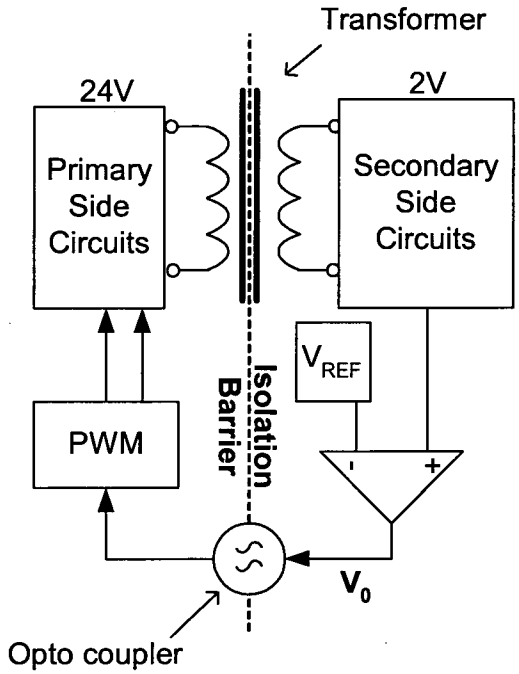
21. A digital power converter as claimed in claim 20, wherein the secondary side circuits are adapted to transmit data packages to the primary side circuits in synchronism with said clock.

22. A digital power converter as claimed in either of claims 20 or 21, wherein said clock synchronizer comprises a master clock which operates at a multiple N of a nominal primary side clock, and a state machine which has a number 2N+2 of intermediate states and 2 start-up states; wherein each state is represented by a received serial data bit and a bit which is the secondary side master clock; and the state machine moves between states directed by a change in either of

said bits and while the state machine remains in states 0-N the recovered clock is nominally zero, and while the machine is in states N-2N-1 the state is 1.

23. A digital power converter as claimed in any preceding claim, wherein the loop controller comprises a digital pulse width modulator adapted to provide a signal that controls the primary side switches, in which rising and falling edges of this signal cause the switches to turn ON/OFF, causing a transient disturbance on the secondary side output; and the loop controller is adapted to transmit a signal to the ADC to cause the sampling instant to occur midway between the rise and fall of the DPWM signal, to allow optimal positioning of the ADC sampling instant.

24. A digital power converter as claimed in any preceding claim, wherein the loop controller is adapted to compensate for latency in communication between the primary side circuits and the secondary side circuits by advancing timing of a data packet transmission.



Traditional Analog Control Isolated SMPC.

Fig. 1 (PRIOR ART)

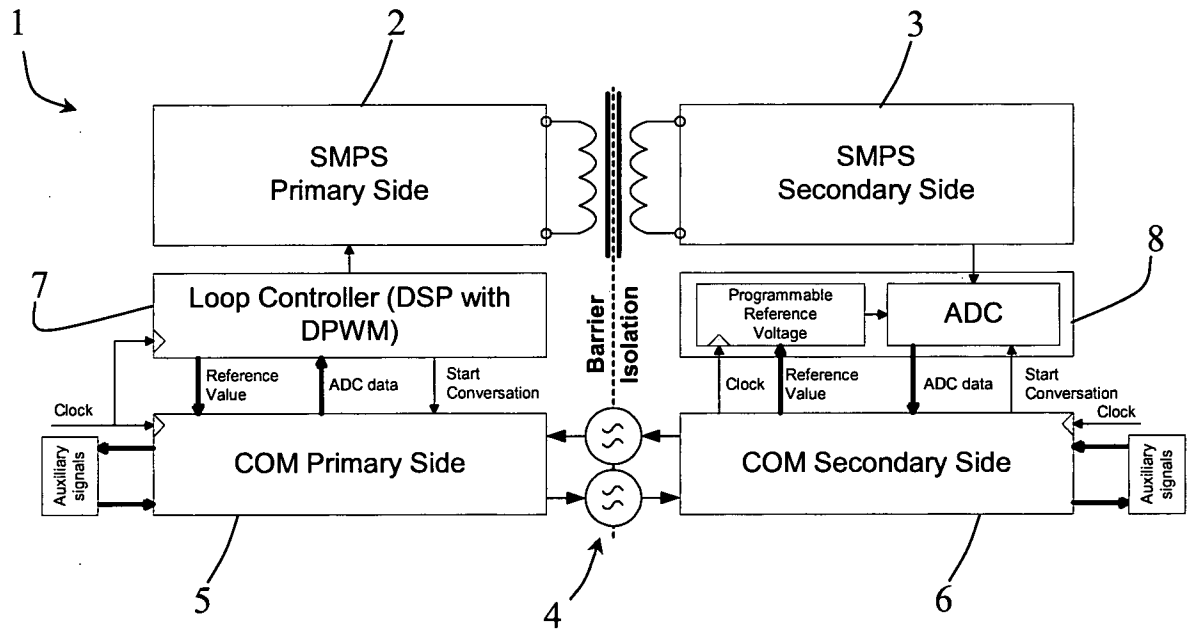
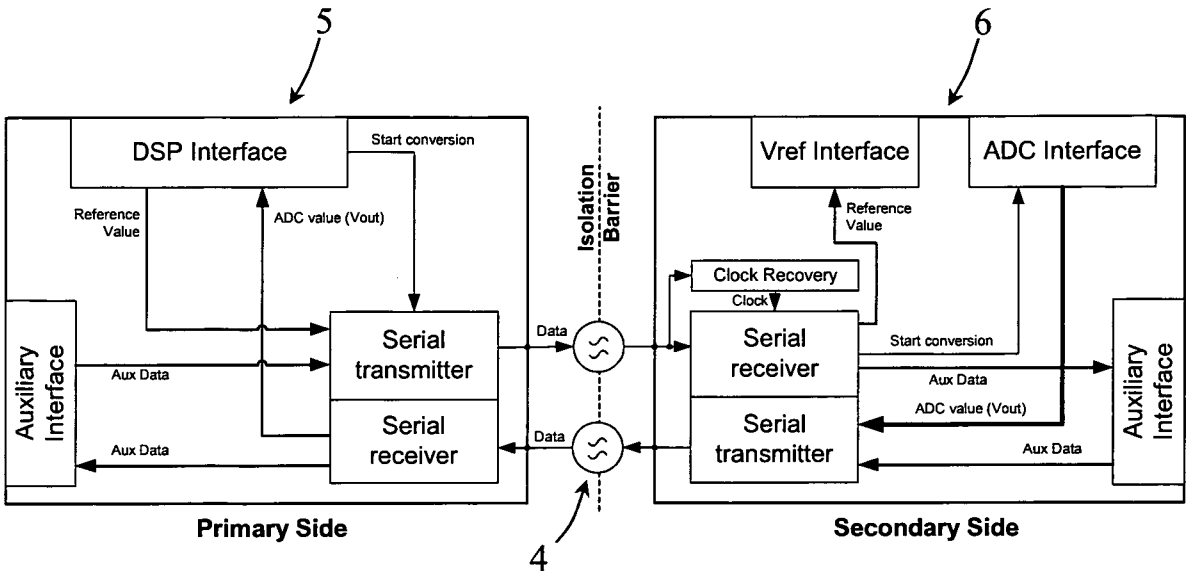
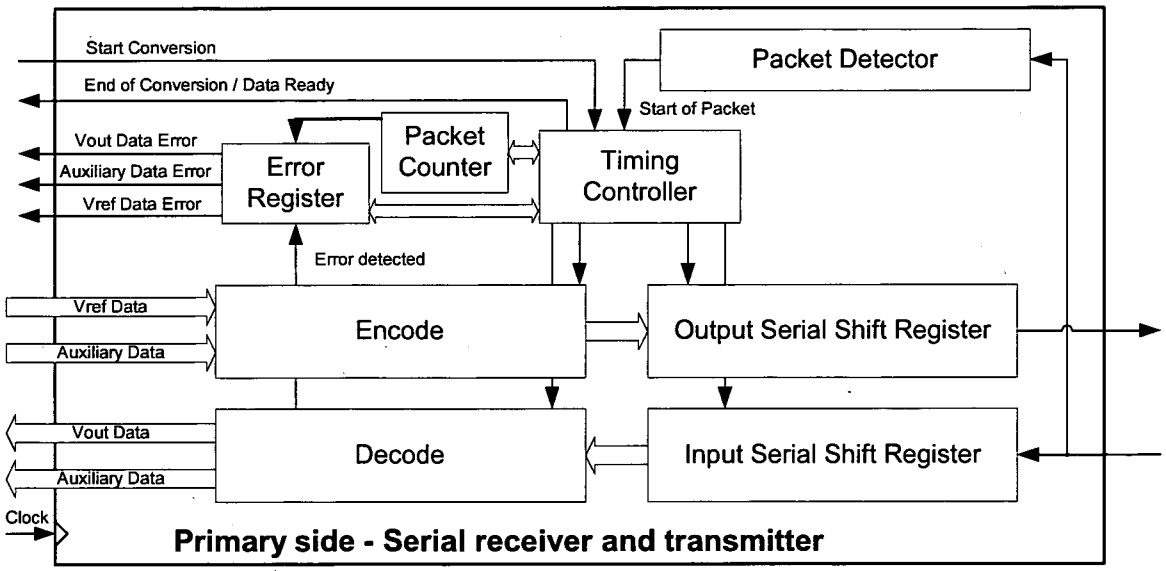


Fig. 2



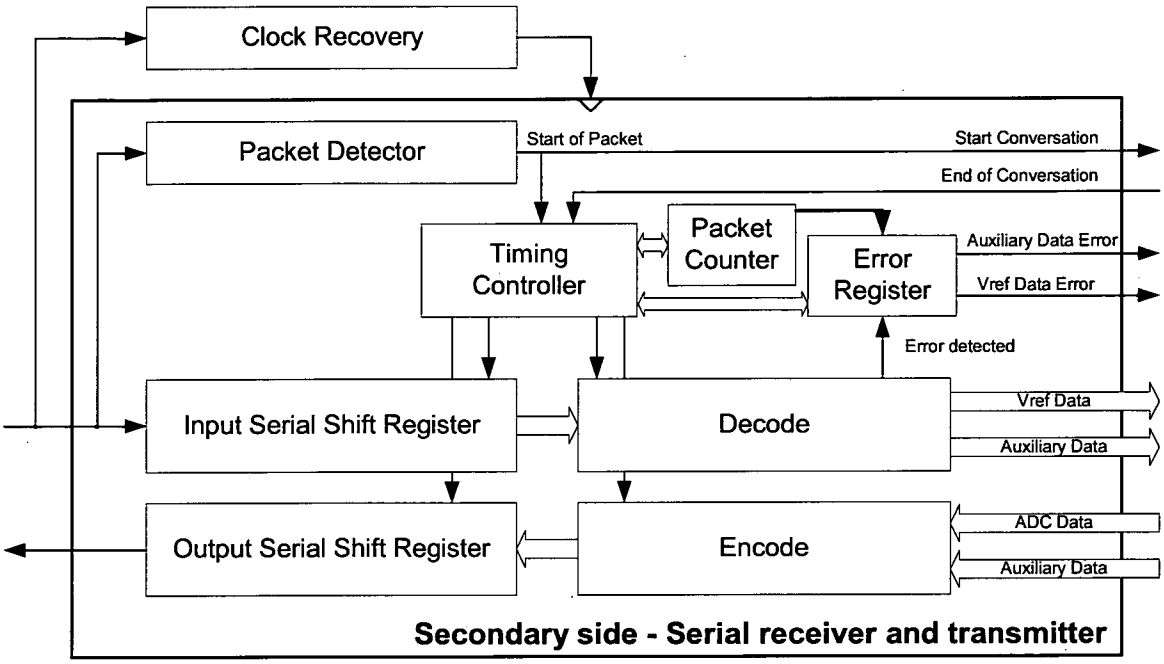
Bi-directional Communication Blocks.

Fig. 3



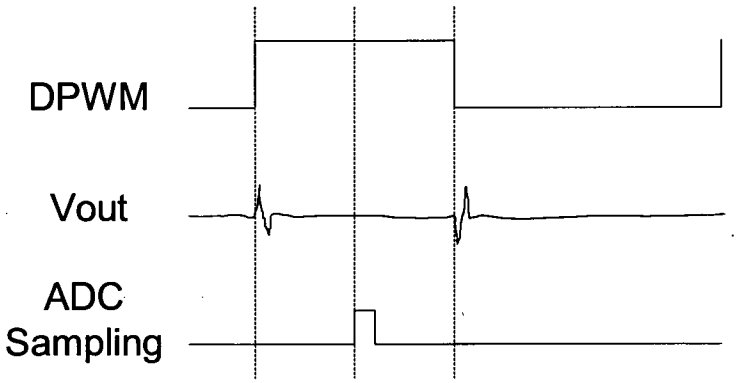
Primary Side Transceiver.

Fig. 4



Secondary Side Transceiver.

Fig. 5



Control of ADC Sampling.

Fig. 6

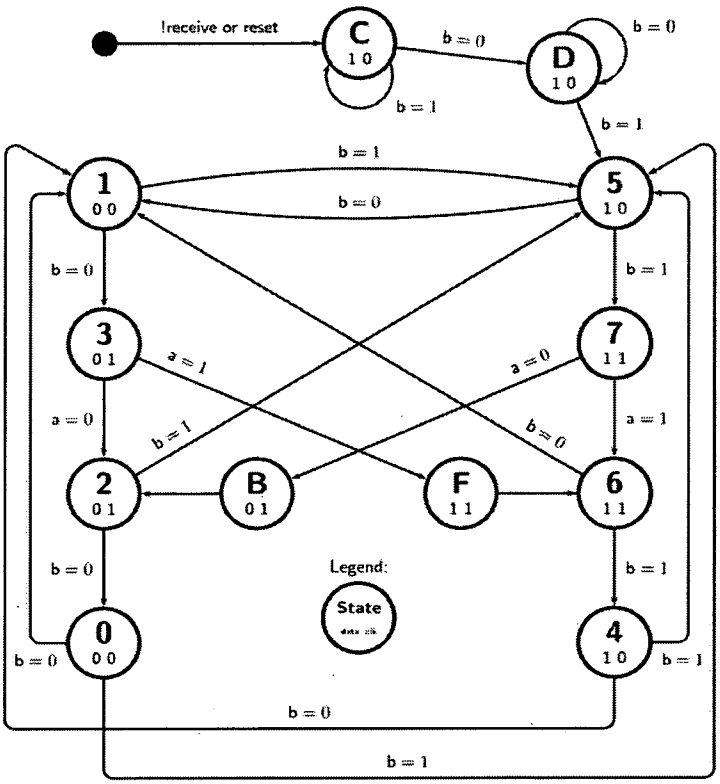

!receive or reset
C
1 0
b = 0
D
1 0
b = 0
b = 1
b = 1
1
0 0
5
1 0
b = 1
b = 0
b = 0
b = 1
3
0 1
7
1 1
a = 1
a = 0
a = 0
a = 1
b = 1
b = 0
2
0 1
B
0 1
F
1 1
6
1 1
b = 0
Legend:
b = 1
State
0
0 0
4
1 0
b = 0
b = 1
b = 0
b = 1

Fig. 7

INTERNATIONAL SEARCH REPORT

International application No
PCT/IE2008/000110

A. CLASSIFICATION OF SUBJECT MATTER
INV. H02M3/335

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y A	US 2006/022656 A1 (LEUNG KAFAI [US] ET AL) 2 February 2006 (2006-02-02) paragraphs [0076], [0077] paragraphs [0085], [0089] paragraphs [0101], [0102] figures 1,4,6a,6b,6c	1 2,3,5 4,6-24
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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
31 March 2009	09/04/2009

Name and mailing address of the ISA/	Authorized officer
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INTERNATIONAL SEARCH REPORT

International application No
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