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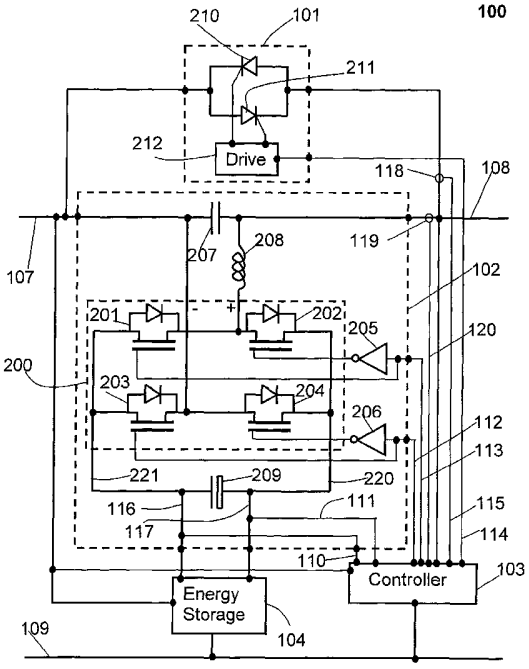
(54) **Title:** DYNAMIC SERIES VOLTAGE COMPENSATOR WITH CURRENT SHARING STATIC SWITCH



(57) **Abstract:** A dynamic series voltage compensator (lOO) for compensating voltage dips in a power line is described. The compensator (100) includes a current sharing static switch (101), a series injection inverter (102), an energy storage unit (104) and a system controller (103). The current sharing static switch (101) includes a pair of anti-parallel thyristors (210) and (211). The series injection inverter includes 4 IGBTs (201), (202), (203) and (204) that form a full bridge of switching devices (200). The system controller (103) monitors the input voltage to determine if voltage compensation is required and monitors the output to determine how much compensation is required. Under normal power line operating condition, that is when no voltage compensation is required, the load current is shared between the current sharing static switch (101) and the series injection inverter (102) by controlling the conduction angle of thyristors (210) and (211). While the current sharing static switch (101) is conductive, the inverter (102) is also controlled to do toggle switching such that no voltage compensation is performed. The toggle switching of the series injection inverter (102) and conduction angle control of current sharing static switch (101) are used to prove the functionality of switching devices of the inverter (102) and the current sharing static switch (101). When there is a voltage dip in the power line, the current sharing static switch (101) is immediately turned off by force commutation, and the inverter (102) carries out the compensation. As the voltage drop across the compensator (100) is controlled to a very low value during normal power line operating conditions, the compensator (100) has very high operation efficiency. Due to the small amount of current flowing though the inverter (102) under the normal power line operating condition; the switching devices (201), (202), (203) and (204) and the filter (207) and (208) of the inverter (102) may be rated low. Thus a high efficient, lightweight and small dynamic series voltage compensator (100) is disclosed.

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

DYNAMIC SERIES VOLTAGE COMPENSATOR WITH CURRENT SHARING STATIC SWITCH

Technical Field of the Invention

This present invention relates generally to the field of alternating current (AC) electric power systems and electric power conversion systems, and in particular, to a system for correcting a voltage dip condition in a power line providing electric power to a load.

Background

In an electric power system, electric power is typically generated by a generator and is transmitted through a transmission and distribution network to customer locations, where the electric power is fed to a load. Normally the supplied electric power should meet a number of requirements. Such requirements include that the voltage should be sinusoidal, the frequency should be 50 or 60 Hz, dependent on the country, and that the voltage amplitude should be of nominal value, with deviation within normal regulation.

Deviation by the voltage of the electrical power supply from the requirements may cause operational problems at the load. In particular, one such deviation known as a voltage dip, often causes the malfunction of equipment, and the shutdown of sophisticated manufacturing plants, or other industrial and commercial systems. A voltage dip is a sudden and momentary reduction in the voltage of electric power supply, and is typically caused by a fault on the electric power system. A voltage dip may also be caused by a load on the electric power system drawing a high current from the electric power system, creating a voltage drop across the impedance of the electric power system. This voltage drop appears as a voltage dip at the load. In a 3-phase electric power system, the magnitude of the voltage dip will generally be different in each voltage of the 3 phases, although the duration of the voltage dip is typically approximately the same.

A variety of power conversion and control method or voltage compensators has been developed to compensate for a voltage dip. One technique used to compensate for a voltage dip is described in US Patent No. 5,329,222 to Gyugyi et al. This patent describes an apparatus and method for compensating utility power line transients with a

series injection voltage that is generated by a three-phase inverter with a common direct current (DC) bus and is coupled to the three-phase power line through a coupling injection transformer. However, if applied in a low voltage electric power system, the use of a three-phase inverter with one common DC bus and an injection transformer is not proper. This is because the cost of the coupling injection transformer is high, and the injection transformer is heavy and has a big footprint. Furthermore, the injection transformer may have internal impedance that may cause additional voltage drop across the injection transformer during normal operation. This voltage drop may be overcome by configuring the inverter to output a voltage to compensate for the voltage drop during normal operation, but this causes a reduced operation efficiency of the apparatus disclosed.

Another technique of compensating for voltage dips is described in US Patent No. 5,883,796 to Cheng et al. This patent describes apparatus and method for restoring voltage dips using a three-phase inverter with a common DC bus and a coupling injection transformer. Consequently this device and the method have a similar limitation as that described in US Patent 5,329,222 in that high operation efficiency and a low voltage drop across the injection transformer cannot be achieved simultaneously.

Yet another technique of compensating for voltage dips is described in International Publication No. PCT/SG00/00057 to SP Systems. This publication describes an apparatus and method that is suitable for application in low voltage electric system for compensating for voltage dips. In this method, independent inverters are directly connected to each phase of the power lines to the load. As no coupling injection transformer is used, the cost, weight and footprint of the compensator can be minimized.

Yet another technique of compensating for voltage dip is described in US Patent No. 6,118,676 to Divan et al. This patent describes apparatus and method to compensate for a voltage dip using the energy derived from the remaining voltage of the power line during the voltage dip. However, when the remaining voltage of the power supply during a voltage dip is very low, or the depth of the voltage dip is high, it is difficult for the method to obtain enough energy to perform the compensation. Further, during the voltage dip and the dip recovery, transient current may be drawn from the power supply. The power conversion method of this patent makes use of a half bridge inverter that

requires a higher DC bus voltage than a full bridge inverter for the same amount of output voltage.

In addition to the above voltage compensators, uninterrupted power supplies (UPSs) has been used to compensate for voltage dips as well as voltage transients, voltage swells and drops. However UPSs normally consists of more switching devices, expensive controllers and huge energy storage units that make UPSs more expensive. Such a UPS has a further limitation in that it normally operates at a lower efficiency.

The prior art thus fails to provide a lightweight, inexpensive and high efficient device to compensate for voltage dips that can cause malfunction and shutdown of industrial and commercial systems.

Summary of the Invention

It is an object of the present invention to substantially overcome, or at least ameliorate, one or more disadvantages of existing arrangements.

According to an aspect of the invention, there is provided a dynamic series voltage compensator for compensating voltage dips in an alternating current electric power system, the dynamic series voltage compensator comprising:

an energy storage unit for storing energy in the form of a DC voltage;

a current sharing static switch connected between input and output terminals of the dynamic voltage compensator for selectively connecting the input and output terminals;

a series injection inverter connected in parallel with the current sharing static switch for converting the DC voltage from the energy storage unit to AC voltage; and

a system controller for detecting a voltage dip on the input terminal and for controlling the current sharing static switch and the series injection inverter wherein, with no voltage dip detected, the system controller controls the current sharing static switch to be conductive for at least part of a current cycle and controls the series injection inverter to conduct part of the current to the output terminals, and upon the system controller detecting a voltage dip, the system controller controls the current sharing static switch to open and controls the series injection inverter to inject a voltage signal between the input and output terminals to compensate for the voltage dip.

Preferably, the current sharing static switch comprises:

anti-parallel connected thyristors; and

a thyristor drive circuit for receiving a control signal from the system controller and for providing the anti-parallel connected thyristors with a firing signal in response to the control signal wherein, with no voltage dip detected, the system controller controls the thyristor drive circuit to provide the firing signal after a predetermined period after current through the current sharing static switch crosses zero.

Preferably the series injection inverter comprises a full bridge of switching devices, and while the current sharing static switch is controlled to be conductive, the switching devices are switched such that no voltage signal is injected between the input and output terminals.

Brief Description of the Drawings

Embodiments of the present invention will now be described with reference to the drawings, in which:

FIG. 1 is a schematic block diagram illustrating a single-phase implementation of a dynamic series voltage compensator with a current sharing static switch, and the manner in which the dynamic series voltage compensator is connected in an application circuit;

FIG. 2 is a detailed schematic diagram of the dynamic series voltage compensator;

FIG. 3 is a detailed schematic diagram of a system controller of the dynamic series voltage compensator;

FIG. 4 is a schematic block diagram illustrating a three-phase implementation of a dynamic series voltage compensator with current sharing static switch;

FIG. 5A shows an oscillogram of a typical voltage dip from the AC power source;

FIG. 5B shows an oscillogram of the output voltage of the single-phase dynamic series voltage compensator during the voltage dip illustrated in Fig. 5A;

FIG. 6A shows an oscillogram of a typical voltage dip from a three-phase AC power source; and

FIG. 6B shows an oscillogram of the output voltages of the three-phase dynamic voltage compensator during the voltage dip illustrated in Fig. 6A.

Detailed Description

Where reference is made in any one or more of the accompanying drawings to features, which have the same reference numerals, those features have for the purposes of this description the same function(s) or operation(s), unless the contrary intention appears.

FIG. 1 is a schematic diagram illustrating a single-phase implementation of a dynamic series voltage compensator 100 connected between an AC power source 105 and an AC load 106. The dynamic series voltage compensator 100 is operable to compensate for voltage dips in the supply voltage from the AC power source 105. A waveform 121 of a typical voltage dip is also illustrated. The dynamic series voltage compensator 100 may also be employed in a multi-phase system to compensate for voltage dips on the supply voltages from the respective supply phases of such a multi-phase system. A three-phase implementation of the dynamic series voltage compensator 100 is illustrated in, and is described with reference to, FIG. 4.

Referring to FIG. 1, the dynamic series voltage compensator 100 of the preferred embodiment includes a current sharing static switch 101, a series injection inverter 102, a system controller 103 for controlling the current sharing static switch 101 and the series injection inverter 102, and an energy storage unit 104 for providing energy in the form of direct current (DC) voltage to the series injection inverter 102. The energy storage unit 104 may be formed from an ultra capacitor, a flywheel system, a battery or any other means that can provide energy in the form of DC voltage.

The current sharing static switch 101 is connected in parallel to the series injection inverter 102, and both are connected between the AC power source 105 and load 106 through wires 107 and 108 respectively. A neutral wire 109 is provided as return path. The energy storage unit 104 provides the DC voltage to the series injection inverter 102 though wires 116 and 117. The system controller 103 and energy storage unit 104 are also connected to the neutral wire 109, from which a reference voltage is acquired.

The system controller 103 obtains an input voltage signal to the dynamic series voltage compensator 100 from wire 107, obtains an output voltage signal of the dynamic

voltage compensator 100 from wire 108, obtains a current signal though signal wire 115 of the current through the current sharing static switch 101 measured with a current sensor 118, obtains a current signal through signal wire 120 of the current through the series injection inverter 102 measured with a current sensor 119, and obtains a DC bus voltage of serial injection inverter 102 through signal wire 110 and signal wire 111. The system controller 103 controls the current sharing static switch 101 through control line 114, and controls the serial injection inverter through control lines 112 and 113.

During normal operation conditions, that is when the power source 105 provides a voltage within predefined limits, the system controller 103 controls the current sharing static switch 101 and the series injection inverter 102 such that the current to the load 106 is shared by the current sharing static switch 101 and the series injection inverter 102. The normal operation condition is also referred to hereinafter as the current sharing mode.

When the system controller 103 detects a voltage dip from the AC power source 105 by more than the predefined limits, which is detected through the measurement of the voltage on wire 107, the system controller 103 controls the current sharing static switch 101 to open and the series injection inverter 102 to inject energy between terminals 107 and 108 so that AC power at or near the nominal voltage level is provided to the load 106. The dynamic series voltage compensator 100, and in particular the series injection inverter 102, thus injects voltage between wire 107 and wire 108 so that the load 106 receives a dip free supply, as is illustrated by waveform 122.

A more detailed schematic diagram of the dynamic series voltage compensator 100 illustrated in FIG. 1 is illustrated in, and is described with reference to, FIG. 2. In particular, more detail is shown of the current sharing static switch 101 and the series injection inverter 102. The connections to and from the system controller 103 and the energy storage unit 104 are also illustrated.

The current sharing static switch 101 includes anti parallel-connected thyristors 210 and 211, and a thyristor drive circuit 212. The thyristor drive circuit 212 receives a control signal from controller 103 through control line 114. When the control signal on control line 114 is 'HIGH', the thyristor drive circuit 212 provides thyristors 210 and 211 with firing signals so that each of thyristors 210 and 211 becomes conductive while

respective proper voltage polarity is applied. Conversely, when the signal on control line 114 is 'LOW', the thyristor drive circuit 212 does not provides thyristors 210 and 211 with firing signals and the thyristors 210 and 211 form an open circuit when the respective current through thyristors 210 and 211 reaches zero.

The series injection inverter 102 includes a full bridge of switching devices 200, bridge drive units 205 and 206, a switching harmonics filter, and DC bus capacitor 209 connected over the DC supply voltage supplied from the energy storage unit 104 over lines 116 and 117. The full bridge of switching devices 200 consists of 4 Insulated-Gate-Bipolar-Transistors (IGBT) with anti-parallel connected freewheeling diodes 201, 202, 203 and 204. The switching harmonics filter consists of a series connected inductor 208 and capacitor 207, and is connected between the output terminals of the full bridge of switching devices 200, with the inductor 208 being connected to the positive output terminal '+' and the capacitor 207 being connected to the negative output terminal '-'. The connection point between the capacitor 207 and inductor 208 is connected to wire 108 for forming the output terminal of the series injection inverter, whereas the negative output terminal of the full bridge of switching devices 200 is connected to wire 107 forming the input terminal of the series injection inverter.

The series injection inverter 102 receives control signals from the system controller 103 over control lines 112 and 113. When the control signal on control line 112 is 'HIGH', IGBT 203 is in a conductive mode, and because the control signal on control line 112 is inverted by bridge drive unit 206, IGBT 204 is in a cut-off mode, and vice versa. Similarly, when the control signal on control line 113 is 'HIGH', IGBT 201 is in a conductive mode, and because the control signal on control line 113 is inverted by bridge drive unit 205, IGBT 202 is in a cut-off mode, and vice versa.

The system controller 103 measures the DC bus voltage supplied by the energy storage unit 104 to the series injection inverter 102 through lines 110 and 111 connected to lines 116 and 117.

FIG. 3 is a more detailed schematic diagram of the system controller 103 of the dynamic series voltage compensator 100. Although the schematic diagram of FIG. 3 shows a digital circuit implementation of the system controller 103, the system controller

103 may also be implemented in an analog circuit or in a combination of a digital circuit and an analog circuit.

As is described in relation to FIGS. 1 and 2, the system controller 103 receives 5 inputs, those being:

the input voltage signal to the dynamic voltage compensator 100 obtained from wire 107;

the output voltage signal of the dynamic voltage compensator 100 obtained from wire 108;

the current through the current sharing static switch 101 measured by current sensor 118 and provided through signal wire 115;

the current through the series injection inverter 102 measured by current sensor 119 and provided to the system controller 103 through signal wire 120; and

the DC bus voltage of the series injection inverter 102 which is the difference in the voltages received through signal wire 110 and signal wire 111, and is obtained by passing the voltages received through signal wire 110 and signal wire 111 through a differential attenuation circuit 306.

Each of these inputs, which are in analogue form, is converted to digital form by analogue-to-digital (A/D) converters 301, 302, 303, 305 and 304 respectively. In addition, the digital signal of the input voltage signal to the dynamic series voltage compensator 100 is pre-processed by digital filter 307.

The outputs of the system controller 103 are the control signal to IGBT 201 and IGBT 202 which is output through control line 113, the control signal to IGBT 203 and IGBT 204 which is output through control line 112, and the control signal to the thyristor drive circuit 212 of the current sharing static switch 101 which is output through control line 114. The neutral wire 109 is connected to the internal ground of the system controller 103 and is indicated by 327 in FIG. 3.

An over-current detection block 314 receives as inputs the digital version of the current through the current sharing static switch 101 and the digital version of the current through the series injection inverter 102, and determines whether an over-current condition exists. When the over-current detection block 314 determines that the current through either of the current sharing static switch 101 (FIG. 2) or the series injection

inverter 102 is higher than the capability of the IGBTs of the full bridge of switching devices 200, the over-current detection block 314 outputs a 'LOW' signal though signal wire 360. The signal on signal wire 360 is normally 'HIGH'. A 'LOW' signal on signal wire 360 keeps or turns the current sharing static switch 101 'ON" through NAND gate 321 and turns IGBTs 201 and 203 'OFF' and IGBTs 202 and 204 'ON' by feeding a 'LOW' signal to control lines 112 and 113 through AND gates 324a and 324b. Hence, under such an over-current condition, the current sharing static switch 101 is forced into conductive mode while the series injection inverter 102 does not inject any energy between wire 107 and wire 108. The dynamic series voltage compensator 100 does not compensate for a voltage dip under the over-current condition.

In operation, the filtered digital signal of the input voltage to the dynamic series voltage compensator 100 is sent to a reference table-updating block 308. The reference table-updating block 308 is controlled by a signal on signal wire 345. When the signal on signal line 345 is 'LOW', which is the case during normal operation conditions or current sharing mode, the reference table-updating block 308 continuously updates a reference signal table which stores a digital representation of the input voltage on wire 107. When the signal on signal wire 345 is 'HIGH', which is the case when a voltage dip has been detected, the reference table-updating block 308 freezes the available reference signal table. The reference table-updating block 308 generates a reference signal, which is feed to a dip detection block 309 via signal wire 362 for detecting a voltage dip condition, and also to subtracters 310 and 311 via signal line 341 for generating an injection voltage signal.

Subtracter 310 calculates the difference between the reference signal on signal wire 341 and the filtered digital signal of the input voltage on wire 107 via signal wire 340. Subtracter 311 calculates the difference between the reference signal on signal line 341 and the digital signal of the output voltage on signal line 342, which is then adjusted through PI control 312. The sum of outputs from subtracter 310 and PI control 312, calculated by adder 313, is then provided as input to pulse width modulation (PWM) generator 318. Additionally, the PWM generator 318 makes use of the DC bus voltage of the series injection inverter 102 from A/D converter 304 in generating PWM switching signals on signal wire 343 and signal wire 344.

The dip detection block 309 receives as inputs the filtered digital signal of the input voltage on wire 107 via signal line 340, the reference signal from the reference table-updating block 308, the digital signal of the output voltage on wire 108 via signal line 342, and the digital version of the current through the current sharing static switch 101 via signal wire 346, and determines from those inputs whether a voltage dip occurred, what kind of force commutation should be applied and whether the force commutation is completed. The dip detection block 309 generates a conduction angle control signal as output provided on signal wire 353 to current sharing static switch 101 through NAND gate 326 and NAND gate 321, and also a two-bit signal as output provided on signal wires 351 and 352 to block 315. In a preferred implementation, the dip detection block 309 only determines whether a voltage dip occurred when the instantaneous value of reference signal from the reference table-updating block 308 is higher than 30% of a peak value stored.

The conduction angle control signal on line 353 is set to 'HIGH' when a predefined delay elapsed after each zero crossing of the current. The conduction angle control signal is set to 'LOW' again before a following zero crossing of the current. When the conduction angle of the current sharing static switch is set to 180 electric-degrees, the delay after each zero crossing of the current is set to zero. In this case the conduction angle control signal on signal wire 353 is always set to 'HIGH'.

Block 315 decodes the two-bit signal received from the dip detection block 309 into four signals provided on signal wires 350, 349, 348 and 347. When the two-bit signal is '00', the signal on signal line 350 is set to 'HIGH'; and the other three signals are set to 'LOW'. When the two-bit signal is '01', the signal on signal line 349 is set to 'HIGH'; and the other three signals are set to 'LOW'. When the two-bit signal is '10', the signal on signal line 348 is set to 'HIGH'; and the other three signals are set to 'LOW'. Finally, when the two-bit signal is '11', the signal on signal line 347 is set to 'HIGH'; and the other three signals are set to 'LOW'.

When the difference between the reference signal provided on signal wire 362 and the filtered digital signal of the input voltage provided on signal wire 340 is larger than a predefined setting, and the digital version of the current through the current sharing static switch 101 is negative, then dip detection block 309 generates the two bit signal '00'.

The two-bit signal '00' indicates that a positive force commutation (Positive FC) is required.

When the difference between the reference signal provided on signal wire 362 and the filtered digital signal of the input voltage provided on signal wire 340 is larger than a predefined setting, and the digital version of the current through the current sharing static switch 101 is positive, then dip detection block 309 generates the two bit signal '01'. The two-bit signal '01' indicates that a negative force commutation (Negative FC) is required.

When the difference between the reference signal provided on signal wire 362 and the filtered digital signal of the input voltage provided on signal wire 340 is larger than the predefined setting, and a zero crossing of the digital version of the current through the current sharing static switch 101 is detected, the dip detection block 309 generates the two bit signal '11'. The two-bit signal '11' indicates that force commutation is completed and series voltage injection could be started. This state typically follows one of the above states in which two-bit signals '00' or '01' is generated.

During normal operation, that is when the difference between the reference signal provided on signal wire 362 and the filtered digital signal of the input voltage provided on signal wire 340 is smaller than the predefined setting, then dip detection block 309 generates the two bit signal '10', which indicates that no dip compensation is required and referred to as the toggling state. The signal on signal wire 348 is set to 'HIGH'; and the other three signals are set to 'LOW' by block 315, causing the output of OR gate 316 to be 'LOW'. During this condition the signal on signal wire 345 is also 'LOW' and the reference table-updating block 308 continuously updates a reference signal table. The output of OR gate 316 is inverted by an INVERT gate 325 before being fed to the AND gate 326 with the conduction angle control signal on line 353. During this normal condition the output of the INVERT gate 325 provided on signal wire 361 is 'HIGH'. In the absence of an over-current condition, the state of the signal on line 114 will be that of the conduction angle signal on signal wire 353. Thus, in the absence of an over-current condition, when the phase angle of current is within the conductive angle (signal on signal wire 353 is 'HIGH'), control line 114 is forced 'HIGH', and the thyristor drive circuit 212 provides thyristors 210 and 211 with firing signals.

When any one of the signals on signal lines 350, 349 or 347 is high, which occurs when dip detection block 309 detects a voltage dip and generates the two bit signal '00', '01, or '11' respectively, the output of OR gate 316 is 'HIGH', the signal on signal wire 361 is 'LOW'. In the absence of an over-current condition, when a voltage dip is detected control line 114 is forced 'LOW' irrespective of the state of the conduction angle control signal on signal wire 353, and the thyristor drive circuit 212 does not provide thyristors 210 and 211 with firing signals. Also, the signal on signal wire 345 is 'HIGH', and the reference table-updating block 308 freezes the available reference signal table.

Hence, from the above, the current sharing static switch 101 is turned 'OFF' when a voltage dip is detected and the current through the current sharing static switch 101 has crossed zero. The current sharing static switch 101 is turned or kept 'ON' when an over-current condition is detected; or when no dip compensation is required and the phase of current is in the conduction phase angle. In current sharing mode, the static current sharing switch 101 is only turn 'ON' when the phase of current is in the conduction phase angle.

As set out above, when positive force commutation is required and the two-bit signal is '00', the signal on signal wire 350 is set to 'HIGH'. The signal on signal wire 358, after OR gate 322, is also 'HIGH'. In the absence of an over-current condition, the output of AND gate 324a is 'HIGH', which forces control line 112 'HIGH', and IGBT 203 is turned 'ON', while IGBT 204 is turned 'OFF'. With signals on signal wires 347 and 348 'LOW', the outputs of AND gates 319, 320a and 320b, provided on signal wires 354, 356 and 367 respectively, are 'LOW', and with the signal on signal wire 349 also being 'LOW', the output of OR gate 323 provided on signal wire 359 is also 'LOW'. The output of AND gate 324b is 'LOW', which forces control line 113 'LOW', and IGBT 202 is turned 'ON', while IGBT 201 is turned 'OFF'.

In a similar manner, when negative force commutation is required and the two-bit signal is '01', the signal on signal wire 349 is set to 'HIGH' resulting in the signal on line 359, after OR gate 323, to be 'HIGH'. In the absence of an over-current condition, the output of AND gate 324b is 'HIGH', which forces control line 113 HIGH', and IGBT 201 is turned 'ON', while IGBT 202 is turned 'OFF'. With the signals on signal wires

347 and 348 being 'LOW', the outputs of AND gates 320a and 319 are 'LOW', and with the signal on signal wire 350 'LOW', the signal on line 358, after OR gate 322, is also 'LOW'. The signal on line 112 is forced 'LOW' by AND gate 324a, and IGBT 204 is turned 'ON', and IGBT 203 is turned 'OFF'.

After the negative or positive force commutation (corresponding to two-bit signals '00' and '01' respectively), when a zero crossing of the digital version of the current through the current sharing static switch 101 is detected, the two-bit signal is '11' for dip compensation. The signal on signal line 347 is set 'HIGH' and the other 3 output signals of block 315 are set low. The PWM switching signals on signal wires 343 and 344 generated by PWM generator 318 are switched to control lines 112 and 113 respectively. The IGBTs 201, 202, 203 and 204 of the full bridge of switching devices 200 (FIG. 2) are controlled by the PWM switching signals to generate an PWM output which, after the filtering provided by inductor 208 and capacitor 207, results in a required sinusoidal signal that makes the output voltage of the dynamic voltage compensator on line 108 dip free.

Finally, when no dip compensation is required, the toggle state, the two-bit signal is '10', and the signal on signal wire 348 is set to 'HIGH'. With the 'HIGH' signal on signal wire 348 and a toggling signal provided by block 317 provided as inputs to AND gate 319, the output of AND gate 319 provided on signal wire 354 is that state of the toggle signal. The outputs of OR gates 322 and 323 also toggles with the toggle signal. In the absence of an over-current condition, the outputs of AND gates 324a and 324b also toggles, which in turn toggles control lines 112 and 113. When the toggle signal of block 317 is 'HIGH', IGBTs 201 and 203 are turned 'ON', while IGBTs 202 and 204 are turned 'OFF'. When the toggle signal of block 317 then switches to 'LOW', IGBTs 201 and 203 are turned 'OFF', while IGBTs 202 and 204 are turned 'ON'. During the toggling state, the output terminals of the full bridge of switching devices 200, '+' and '-' are simultaneously switched from negative DC bus 221 to positive DC bus 220, or simultaneously switched from positive DC bus 220 to negative DC bus 221. Neither of these toggling state conditions causes any disturbance between input terminal 107 and output terminal 108. During toggling state, after each zero crossing of the current and before the conduction angle control signal on line 353 is set to 'HIGH', the current

sharing static switch 101 is non-conductive and the load current flows though the inverter 102 that is in short circuit mode. When the conduction angle control signal on line 353 is set to 'HIGH' following the predefined delay, the current sharing static switch 101 is conductive and the load current flows though current sharing static switch 101.

Typically power compensation devices operates several months or even years in a condition where no voltage dip is detected. The dynamic series voltage compensator 100 proves the switching functionality of the current sharing static switch 101 and switching devices 201, 202, 203 and 204 of series injection inverter 102 during such no voltage dip periods. In particular, the switching functionality of the current sharing static switch 101 is proven through the conduction angle control, while the switching functionality of the switching devices 201, 202, 203 and 204 is proven by the toggle switching. The frequency of the toggle switching is controlled by the frequency of the signal of block 317, which is determined according to how often the switching functionality of the switching devices 201, 202, 203 and 204 is to be proven. In a preferred implementation, the toggling frequency is 0.1 Hz.

FIG. 4 is a schematic block diagram illustrating a three-phase implementation of a dynamic voltage compensator with a current sharing static switch. In fact, three single-phase implementations of the dynamic voltage compensator with current sharing static switch illustrated in FIG. 2 are combined to form the three-phase dynamic voltage compensator. In FIG. 4, control lines, signal lines, the energy storage units and series injection inverters for phase-b and phase-c are not illustrated. Although three independent system controllers may be used in the three-phase implementation of the dynamic series voltage compensator, typically a single controller is used to control the three series injection inverters and the three current sharing static switches using the principles described in relation to FIG. 3.

FIG. 5A shows an oscillogram 501 of a typical voltage dip from the AC power source 105 (FIG. 1) on wire 107. FIG. 5B shows an oscillogram 502 of the output voltage of the single-phase dynamic series voltage compensator 100 on wire 108 during the voltage dip illustrated in Fig. 5A. FIG. 6A shows an oscillogram 601 of a typical voltage dip from a three-phase AC power source 105, and FIG. 6B shows an oscillogram

602 of the output voltages of the three-phase dynamic series voltage compensator (FIG. 4) during the voltage dip illustrated in Fig. 6A. The voltage dip appearing in the input voltages 501 and 602 are compensated so that the output voltages 502 and 602 are dip free.

The advantages of the embodiments of the invention are manifold. One advantage is that in the current sharing mode or when there is no voltage dip from the AC power source 105, the load current is shared by the current sharing static switch 101 and the series injection inverter 102. As the main fraction of the load current flows through the current sharing static switch 101 whose voltage drop in conductive mode is very small (less than 1 V), there is no obvious voltage drop between the input and the output of the dynamic series voltage compensator 100.

Another advantage of the embodiments of the invention is that in the current sharing mode or when there is no voltage dip from the AC power source 105, only a minor part of the load current flows though the inverter 102, so that the inverter 102, and the filter (capacitor 207 and inductor 208 illustrated in FIG. 2) may be kept small in size.

Yet a further advantage of the embodiments of the invention is that in the current sharing mode or when there is no voltage dip from the AC power source 105, the switching functionality of the switching devices 201, 202, 203, 204, 210 and 211 of the inverter 102 and the current sharing static switch 101 is proved through toggling switch and conduction angle control continuously.

The foregoing describes only some embodiments of the present invention, and modifications and/or changes can be made thereto without departing from the scope and spirit of the invention, the embodiments being illustrative and not restrictive.

Claims:

1. A dynamic series voltage compensator for compensating voltage dips in an alternating current electric power system, said dynamic series voltage compensator comprising:

an energy storage unit for storing energy in the form of a DC voltage;

a current sharing static switch connected between input and output terminals of said dynamic voltage compensator for selectively connecting said input and output terminals;

a series injection inverter connected in parallel with said current sharing static switch for converting said DC voltage from said energy storage unit to AC voltage; and

a system controller for detecting a voltage dip on said input terminal and for controlling said current sharing static switch and said series injection inverter wherein, with no voltage dip detected, said system controller controls said current sharing static switch to be conductive for at least part of a current cycle and controls said series injection inverter to conduct part of the current to said output terminals, and upon said system controller detecting a voltage dip, said system controller controls said current sharing static switch to be non-conductive and controls said series injection inverter to inject a voltage signal between said input and output terminals to compensate for said voltage dip.

2. The dynamic series voltage compensator as claimed in claim 1 wherein, with no voltage dip detected, said system controller controls said current sharing static switch to be non-conductive for a predetermined period after current through said current sharing static switch crosses zero, and conductive thereafter until said current through said current sharing static switch again crosses zero.

3. The dynamic series voltage compensator as claimed in claim 1 wherein said current sharing static switch comprises:

anti-parallel connected thyristors; and

a thyristor drive circuit for receiving a control signal from said system controller and for providing said anti-parallel connected thyristors with a firing signal in response to

said control signal wherein, with no voltage dip detected, said system controller controls said thyristor drive circuit to provide said firing signal after a predetermined period after current through said current sharing static switch crosses zero.

4. The dynamic series voltage compensator as claimed in claim 3 wherein, said part of said current supplied by said series injection inverter to said output terminals is controlled by controlling said predetermined period.

5. The dynamic series voltage compensator as claimed in claim 1 wherein said series injection inverter comprises a full bridge of switching devices.

6. The dynamic series voltage compensator as claimed in claim 5 wherein, while said current sharing static switch is controlled to be conductive, said switching devices are switched such that no voltage signal is injected between said input and output terminals.

7. The dynamic series voltage compensator as claimed in claim 5 wherein said full bridge comprises four Insulated-Gate-Bipolar-Transistors with anti-parallel connected freewheeling diodes.

8. The dynamic series voltage compensator as claimed in claim 5 wherein said series injection inverter further includes a low pass filter comprising a capacitor and an inductor.

9. The dynamic series voltage compensator as claimed in claim 1 wherein said system controller includes a reference signal table for storing values indicative of voltage on said input terminal when no voltage dip is detected, said system controller using said values in said reference signal table for detecting said voltage dip and for controlling said voltage signal injected by said series injection inverter.

10. The dynamic series voltage compensator as claimed in claim 9 wherein said system controller detects said voltage dip when a difference between voltage on said input terminal and a corresponding value stored in said reference signal table exceeds a predetermined value.

11. The dynamic series voltage compensator as claimed in claim 10 wherein said system controller performs voltage dip detection only when said corresponding value in said reference signal table exceeds 30% of a peak value stored in said reference signal table.

12. The dynamic series voltage compensator as claimed in claim 9 wherein said reference signal table is frozen when said voltage dip is detected.

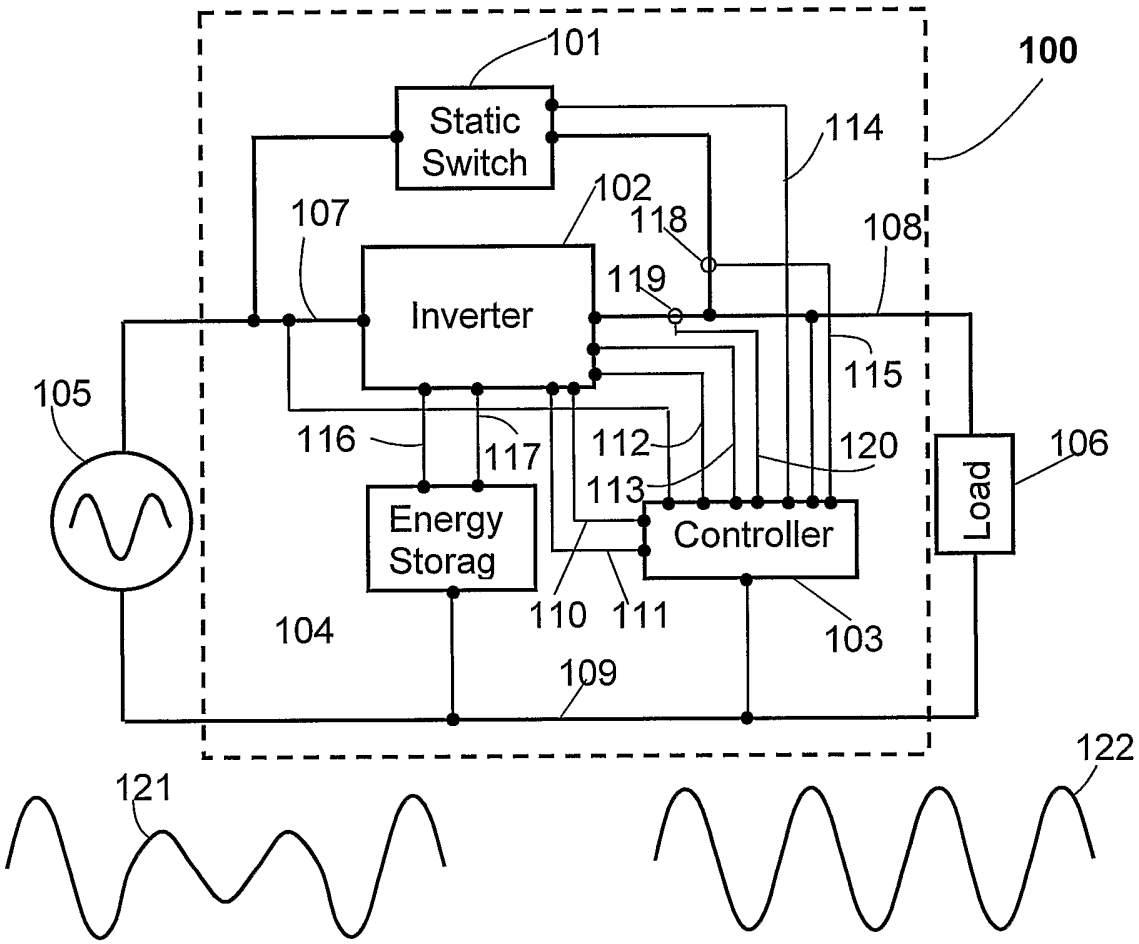
13. The dynamic series voltage compensator as claimed in claim 9 wherein at least a difference between voltage on said input terminal and a corresponding value stored in said reference signal table is used for generating a pulse width modulation control signal to said series injection inverter.

14. The dynamic series voltage compensator as claimed in claim 13 wherein a difference between voltage on said output terminal and said corresponding value is further used for generating said pulse width modulation control signal.

15. The dynamic series voltage compensator as claimed in claim 1 wherein said system controller further monitors current through said series injection inverter and current through said current sharing static switch for detecting an over-current condition.

16. The dynamic series voltage compensator as claimed in claim 15 wherein said system controller controls said current sharing static switch to be conductive for a full current cycle upon detecting that at least one of said current through said current sharing static switch or said current through said series injection inverter is higher than the capability of switching devices of said series injection inverter.

17. The dynamic series voltage compensator as claimed in claim 1 wherein said energy storage unit comprises one or more of an ultra capacitor, a flywheel system and a battery bank.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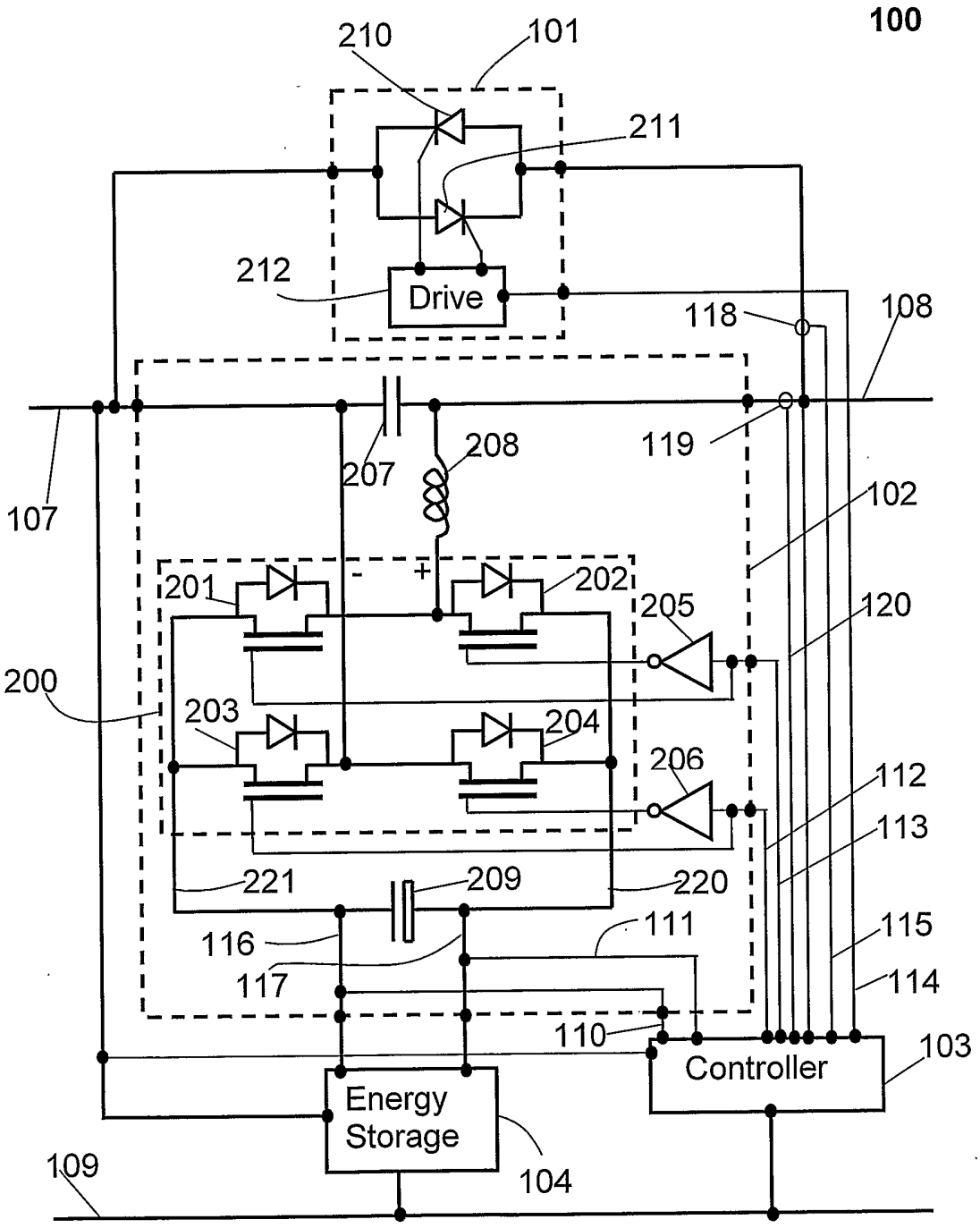
100
Static Switch
114
102
107
118
108
Inverter
119
115
105
116
117
112
120
106
113
Energy Storag
Controller
Load
104
110
111
103
109
122
121

FIG. 1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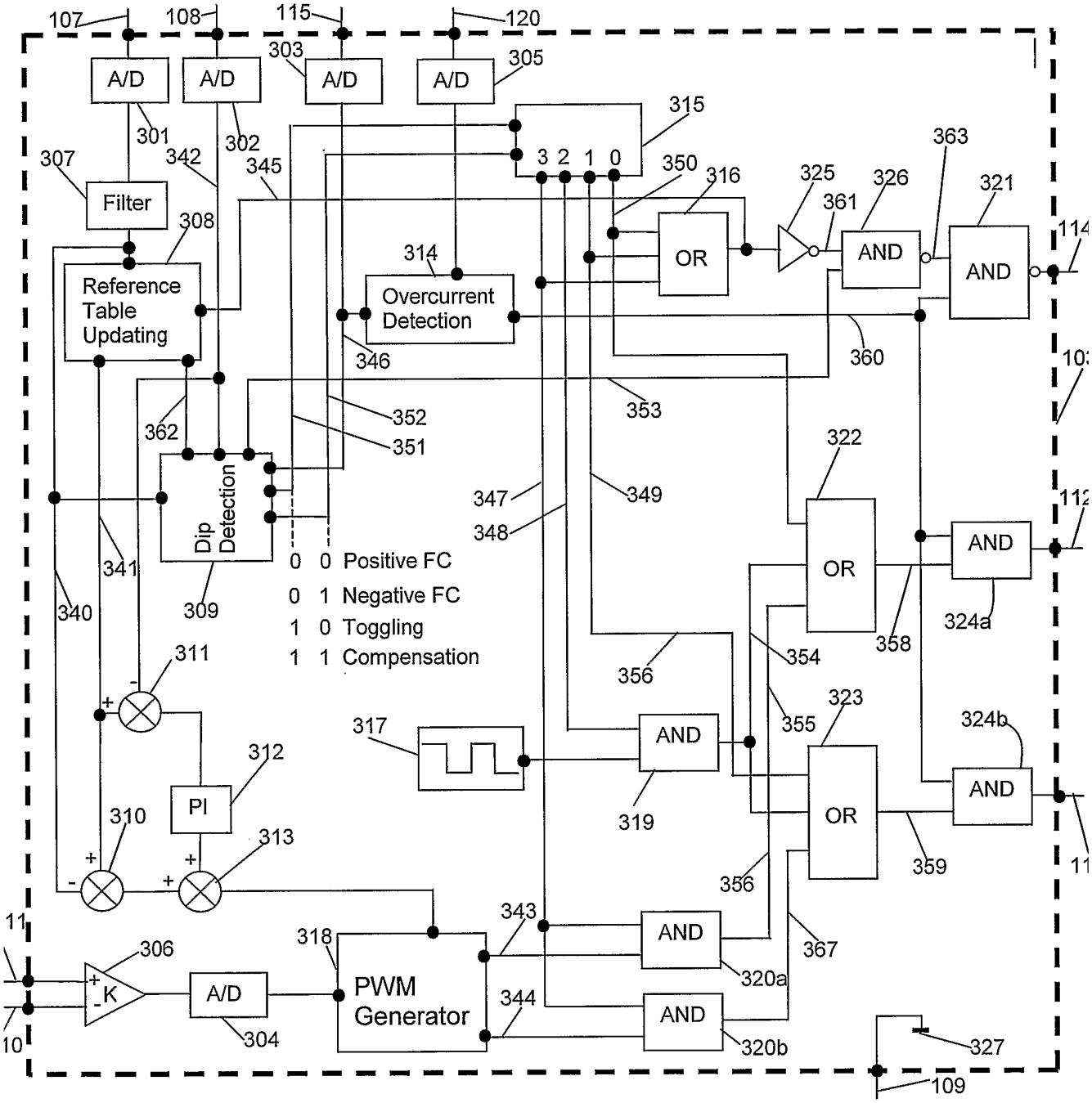
210
101
211
212
Drive
118
108
119
107
207
208
102
201
202
205
120
200
203
204
206
112
113
221
209
220
116
111
115
117
114
110
103
Controller
Energy
Storage
109
104

FIG. 2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108
115
120
303
305
A/D
A/D
A/D
A/D
315
3 2 1 0
301
302
307
342
345
350
316
325
326
363
321
361
Filter
308
OR
AND
AND
114
Reference Table Updating
314
Overcurrent Detection
346
360
103
353
352
351
362
322
347
349
112
348
Dip Detection
OR
AND
341
0 0 Positive FC
0 1 Negative FC
1 0 Toggling
1 1 Compensation
340
309
324a
358
354
356
311
323
355
324b
317
AND
312
PI
319
OR
AND
310
313
359
356
11
343
AND
367
306
318
320a
A/D
PWM Generator
344
AND
320b
327
10
304
109

FIG. 3

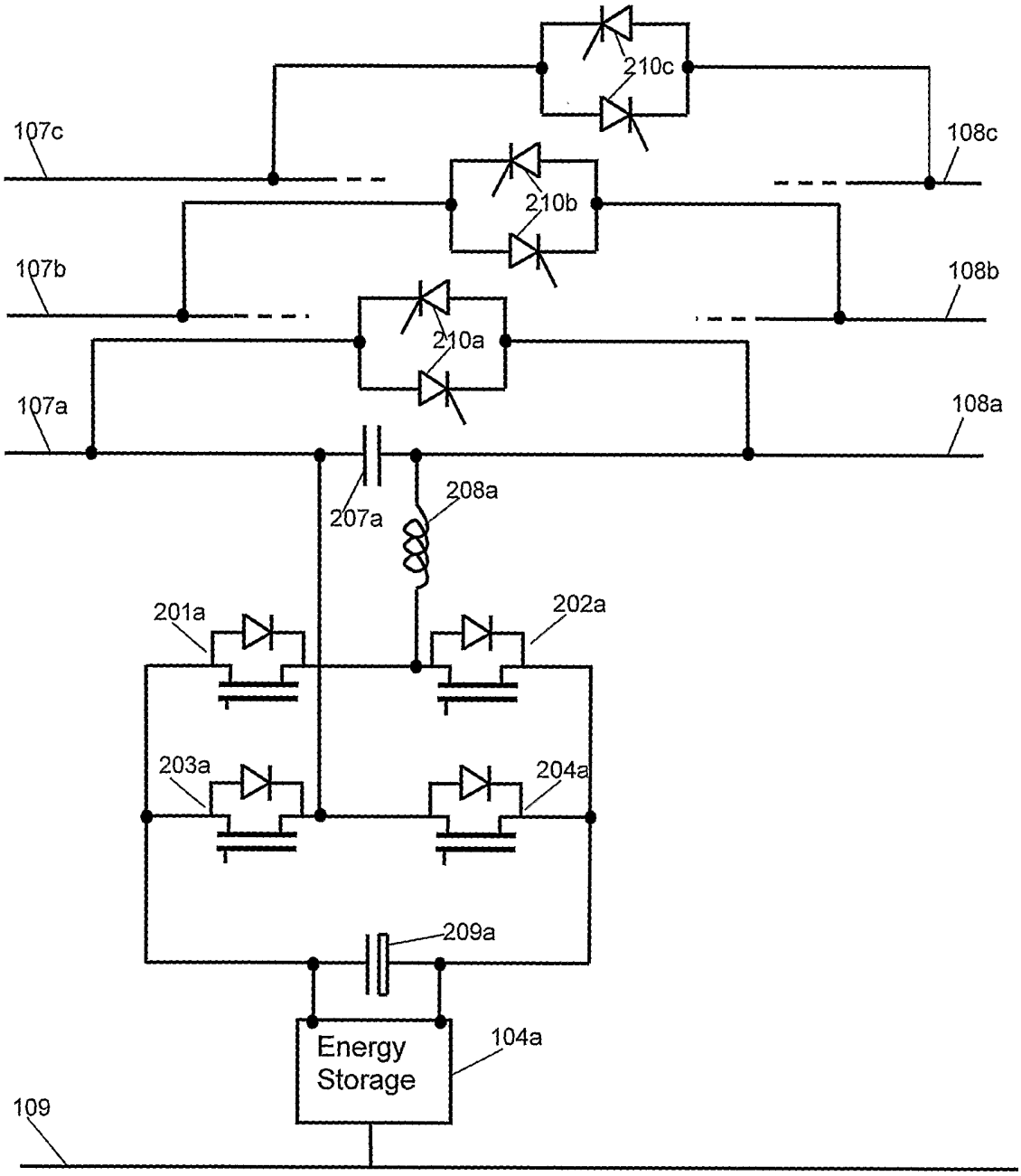
210c
107c
108c
210b
107b
108b
210a
107a
108a
207a
208a
201a
202a
203a
204a
209a
Energy Storage
104a
109

FIG. 4

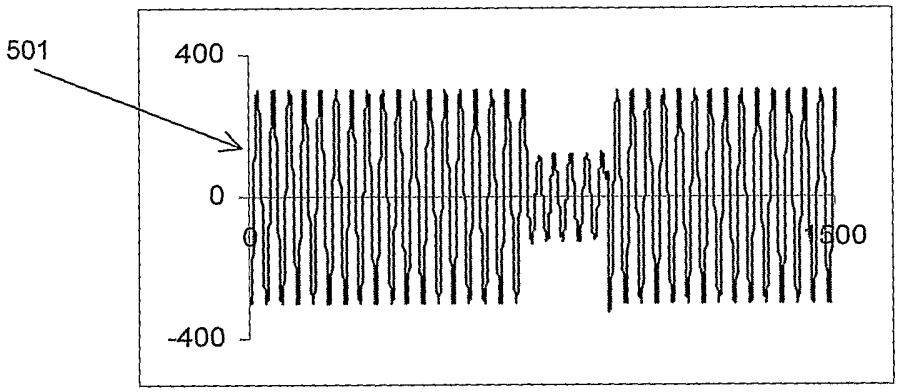

FIG. 5A

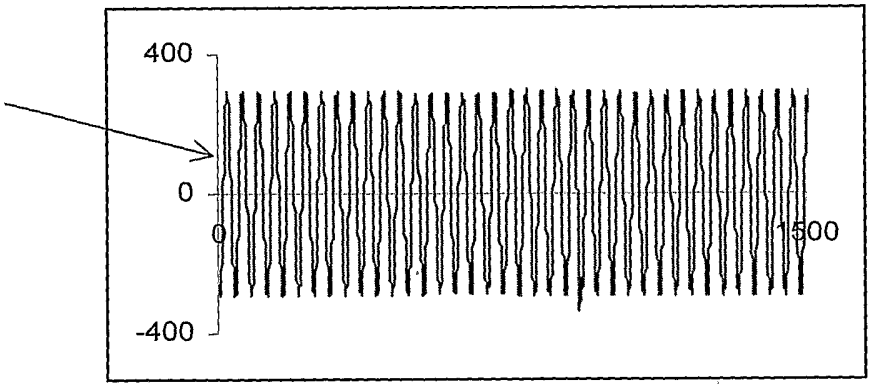

FIG. 5B

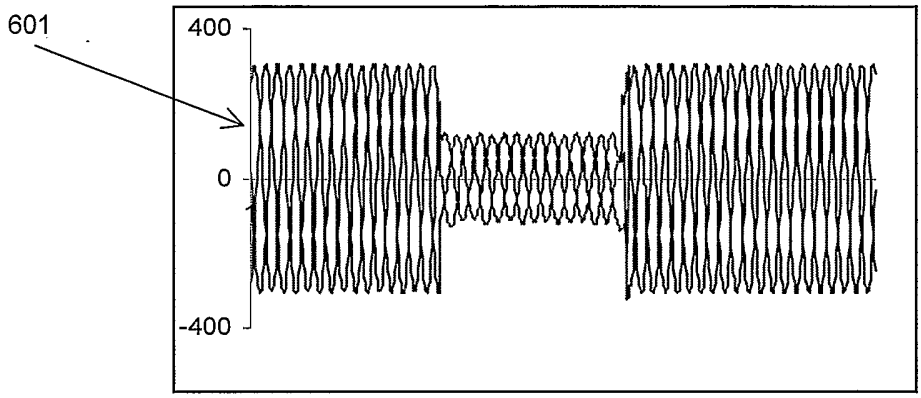

FIG. 6A

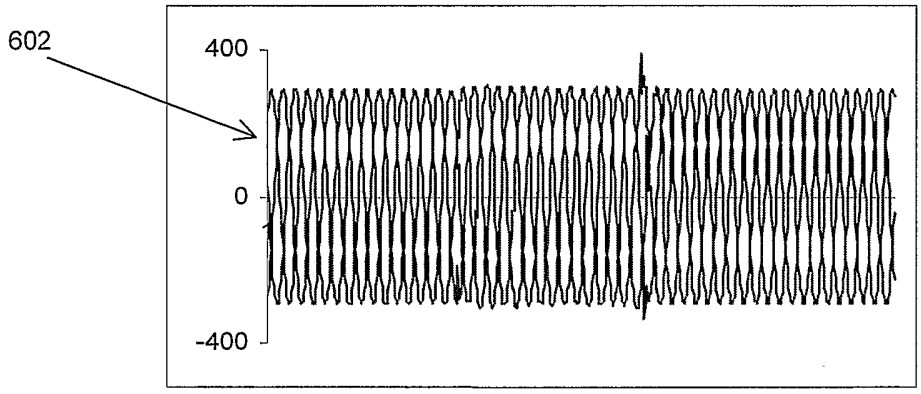

FIG. 6B

INTERNATIONAL SEARCH REPORT

Internati Application No
PCT/SG 02/00077

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H02J3/18

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H02J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CLEWING M: "STATISCHE USV IM LEISTUNGSBEREICH UNTER 6 KVA" ELEKTROTECHNISCHE ZEITSCHRIFT - ETZ, VDE VERLAG GMBH. BERLIN, DE, vol. 121, no. 3/4, February 2000 (2000-02), pages 26-28, XP000954896 ISSN: 0948-7387 the whole document ---	1,17
A	WO 01 82443 A (SINGAPORE POWER LTD) 1 November 2001 (2001-11-01) page 10, line 13 -page 21, line 30; figures 1-7 ---	1,5-10, 12,13,17
	-/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 January 2003	24/01/2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Calarasanu, P

INTERNATIONAL SEARCH REPORT

Interna Application No
PCT/ 02/00077

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	VISSER A J ET AL: "Direct-coupled cascaded multilevel sag compensator" 31ST.ANNUAL POWER ELECTRONICS SPECIALISTS CONFERENCE, vol. 1, 18 - 23 June 2000, pages 463-469, XP010517279 galway, ireland the whole document ---	1,3,5-8, 16,17
A	US 6 118 676 A (DIVAN ET AL) 12 October 2000 (2000-10-12) cited in the application the whole document -----	

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Internat - pplication No
PCT/SG 02/00077

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WO 0182443 A	01-11-2001	WO 0182443 A1	01-11-2001
		AU 4163200 A	07-11-2001
		EP 1249061 A1	16-10-2002
		TW 466391 B	01-12-2001
US 6118676 A	12-09-2000	NONE	