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(74)  
:

(54) 가

가

, 가 , ,  
2 4 1 2 ,  
.

1

1 MPU LSI(100)

2	1			(803)	.	
3	1			(804)	.	
4	1			(805)	.	
5	1		-	(806)	.	
6	1			(103)	.	
7	1			/	(101)	.
8	7			(tristate)	(203,204)	.
9	1				.	
10	7	3			.	
11	1			/	(102)	.
12a	12c	1	MPU		LSI(100)	(1,2)
13	1		MPU		LSI(100)	(3 - 9)
14					MPU	LSI(100)
15	14			/	(501)	.
16	14				(503)	.
17	14		MPU		LSI(100)	(3 - 12)
18					LSI(300)	.
19				MPU	LSI(400)	.

\* \* \*

100 :

101 : /

102 : /

103 :

( )

MPU 가 IC, (microprocessing unit; MPU)

( )

z , MPU MHz , MPU LSI , MPU LSI , MPU 3 46 - 53 MPU 가 LSI가

MPU 가 , MPU LSI (DRAM) MPU 가 LSI - M RAM

LSI , MPU 가 , MPU 가 , MPU MPU , MP U 가 MPU

LSI 가

MPU

LSI

가

MPU

LSI

( )

1 ,

가

2 ,

가 2

3 ,

4 ,

가

5 ,

가 5

6

가

1 ,

2 ,

( )

MPU

(400)

LSI

19

19 MPU  
(802) 1M × 1024  
MPU(801) 1024

LSI(400) MPU(801) (802)  
( : 1Gbits) RAM(DRAM) (802)  
(BUS<sub>0</sub> - BUS<sub>1023</sub>)

(802)  
4 S(Column Address Strobe)  
가 (n+1)  
(807)

(803), TE(Test Enable)  
(804), RAS(Row Address Strobe), CA  
WE(Write Enable), (a<sub>0</sub> - a<sub>n</sub>)  
(805), I/O<sub>1</sub> - I/O<sub>8</sub> 8 - (806),  
(SW<sub>0</sub> - SW<sub>127</sub>) BUS I/O' 1024 (128 × 8)  
" /RAS" , " /CAS" , " /WE" RAS (bar), CAS , WE  
" /"

E가 (" H" ) , MPU(801) , MPU (" L" ) , LSI(400) T TE가  
 (803) (SW<sub>0</sub> - SW<sub>127</sub>) (A<sub>0</sub> - A<sub>6</sub>) (803) TE가  
 (803) (SW<sub>0</sub> - SW<sub>127</sub>) BUS I/O' , BUS I/O' , 8 128 1024  
 (SW<sub>0</sub> - SW<sub>127</sub>) BUS I/O' , 8 128 1024 (A  
 (BUS<sub>0</sub> - BUS<sub>1023</sub>) I/O'<sub>1</sub> - I/O'<sub>8</sub> , (high) , BUS I/O' 1024  
 0 - A<sub>6</sub>) (SW<sub>i</sub>)가 (high) , BUS<sub>8</sub> I/O'<sub>1</sub>, BUS<sub>9</sub> I/O'<sub>2</sub>,...BUS<sub>1</sub>  
 5 I/O'<sub>8</sub> 8 , SW<sub>1</sub> (on) , BUS<sub>8</sub> I/O'<sub>1</sub>, BUS<sub>9</sub> I/O'<sub>2</sub>,...BUS<sub>1</sub>  
 /RAS , /CAS /WE (804) (807)  
 OE), (CLK) (807) (WE'), (D  
 ) (a<sub>0</sub> - a<sub>n</sub>) (805) (802) (  
 , 1M (802)가 1M × 1024 ( : 1Gbits)  
 , a<sub>n</sub> n 19 . 1M 2<sup>20</sup> , 20  
 8 / (I/O'<sub>1</sub> - I/O'<sub>8</sub>) - (806) I/O (I/O'<sub>1</sub> - I/O'<sub>8</sub>) /  
 MPU LSI(400) (802)  
 , SW<sub>i</sub>가 (TE) , 1024 (A<sub>0</sub> - A<sub>6</sub>) ,  
 7 (i=0,1,...127) I/O (I/O'<sub>1</sub> - I/O'<sub>8</sub>) , " 0" (all " 0" ) (BUS<sub>8i</sub> - BUS<sub>8i+</sub>  
 1" ) (a<sub>0</sub> - a<sub>n</sub>) /RAS, /CAS, /WE가 " 1" (all "  
 8 I/O'<sub>1</sub> - I/O'<sub>8</sub> .  
 (1) '0' (802) (A<sub>0</sub> - A<sub>6</sub>) 128  
 (2) , '0' , '1' ,  
 (802) (A<sub>0</sub> - A<sub>6</sub>) 128  
 (3) , '1' , '0' ,  
 (802) (A<sub>0</sub> - A<sub>6</sub>) 128  
 (4) , '0' , (802)  
 (802) (A<sub>0</sub> - A<sub>6</sub>) 128 (i 0 127  
 )

(1) (2),(3)

(4) 3 200ns (T)

$$T = 200 \text{ ns} \times 10^{-9} \times ((3 + 3) \times 1048576) \times 128 \times 161$$

, MPU LSI(400) (802) 161

, MPU LSI(400) , 161 (802)

가

1 LSI(100)가 19 MPU 가 MPU LSI(400)

1 MPU LSI(100) MPU LSI(400) M

PU(801) (802) (802) 1M  $\times 1024$  ( : 1Gbits)

RAM(DRAM) 1024 (BUS<sub>0</sub> BUS<sub>1023</sub>) (80

1) MPU(802) (802) 1G

1024

(802)

(803), 1 (Test Enable 1: TE1), 2 (Test En

able 2: TE2), RAS(Row Address Strobe), CAS(Column Address Strobe) WE(Write Enable)

4 (804), (a<sub>0</sub> - a<sub>n</sub>) 가 (n+1)

(805), I/O<sub>1</sub> - I/O<sub>8</sub> 8 (806), (807)

(SW<sub>0</sub> - SW<sub>127</sub>) BUS I/O' 1024 (128  $\times$  8)

(103), / (101) / (102)

, MPU LSI(100) 19 MPU LSI(400)

가 1 (TE1) , 2 (TE2)

(103), / (101) /

(102)가 가

1 (TE1) 1 TE1 (" H" )

MPU LSI(100) 1

2 (TE2) 2 TE1 (" H" )

, MPU LSI(100) 2

가 TE1, TE2가 ("

L" ) , MPU LSI(100)

MPU LSI(100)

(1) , 2 (TE2)가 , MPU LSI(100) 2

가 (802)

(2) MPU (802) LSI(100) 2 , 2 (TE2)가 ,  
 가 .

(3) 가 가 , 2 (TE  
 2) (" L" ) , MPU LSI(100) (" H" ) , 1  
 , 1 (TE1) (" H" ) , 1  
 , MPU LSI(100)  
 , 1 (TE1), 2 (TE2), /RAS , /CAS , /WE  
 (804) 3 2  
 (804) 1 (TE1) 2 (TE2)  
 1 (TE1') 2 (TE2')  
 , (803) 2 (A<sub>0</sub> - A<sub>6</sub>)  
 (803) 7 - (A<sub>0</sub> - A<sub>6</sub>)  
 (A<sub>0</sub> - A<sub>6</sub>) (/A<sub>0</sub>' - /A<sub>6</sub>')  
 4) 1 (/A<sub>0</sub>' - /A<sub>6</sub>') (80  
 /A<sub>6</sub>) (SW<sub>0</sub> - SW<sub>127</sub>) (SW<sub>0</sub> - SW<sub>127</sub>) (/A<sub>0</sub>' - /A<sub>6</sub>') (/A<sub>6</sub>' -  
 (A<sub>0</sub> - A<sub>6</sub>) (SW<sub>0</sub> - SW<sub>127</sub>) (SW<sub>0</sub> - SW<sub>127</sub>) (SW<sub>0</sub> - SW<sub>127</sub>)  
 (SW<sub>0</sub>) (A<sub>0</sub> - A<sub>6</sub>) '0000000' (SW<sub>0</sub> - SW<sub>127</sub>)  
 - SW<sub>127</sub>) (SW<sub>1</sub>) (A<sub>0</sub> - A<sub>6</sub>) '1000000' (SW<sub>0</sub>)  
 (SW<sub>0</sub> - SW<sub>127</sub>) (SW<sub>127</sub>) (A<sub>0</sub> - A<sub>6</sub>) '1111111'  
 (803) (SW<sub>0</sub> - SW<sub>127</sub>) BUS I/O' (SW<sub>0</sub> - SW  
 , BUS I/O' , 8 128 1024 (BUS<sub>0</sub> -  
 127 ) BUS I/O' I/O (I/O<sub>1</sub>' I/Q<sub>8</sub>') , BUS I/O' 102  
 4 (A<sub>0</sub> - A<sub>6</sub>) (SW<sub>i</sub>) (TE1') , SW  
 1 (" H" ) , SW<sub>1</sub> 8 , , BUS<sub>8</sub> I/O<sub>1</sub>' , BUS<sub>9</sub> I  
 /O<sub>2</sub>' , .... BUS<sub>15</sub> I/O<sub>8</sub> ( 8 ) , ,  
 9 BUS I/O' . 9 BUS I/O'  
 - " a" , " b" , (SW<sub>0</sub> - SW<sub>127</sub>) 가 " c" , 9  
 , a b  
 /RAS , /CAS , /WE (804) (807)  
 , (807)가 (WE') , (DOE),  
 (CLK)

$(a_0 - a_n)$  (805) 4 (802) (CLK) (a<sub>i</sub>)  
 ) . 가 . (a')  
 (802) , 1M × 1024 ( : 1G )  
 , 1M (a<sub>0</sub>' - a<sub>n</sub>') . 1M 2<sup>20</sup> , 20  
 , a<sup>n</sup> n 19 . , DRAM  
 , 10 . n 9 .  
 I/O (I/O<sub>1</sub>' - I/O<sub>8</sub>') 5 - (806) I/O (I/O<sub>1</sub> - I/O  
 8) . 5 , - (806) (DOE)  
 , (WE') 가 . (WE')  
 (DOE) (tristate) ,  
 , 6 (103) (803) (A<sub>0</sub>' - A<sub>6</sub>')  
 , (A<sub>0</sub>" - A<sub>6</sub>" ) (S0 - S127) 6  
 , A<sub>i</sub>" , /A<sub>i</sub>" . 6 NAND  
 (" H" ) , A<sub>i</sub>'가 (" H" )  
 (" L" ) , A<sub>i</sub>'가 (" L" ) , A<sub>i</sub>"  
 , A<sub>0</sub>'가 A<sub>i</sub>'가 , A<sub>0</sub>" 가 , /A<sub>0</sub>"  
 /A<sub>i</sub>" /A<sub>i</sub>" (A<sub>1</sub>' - A<sub>6</sub>')  
 N - (MOS) , MN410 - MN460, MN411 - MN461, ..., M  
 N41127 - MN46127 (A<sub>0</sub>" )가, (A<sub>0</sub>')  
 N - MOS , MOS (MN400, MN402, MN404, ...  
 MN40126) , (/A<sub>0</sub>" ) , , MOS (   
 MN401, MN403, ..., MN40127) (S0 - S127) ,  
 S0,S2,S4, ..., S126 , S1,S3, ..., S127 .  
 (MN400 - MN40127) . A<sub>0</sub>" /A<sub>0</sub>" 6 , N - MOS  
 (" L" ) , MN400 , MN401 , A<sub>0</sub>" 가 (" H" ) /A<sub>0</sub>" 가  
 MN40127 . P - MOS MP400 ON - 7 N - M  
 OS (MN400, MN410, MN420, ..., MN460) ON -  
 , S1 (" H" ) , S2 , S126 , S0가 (" L" )  
 . , 2 (LHLHLH...LHLH) , S127  
 가 , A<sub>1</sub>'가 , A<sub>1</sub>'(i-1)가 , A<sub>1</sub>"  
 , A<sub>1</sub>"(i-1) , /A<sub>1</sub>" 가 , /A<sub>1</sub>"  
 , S1 , S2 , S126 , S127 .  
 , 4 " LLHLLHH...LLHH"  
 가 , " A<sub>i</sub>" " i" 가 가 , 8,16... , " i" 가 6 , 128  
 " LLLLL - - LLHH - - HHHH" (L 64 H 64 ) .  
 (103) (A<sub>0</sub>' - A<sub>6</sub>') " 0000000" ,  
 (S0 - S127) .



, 2 (202)가 (TE2')가 (WE')  
 , (BUS<sub>i</sub>' ) (i=0,1,2,...,126,127) (201)가 OR  
 (N202) 10 , BUS<sub>0</sub>' - BUS<sub>27</sub>' 가 ( (N202) , , BUS<sub>0</sub>' - BUS  
 127 ' (N202) (202)가  
 (BUS<sub>i</sub>' ) (i=0,1,2,...,126,127) / (102)  
 , MPU LSI(100) 128 / (102)가  
 1 , (102)가  
 / (102) 8 (BUS<sub>i</sub> - BUS<sub>i+7</sub> )  
 , 1 (BUS<sub>0</sub>' ) / (102)  
 (BUS<sub>0</sub> - BUS<sub>7</sub>) (BUS<sub>127</sub>' ) / (102)  
 (BUS<sub>1016</sub> - BUS<sub>1023</sub> )  
 11 / (102) 11  
 / (102) 2 (TE2') (WE')  
 , / (102)  
 , / (102)가  
 BUS 8 (BUS<sub>0</sub>' )  
 / (102) 8 (BUS<sub>0</sub> - BUS<sub>7</sub>) (BUS<sub>0</sub>' )  
 / (102)가 8  
 ) , (N301) (202) ( (N301) , , 8  
 가 (N301) , , 8  
 MPU LSI(100)  
 , MPU (100) LSI  
 (1) 2 (TE2)가 , (802) 가  
 (2) (802) , 2 (TE2)  
 가 가  
 (3) 가 가 , 1 (TE1)  
 , 12 (1) , 2 (TE2)  
 (802)

LSI(100)가 (A<sub>0</sub>" - A<sub>6</sub>" ) (/A<sub>0</sub>" - /A<sub>6</sub>" ) (TE2) MPU (A<sub>0</sub> - A<sub>6</sub>) (WE) MPU LSI(100) 2 (S0 - S127)

(806) I/O<sub>1</sub>' ( 12a - 12c (1)). I/O<sub>1</sub>'가 (101) (BUS<sub>0</sub>' - BUS<sub>27</sub>' )

(102) (BUS<sub>0</sub> - BUS<sub>1023</sub> ) / (102) (a<sub>0</sub> - a<sub>n</sub>) " 0" " 1"

(a<sub>0</sub> - a<sub>n</sub>) (WE)가 (802) 가 (BUS<sub>0</sub> - BUS<sub>1023</sub> ) 가 (102) / (101) I/O (I/O<sub>1</sub>)

(BUS<sub>0</sub> - BUS<sub>1023</sub> ) 가 (102) / (102) I/O (I/O<sub>1</sub>) ( 12a 12b (1))

(BUS<sub>0</sub> - BUS<sub>1023</sub> ) 가 (BUS<sub>0</sub>' - BUS<sub>27</sub>' ) (102) / (101) I/O (I/O<sub>1</sub>) 가 (a<sub>0</sub> - a<sub>n</sub>) 0 ( 12c (1)).

(a<sub>0</sub> - a<sub>n</sub>) '0' '1'

가 I/O<sub>1</sub> (1) 가 ( 12a - 12c (2)). 가 I/O (I/O<sub>1</sub>) ( 12a c (2)). ( 12b (2)). (a<sub>0</sub> - a<sub>n</sub>) '0' '1'

(802)가 (802)가 200ns

$$T = 200\text{ns} \times 10^{-9} \times ((1 + 1) \times 1048576) \times 2 = 0.8(\text{s})$$

, MPU LSI(10) (802) ,  
 0.8 가 .

(3-9) (802) , 13  
 (2)가 .

가 (1) (12b)가

13 (2) 2 (TE2)  
 (WE) MPU LSI(100) MPU LSI(100)  
 2 , '1000000' (3)가 (A<sub>0</sub> - A<sub>6</sub>)  
 , (S<sub>0</sub> - S<sub>127</sub>) 13 , "LHLHLHLHL...LHLH" 가 .

I/O<sub>1</sub> , I/O<sub>1</sub>'가 - (806)  
 (BUS<sub>0</sub>' - BUS<sub>27</sub>' ) "LHLHLHLHL...LHLH" / (101)

/ (101)

/ (102)

(BUS<sub>0</sub> - BUS<sub>1023</sub> ) "LLLLLLLLHHHHHHHHLL,....,HHHH" ,

8

(a<sub>0</sub> - a<sub>n</sub>) '0' '1' . (BUS  
 - BUS<sub>7</sub>, BUS<sub>16</sub> - BUS<sub>23</sub>, BUS<sub>32</sub> - BUS<sub>39</sub>, ....)  
 (BUS<sub>8</sub> - BUS<sub>15</sub>, BUS<sub>24</sub> - BUS<sub>31</sub>, BUS<sub>40</sub> - BUS<sub>47</sub>, ....)

(WE) (802) 가 . ,  
 (a<sub>0</sub> - a<sub>n</sub>) '0' , (BUS<sub>8</sub> - BUS<sub>1023</sub> ) 가  
 / (102) / (101) I/O (I/O<sub>1</sub>) .

가 (BUS<sub>0</sub> - BU  
 S<sub>7</sub>, BUS<sub>16</sub> - BUS<sub>23</sub>, BUS<sub>32</sub> - BUS<sub>39</sub>, ....)  
 가 (BUS<sub>8</sub> - BUS<sub>15</sub>, BU  
 S<sub>24</sub> - BUS<sub>31</sub>, BUS<sub>40</sub> - BUS<sub>47</sub>, ....)  
 가

(BUS<sub>8</sub> - BUS<sub>15</sub>, BUS<sub>24</sub> - BUS<sub>31</sub>, BUS<sub>40</sub> - BUS<sub>47</sub> ....) 가  
 /

(102) (BUS<sub>1</sub>' , BUS<sub>3</sub>' , BUS<sub>5</sub>' , ... BUS<sub>127</sub>' )  
 / (101)

(BUS<sub>8</sub> - BUS<sub>15</sub>, BUS<sub>24</sub> - BUS<sub>31</sub>, BUS<sub>40</sub> - BUS<sub>47</sub>, ....) 가  
 , 13

(3)

가 (4-9) (4) '0100000'  
 (A<sub>0</sub> - A<sub>6</sub>) (S<sub>0</sub> - S<sub>127</sub>) " LLHHLHH...LLHH" 가 (5)  
 '0010000' (A<sub>0</sub> - A<sub>6</sub>) (S<sub>0</sub> - S<sub>127</sub>) " LLLL  
 HHHHL...HHHH" 가

(4) (BUS<sub>0</sub> - BUS<sub>15</sub>, BUS<sub>32</sub> - BUS<sub>47</sub>, ...)  
 가 (BUS<sub>15</sub> - BUS<sub>31</sub>, BUS<sub>48</sub> - B  
 US<sub>63</sub>, ...)

(9) (BUS<sub>0</sub> - BUS<sub>1023</sub>)

13 (3,5) (3,5)  
 가 '1010000' 가 '1000000' '0010000'  
 BUS<sub>40</sub> - BUS<sub>47</sub>)

b)가 (1) (12)  
 (12c), (2) I/O<sub>1</sub> 가 가  
 (BUS<sub>0</sub> - BUS<sub>1023</sub>)

(802) 가 (1,2) (3-9)

가 (TE1) (3) (1-9)

(full test) 가 (BUS<sub>5</sub>)  
 (3)

2 (TE2) (TE1)  
 (803) (A<sub>0</sub> - A<sub>1</sub>) '1010000'  
 SW<sub>5</sub> SW<sub>i</sub> BUS<sub>40</sub> I/O<sub>1</sub> BUS<sub>41</sub> I/O<sub>2</sub>  
 , BUS<sub>42</sub> I/O<sub>3</sub> , ..., BUS<sub>47</sub> I/O<sub>8</sub> BUS<sub>40</sub> - BUS<sub>47</sub> I/O  
 I/O<sub>1</sub> - I/O<sub>8</sub> (a<sub>0</sub> - a  
 n) '0' '1' (BUS<sub>40</sub> - BUS<sub>47</sub>)

(full test) MPU LSI(400) , /RAS, /CAS, /WE가  
 I/O<sub>1</sub> - I/O<sub>8</sub> (a<sub>0</sub> - a<sub>n</sub>)가 '0' '1'  
 8

- (1) '0'가
- (2) , '0' , '1'
- (3) , '1' , '0'
- (4) , '0' , (1) , 3 (2),(3) , (4) , 3 (T)

$$T = 200\text{ns.} \times 10^{-9} \left( (1 + 1) \times 1048576 \right) \times 9 + 200\text{ns.} \times 10^{-9} \times ((3 + 3) \times 1048576) \times 1$$

MPU , MPU LSI(100) , (802) (T) 5 가 , MPU LSI(400) 161

0.8 5 (101) / (102) (103), /

14 - 17 MPU LSI(200)가

MPU LSI(100) , LSI(200) , / (102) MPU / (501) , (503)가 가 (101) / MPU 8 - LSI(100) , 7

MPU LSI(200) 16 (A<sub>N</sub>) , '1010000000' A<sub>IN</sub> (807) , (CLK)가 /RAS (trailing edge) ( ) 16 (shift) , '1010000000' A<sub>N</sub> , '1010000000' (503) (A<sub>0</sub> - A<sub>9</sub>)가 (5 (A<sub>0</sub>' - A<sub>9</sub>' )

$(A_0' - A_4')$  (503)  $(A_0' - A_9')$  (504 - 2)  
 $(A_5' - A_9')$  (504 - 1) , (504 - 2)  
 $(A_0' - A_4')$  (504 - 1) , (504 - 2)  
 $(A_5' - A_9')$  (503)  
 NAND (502)  
 $(A_0' - A_9')$  (502)  
 $(A_0'' - A_9'')$ ,  $(A_0'' - A_9'')$  (103) (S0,S  
 LSI(100)  
 $(A_0' - A_9')$  (101) (S0 - S1023),  
 (WE') 2 (TE2') / (101) (WE')가 / (101) 2  
 (TE2') (WE')가 (WE')가  
 / (101) / (101)  
 (TE2')가 (WE')가  
 (601) (602) 2  
 (TE2')가 (WE')가 (202)  
 (201)  
 (TE2')가 (WE')가 (N6  
 01) / (501) / (101) / (BUS<sub>0</sub>,  
 (501) (601) / (101)  
 BUS<sub>1</sub>, BUS<sub>2</sub>, ..., BUS<sub>1022</sub>, BUS<sub>1023</sub>)  
 TE2가 WE가 가  
 (BUS<sub>i</sub>) (i=0,1,2,...,1022,1023)  
 OR (N620,N621,M622,...,N621022,N621023)  
 OR OR  
 (602) 15 (N602)  
 N620 - N621023 (N602)  
 N620 - N621023 (N602)  
 (602) ( )  
 / (501) / 가  
 (on)(TE2가 , WE'가 ) I/  
 (806) (601)  
 , BUS<sub>0</sub> , BUS<sub>1</sub> , BUS<sub>2</sub> , ....., BUS<sub>1022</sub>  
 , BUS<sub>1023</sub> (802)  
 (a<sub>0</sub> - a<sub>n</sub>: ) (a<sub>0</sub> - a<sub>n</sub>: )

(TE2가 , WE'가 ) . 2  
 , BUS<sub>1</sub> , BUS2 ,.....,BUS<sub>1022</sub> , BUS<sub>0</sub>  
 가 2 (Si) " i" 가 , BUS<sub>1023</sub>  
 (602) , " i" 가  
 , 1024 (N601 - N621023) .  
 OR (tree) (N602) , I/O' I/O  
 / (501) 가 ,  
 (4,8,...) .  
 , 17 (802) 가 , 1  
 , BUS<sub>5</sub> (BUS<sub>5</sub>) , BUS<sub>5</sub> , S5가  
 (602) (N625)( , S5 ,  
 )  
 , 1023 (N620 - N624),(N626 - N621023)  
 I/O , OR (602) , I/O' ,  
 MPU LSI(200) MPU LSI(100)  
 . ,  
 (1) 2 (TE2)가 , (802) 가  
 .  
 (2) (802) , 가 .  
 (3) 가 가 , 1 (TE1)  
 가 .  
 (1),  
 ( 1) , ( 2) , M  
 PU (100) LSI .  
 , (802) ,  
 .  
 , (802) , 17  
 (3 - 12) , 2,4,8,....,1024 A<sub>IN</sub>  
 (A<sub>0</sub> - A<sub>9</sub>) (502) ,  
 , MPU LSI(100) , BUS<sub>5</sub> , 17  
 , 가 , 12  
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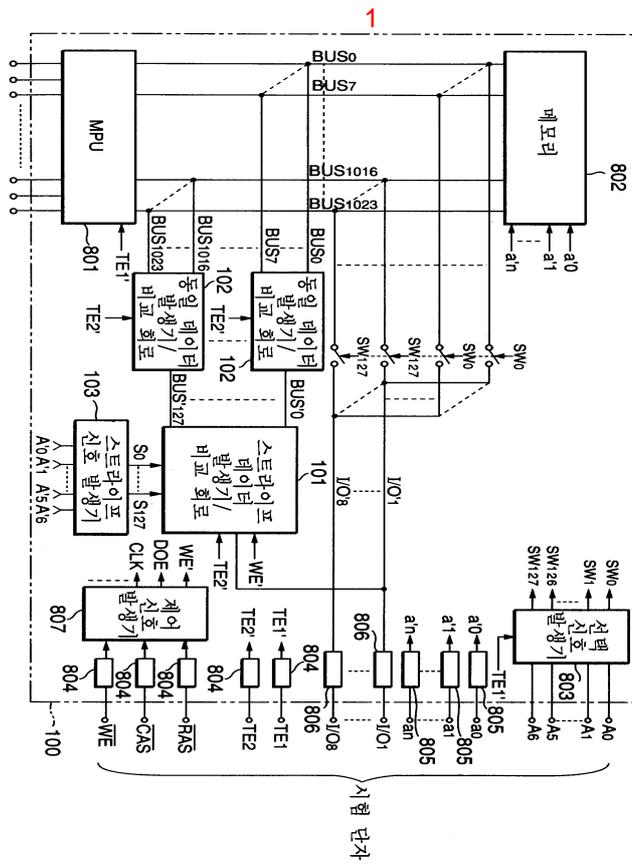
17.

16

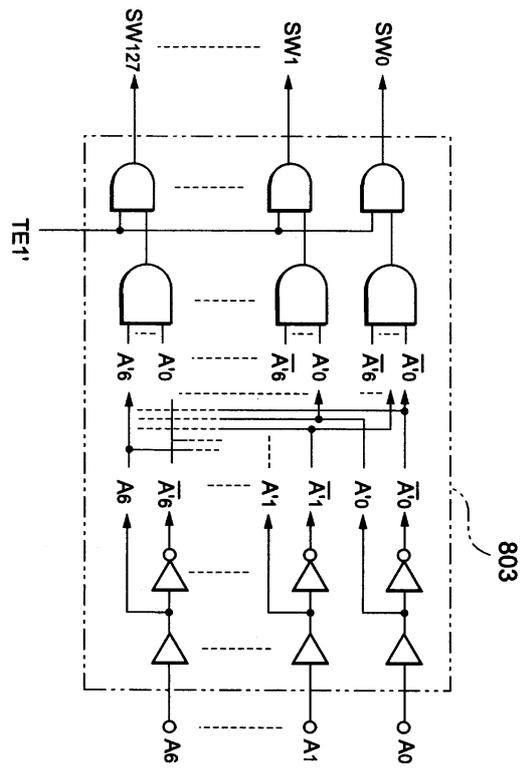
18.

17

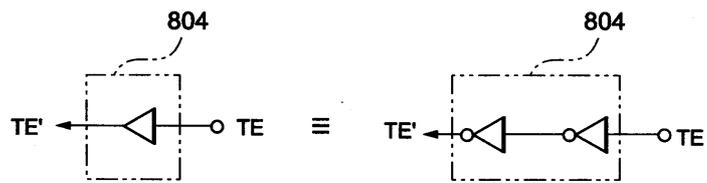
(indication)



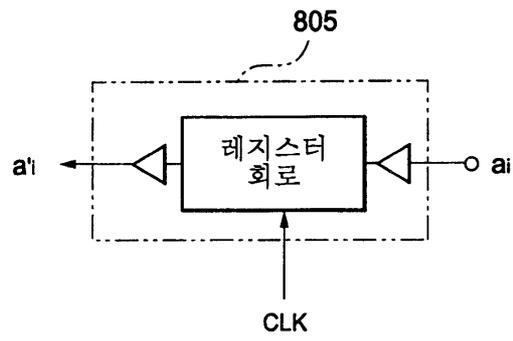
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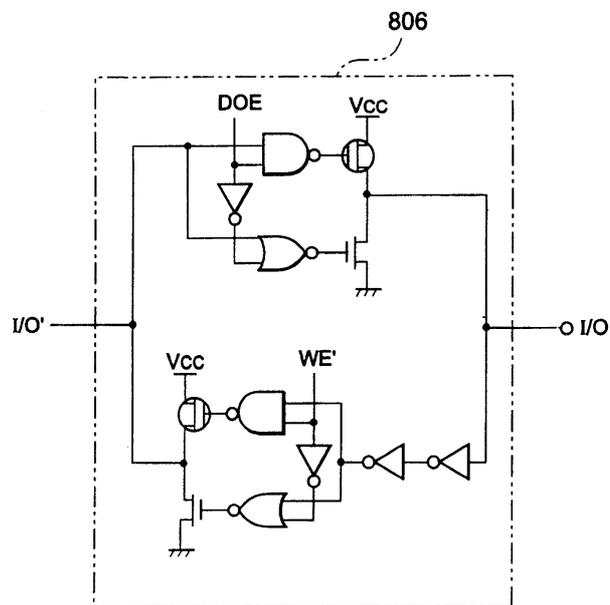
3



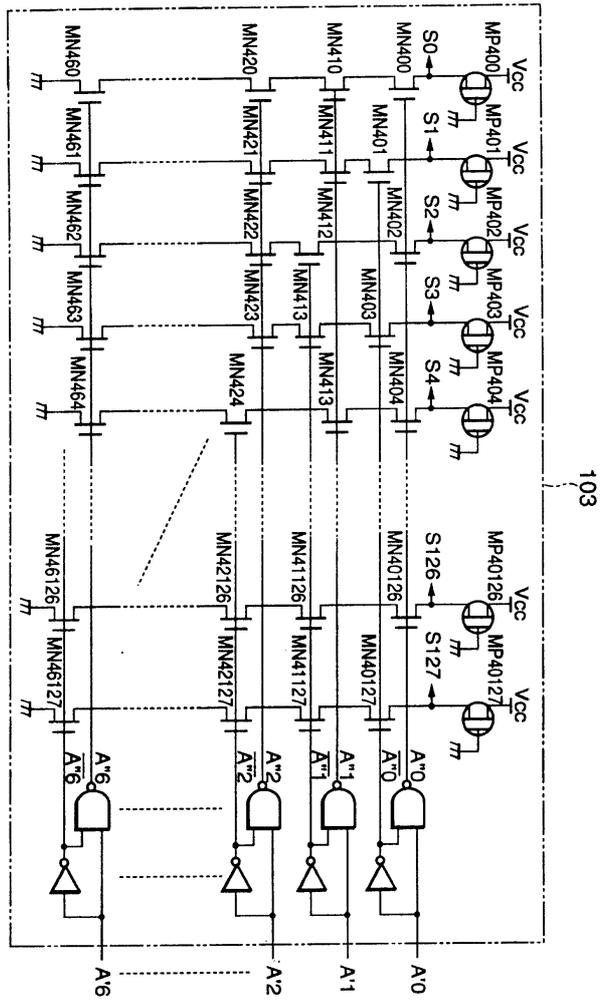
4



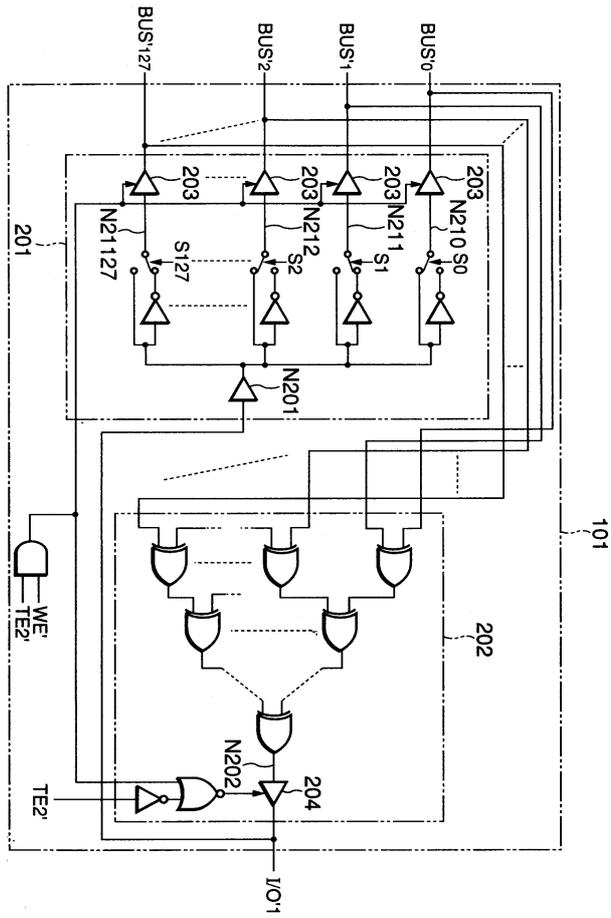
5



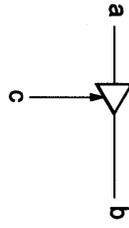
6



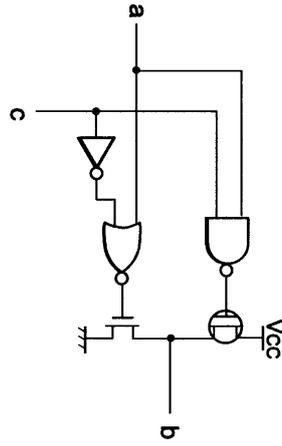
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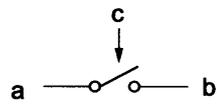
8



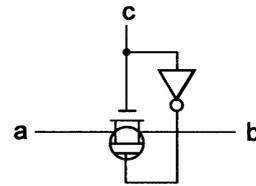
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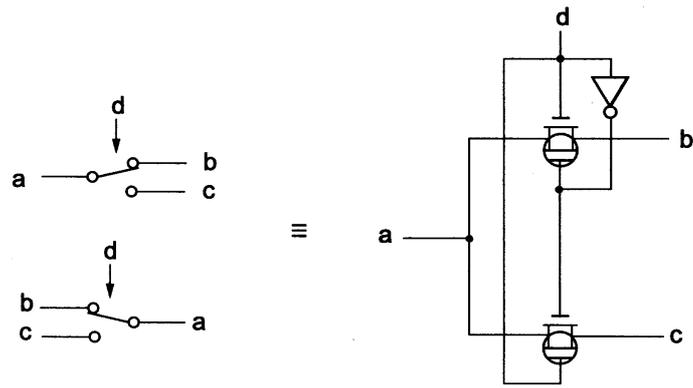
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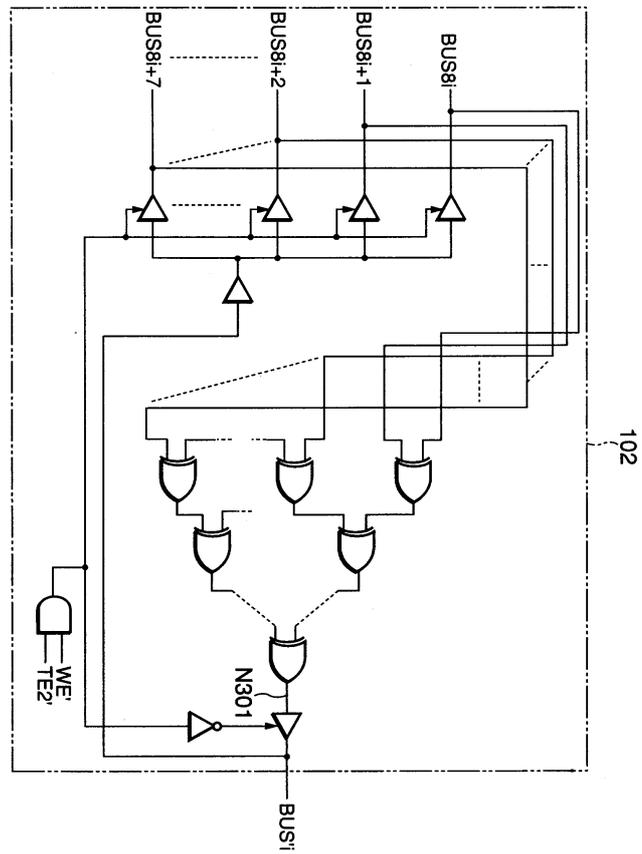
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## 12a

시험 패턴 번호	블록 어드레스 (A0-A6)	스트라이프 신호 패턴(S0-S127)	I/O1 (입력)	I/O1 (판독)
1	0000000	LLLLLLLLLLLLLLLLLLLL.....LLLLLLLLL	L	L
2	0000000	LLLLLLLLLLLLLLLLLLLL.....LLLLLLLLL	H	L

## 12b

시험 패턴 번호	블록 어드레스 (A0-A6)	스트라이프 신호 패턴(S0-S127)	I/O1 (입력)	I/O1 (판독)
1	0000000	LLLLLLLLLLLLLLLLLLLL.....LLLLLLLLL	L	L
2	0000000	LLLLLLLLLLLLLLLLLLLL.....LLLLLLLLL	H	H

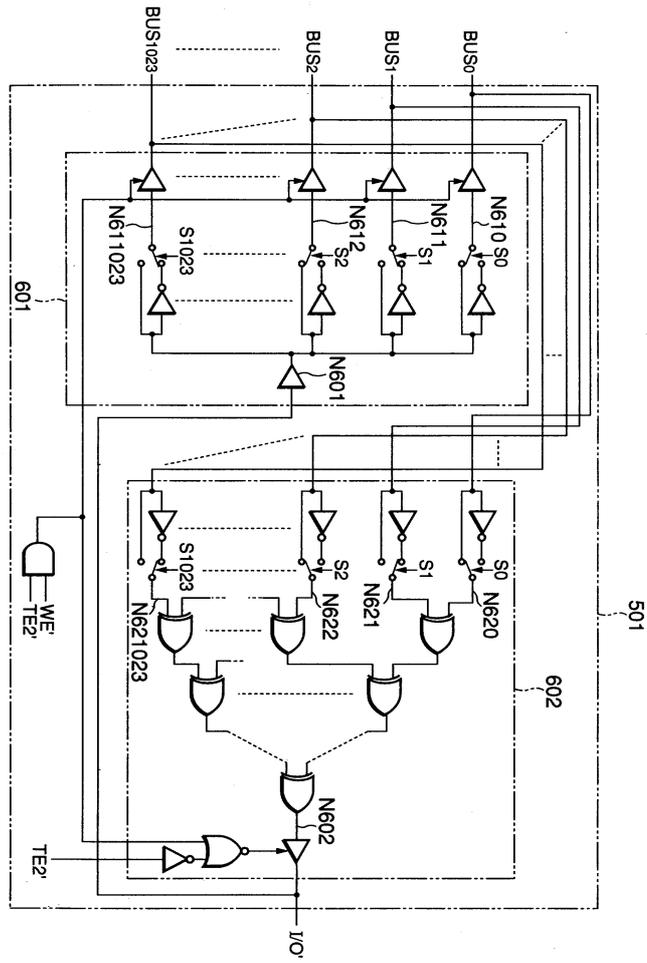
## 12c

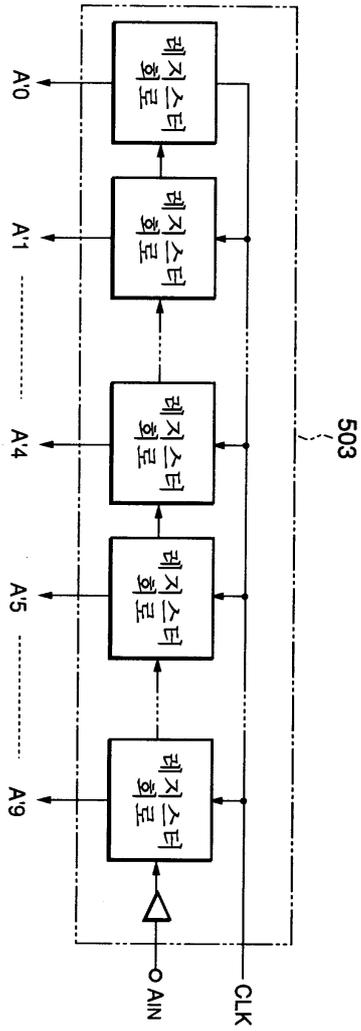
시험 패턴 번호	블록 어드레스 (A0-A6)	스트라이프 신호 패턴(S0-S127)	I/O1 (입력)	I/O1 (판독)
1	0000000	LLLLLLLLLLLLLLLLLLLL.....LLLLLLLLL	L	H
2	0000000	LLLLLLLLLLLLLLLLLLLL.....LLLLLLLLL	H	L

시험 패턴 번호	블록 아이디레스 (A0-A6)	스트라이프 신호 패턴 (S0-S127)	I/O1 (입력)	I/O1 (반동)
3	1000000	LHLHLHLHLHLHLHL.....LHLHLHL	L	H
4	0100000	LHLHLHLHLHLHLHL.....LLHLLHL	L	L
5	0010000	LLLLHHHLLLLLHHHL.....LLLLHHH	L	H
6	0001000	LLLLLLLLLHHHHHHHL.....HHHHHHH	L	L
7	0000100	LLLLLLLLLLLLLLLLLH.....HHHHHHH	L	L
8	0000010	LLLLLLLLLLLLLLLLL.....HHHHHHH	L	L
9	0000001	LLLLLLLLLLLLLLLLL.....HHHHHHH	L	L



15





시험 패턴 번호	블록 어드레스 (A0-A9)	스트라이프 신호 패턴 (S0-S1023)	I/O: (입력)	I/O: (반동)
3	1000000000	LHLHLHLHLHLHL.....LHLHLHL	L	H
4	0100000000	LHHLHLHLHLHLHL.....LHHLHLH	L	L
5	0010000000	LLLLHHHLHLHLHL.....LLLLHHH	L	H
6	0001000000	LLLLLLLLHHHHHHHL.....HHHHHHH	L	L
7	0000100000	LLLLLLLLLLLLLLLL.....HHHHHHHH	L	L
8	0000010000	LLLLLLLLLLLLLLLL.....HHHHHHHH	L	L
9	0000001000	LLLLLLLLLLLLLLLL.....HHHHHHHH	L	L
10	0000000100	LLLLLLLLLLLLLLLL.....HHHHHHHH	L	L
11	0000000010	LLLLLLLLLLLLLLLL.....HHHHHHHH	L	L
12	0000000001	LLLLLLLLLLLLLLLL.....HHHHHHHH	L	L



