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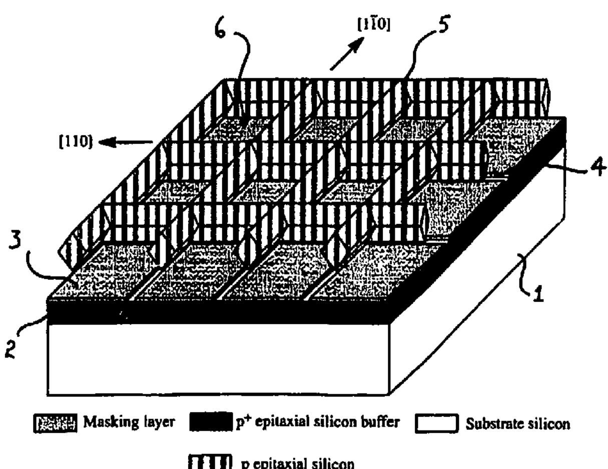
(54) Title: A METHOD OF PRODUCING THIN SILICON FILMS



(57) Abstract

A method of producing thin single crystal silicon films (5). The method includes forming a single crystal substrate (1), depositing or forming a thin single crystal silicon film (5) having the same crystal orientation as said substrate in, on or adjacent to the substrate (1) and providing a plurality of spaced apart etchant access regions (6) through the film (5) or substrate (1). Liftoff of the film (5) is effected by simultaneous etching via the etchant access regions (6). The amount of etching required and the degree of access for etchant provides for detachment without significant degradation of film (5).

A METHOD OF PRODUCING THIN SILICON FILMS

FIELD OF THE INVENTION

This invention relates to an improved method of production of single crystalline layers of silicon of arbitrary size and shape, suitable for processing into silicon solar cells and other semiconductor devices.

BACKGROUND ART

Silicon films several tens of microns thick are an excellent material on which to fabricate highly efficient solar cells. For the highest solar cell conversion efficiency (ie. the maximum conversion of solar radiation input into electric power output) the silicon material should be single crystalline, or the grains of the multicrystalline material should be as large as possible.

Single crystal silicon can be obtained by the Czochralski (Cz) or floating zone (FZ) techniques, while large grained multicrystalline silicon can be obtained by casting techniques. All these methods produce large blocks of silicon which have to be sliced to produce wafers suitable for solar cells. Half the silicon is wasted as sawdust during slicing. The wafers are expensive and usually several hundred microns thick.

A procedure is in use for gallium arsenide devices, which relies on the large selectivity of some etchants for AlAs over GaAs and some AlGaAs compounds. AlGaAs is grown on a GaAs wafer followed by GaAs and/or AlGaAs. Black wax applied to the upper GaAs/AlGaAs layer places it under tension. The structure is then immersed in a suitable etchant, which etches AlAs laterally without significantly etching the GaAs or AlGaAs layers. After a long period the top GaAs layer floats off. The process is not suitable for silicon because no known silicon etchant has the large selectivity that is available for the GaAs/AlAs system. To date, no suitable non-silicon compound has been developed that can act as an intermediary layer, analogous to AlAs. Although CaF_2 can be deposited epitaxially on silicon, and silicon on CaF_2, the procedure is not well developed and expensive, and silicon grown

on CaF_2 has a very high defect density.

In another procedure, known as the CLEFT process, a masking layer is deposited on a single crystal substrate, usually GaAs. Line openings formed in the masking layer provide the seeds for subsequent epitaxial growth. The epitaxial layers overgrow the line seed openings laterally and eventually impinge on each other to produce a continuous epitaxial film. The masking layer is completely buried beneath the epitaxial layer. The epitaxial layer is then attached to a suitable secondary substrate. If the regions where the epitaxial layer is attached to the substrate are sufficiently narrow, and if the adhesion of the epitaxial layer to the masking layer is sufficiently weak, the epitaxial layer can be cleaved off the substrate. The process has not been successfully applied to silicon.

A procedure known as zone melting recrystallization (ZMR) process has been applied to silicon. In this process, a thin layer of amorphous or microcrystalline silicon is deposited on a foreign substrate which is capable of withstanding high temperatures, and then recrystallized by zone melting the silicon using strip heaters. Then, a thicker silicon layer is grown epitaxially on the recrystallised, multicrystalline silicon. In the case where an oxidised silicon wafer serves as the substrate, via holes can be etched in the epitaxial silicon layer following growth in order to access the oxide separating the epitaxial layer and the substrate. HF can then be made to enter into the holes and etch away the oxide, eventually lifting off the silicon substrate, ready for re-use. The disadvantages of the ZMR approach are that an expensive, high temperature zone-melting recrystallization step is needed and that the epitaxial layers are multicrystalline.

DISCLOSURE OF THE INVENTION

It is an object of this invention to provide a method of producing thin silicon epitaxial films.

Accordingly, this invention provides a method of producing thin single crystal silicon films, said method including the steps of:

forming a single crystal substrate;

depositing or forming a thin single crystal silicon film having the same crystal orientation as said substrate in, on or adjacent to said substrate, the thin single crystal silicon film disposed for liftoff from the substrate;

providing a plurality of spaced apart etchant access regions through said thin single crystal silicon film or substrate; and

causing liftoff of said thin single crystal silicon film by etching via said etchant access regions through said single crystal substrate and/or said thin single crystal silicon film, the amount of etching required and the degree of access for etchant providing for

AUSTRALIAN PATENT OFFICE

detachment of said thin single crystal silicon film without significant degradation of said thin single crystal silicon film.

In a first form of the invention there is provided a method of producing thin single crystal silicon films, said method including the steps of:

5 forming a single crystal substrate;

depositing or forming a thin single crystal silicon film having the same crystal orientation as said substrate in, on or adjacent to said single crystal substrate, the thin single crystal film disposed for liftoff from the substrate;

providing a plurality of spaced apart etchant access regions through said thin 10 single crystal silicon film or substrate;

epitaxially growing or forming between said single crystal substrate and said thin single crystal silicon film a buffer layer of silicon having the same crystal orientation as said single crystal substrate and containing concentrations of impurities resulting in the buffer layer having a significantly faster etch rate in a selected etchant than either said 15 thin single crystal silicon film or said substrate; and

causing liftoff of said thin single crystal silicon film by etching said buffer layer through said etchant access regions, the amount of etching required and the degree of access for etchant providing for detachment of said thin single crystal silicon film without significant degradation of said thin single crystal silicon film.

20 In a second form of the invention an etch stop layer of silicon having the same crystal orientation as the substrate and containing concentrations of impurities which result in the etch stop layer having a significantly slower etch rate in a selected etchant than the silicon of the substrate or film, is epitaxially grown or formed on or in the substrate or film to define the etchant access regions.

25 In a third form of the invention a masking layer of non silicon material is deposited and patterned on the substrate to define attachment regions of exposed substrate, the attachment regions having at least one dimension small in comparison to spacings between adjacent regions, and the film is deposited on the substrate at the attachment regions.

30 Where a buffer layer is epitaxially grown or formed in the first form of the invention a masking layer of non silicon material is preferably deposited and patterned on the substrate or buffer layer to define attachment regions of exposed substrate or buffer layer. Preferably, the masking layer is deposited and patterned on a surface of the substrate, followed by deposition of the buffer layer at the attachment regions and the film 35 is then deposited on the buffer layer. The substrate can be formed with a plurality of

AUSTRALIAN PATENT OFFICE

apertures extending through the entire thickness of the substrate. The apertures can be formed by means of reactive ion etching or laser ablation.

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Alternatively, the buffer layer is formed or deposited on or in the substrate, the masking layer is deposited and patterned on the buffer layer, the film is deposited on the buffer layer at the attachment regions, and the masking layer is removed prior to liftoff of said film.

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In another alternative, the method can include the further steps of depositing the film by chemical vapour deposition so that polycrystalline silicon is deposited on said masking layer and subsequently removing the polycrystalline silicon in an etchant which does not significantly attack the single crystal layers constituting the substrate, buffer and film, the

10 removal of the polycrystalline film and the removal of said masking layer creates the etchant access regions.

In another alternative, the buffer layer is formed or deposited substantially continuously over a surface of the substrate, the film is deposited on the buffer layer and the

15 etchant access regions are formed through the film. In this form of the invention, the buffer layer is preferably doped p type to a concentration of about 5×10^{19} cm^{-3} and the anisotropic etchant is ethylenediamine procatechol.

In some forms of the methods of this invention the buffer layer can be formed by

20 selectively doping the surface of the substrate. In other forms of the invention the buffer layer is deposited on a surface of the substrate.

In the second form of the invention it is preferred that a masking layer of non silicon material is deposited and patterned on the substrate to define attachment regions of exposed

25 substrate, the film is subsequently deposited on the substrate at the attachment regions and at least part of the masking layer is removed prior to liftoff of the film. Preferably, the film is deposited on the substrate such that holes remaining in the film following deposition form at least part of the etchant access regions.

30 In one alternative the film forms said etch stop layer. In a variation the etch stop layer

can be formed or deposited in or on the film to protect a corresponding part of said film from being etched during selective etching to effect liftoff of the film. Preferably, the etch stop layer is formed by means of a phosphorus diffusion into the film.

5 In an alternative in accordance with the second form of the invention the film is formed in the substrate by selectively doping part of the substrate with a suitable dopant, the film acting as an etch stop layer during subsequent etching to effect liftoff of the film with those regions of the substrate not doped forming the plurality of etchant access regions. In this alternative the substrate is preferably p type and said film is preferably n type and the 10 liftoff is effected by electrochemical etching in an aqueous, hydrofluoric acid containing etchant which does not significantly etch n type silicon. The etch stop layer preferably is formed by means of a phosphorus diffusion into the substrate. Preferably, an epitaxial layer is grown on the film following liftoff but prior to final detachment of the film from the substrate.

15

In another alternative of the second form of the invention the film is formed from part of the substrate. In this alternative the invention preferably includes the further steps of forming blind access apertures in the substrate, doping the exposed aperture surfaces of the substrate to form a doped lining layer, removing the lining layer at the blind end of the 20 apertures to expose the substrate and etching the substrate to provide for liftoff of the film, the doped lining layer forming part of the film and acting as an etch stop layer during the etching to provide for liftoff of the film. Preferably, the substrate is p type and the lining layer is n type and liftoff is effected by electrochemical etching in an aqueous, hydrofluoric acid containing etchant which does not significantly etch n type silicon. The doped lining 25 layer is preferably formed by means of a phosphorus diffusion.

In the second form of the invention it is strongly preferred that the amount of substrate being etched to provide for liftoff of the film is small compared to the overall thickness of the substrate.

30

In the third form of the invention it is preferred that the masking layer is removed prior to liftoff of the film, the removal of the masking layer forming cavities between the film and the substrate, with the cavities forming at least part of the etchant access regions.

In the third form of the invention the film is deposited on the substrate such that holes in the film form the etchant access regions. The amount of overgrowth of the film over the masking layer is preferably limited, and the invention preferably further including the steps of etching the film at or adjacent the attachment regions to effect liftoff, the dimensions of the attachment regions providing for liftoff without significant degradation of the film. Preferably, the substrate is of (100) orientation and said attachment regions form two mutually perpendicular sets of equally spaced elongate regions in the $\langle 110 \rangle$ directions of the substrate and growth of the buffer layer and the film is carried out by liquid phase epitaxy, resulting in a highly textured film surface displaying faces orientated close to $\{111\}$ crystallographic planes.

In a variation, the third form of the invention preferably includes the further steps of depositing the film by chemical vapour deposition, so that polycrystalline silicon is deposited on the masking layer; and subsequently removing said polycrystalline silicon in an etchant which does not significantly attack the single crystal layers constituting the substrate, buffer and film, removal of said polycrystalline film and the removal of said masking layer creating the etchant access regions.

In another variation, the substrate is preferably of near (111) orientation and the film overgrows the masking layer essentially without leaving a gap between the masking layer and said film.

Preferably, at least some of the etchant access regions are less densely spread than the remaining etchant access regions so that at least part of the film or substrate is not completely etched through when liftoff is complete and provides a physical connection between said film and substrate.

The etchant access regions preferably form a regular array.

Liquid phase epitaxy (LPE) or chemical vapour deposition (CVD) can be used as the epitaxial growth technique. Either wet chemical etching or gas phase etching can be used 5 to perform the various etching steps.

It will be apparent that in several forms of the method of this invention the silicon substrate is only exposed in well defined attachment regions on the surface of the substrate. This can be achieved by patterning the substrate with the masking layer. Growth of the 10 epitaxial film or buffer layer occurs only out of the regions where the silicon substrate is exposed, and in such a way that the epitaxial silicon film or layer forms a continuous structure. Following growth, the epitaxial layer is detached from the substrate with a suitable etchant, which is brought in contact with those regions where the epitaxial layer is attached to the silicon of the substrate through numerous holes in the substrate or in the epitaxial layer, 15 or by cleaving the epitaxial layer off the substrate. The epitaxial layer can be several microns to more than 100 microns thick.

In some forms of the invention the substrate forms the film and in some forms the substrate only acts as a growth template. In both cases the substrates can be re-used.

20

Handling of the epitaxial layers can be done either by growing the layers sufficiently thick so that they are self supporting, or by carrying out the processing while the layer is still attached to the substrate. In the latter case, the layer is attached to a supporting superstrate prior to final detachment from the substrate.

25

One of the features of the thin silicon films produced in the majority of the embodiments of the invention, is that the films are perforated, in other words, they contain a plurality of holes. Advantage can be taken of these holes in the fabrication of solar cells. In standard solar cells, a metal grid is required on the sunward facing or 'top' side of the cell 30 in order to collect one type of carriers (electrons or holes) which are generated by the action

of sunlight, with the other type of carrier being collected by an electrical contact on the reverse, or 'bottom' side of the cell. The presence of a metal grid on the sunward side of the cell leads to the shadowing of a part of the underlying cell from sunlight and consequently in a loss of electrical energy and energy conversion efficiency of the cell. However, when 5 a perforated silicon layer is used for fabrication of the solar cell, it is possible to position both sets of metal contact grids on the bottom side of the cell. A further advantage arising out of the fact that the films are perforated, is that solar cells can be made semi-transparent, and that the amount of transparency can be easily varied. This can be of benefit where the films are used for the fabrication of solar cells for special applications, such as for buildings, where a 10 certain degree of transparency is desirable.

Another feature of the thin silicon films produced in some of the embodiments of the invention, is that the resulting film surface is highly textured with faces whose orientation is close to that of {111} crystallographic planes. This type of texturing is desirable for the case 15 where the films are used for the fabrication of solar cells as it significantly increases the average probability of absorption of a ray of sunlight in the film, and therefore significantly increases the conversion efficiency potential of the solar cells.

It will be apparent that the present invention provides a method to grow thin silicon 20 epitaxial films on a pre-existing silicon template, lift off the epitaxial film and then re-use the template. In some of the variations of the invention the substrate is slowly consumed but can be made thick enough to be used many times. The methods of this invention have the potential to lower the cost of producing the silicon films as well as increase the efficiency of the solar cells made on the films, since the resulting film thickness is closer to the optimal 25 thickness for solar cells. The large area growth and liftoff of silicon films grown epitaxially on a silicon substrate, followed by re-use of that substrate, has not been carried out previously.

The invention will now be further described, by way of example only, with reference 30 to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a perspective view of a part of a silicon wafer after growth of the silicon buffer layer and deposition of the masking layer but prior to growth of a liftoff layer according to one embodiment of the invention;

5 Figure 2 shows a cross sectional view of the structure resulting after growth of a liftoff layer on the substrate shown in Figure 1;

Figure 3 shows a perspective view of the structure shown in Figure 2;

Figure 4 shows a perspective view of a part of a silicon wafer prior to growth of buffer and liftoff layers according to another embodiment of the invention;

10 Figure 5 shows a cross sectional view of the structure resulting after growth of a heavily doped silicon buffer layer, followed by a liftoff layer, on the substrate shown in Figure 3;

Figure 6 shows a perspective view of a part of a silicon wafer prior to growth of buffer or liftoff layers according to another embodiment of the invention;

15 Figure 7 shows a perspective view of a part of a silicon wafer following deposition of a patterned masking layer but prior to growth of a liftoff layers according to another embodiment of the invention;

Figure 8 shows a cross-sectional view of the structure resulting after growth of the liftoff layer on the substrate shown in Figure 7;

20 Figure 9 shows a perspective view of a part of a silicon wafer deposition and patterning of the masking layer according to another embodiment of the invention;

Figure 10 shows a cross sectional view of the structure resulting after growth of an epitaxial liftoff layer on a (111) oriented silicon wafer patterned with a masking layer to form a pattern similar to that shown in Figure 1;

25 Figure 11 shows a cross sectional view of a part of a silicon wafer prior to growth of the liftoff layer according to another embodiment of the invention;

Figure 12 shows a plan view of the wafer of Figure 9;

Figure 13 shows a cross sectional view of the structure resulting after growth of a liftoff layer, on the substrate shown in Figure 11; and

30 Figure 14 shows a plan view of a corner of a silicon wafer prior to growth of the

liftoff layer according to another embodiment of the invention.

Figure 15 shows a plan view of part of a silicon wafer used in another embodiment of the method of this invention;

Figure 16 shows a cross-sectional view of the wafer shown in Figure 15;

5 Figure 17 is a cross-sectional view similar to Figure 16 schematically showing an etching step in the method according to the embodiment of this invention;

Figure 18 is a plan view of a corner of a wafer of the kind shown in part in Figure 15;

Figure 19 is a cross-sectional view of a structure resulting after the growth of a epitaxial layer on the structure shown in Figure 17;

10 Figure 20 is a cross-sectional view of a silicon wafer on which a buffer layer and epitaxial layer have been grown in accordance with a method of a further embodiment of this invention;

Figure 21 is a plan view of the structure shown in Figure 20 after deposition and patterning of an etch protect layer;

15 Figure 22 is a cross-sectional view of the structure found in Figure 21 after anisotropic etching;

Figure 23 is a cross-sectional view of the structure of Figure 22 after further etching to detach the epitaxial layer;

Figure 24 is a plan view of a silicon wager after deposition and patterning of an etch 20 protect layer as used in a further embodiment of this invention;

Figure 25 is a cross-sectional view of the structure shown in Figure 24 after anisotropic etching;

Figure 26 is a cross-sectional view of the structure shown in Figure 25 after further doping and etching;

25 Figure 27 is a cross-sectional view similar to Figure 26 schematically showing a detaching etching process;

Figure 28 is a cross-sectional view of the resulting detached silicon film;

Figure 29 is a cross-sectional view of a structure formed as part of a method according to a further embodiment of this invention;

30 Figure 30 is a plan view of the structure shown in Figure 29;

Figure 31 is a cross-sectional view of a structure formed during performance of a method according to another embodiment of this invention;

Figure 32 is a plan view of the structure shown in Figure 31;

Figure 33 is a cross-sectional view of a structure formed during performance of a
5 method according to yet another embodiment of the inventions;

Figure 34 is a cross-sectional view of a structure formed during performance of a method according to yet another embodiment of the invention;

Figure 35 is a schematic cross-sectional view of solar cell produced using a thin silicon film formed according to the method of this invention.

10

BEST MODES FOR CARRYING OUT THE INVENTION

The following terms are explained to assist in the understanding of the invention. As used throughout this specification and claims the terms have these meanings unless the context
15 requires otherwise.

Liftoff layer:

A thin single crystal silicon film which is detached from the substrate and subsequently used for the fabrication of devices, for example solar cells. It has the same crystallographic
20 orientation as the substrate. In some cases an epitaxial layer is grown on the liftoff layer following liftoff but prior to final detachment from the substrate.

Liftoff:

A process by which all, or the vast majority, of the attachment regions physically
25 connecting the substrate and the liftoff layer are etched through. However, the liftoff layer may still remain attached to the substrate by a few remaining attachment regions. Final detachment can be carried out at a later stage by cutting through the remaining attachment regions, or by applying a slight force between the substrate and the liftoff layer, sufficient to break through the attachment regions.

30

Detachment:

The process of physically separating the liftoff layer from the substrate. This can occur at the same time as liftoff, or at some stage following liftoff.

5 Masking layer:

A layer of non-silicon material, such as SiO_2, which prevents the growth of an epitaxial layer of silicon on top of it.

Buffer layer:

10 A layer of silicon between the silicon substrate and the liftoff layer, and containing concentrations of impurities which result in a significantly faster etch rate in the etchant used for liftoff of the liftoff layer from the substrate, than the etch rate of either liftoff layer or substrate in that etchant. This results in the preferential etching of the buffer layer. The buffer layer has the same crystallographic orientation as both the liftoff layer and the 15 substrate.

Etch stop layer:

A layer of silicon containing concentrations of impurities which result in a small or negligible etch rate of the layer, in the etchant used for liftoff of the liftoff layer from the 20 substrate, compared to the etch rate of the attachment regions physically connecting the substrate and the film. The etch stop layer has the same crystallographic orientation as the substrate and always forms part of the liftoff layer.

Etch protect layer:

25 A layer of non-silicon material deposited and patterned on top of a silicon surface for the purpose of protecting the silicon immediately underlying the etch protect layer from being etched during a subsequent selective etching step.

Selective etching:

30 The process by which two materials which are simultaneously exposed to the same

etchant, are etched at significantly different rates, as a result of differences in the physical or chemical properties of the bulk or the surfaces of the two materials. Relevant examples of material/etchant systems which display such selective behaviour are the following:

5 - silicon dioxide and silicon with a (100) surface orientation etched in a potassium hydroxide (KOH) solution at 80° C; the silicon layer will etch much more quickly than the silicon dioxide layer

- silicon containing no impurities and silicon containing a high concentration
10 (5×10^{19} atoms/cm^3) of boron atoms etched in the etchant ethylenediamine pyrocatechol (EDP) at 110° C; the former material will etch much more quickly than the latter material

- pure silicon with a (100) surface orientation and pure silicon with a (111) surface orientation etched in a potassium hydroxide (KOH) solution at 80° C; the former material will
15 etch much more quickly than the latter material. This type of selective etching is known as anisotropic etching.

In the following examples growth of the epitaxial layers is by way of liquid phase epitaxy (LPE) unless stated otherwise. It will however be appreciated that gas phase epitaxy
20 can also be used in many of the examples.

Example 1

Figure 1 shows a substrate 1 formed from undoped silicon of (100) orientation. An epitaxial buffer layer 2 has been grown on the substrate, followed by deposition and
25 patterning of a suitable masking layer 3. Alternatively, the buffer layer 2 could have been formed by means of a boron diffusion into the substrate. The buffer layer 2 is typically 10 μm thick, while the masking layer 3 is typically 0.1 μm thick. Elongate regions 4 of exposed substrate defined by the masking layer 3 run along the <110> directions. The regions 4 are typically 10 μm wide and spaced 100 μm apart. In this example, the buffer layer 2 consists
30 of a layer of p type silicon which has been doped to about 5×10^{18} cm^{-3} with a suitable

dopant such as gallium, while the substrate is much more lightly doped. The masking layer 3 can be SiO_2. The areas in which the silicon substrate is exposed form a continuous mesh. The continuous mesh results in a continuous supply of atomic attachment sites during growth of the liftoff layer and ensures that the whole structure can overgrow without two epitaxial 5 growth fronts impinging on one another, with a possible introduction of structural defects, such as dislocations.

Figures 2 and 3 show the structure resulting after epitaxial growth of a p type liftoff layer 5 on the substrate 1. The liftoff layer 5 is typically 50 - 100 μm thick and is more 10 lightly doped than the buffer layer 2. In Figure 2, the cross sectional view is along a <110> direction. Growth of the liftoff layer 5 has occurred only in those regions not covered by the masking layer 3. It can be seen that the liftoff layer 5 displays a diamond shape in the cross sectional view. The liftoff layer 5 is bounded by faces with near {111} orientations. Growth has been terminated in time to ensure that an array of holes 6 remains 15 in the liftoff layer to provide etchant access regions. To lift off the liftoff layer, the masking layer 3 is removed with a suitable etchant which does not significantly attack any of the silicon layers 1,2,5, such as a mixture of HF and H_2O in the case where the masking layer 3 is SiO_2. Access is provided through the holes 6 in the liftoff layer 5. The buffer layer 2 is then removed with an etchant which etches the heavily doped silicon faster than the more 20 lightly doped silicon of the substrate 1 or the liftoff layer 5. Access is again provided through the array of holes 6 in the liftoff layer. One suitable etchant is the mixture $HF:HNO_3:CH_3COOH$ in the ratio 1:3:8. The etchant initially contacts the heavily doped buffer layer 2 in the regions where the masking layer prevented growth of the liftoff layer and gradually undercuts the liftoff layer 5 until the buffer layer 2 has been completely removed. 25 The resultant structure is textured. Advantage can be taken of this for purposes such as the reflection control of light in a solar cell, for example.

Example 2

Figure 4 shows a substrate 1 formed from undoped silicon of (100) orientation. A 30 masking layer 3 has been deposited and patterned on the substrate 1. The masking layer 3

defines two mutually perpendicular sets of elongate regions 4 of exposed substrate which run along <110> directions.

Figure 5 shows the structure resulting after growth of a silicon buffer layer 2 and a
5 liftoff layer 5 on the substrate of Figure 4 . In Figure 5, the cross sectional view is along a <110> direction. Growth of the epitaxial buffer 2 and liftoff layer 5 has occurred only in those attachment regions 4 not covered by the masking layer 3. Growth has been terminated in time to ensure that an array of holes 6 remains in the liftoff layer 5 to provide etchant access regions. In this example, the buffer layer 2 consists of p type silicon which has been
10 doped to at least 5×10^{18} cm^{-3} with a suitable dopant such as gallium, while the liftoff layer 5 is more lightly doped. To detach the liftoff layer 5, the masking layer 3 can be removed with a suitable etchant which does not significantly attack any of the silicon layers 1, 2, 5, although removal of the masking layer 3 is not essential. If the masking layer 3 is not removed, it can be re-used for the growth of subsequent liftoff layers. The buffer layer 2 is
15 removed with an etchant which etches the heavily doped silicon faster than the more lightly doped silicon of the substrate 1 or the liftoff layer 5, in order to effect liftoff of the liftoff layer 5.

Example 3

20 The substrate 1 shown in Figure 6 is undoped silicon of (100) orientation. A masking layer 3 has been deposited and patterned on the substrate. As in example 2 mutually perpendicular sets of elongate regions 4 of exposed substrate run in <110> directions. The structure is identical to that shown in Figure 4, except that the elongate regions 4 are much narrower, typically 1 μm wide. Growth of the epitaxial layers (not shown) on this structure
25 proceeds as described above in relation to Example 2 with the difference that the elongate attachment regions 4 where the epitaxial layer is attached to the substrate are much narrower. Liftoff is carried out as described above in Example 2. However, even if no buffer layer is grown, the epitaxial layer can still be lifted off the substrate with a silicon etchant, due the narrowness of the attachment regions which have to be etched through.

30

Example 4

The substrate 1 shown in Figure 7 is p type silicon of (100) orientation which has been doped to at least $5 \times 10^{18}\ cm^{-3}$ with a suitable dopant such as boron. A masking layer 3 has been deposited and patterned on the substrate. The masking layer defines mutually perpendicular sets of elongate regions 4 of exposed substrate running along <110> directions.

Figure 8 shows the structure resulting after growth of a liftoff layer 5 on the substrate of Figure 7. In Figure 8, the cross sectional view is along a <110> direction. To lift off the liftoff layer, the masking layer 3 is removed with a suitable etchant which does not significantly attack any of the silicon layers 1, 5. Holes 6 in the lift off layer 5 form etchant access regions. Some of the substrate is etched with an etchant which etches the heavily doped silicon of the substrate 1 faster than the more lightly doped silicon of the liftoff layer 5. The liftoff layer 5 therefore acts as an etch stop layer. The thickness of the layer of substrate that is etched away is small compared to the initial substrate thickness and therefore the substrate can be re-used many times.

Example 5

Figure 9 shows a silicon substrate 1 in which array of holes 6 has been created by laser ablation or reactive ion etching. The holes have typical dimensions of 50 μm by 50 μm. A masking layer 3 has been deposited and patterned on the substrate 1 to define attachment regions 4 of exposed substrate. The inside of the holes 6 has also been coated with the masking layer 3. Growth of the epitaxial buffer and liftoff layers (not shown) proceeds as described in the preceding examples. Growth of the liftoff layer may be continued until it forms a closed structure. Etchant access regions for etchant solutions required to lift off the liftoff layer and/or the masking layer are provided by holes 6 in the substrate 1.

Example 6

A (111) oriented silicon substrate 1 is shown in cross section in Figure 10, patterned with a thick masking layer 3 to produce a pattern similar to that shown in Figure 1. The

masking layer 3 is typically 1 μm thick, and elongate openings 4 in the masking layer 3 are typically 1 μm wide. An epitaxial liftoff layer 5 has overgrown the masking layer without creating a cavity. In this way, solvent entrapment, which can occur in structures such as that shown in Figure 3 if grown by LPE, can be avoided. In order to lift off the liftoff layer 5, the masking layer 3 is first removed using an etchant which etches the masking layer 3 but not either of the silicon layers 1, 5. Removal of the masking layer 3 creates etchant access regions or cavities between the substrate and the liftoff layer. A silicon etchant is poured into the cavities. After some time the etchant removes the regions where the liftoff layer 5 is attached to the substrate. Due to the narrowness of the attachment regions, liftoff can be carried out without substantially etching the liftoff layer 5.

Example 7

Figures 11 and 12 show an undoped (100) oriented silicon substrate 1 textured to produce square base upright pyramids 7 on the substrate surface. In Figure 11, the view is in a <110> direction. The sidewalls of the pyramids 7 have {111} orientations. The bases of the pyramids 7 run along <110> directions. The texturing can be achieved, for example, through the use of a potassium hydroxide (KOH) solution which etches the {111} planes of silicon much slower than other planes. A masking layer 3 is deposited to define attachment regions 4 of silicon substrate exposed in narrow lines which run along the bases of the pyramids 7 in <110> directions. The attachment regions 4 are typically 1 μm wide.

Figure 13 shows an epitaxial liftoff layer 5 grown on the substrate shown in Figures 11 and 12. The view is in a <110> direction. If growth is carried out by LPE, entrapment of solvent may be kept very small with this structure. To lift off the epitaxial layer 5 from the substrate 1, the masking layer 3 is removed by an etch which does not etch either of the silicon layers 1, 5. Removal of the masking layer 3 creates etchant access regions or cavities between the substrate and the liftoff layer. A silicon etchant is poured into the cavities so formed. After some time the etchant removes the regions where the liftoff layer 5 is attached to the substrate. Due to the narrowness of the attachment regions, the liftoff layer 5 is not significantly etched.

Example 8

Figure 14 shows a substrate 1 formed from silicon of (100) orientation. A masking layer 3 has been deposited and patterned on the substrate 1. Attachment regions 4 of exposed substrate are defined by the masking layer and run in <110> directions. Growth of the epitaxial buffer and liftoff layers (not shown) on this substrate is carried out as described in the preceding examples. The attachment regions 4 are wider at the substrate 1 edges than in the inner parts of the substrate. Consequently, etchant access regions formed by removing the masking layer 3 are less densely spaced at the periphery of the substrate 1. When a suitable etchant is used to remove the buffer layer, the liftoff layer is detached from the substrate in the inner regions of the substrate before it is detached at the edges. Etching can be stopped at this stage and the epitaxial layer can be processed. The liftoff layer is not attached to the substrate 1 anywhere except at the edges, but it is still supported by the substrate 1. Following processing, the liftoff layer can be attached to a suitable superstate such as glass, and the regions of the liftoff layer which are still attached to the substrate are removed. This can be done, for example, by dicing through the liftoff layer at the edges. This approach provides a means of processing liftoff layers which are too thin to be self supporting.

Example 9

Figures 15 and 16 show a single crystal silicon substrate 1 of arbitrary crystal orientation. The substrate is p type with a dopant concentration of typically 10^{17} cm $^{-3}$. A selective phosphorus diffusion has been made into the substrate 1 after suitable photolithographic masking (not shown), to create a moderately doped n type layer, which forms the liftoff layer 5. The p type areas 8 remaining on the surface of the substrate 1 following the phosphorus diffusion are typically 4 μm across and are spaced apart by typically 10 μm. The liftoff layer 5 is typically 4 μm deep. The wafer is etched in an electro-chemical etchant consisting of, for example, 5% aqueous hydrogen fluoride which attacks p-type silicon of the substrate 1 but does not significantly etch moderately doped n-type silicon of the liftoff layer 5. In consequence, the liftoff layer 5 acts as an etch stop layer. The etching process proceeds to remove a layer of the substrate through the exposed

p type areas 8 surrounded by the liftoff layer 5 which form etchant access regions. The etching eventually removes all the substrate 1 from below the liftoff layer, thus lifting off the liftoff layer 5, as schematically shown in Figure 17. The liftoff layer 5 is kept attached to the substrate 1 by using a slightly different pattern at the wafer corners as shown in Figure 18 and described above in Example 8. That is, a greater distance is provided between the exposed p type areas 8 of the substrate so that the etchant takes longer to completely undercut the liftoff layer 5 adjacent those areas.

Further, an epitaxial layer 9 can be grown on the liftoff layer as shown in Figure 19. The composite epitaxial layer 9 and liftoff layer 5 can be detached from the substrate 1 by the application of a small shear force sufficient to break through the remaining corner attachment regions, or by cutting through the remaining attachment regions. The substrate 1 is etched slightly during this process but can be reused many times as the amount of silicon lost during the production of each layer is only of the order of 10 μm, and the substrate can be made greater than 500 μm thick.

Example 10

A p-type epitaxial buffer layer 2, doped to greater than 10^{19} cm $^{-3}$ is grown on an n-type silicon substrate 1 of (110) orientation followed by an n-type epitaxial liftoff layer 5. Both the substrate 1 and the liftoff layer 5 are doped to a concentration of typically 10^{17} cm $^{-3}$. The resulting structure is shown in Figure 20. In Figure 20, the cross sectional view is along the [1 -1 -2] direction. The buffer layer 2 is typically 20 μm thick and the liftoff layer 4 is typically 50 μm thick. An etch protect layer 10 of silicon dioxide (SiO_2) or other suitable material is deposited and patterned on the surface of the liftoff layer 5 using photolithographic techniques to define elongate strips 11 of exposed substrate 1. As shown in Figure 21 the pattern is characterised by staggered arrangements of strips 11 typically 400 μm long and 10 μm wide. The strips 11 are oriented along the [1 -1 -2] direction. The lines of strips 11 are typically spaced by 30 μm. The structure is etched in an anisotropic etchant such as ethylenediamine pyrocatechol (EDP). The anisotropic etchant has the characteristics that it etches the silicon (111) planes very slowly compared to other crystal planes, it

essentially stops etching at heavily doped p-type layers and it etches the SiO_2 etch protect layer much more slowly than silicon. As a consequence, blind slots 12 with two parallel vertical sidewalls 13 are etched in the liftoff layer 5 where the strips 11 are formed in the masking layer 1. The resulting structure is shown in Figure 22, where the view is along the
5 [1 -1 -2] direction. Slots 12 with two parallel vertical sidewalls 13 have been formed in the liftoff layer 5 to provide etchant access regions to the buffer layer 2. An electro-chemical etchant is used to etch the buffer layer 2, the etchant having the characteristic of attacking p-type silicon but not significantly etching moderately doped n-type silicon. Consequently the buffer layer 2 is etched away to lift off the liftoff layer 5 from the substrate 1. This is
10 schematically illustrated in Figure 23. It will be apparent that the staggered slot configuration is such that the liftoff layer 5 is continuous.

Example 11

An n-type region 14 is created on the surface of a moderately doped p-type (110)
15 oriented silicon substrate 1, by means of a phosphorus diffusion. An etch protect layer 10 of silicon dioxide or other suitable material is deposited on the surface and patterned using photolithographic techniques to produce the staggered pattern of strips 11 shown in Figure 24. The strips 11 are typically 400 μm long, 10 μm wide, spaced 20 μm apart and are oriented along the [1 -1 -2] direction. The upper surface of the structure is similar to that
20 shown in Figure 21. As in example 10 the structure is etched with an anisotropic etchant such as EDP to form slots 12 which partly form etchant access regions.

Figure 25 shows the structure following etching, with the slots 12 extending typically 70 μm deep into the substrate 1. In Figure 25, the view is along the [1 -1 -2] direction.
25 Another phosphorus diffusion is made with phosphorus driven into the substrate 1 at a high temperature to produce a moderately doped n-type region 14 typically 2 μm deep. Alternatively, if the second phosphorus diffusion is driven in sufficiently deep that a significant amount of phosphorus penetrates through the etch protect layer and into the underlying substrate silicon, then the first phosphorus diffusion may be omitted. The
30 structure is again etched in an antistrophic etchant such as EDP. The etching is continued

until the n type region (not shown) at the bottom or blind end 15 of the slots 12 is completely etched through resulting in the structure shown in Figure 26. An electro-chemical etch which attacks p-type silicon but does not significantly etch moderately doped n-type silicon is then used to etch through part (shown at 16) of the substrate 1 as schematically shown in Figure 5 27. The n doped layer 14 acts as an etch stop during the electrochemical etching. This results in the liftoff of a thin silicon layer 5 as shown in Figure 28. As in the previous example, the arrangement of the slots 12 is such that the layer is continuous.

Example 12

10 Oxide dots 3 having a thickness of about 1 μm are deposited on the surface of an n-type silicon substrate 1, to act as a masking layer. The dots 3 are typically 30 μm in diameter and are spaced typically 200 μm apart. A p-type silicon buffer layer 2 is grown on the substrate 1 in such a way that the buffer layer 2 does not substantially grow over the oxide dots 3. There will be some amount of overgrowth at the edges of the dots 3. The buffer 15 layer 2 is typically 10 μm thick . A moderately doped n-type silicon liftoff layer 5 typically 50 μm thick is then grown over the buffer layer 2 as shown in Figures 29 and 30. The structure is etched in hydrofluoric acid to remove the oxide dots 3 and form etchant access regions to the p-type silicon buffer 2. An electro-chemical etch is then used to selectively etch the p-type silicon buffer 2 and liftoff the liftoff layer 5.

20

Example 13

A typically 10 μm thick p-type silicon buffer layer 2 followed by a typically 50 μm thick n-type liftoff layer 5 is grown on an n-type substrate 1. A laser or other suitable cutting device (not shown) is used to form an array of holes 6 through the n-type layer 5 and 25 provide etchant access regions to the buffer layer 2, as shown in Figures 31 and 32. The holes 6 are approximately 50 μm in diameter and are spaced approximately 200 μm apart. A selective electro-chemical etch is used to etch the p-type buffer layer 2 and lift off the n-type liftoff layer 5.

30 Example 14

As in example 12, oxide dots 3 having a thickness of about 1 μm are deposited on the surface of an n-type silicon substrate 1, to act as a masking layer. The dots are typically 30 μm in diameter and are spaced typically 200 μm apart. Silicon deposition is carried out by chemical vapour deposition (CVD) single crystal, p-type epitaxial silicon buffer layer 2 is grown on the exposed regions of the substrate at the same time, polycrystalline silicon 16 is deposited on top of the oxide dots 3. The buffer layer 2 is typically 10 μm thick . A moderately doped n-type silicon liftoff layer 5 typically 50 μm thick is then grown over the buffer layer 2. The resulting structure is shown in Figure 33.

To liftoff the liftoff layer 5, the structure is first etched in an etchant which etches polycrystalline silicon 16 at a much faster rate than single crystalline silicon to form etchant access regions to the buffer layer. One such etchant is potassium hydroxide (KOH) in the case where the silicon substrate 1 and epitaxial layer 5 are of (111) orientation. Following removal of the polycrystalline silicon layer 16, an electro-chemical etch is used to selectively etch the p-type silicon buffer 2 to liftoff the liftoff layer 5.

Example 15

A masking layer 3 is deposited and patterned on a (100) oriented p type silicon substrate 1 to produce a structure as shown in Figure 4. A p type epitaxial layer 5 is then grown on the substrate to produce a structure as shown in Figure 8. A phosphorus diffusion is made over the entire surface. The diffusion temperature and time, and the thickness of the masking layer 3, are chosen to ensure that no significant amount of phosphorus diffuses through the masking layer 3 and into the underlying silicon of the substrate 1. The phosphorus diffusion results in an n-type layer 17 surrounding the liftoff layer 5. The masking layer 3 is removed in an etchant which does not significantly attack any of the silicon layers to form etchant access regions. The phosphorus can now be driven in deeper into the silicon if required. The resulting structure is shown in Figure 34. An electro-chemical etch which etches p-type silicon but does not significantly attack n-type silicon is now used to selectively etch the exposed regions of p-type silicon of the substrate until the epitaxial layer has been lifted off. The n-type silicon layer 17 resulting from the phosphorus diffusion acts as an etch

stop layer which protects the epitaxial layer during the etching process.

Example 16

In Figure 35, a thin silicon film 5, produced in a manner as described in example 1, has been used for the fabrication of a solar cell 18 using standard semiconductor processing techniques. A phosphorus diffusion has been made over the entire top or sunward surface of the film 5, as well as over most of the bottom surface to produce an n-type layer 19. Some regions 20 on the bottom surface have been left undiffused. Electrical contacts 21 are provided to both p-type and n-type silicon regions, these contacts serving to collect photo generated holes and electrons, respectively. Because the n-type regions 19 extend continuously from the front to the rear of the film, electrons which are generated near the top of the n region 19 can readily flow to a contact 21 on the rear of the cell 18. Due to the short distances that carriers have to travel before reaching the metal contacts, series resistance losses can be kept small.

The claims defining the invention are as follows:

1. A method of producing thin single crystal silicon films, said method including the steps of:

forming a single crystal substrate;

5 depositing or forming a thin single crystal silicon film having the same crystal orientation as said substrate in, on or adjacent to said substrate, the thin single crystal silicon film disposed for liftoff from the substrate;

providing a plurality of spaced apart etchant access regions through said thin single crystal silicon film or substrate; and

10 causing liftoff of said thin single crystal silicon film by etching via said etchant access regions through said single crystal substrate and/or said thin single crystal silicon film, the amount of etching required and the degree of access for etchant providing for detachment of said thin single crystal silicon film without significant degradation of said thin single crystal silicon film.

15 2. A method of producing thin single crystal silicon films, said method including the steps of:

forming a single crystal substrate;

depositing or forming a thin single crystal silicon film having the same crystal orientation as said substrate in, on or adjacent to said single crystal substrate, the thin 20 single crystal film disposed for liftoff from the substrate;

providing a plurality of spaced apart etchant access regions through said thin single crystal silicon film or substrate;

epitaxially growing or forming between said single crystal substrate and said thin single crystal silicon film a buffer layer of silicon having the same crystal orientation as 25 said single crystal substrate and containing concentrations of impurities resulting in the buffer layer having a significantly faster etch rate in a selected etchant than either said thin single crystal silicon film or said substrate; and

causing liftoff of said thin single crystal silicon film by etching said buffer layer through said etchant access regions, the amount of etching required and the degree of 30 access for etchant providing for detachment of said thin single crystal silicon film without significant degradation of said thin single crystal silicon film.

3. A method as claimed in claim 1 wherein an etch stop layer of silicon having the same crystal orientation as said substrate and containing concentrations of impurities which result in said etch stop layer having a significantly slower etch rate in a

selected etchant than the silicon of the substrate or film, is epitaxially grown or formed on or in said substrate or said film to define said etchant access regions.

4. A method as claimed in claim 1 wherein a masking layer of non silicon material is deposited and patterned on said substrate to define attachment regions of exposed substrate,

said attachment regions having at least one dimension small in comparison to spacings between adjacent regions, and said film is deposited on said substrate at said attachment regions.

5. A method as claimed in claim 2 wherein a masking layer of non silicon material is deposited and patterned on said substrate or said buffer layer to define attachment regions of

exposed substrate or buffer layer.

6. A method as claimed in claim 2 wherein said buffer layer is formed or deposited substantially continuously over a surface of said substrate, said film is deposited on said buffer
5 layer and further including the step of forming said etchant access regions through said film.

7. A method as claimed in claim 5 wherein said buffer layer is formed or deposited on or in said substrate, said masking layer is deposited and patterned on said buffer layer, said film is deposited on said buffer layer at said attachment regions, and said masking layer is removed prior
10 to liftoff of said film.

8. A method as claimed in claim 7 wherein said film is deposited on said buffer layer such that holes remaining in said film following deposition form at least part of said etchant access regions.
15

9. A method as claimed in claim 7 further including the steps of depositing said film by chemical vapour deposition, so that polycrystalline silicon is deposited on said masking layer; and subsequently removing said polycrystalline silicon in an etchant which does not significantly attack the single crystal layers constituting said substrate, buffer and film, removal
20 of said polycrystalline film and the removal of said masking layer creating said etchant access regions.

10. A method as claimed in claim 5 wherein said masking layer is deposited and patterned on said substrate, followed by deposition of said buffer layer at said attachment regions and said
25 film is deposited on said buffer layer.

11. A method as claimed in claim 10 wherein said substrate is formed with a plurality of apertures extending through the entire thickness of said substrate, said apertures at least partly forming said etchant access regions, and said masking layer is deposited to define attachment
30 regions of exposed substrate only on an upper surface of said substrate.

12. A method as claimed in claim 11 wherein said apertures are formed by means of reactive ion etching or laser ablation.

13. A method as claimed in claim 10 wherein said film is deposited on said buffer layer such that holes remaining in said film following deposition at least partly form said etchant access regions.

14. A method as claimed in claim 10 further including the steps of depositing said buffer layer and said film by chemical vapour deposition so that polycrystalline silicon is deposited on said masking layer; and

subsequently removing said polycrystalline silicon in an etchant which does not significantly attack the single crystal layers constituting said substrate, buffer and film, removal of said polycrystalline film creating said etchant access regions.

15. A method as claimed in claim 6 wherein said etchant access regions are formed by laser ablation or reactive ion etching.

16. A method as claimed in claim 6 wherein said substrate is of (110) orientation and said etchant access regions are formed by depositing a non silicon etch protect layer on said film patterned to define elongate strips of exposed film each extending along the [1 -1 -2] direction and forming a staggered pattern, and etching said film through said strips using an anisotropic etchant to create slots in said film extending to said buffer layer, said etch protect layer preventing the regions of said film to which it is deposited from being etched.

17. A method as claimed in claim 16 wherein said buffer layer is doped p type to a concentration of about 5×10^{19} cm^{-3} and said anisotropic etchant is ethylenediamine pyrocatechol.

18. A method as claimed in any one of claim 5, 7, 8, 10, 11, 12, or 13 wherein the substrate is of (100) orientation and said attachment regions form two mutually perpendicular sets of equally spaced elongate regions in the <110> directions of the substrate; and

growth of said buffer layer and said film is carried out by liquid phase epitaxy, resulting in a highly textured film surface displaying faces orientated close to {111} crystallographic planes.

5 19. A method as claimed in any one of claims 2, 5, 6, 7, 8, 9, 15, 16 or 17 wherein said buffer layer is formed by selectively doping the surface of the substrate.

20. A method as claimed in any one of claims 5, 7, 8, 9, 10, 11, 12, 13, 14 or 19 wherein said attachment regions form a continuous mesh.

10

21. A method as claimed in any one of claims 2, or 5 to 18 wherein the buffer layer is deposited on a surface of said substrate.

22. A method as claimed in any one of claims 2 or 5 to 21 wherein at least some said etchant
15 access regions are less densely spaced than the remaining etchant access regions, so that at least some buffer layer connecting the substrate to the film is not completely etched through when liftoff is complete.

23. A method as claimed in claim 3 wherein a masking layer of non silicon material is
20 deposited and patterned on said substrate to define attachment regions of exposed substrate, said film is subsequently deposited on said substrate at said attachment regions and at least part of the masking layer is removed prior to liftoff of said film.

24. A method as claimed in claim 23 wherein said film is deposited on said substrate such that
25 holes remaining in said film following deposition form at least part of said etchant access regions.

25. A method as claimed in claim 24 wherein said substrate is of (100) orientation and said attachment regions form two mutually perpendicular sets of equally spaced elongate regions in the <110> directions of the substrate; and

30 deposition of said film is carried out by liquid phase epitaxy, resulting in a highly textured film surface displaying faces orientated close to {111} crystallographic planes.

26. A method as claimed in claim 3 wherein said film is formed in said substrate by selectively doping part of the substrate with a suitable dopant, said film acting as an etch stop layer during subsequent etching to effect liftoff of said film, those regions of said substrate not doped forming said plurality of etchant access regions.

5

27. A method as claimed in claim 26 wherein said substrate is p type and said film is n type; and

said liftoff is effected by electrochemical etching in an aqueous, hydrofluoric acid containing etchant which does not significantly etch n type silicon.

10

28. A method as claimed in claim 26 or claim 27 wherein said etch stop layer is formed by means of a phosphorus diffusion into said substrate.

29. A method as claimed in any of claims 26 to 28 wherein an epitaxial layer is grown on said

15 film following liftoff but prior to final detachment of said film from said substrate.

30. A method as claimed in claim 3 wherein said film is formed from part of said substrate.

31. A method as claimed in claim 30 and further including the steps of forming blind access

20 apertures in said substrate, doping the exposed aperture surfaces of the substrate to form a doped lining layer, removing said lining layer at the blind end of said apertures to expose said substrate; and

etching the substrate to provide for liftoff of said film, said doped lining layer forming part of said film and acting as an etch stop layer during said etching to provide for liftoff of said

25 film.

32. A method as claimed in claim 31 wherein said substrate is of (110) orientation and said access apertures are formed by depositing a non silicon etch protect layer on said film patterned to define elongate strips extending along a [1 -1 -2] direction and forming a staggered pattern,

30 and etching said film through said strips using an anisotropic etchant to create slots in said film, said etch protect layer preventing the regions of said film to which it is deposited from being

etched.

33. A method as claimed in claim 31 or claim 32 wherein said substrate is p type and said lining layer is n type; and

said liftoff is effected by electrochemical etching in an aqueous, hydrofluoric acid
5 containing etchant which does not significantly etch n type silicon.

34. A method as claimed in any one of claims 31 to 33 wherein said doped lining layer is formed by means of a phosphorus diffusion.

10 35. A method as claimed in claim 31 further including the sequential steps of forming an n doped surface on said substrate by means of a phosphorus diffusion, depositing and patterning said etch protect layer to define elongate strips extending along a [1 -1 -2] direction and forming a staggered pattern, etching said film through said strips using an anisotropic etchant to create blind slots in said film, doping the surfaces of said slots by means of a second phosphorus
15 diffusion, anisotropically etching the blind ends of said slots to remove the phosphorus doped material and expose said substrate, and effecting liftoff by electrochemically etching said substrate in a hydrofluoric acid containing etchant which does not significantly etch n type silicon.

20 36. A method as claimed in claim 31 further including the sequential steps of depositing and patterning said etch protect layer on said substrate to define elongate strips extending along a [1 -1 -2] direction and forming a staggered pattern, etching said film through said strips using an anisotropic etchant to create blind slots in said film, doping the surfaces of said slots by means of a phosphorus diffusion, said phosphorus diffusion also doping the regions of said film
25 to which said etch protect layer is deposited, anisotropically etching the blind ends of said slots to remove the phosphorus doped material and expose said substrate, and effecting liftoff by electrochemically etching said substrate in a hydrofluoric acid containing etchant which does not significantly etch n type silicon.

30 37. A method as claimed in claim 24 or claim 25 wherein said film forms said etch stop layer.

38. A method as claimed in claim 24 or claim 25 wherein an etch stop layer is formed or deposited in or on said film to protect a corresponding part of said film from being etched during said selective etching to effect liftoff of said film.

39. A method as claimed in claim 38 wherein said etch stop layer is formed by means of a phosphorus diffusion into said film.

40. A method as claimed in claim 3 wherein the amount of substrate being etched to provide for liftoff of said film is small compared to the overall thickness of said substrate.

41. A method as claimed in claim 4 wherein said film is deposited on said substrate such that holes remaining in said film following deposition form said etchant access regions.

42. A method as claimed in claim 4 wherein at least part of said masking layer is removed prior to liftoff of said film, the removal of said masking layer forming cavities between said film and said substrate, said cavities forming at least part of the etchant access regions.

43. A method as claimed in claim 41 wherein the amount of overgrowth of said film over said masking layer is limited, and further including the steps of etching said film at or adjacent said attachment regions to effect liftoff, the dimensions of said attachment regions providing for liftoff without significant degradation of said film.

44. A method as claimed in claim 43 wherein said substrate is of (100) orientation and said attachment regions form two mutually perpendicular sets of equally spaced elongate regions in the $<110>$ directions of the substrate; and

growth of said buffer layer and said film is carried out by liquid phase epitaxy, resulting in a highly textured film surface displaying faces orientated close to {111} crystallographic planes.

45. A method as claimed in claim 42 wherein said film is deposited on said substrate such

that holes remaining in said film following deposition form at least part of said etchant access regions.

46. A method as claimed in claim 42 further including the steps of depositing said film
5 by chemical vapour deposition so that polycrystalline silicon is deposited on said masking layer; and subsequently removing said polycrystalline silicon in an etchant which does not significantly attack the single crystal layers constituting said substrate, buffer and film, removal of said polycrystalline film and the removal of said masking layer creating said etchant access regions.

10

47. A method as claimed in claim 45 wherein said substrate is of (100) orientation and said attachment regions form two mutually perpendicular sets of equally spaced elongate regions in the <110> directions of the substrate; and

growth of said buffer layer and said film is carried out by liquid phase epitaxy,
15 resulting in a highly textured film surface displaying faces orientated close to {111} crystallographic planes.

48. A method as claimed in claim 45 wherein said substrate is of near (111) orientation and said film overgrows said masking layer essentially without leaving a gap between said
20 masking layer and said film.

49. A method as claimed in claim 47 wherein said substrate is textured with square base, upright pyramids, the faces of said pyramids being of {111} orientation and said attachment regions of exposed substrate running along the bases of said pyramids; and said film
25 overgrows said masking layer essentially without leaving a gap between said substrate and said masking layer.

50. A method as claimed in any one of claims 3, 4 or 23 to 49 wherein at least some of said etchant access regions are less densely spread than the remaining etchant access regions
30 so that at least part of the film or substrate is not completely etched through when liftoff is

complete and provides a physical connection between said film and substrate.

51. A method as claimed in any preceding claim wherein said etchant access regions form a regular array.

52. A method of producing thin single crystal silicon films, substantially as hereinbefore described with reference to any one of the Examples.

53. A method of forming a silicon solar cell including the step of forming a thin single crystal silicon film in accordance with the method as claimed in any one of claims 1 to 52.

54. A silicon solar cell including a thin single crystal silicon film formed in accordance with the method of any one of claims 1 to 52.

55. A silicon solar cell substantially as hereinbefore described with reference to Figure 35.

56. A thin single crystal silicon film, when prepared by the method of any one of claims 1-52.

Dated 20 June, 2001
Origin Energy Retail Limited

Patent Attorneys for the Applicant/Nominated Person
SPRUSON & FERGUSON

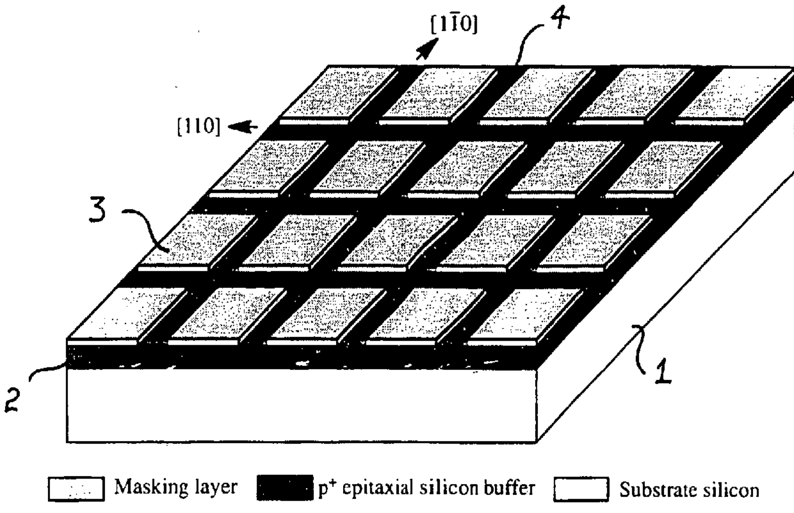


Figure 1

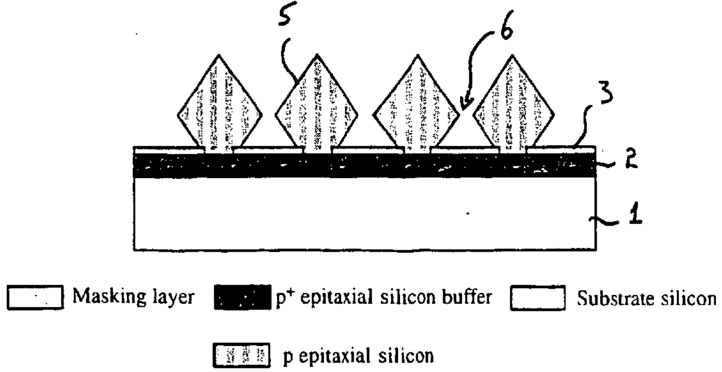


Figure 2

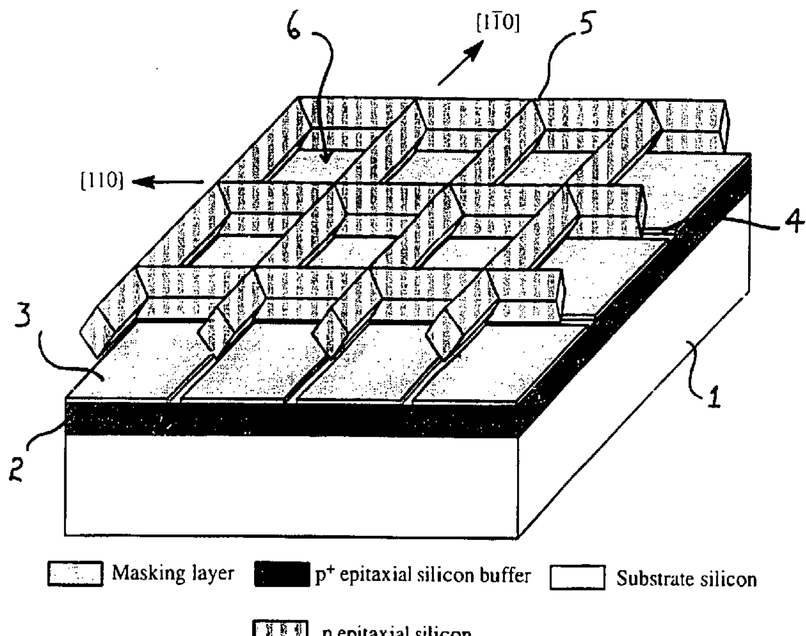


Figure 3

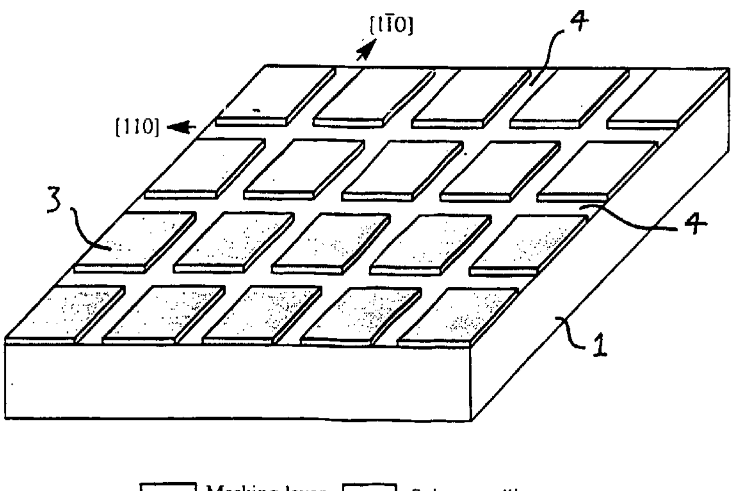


Figure 4

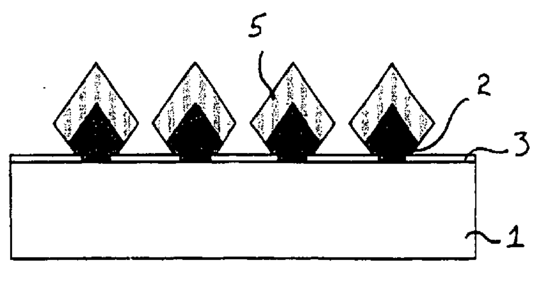


Figure 5

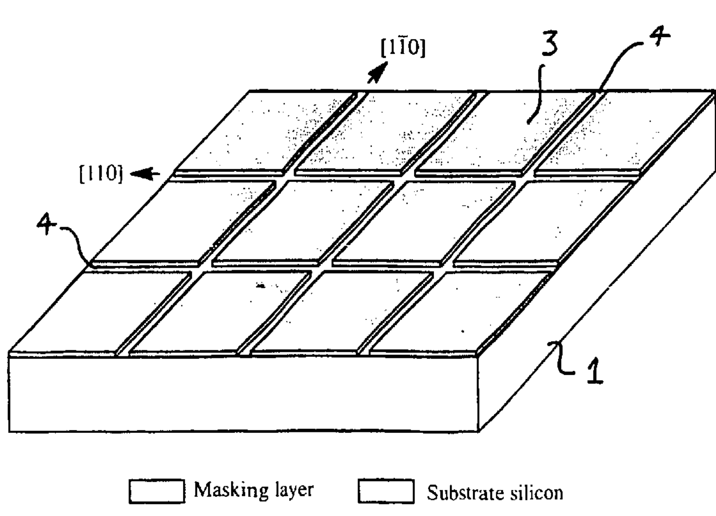


Figure 6

Figure 7

Figure 8

Figure 9

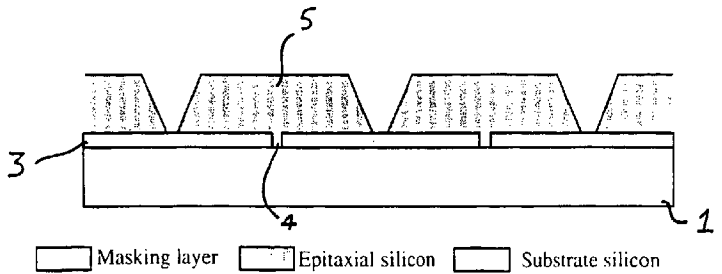


Figure 10

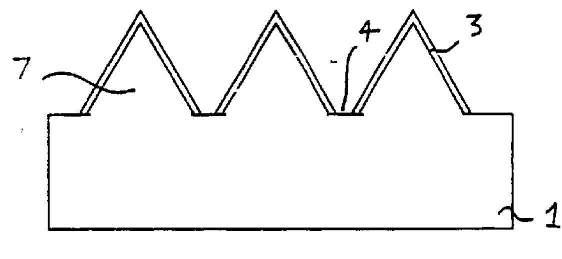
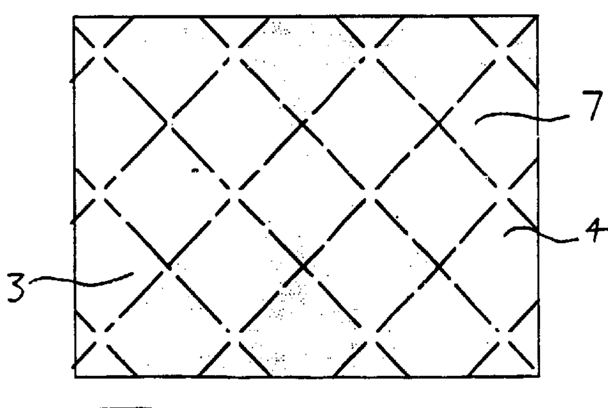


Figure 11



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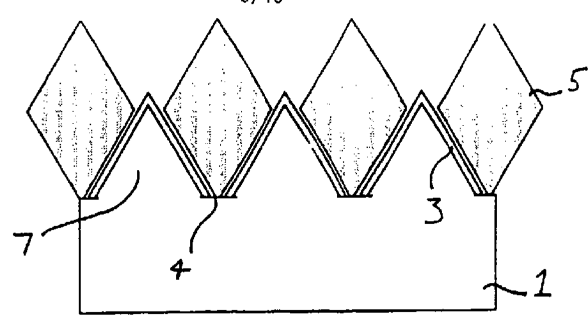
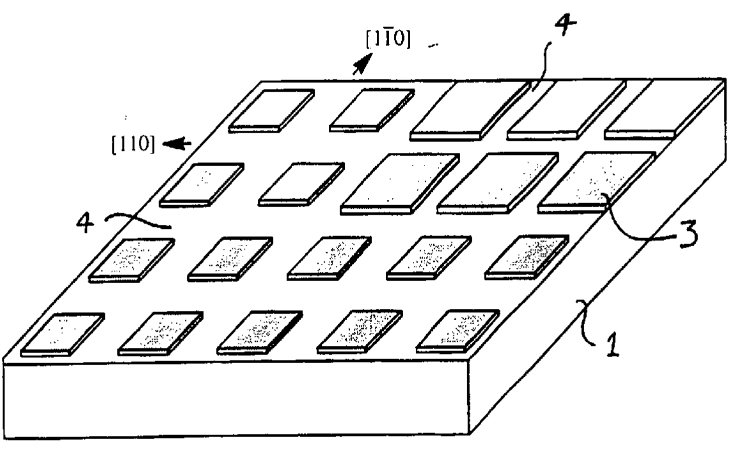


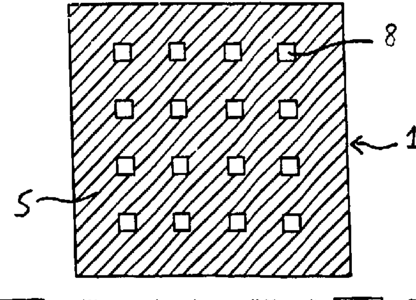
masking layer p epitaxial silicon Substrate silicon

Figure 13



Masking layer Substrate silicon

Figure 14



n silicon (phosphorus diffused) p Si

Figure 15

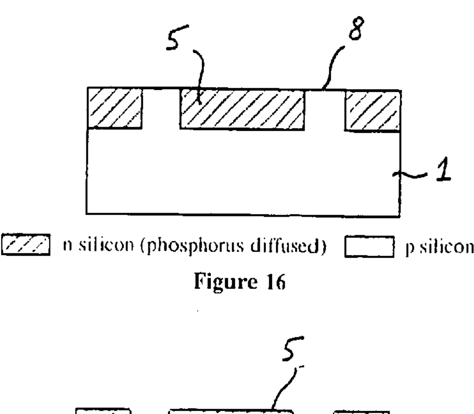


Figure 16

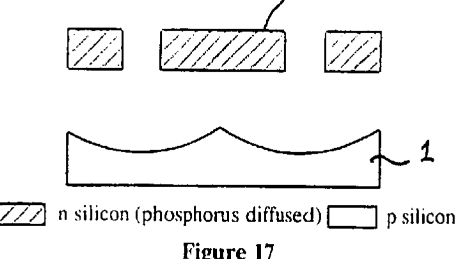
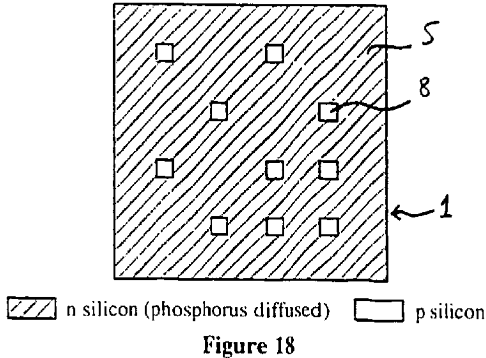


Figure 17



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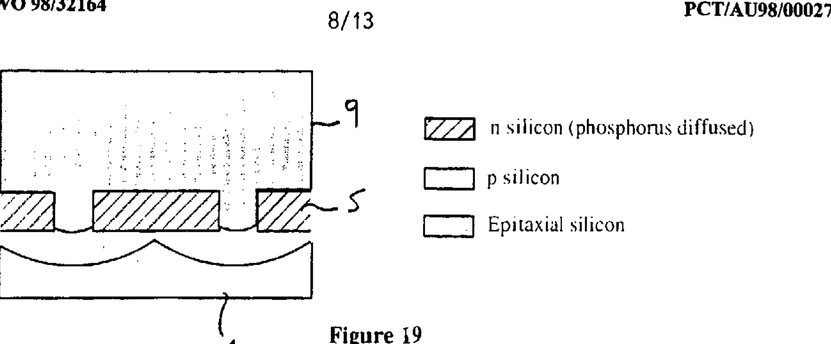

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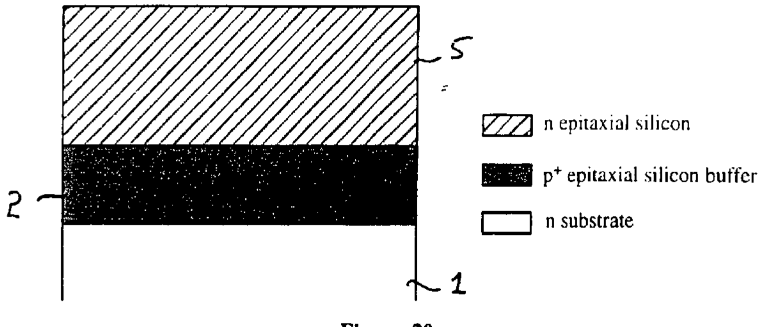

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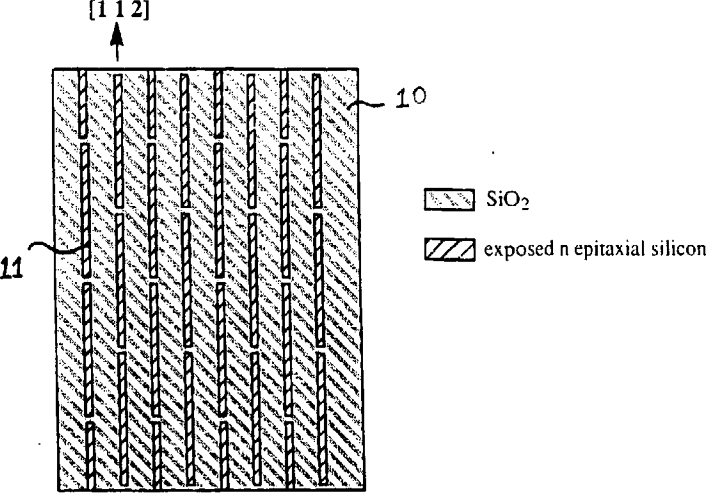

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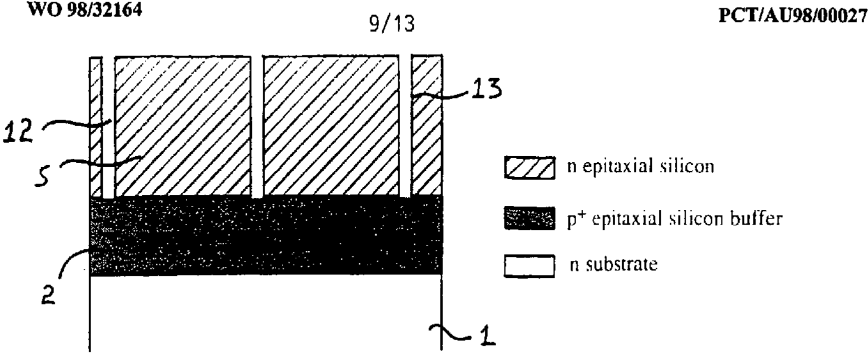

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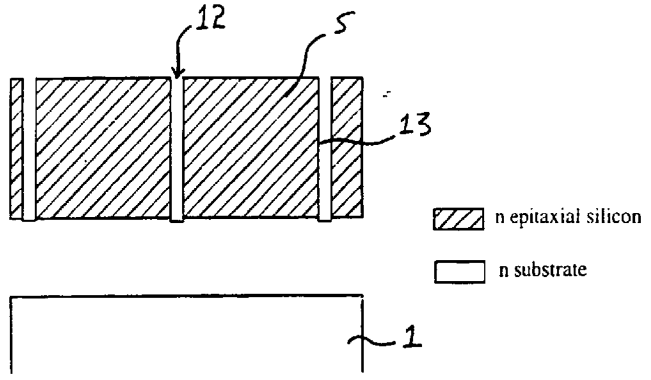
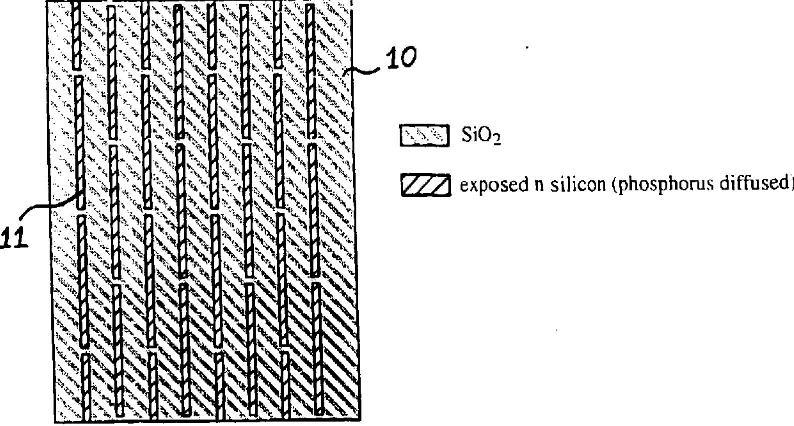


Figure 23



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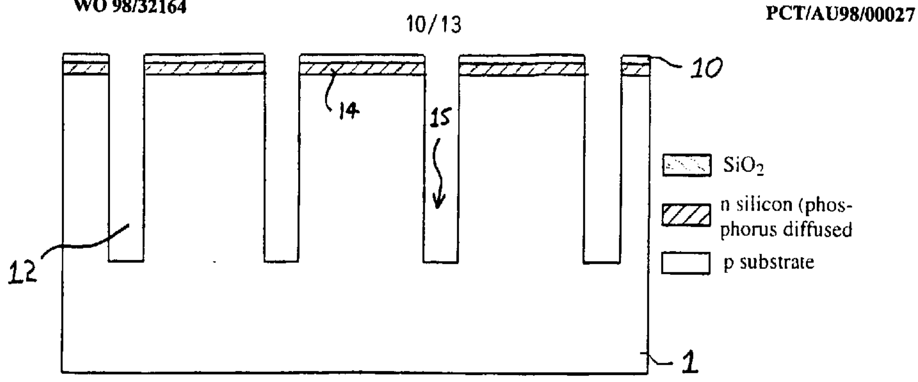
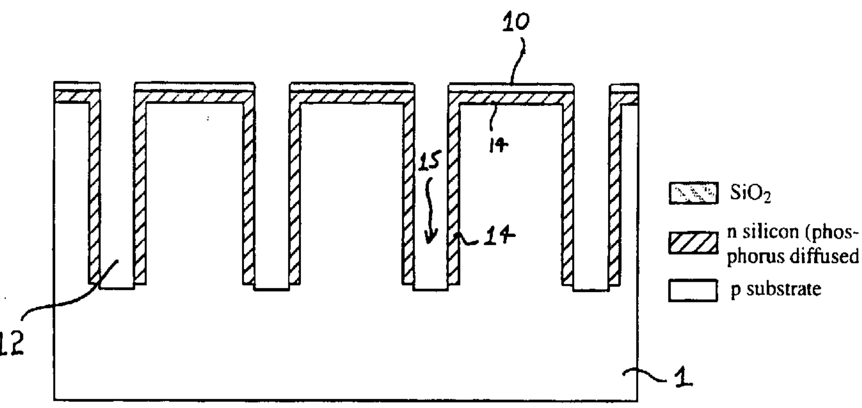


Figure 25



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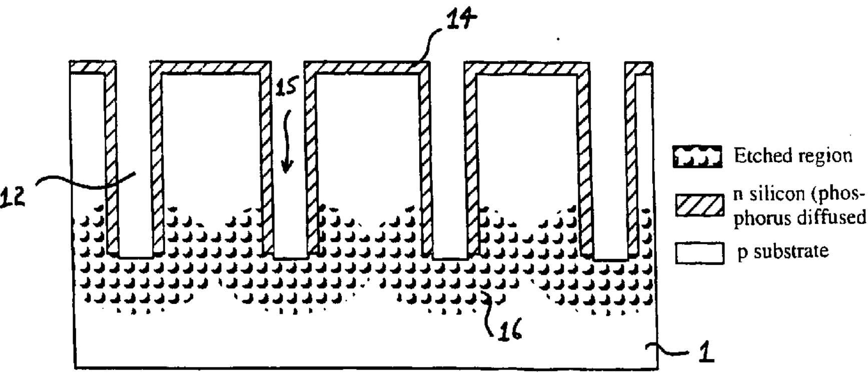

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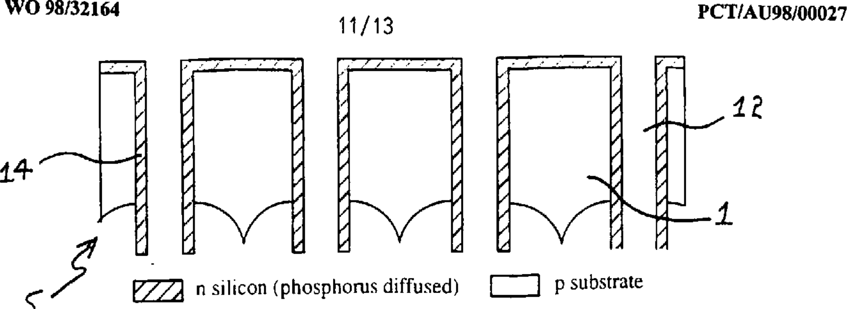


Figure 28

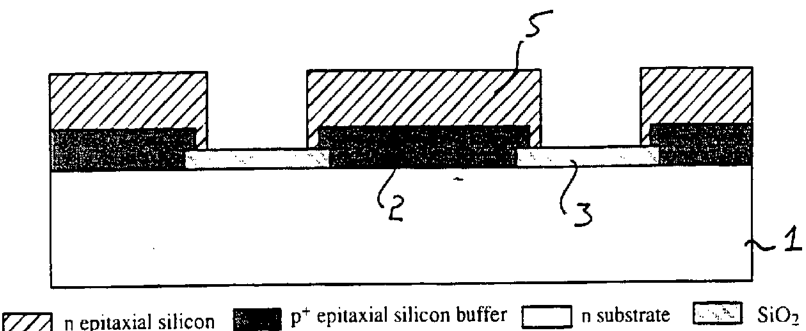


Figure 29

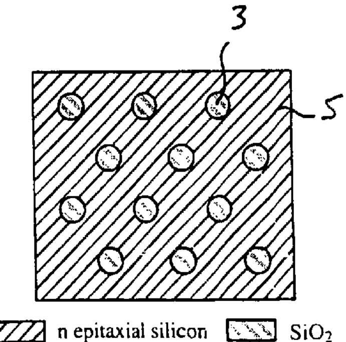


Figure 30

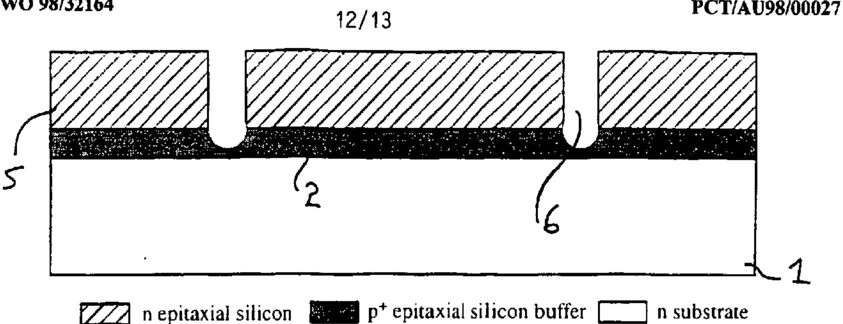


Figure 31

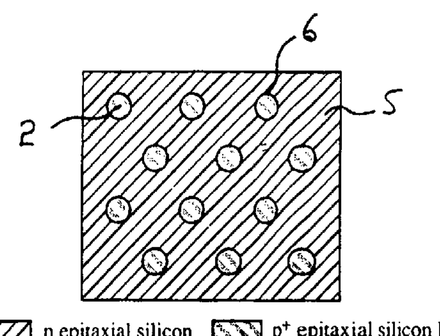


Figure 32

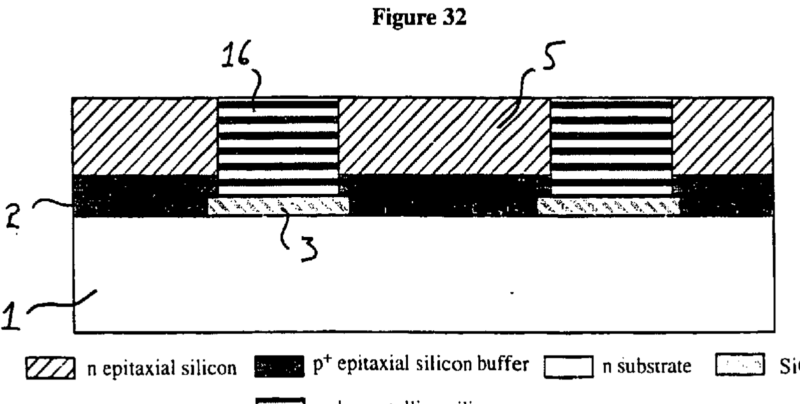
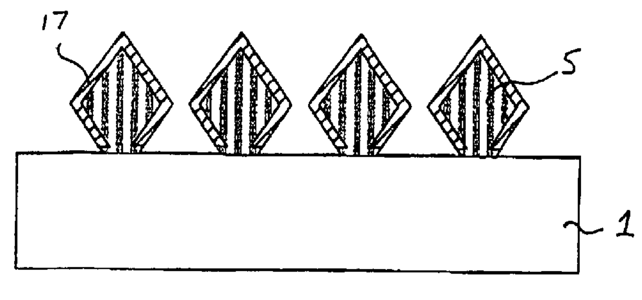
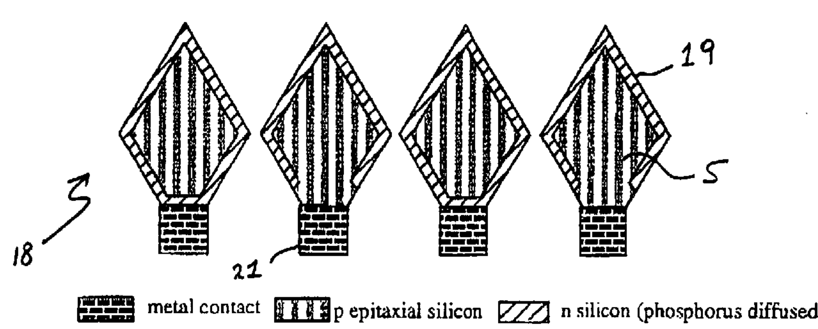


Figure 33



n silicon (phosphorus diffused) p^+ silicon substrate p epitaxial silicon

Figure 34



metal contact p epitaxial silicon n silicon (phosphorus diffused)

Figure 35