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[54] TIME DEPENDENT FAULT DETECTOR

[75] Inventor: **Thomas J. Mooney**, Fairport, N.Y.

[73] Assignee: **Xerox Corporation**, Stamford, Conn.

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[52] **U.S. Cl.** **307/116;** 355/14
[51] **Int. Cl.²** **G03G 15/00**
[58] **Field of Search** 340/309.1, 309.6; 307/94, 307/116; 355/14; 271/57

[56] **References Cited**

UNITED STATES PATENTS

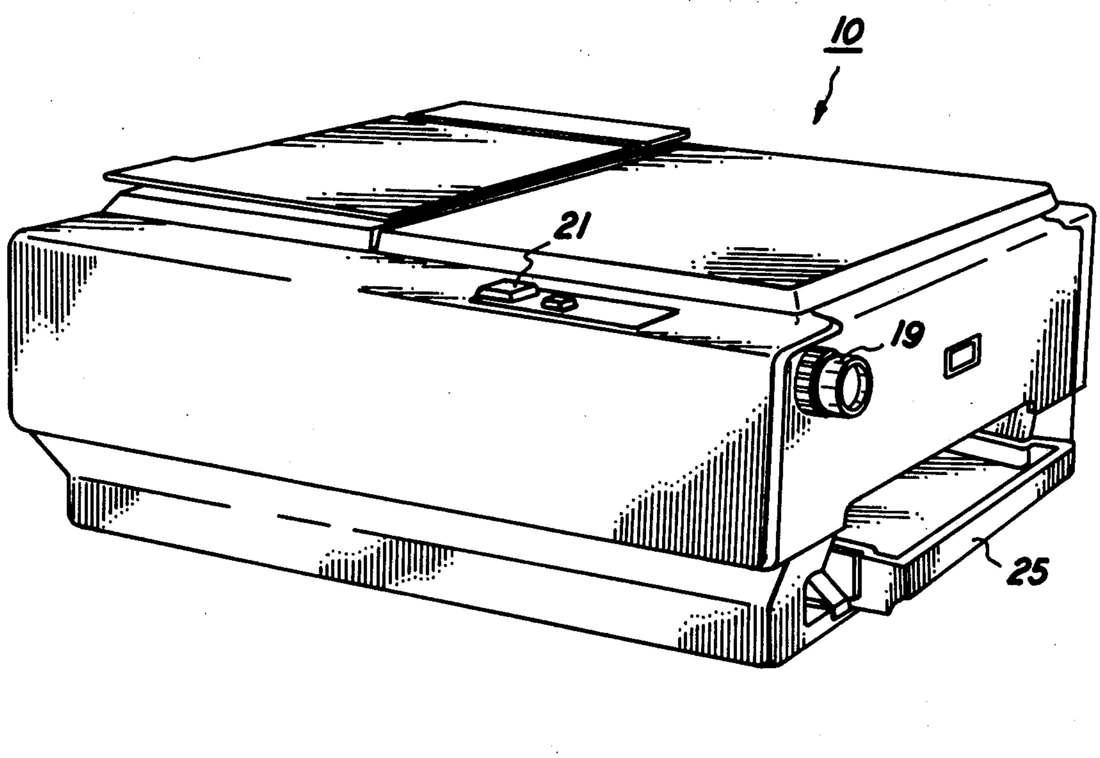
3,734,604 5/1973 Szostak et al. 355/14

Primary Examiner—Herman J. Hohauser

[57] **ABSTRACT**

The RC time constant of a timer in a time dependent fault detector is automatically varied so that the timer may be used to monitor a plurality of mutually exclusive routines to which different maximum permissible periods of time are alloted. For example, the detector may be advantageously used to interrupt the operation of a xerographic copier if any one of a plurality of operating sequences of the copier is not completed on a timely basis.

4 Claims, 3 Drawing Figures



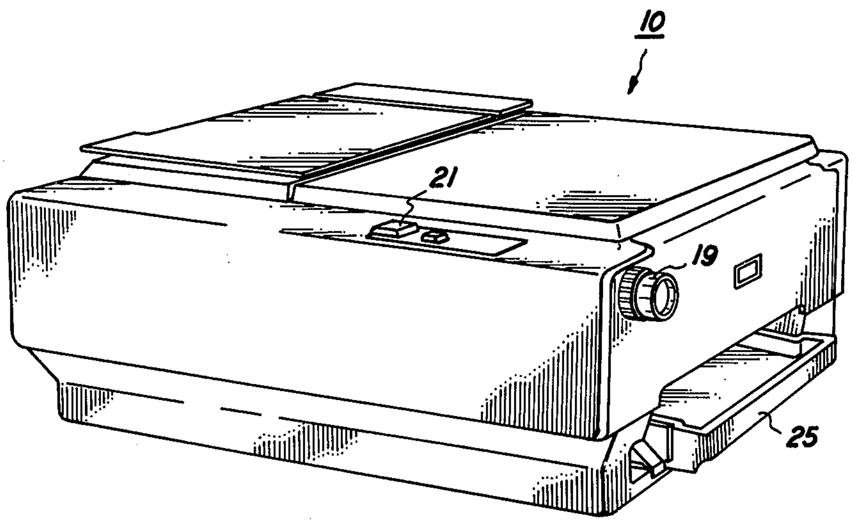

10
21
19
25

FIG. 1

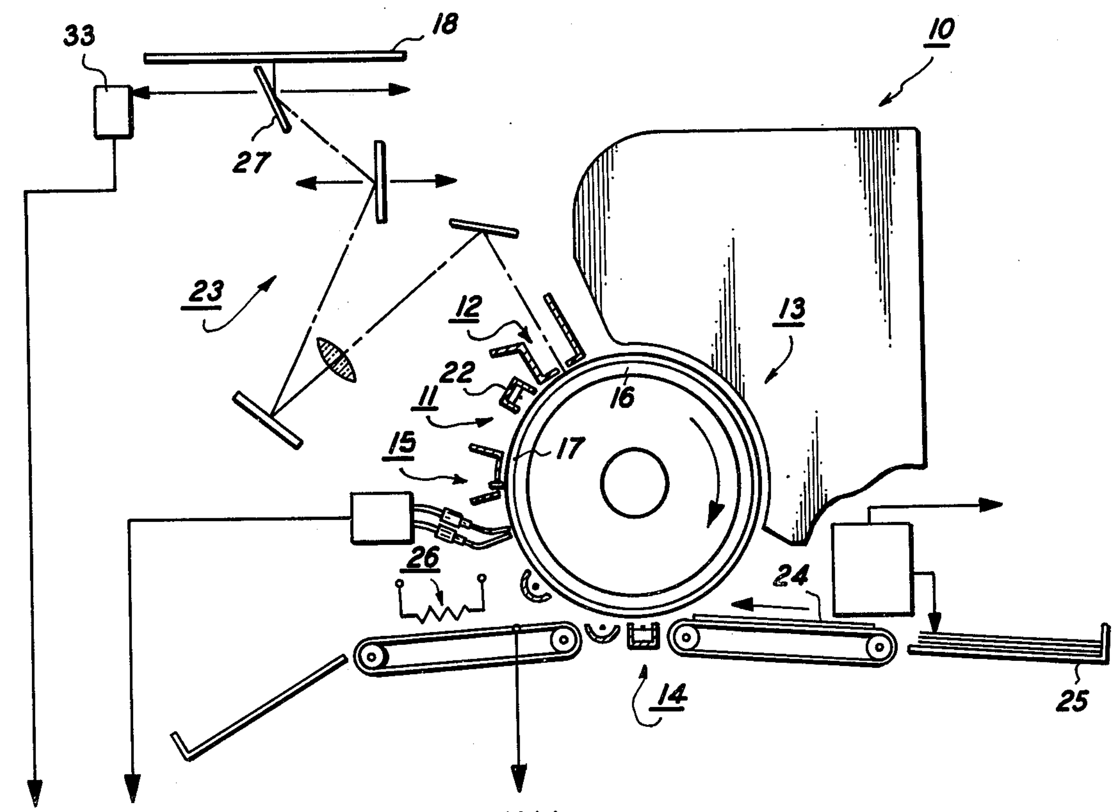

33
18
10
27
23
12
22
11
15
13
16
17
26
24
14
25
SCAN
JAM
JAM

FIG. 2

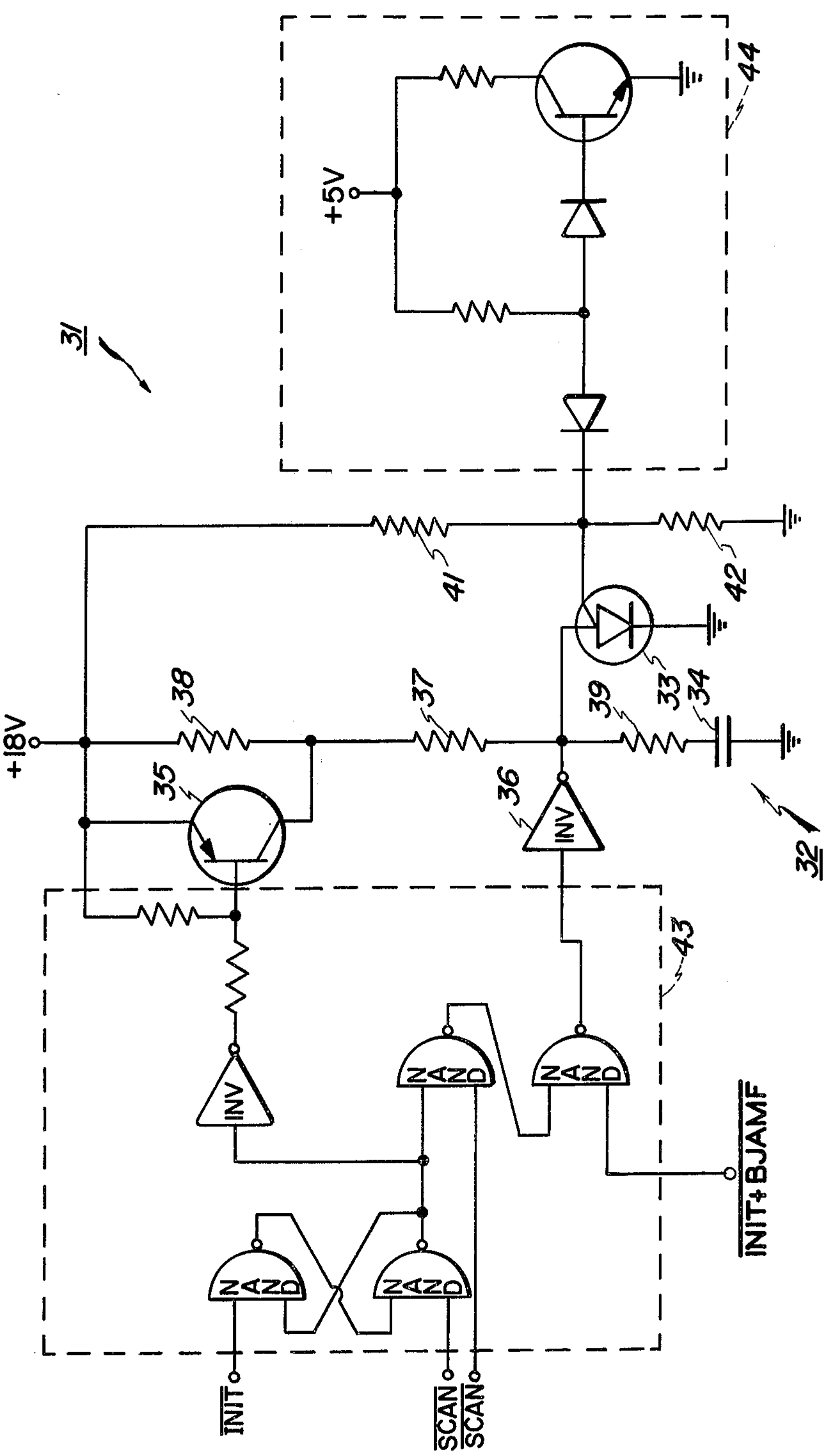

+18V
+5V
INIT
SCAN
SCAN
INIT+BJAMF
INV
NAND
31
32
33
34
35
36
37
38
39
41
42
43
44

FIG. 3

TIME DEPENDENT FAULT DETECTOR

BACKGROUND OF THE INVENTION

This invention relates to failure detectors and, more particularly, to time dependent failure detectors.

As is known, time dependent failure detection is a relatively straightforward technique for monitoring any routine which normally advances from one identifiable point to another within a predetermined amount of time. To carry it out, there typically is a timer having a time out period selected to equal the maximum time period required by a particular routine under normal operating conditions, means for triggering the timer into operation when the routine reaches the first or reference point, and means for resetting the timer when the routine reaches the other or termination point. Thus, if the timer times out, it indicates that there has been a departure from nominal conditions or, in other words, that a failure has occured.

On occasion, several different time dependent fault detectors are used in the same machine or process to monitor mutually exclusive routines, especially when those routines are alloted different amounts of time. As will be seen, this invention eliminates the need for resorting to that wasteful practice.

SUMMARY OF THE INVENTION

More particularly, one of the important objects of the present invention is to provide a time dependent fault detector which may be utilized to monitor a plurality of mutually exclusive routines, even if those routines are alloted different amounts of time.

Another object of this invention is to provide a method and means for automatically adjusting the time out period of a time dependent fault detector to match the maximum amount of time alloted to any one of a plurality of mutually exclusive routines.

A further object of this invention is to provide a time dependent fault detector for automatically interrupting the operation of a xerographic copier if any one of a plurality of mutually exclusive operating sequences is not completed on a timely basis.

Still another object of the present invention is to provide a reliable and economical time dependent fault detector having the above-mentioned characteristics and capabilities.

In keeping with these and other objects, means are provided in accordance with this invention for automatically adjusting the time out period of a timer in a time dependent fault detector. Mutually exclusive routines to which different maximum time periods are alloted can, therefore, be monitored by a single detector since the time out period of the timer may be adjusted to match any one of them. Adjustment of the time out period is conveniently accomplished by switching a transistor into and out of conduction to thereby vary the RC time constant of the timer.

BRIEF DESCRIPTION OF THE DRAWINGS

Still further objects and advantages of the present invention will become apparent when the following detailed description is read in conjunction with the attached drawings, in which:

FIG. **1** is a perspective view of a xerographic copier with which the present invention may be advantageously utilized;

FIG. **2** is a simplified schematic of the processor section of the copier shown in FIG. **1**; and

FIG. **3** is a schematic of a time dependent fault detector constructed in accordance with the present invention.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENT

While the invention is described in some detail hereinafter with reference to a specific embodiment, it is to be understood that there is no intent to limit it to that embodiment. On the contrary, the intent is to cover all modifications, alternatives, and equivalents falling within the spirit and scope of the invention as defined by the appended claims.

Turning now to the drawings, and at this point especially to FIGS. **1** and **2,** there is a xerographic copier **10** having a charging station **11,** an exposure station **12,** a development station **13,** a transfer station **14** and a cleaning station **15** disposed about the periphery of a drum **16** which is coated with a photoreceptor **17.** In operation, an original document is placed image side down on a transparent platen **18,** a dial **19** is set to the desired number of copies, and a print button **21** is depressed to initiate the copying process.

Copying starts with the energization of a corona generator **22** at the charging station **11** to uniformly charge the photoreceptor **17.** The original document is flood illuminated by a suitable lamp (not shown) and is then scanned by a moving optics system **23** so that light reflected from the document is focused on the photoreceptor **17** at the exposure station **12.** The reflected light discharges the photoreceptor **17** in an imagewise configuration to thereby provide a latent electrostatic image. The latent image is developed at the development station **13** by the application of an electroscopic toner powder, and the developed image is then transferred at the transfer station **14** to a copy sheet **24** which is fed from a cassette-type supply tray **25.** Finally, to complete the process, the toner image is permanently affixed to the copy sheet **24** at a fuser station **26** and residual toner is removed from the photoreceptor **17** at the cleaning station **15.**

As will be appreciated, there are a number of routines which must be successfully completed on a timely basis to make a satisfactory copy, and some of those routines are mutually exclusive. For example, in the optics system **23** there is a full rate scanning mirror **27** which is mounted on a carriage (not shown) to be reciprocatingly driven between a home positioned beneath the left-hand margin of the platen **18** (as viewed in FIG. **2**) and an end of scan position beneath the opposite or right-hand margin of the platen **18,** as described in more detail in a copending and commonly assigned application of W. F. Hoppner, which was filed June 6, 1973 under Ser. No. 367,996 on an "Exposure Apparatus." In the ordinary course, the scanning mirror **27** returns to its home position at the outset of each copy cycle and then moves towards its end of scan position to scan the original document. Jam detection and copy quantity control are, therefore, provided for this particular copier through the use of a microswitch **28** which is positioned to be actuated when the scanning mirror **27** is in its home position and deactuated when the mirror **27** is in any other position. Specifically, the jam detection and copy quantity logic are dependent on the successful and repeated actuation of the microswitch **28,** as more fully explained in a copending and commonly assigned application of L. J. Fantozzi, which was filed Apr. 6, 1973 under Ser. No. 348,828 for "Control Circuitry for Trouble Detection and Recovery System in a Copier/Duplicator." Accordingly, if there is a failure within the drive mechanism (not shown) for the optics system 23 or of the microswitch **28,** jam detection and copy quantity control are lost, thereby creating the risk of a run away machine condition and of smoke and odor from undetected jams.

Analysis of this particular copier reveals that a failure of the drives for the optics 23 or of the microswitch **28** is indicated whenever that switch (1) is not actuated within six seconds or so after the print button **21** is depressed or (2) remains actuated during the copying cycle for more than about six tenths of a second. Time dependent failure detection may, therefore, be advantageously utilized. But there are a pair of mutually exclusive routines to be monitored, and those routines are alloted different amounts of time.

Referring to FIG. **3**, there is a time dependent fault detector **31** which is capable of monitoring mutually exclusive routines, even if they are alloted different amounts of time. The capabilities of the detector **31** have been synergistically extended in accordance with this invention by including a timer **32** having an automatically adjustable time out period. To that end, as shown, the timer **32** comprises a three terminal thyristor **33** which is switched from one state of conduction to the other when a timing capacitor **34** charges to a predetermined voltage level. The charging time constant for the capacitor **34** is adjusted under the control of a transistor **35** to thereby match the time out period of the timer **32** to the particular routine being monitored, and the timer **32** is triggered into operation and reset under the control of an inverter **36.**

More particularly, in the illustrated embodiment, current is drawn from a dc. power supply through a resistor **37** and the parallel combination of collector-emitter circuit of the transistor **35** and another resistor **38.** The output of the inverter **36** is connected in parallel with the series combination of the timing capacitor **34** and a further resistor **39** in the ground return path for that current flow. Thus, the current drawn from the dc. power supply is returned to ground through the timing capacitor **34** and it series resistor **39** or through the output of the inverter **36** depending on the logic level of the input signal applied to the input of the inverter **36.** Specifically, if that signal is at a high (1) logic level, the timer **32** is triggered into operation because the current is routed through the timing capacitor **34** to charge it toward the critical voltage level. If, on the other hand, a low (0) logic level signal is applied to the inverter **36,** its output provides a relatively low impedance shunt path to ground for the current drawn from the dc. power supply and for any discharge current drawn by the capacitor **34.**

Now, when the timer **32** is triggered into operation, its time out period depends on the state of conduction of the transistor **35.** If that transistor is in a nonconductive state, the RC charging time constant for the timing capacitor **34** is relatively long and the time out period of the timer **32** is, therefore, relatively long. But, if the transistor **35** is in a conductive state, the resistor **37** is effectively bypassed and, consequently, the charging time constant for the capacitor **34** is reduced to thereby reduce the time out period of the timer **32.**

To ensure that the timer **32** is relatively insensitive to ordinary fluctuations in the output current of the dc. supply source, the thyristor **33** is a programmable unijunction transistor (PUT). As shown, the PUT **33** has its anode-cathode circuit coupled across the timing capacitor **34** and the resistor **39** and its gate coupled to a junction between a pair of voltage dividing resistors **41** and **42** which, in turn, are connected across the dc. supply source. As a result, there is a gate-cathode bias voltage which holds the PUT **33** in a non-conductive state until the timer **32** times out. When that occurs, however, the PUT **33** switches into conduction because there then is sufficient voltage across the timing capacitor **34** to cause the anode-cathode voltage on the PUT **33** to exceed its gate-cathode bias voltage. In other words, time out of the timer **32** is marked by a significant drop in the gate-cathode voltage of the PUT **33.**

The input and output interfaces **43** and **44,** respectively, for the detector **31** are more or less tailored to its particular application to the copier **10** (FIGS. **1** and **2**). That is, they are selected, together with the values of the capacitor **34** and of the resistors **37–39** and **41–42,** to interrupt the operation of the copier **10** if the microswitch **28** (1) is not actuated within six seconds or so after the print button **21** is depressed or (2) remains actuated for more than about six tenths of a second at any time during a copying cycle. Indeed, to accomplish that, the input interface relies on certain signals that are supplied by the copier **10** — viz., (a) an initializing signal (INIT) which drops from a high (1) logic level to a low (0) logic level approximately 20 milliseconds after the print button **21** is depressed, (b) a scan signal (SCAN) which is at a high (1) or a low (0) logic level depending on whether the microswitch **28** is actuated or not, and (c) a run signal (INIT + BJAMF) which is herein assumed to simply be the complement of the initializing signal (INIT). For a description of the provision made in the copier **10** to supply those signals, reference may be had to the aforementioned application Ser. No. 348,828.

Inasmuch as the interfaces **43** and **44** form no part of the present invention, other than to mate the detector **31** with the copier **10,** there is no reason to burden this disclosure with a detailed discussion of them. Indeed, the drawings provide sufficient detail to make their operation self-evident.

CONCLUSION

In view of the foregoing, it will now be appreciated that the present invention provides a time dependent fault detector suitable for monitoring a plurality of mutually exclusive routines, even if different amounts of time are alloted to those routines.

What is claimed is:

1. In combination with a xerographic copier having a plurality of mutually exclusive routines each alloted a different amount of time, a time dependent fault detector for interrupting the operation of said copier whenever any one of said routines fails to be completed within the time alloted thereto; said detector comprising a timing capacitor, a resistive path for supplying charging current for said capacitor, a shunt path coupled in parallel with said capacitor for bypassing said charging current around said capacitor until one of said routines is initiated, means responsive to the initiation of any one of said routines for disabling said shunt path to thereby trigger said timer into operation, and means for selectively bypassing a portion of the resistance in said path to thereby adjust the time out period of said timer to match the time alloted to said one routine.

2. The combination of claim 1 wherein said timer further includes a thyristor which switches from one state to another when said capacitor charges to a predetermined voltage level, thereby marking time out of said timer.

3. The combination of claim 2 wherein said thyristor is a programmable unijunction transistor having an anodecathode circuit and a gate-cathode circuit, and said capacitor is coupled across said anode-cathode circuit; and further including means for applying a bias voltage to said gatecathode circuit, whereby said programmable unijunction transistor switches from a nonconductive state to a conductive state when said timer times out.

4. The combination of claim 3 wherein said bypass means includes a transistor having a collector-emitter circuit connected in parallel with said resistance, whereby the time out period of said timer is adjusted by switching said transistor into and out of conduction.

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