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Naka

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[45] **May 22, 1973**

[54] **DISPLAY APPARATUS UTILIZING CATHODE RAY TUBES**

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[73] Assignee: **Ise Electronics Corporation**, Ise, Japan

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Jan. 30, 1970 Japan 45/7957

[52] **U.S. Cl.** .....**340/324 A**, 315/22

[51] **Int. Cl.** **G06f 3/14**

[58] **Field of Search** .....340/324 A, 324 AD; 315/22, 30

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Primary Examiner—John W. Caldwell
Assistant Examiner—Marshall M. Curtis
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[57] **ABSTRACT**

In a display apparatus utilizing a cathode ray tube, the tube is provided with a dot matrix electrode and the apparatus is provided with a plurality of memories for different types of patterns and connected with the matrix electrode, an address register for storing the positions on the screen at which selected patterns are to be displayed, a memory for storing the information regarding the patterns to be displayed, means responsive to the outputs from the address register and the memory for selectively driving the plurality of memories and means for supplying deflection current to the deflection coil of the cathode ray tube in synchronism with the outputs from the plurality of memories.

10 Claims, 13 Drawing Figures

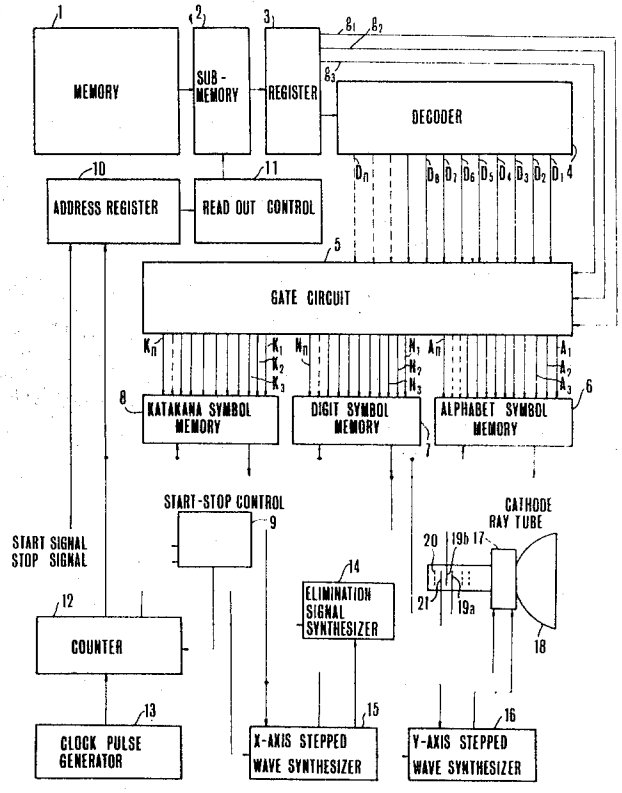

FIG. 1

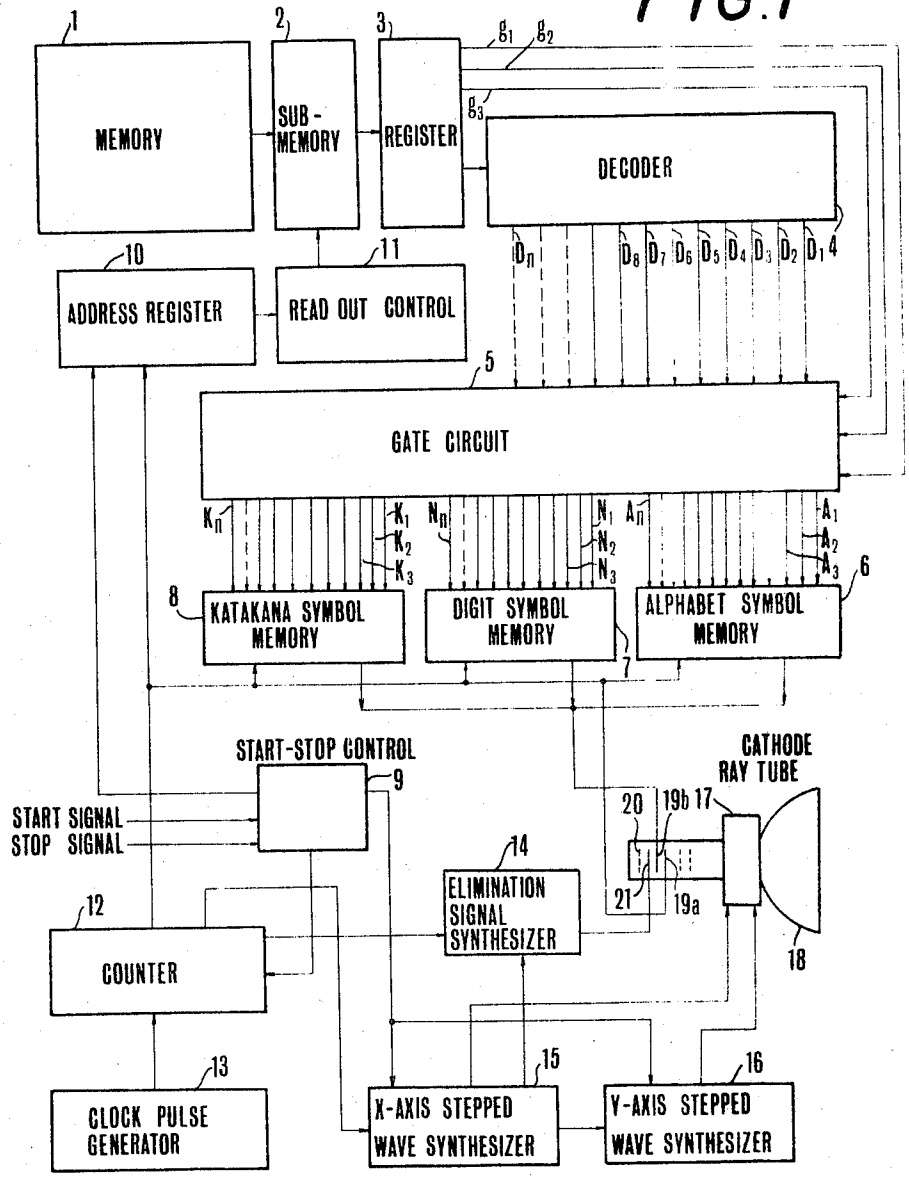

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FIG. 2a

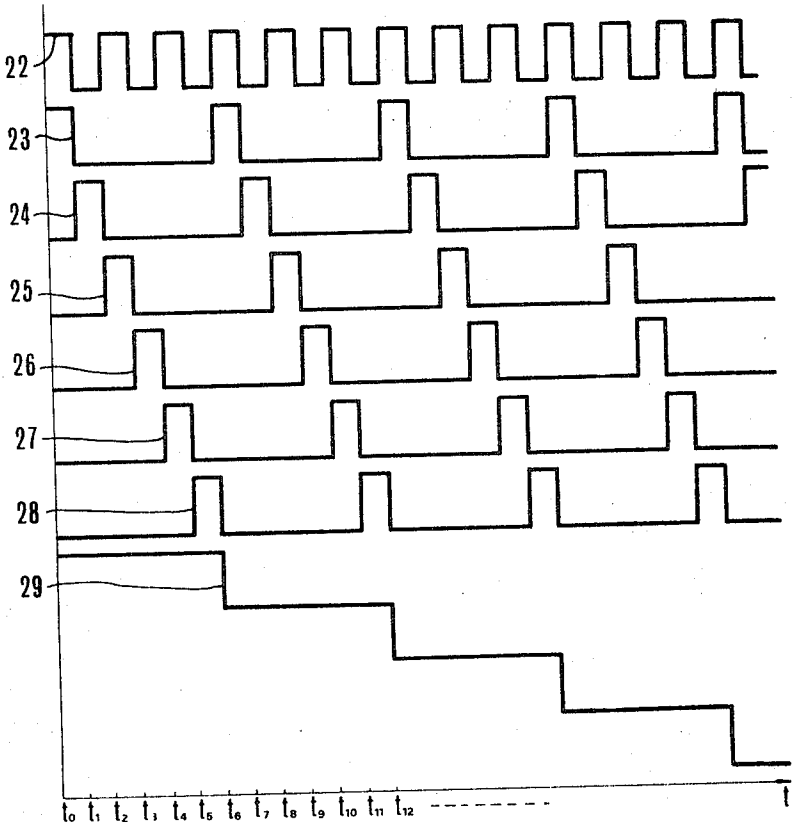

FIG. 2b

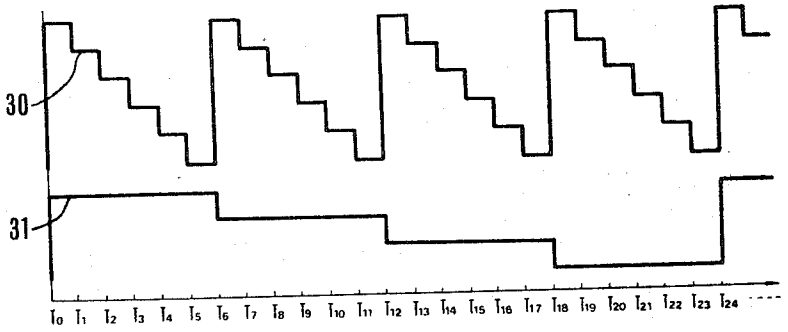

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FIG. 3

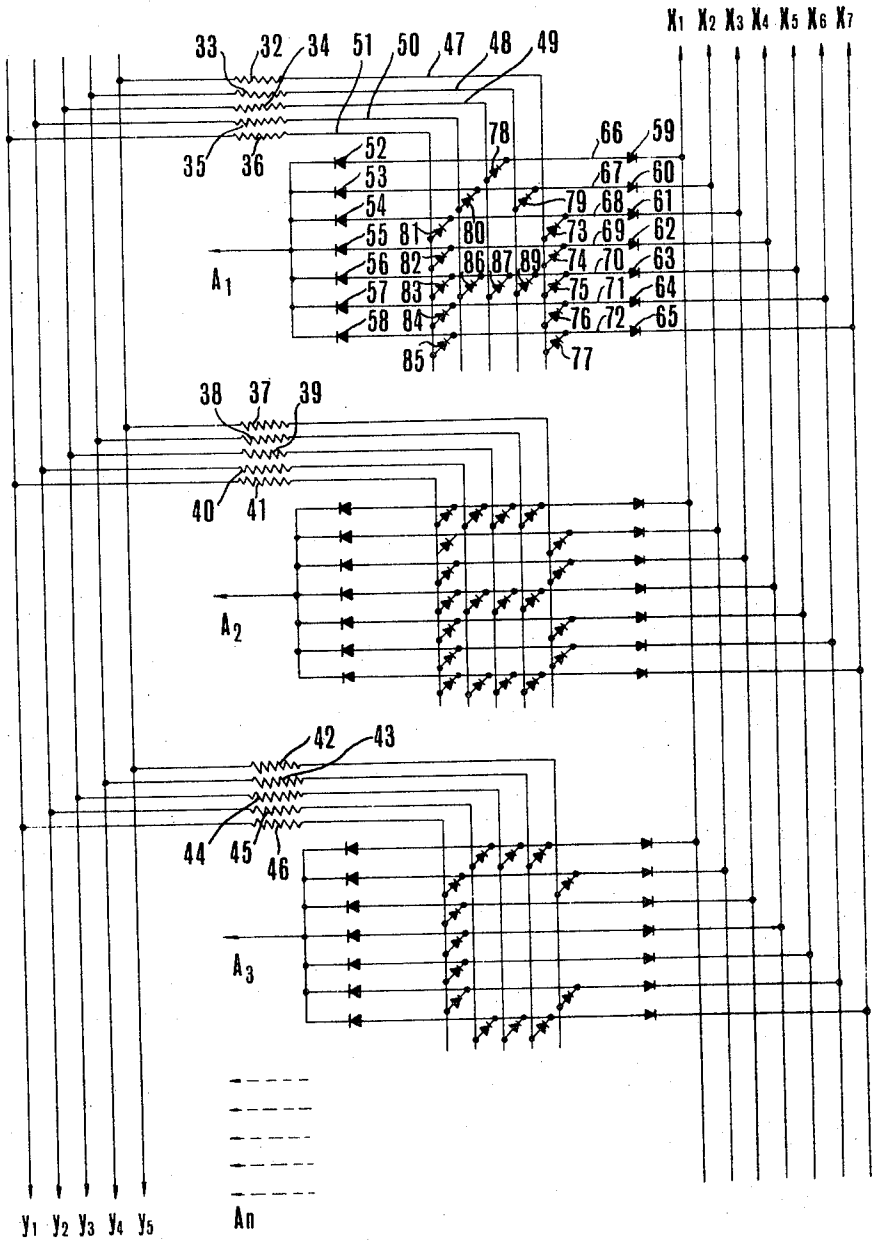

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FIG.4

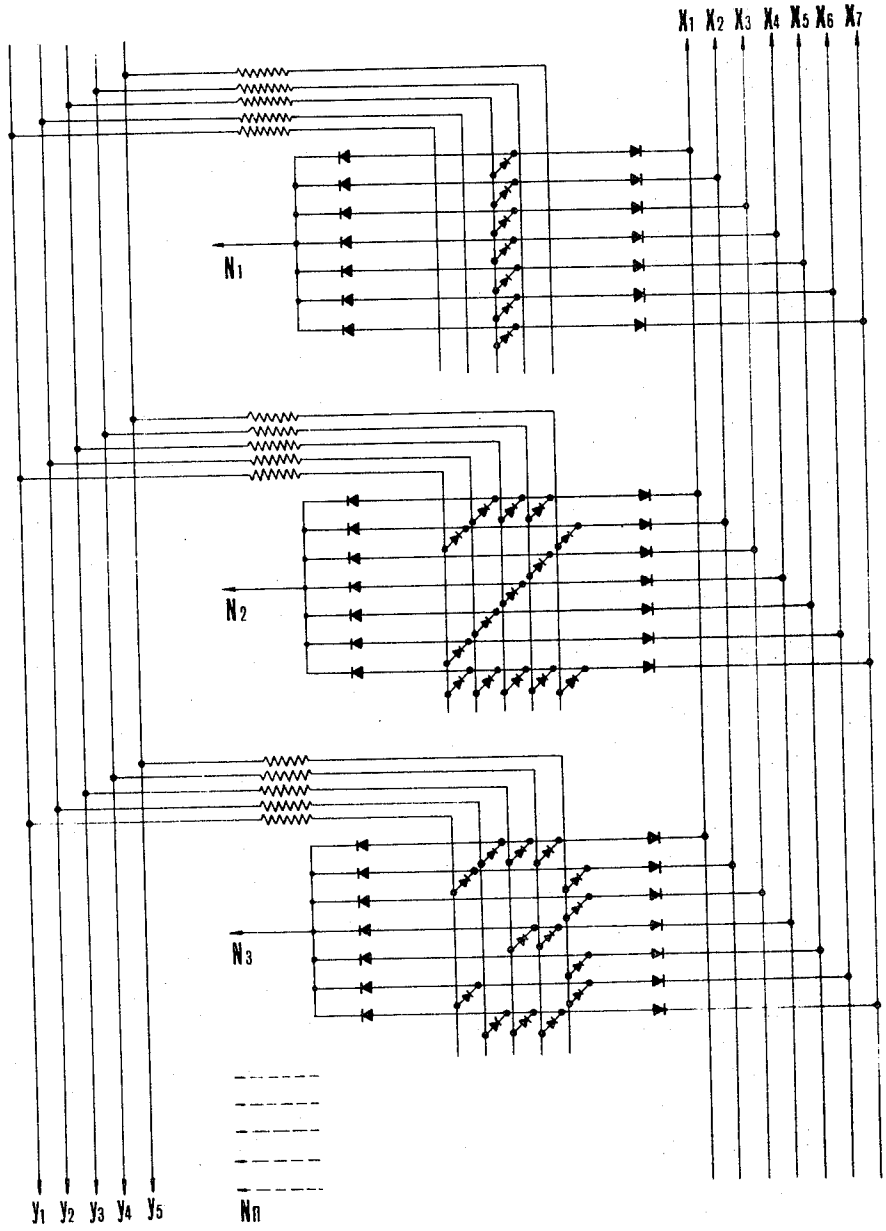

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FIG.5

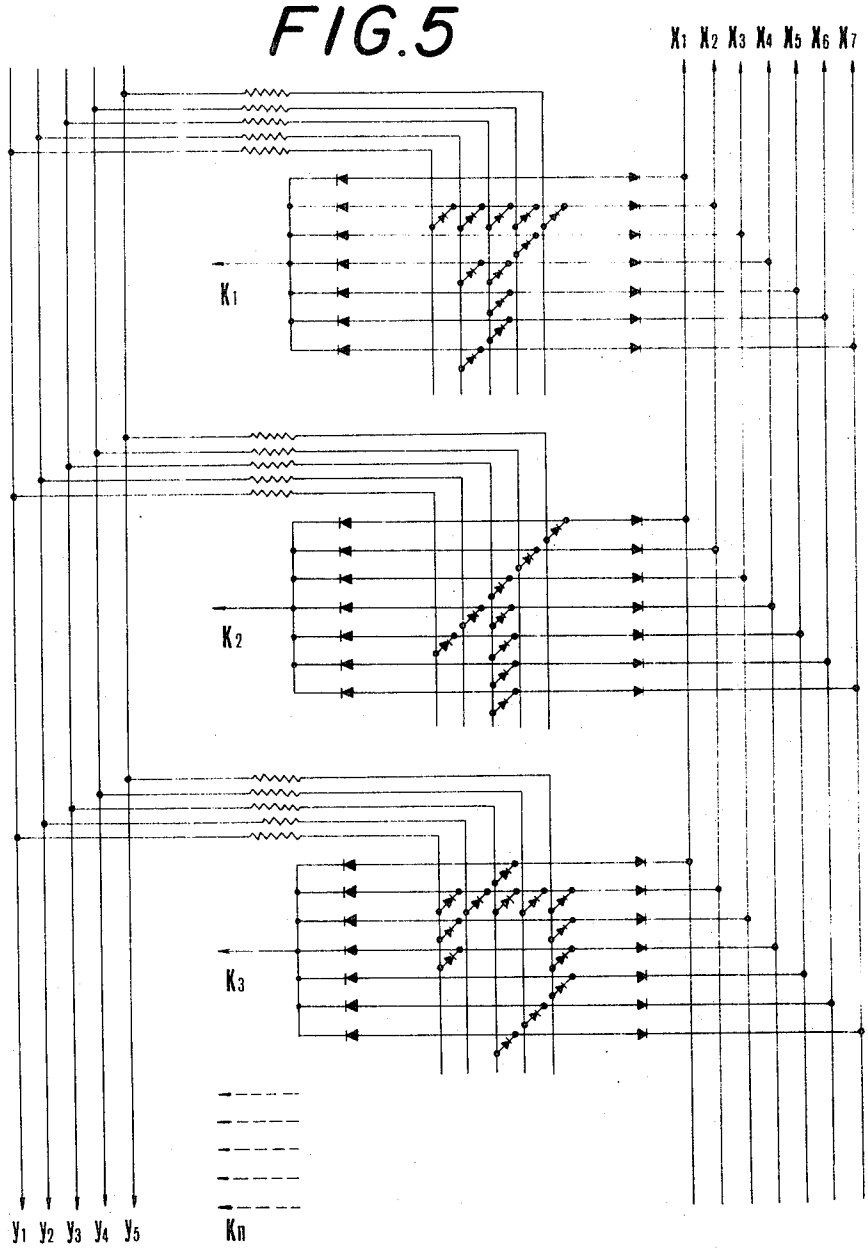

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FIG.6

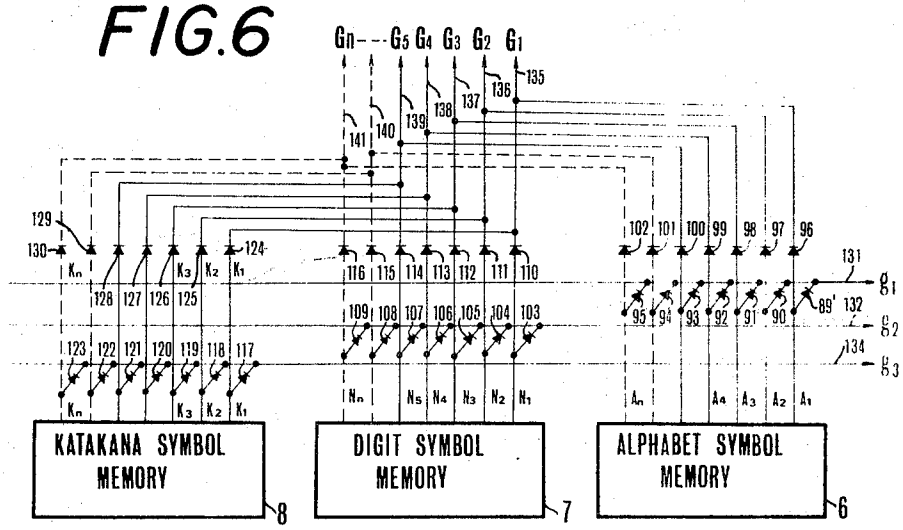

FIG.7a

I	S	E	D	E	N
イ	セ	デ	ン	シ	コ
1	2	3	4	5	6
A	8	ウ	7	B	E

FIG.7c

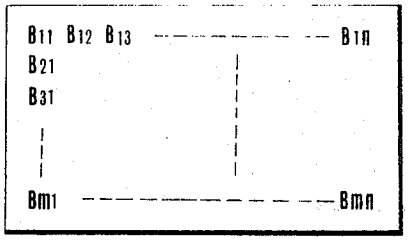

FIG.7b

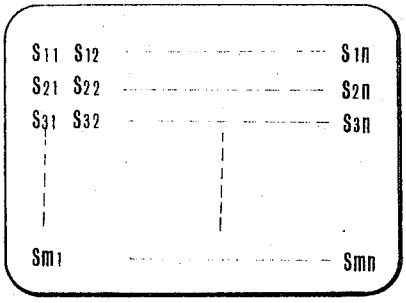

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FIG. 8

	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}
B_{11}	1	0	0	0	0	0	0	0	0	0	0	0	0
B_{12}	0	1	0	0	0	0	0	0	0	0	0	0	0
B_{13}	0	0	1	0	0	0	0	0	0	0	0	0	0
B_{14}	0	0	0	1	0	0	0	0	0	0	0	0	0
B_{1n}	0	0	0	0	0	0	0	0	0	0	0	0	0

D_n	g_1	g_2	g_3
0	1	0	0
0	0	1	0
0	0	0	1
0	1	0	0
1	0	1	0

FIG. 9

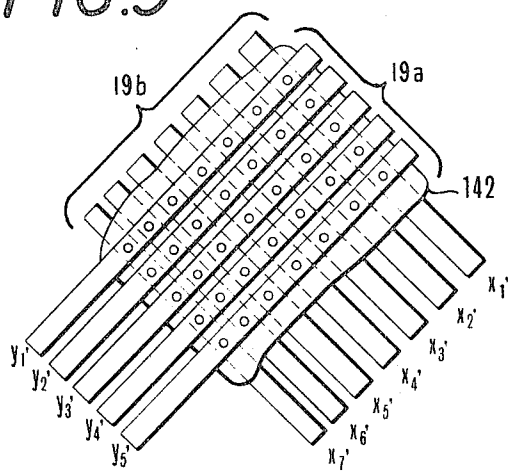
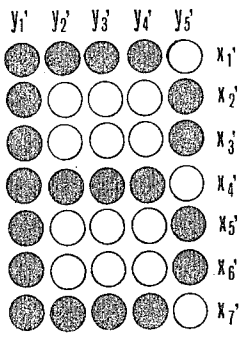


FIG. 10



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DISPLAY APPARATUS UTILIZING CATHODE RAY TUBES

BACKGROUND OF THE INVENTION

This invention relates to apparatus for displaying information regarding, letters, digits, symbols and the like which are stored being stored in a memory of an electronic computer, for example, and more particularly display apparatus utilizing a cathode ray tube employing a dot matrix.

Although many types of display apparatus have been proposed in the past, each and all of them were not perfectly satisfactory.

More particularly, with one type of prior apparatus, use is made of a special cathode ray tube called the beam forming type wherein a letter electrode stamped with letters, digits or symbols is disposed in front of an electron gun and a potential is applied to a deflection electrode disposed in front of the letter electrode on the side of the cathode electrode to select a desired letter, digit or symbol to cause one portion of the letter electrode to pass electrons and remaining portions of the letter electrode to block the electrons. Electrons passed through the letter electrode display the desired letter, digit or symbol on the desired portion of the fluorescent screen of the cathode ray tube. However, with this apparatus dispersion of the electron beam causes poor resolution of lines of the pattern. In addition, with this apparatus, unless the selection of the letter and the like and the deflection voltage are correct, letters adjacent the selected letter are often displayed on the screen. Further, since the selection of the letter is made by an analogue quantity, the operation of the display device is unstable, and since the number of letters and the like which can be formed on the letter electrode is limited, it is impossible to display a large number of letters and the like.

A second prior apparatus is called the dot system according to which a single electron beam is driven to successively scan a letter electrode longitudinally or transversely and when the beam reaches the desired point of the letter electrode the intensity of the beam is increased to cause the corresponding point on the screen to luminesce. Portions not wanted to luminesce are applied with a brightness eliminating signal. This elimination signal is used to select the memory of the letter and the like comprising a group of circuits for displaying the selected letter and the like on a screen by dots. However, with this second type of the apparatus, utilizing scanning lines, in order to display a large number of letters and the like, it is necessary to greatly reduce the scanning period thus complicating the apparatus. Moreover, as the periods of the signals applied to various components are short, it is impossible to display stably the letters and the like.

A third apparatus is termed the segment synthesis system. This system is similar to the dot system described above except that portions between dots are not eliminated but are displayed as a segment of a continuous bright line to display letters and the like. According to this apparatus, vertical, horizontal and inclined segments are stored in a memory and the codes of the stored segments separated from a definite reference point are read out and the read out codes are applied to a deflection coil through a digital-analogue converter to display letters and the like. The operation of this apparatus is unstable because the periods of the vertical and horizontal deflection signals are short. Further, stability of the apparatus is degraded due to aging because the read out codes are converted into analogue quantities for displaying letters and the like.

A fourth apparatus utilizes the Lissajous' pattern wherein waveforms of continuous functions are applied to both vertical and horizontal deflection coils to display letters and the like with Lissajous' patterns. More particularly, the phase relation between the time function of the function wave and the higher harmonic components obtained by subjecting the time function to the Fourier transformation is calculated so as to cause only portions necessary to display letters and the like to luminesce. Although letters displayed by this apparatus are well defined and clear it is necessary to provide a function wave generator for each letter so that the apparatus becomes complicated. Again the operation of the apparatus is unstable because letters and the like are also displayed by analogue quantities.

A fifth apparatus utilizes a special cathode ray tube provided with seven electron beams. The seven dots displayed on the screen by seven electron beams are comprised by bright dots selected by a matrix electrode disposed in the cathode ray tube and eliminated dots. Since these seven dots are sequentially deflected by deflection coils, the patterns of letters and the like are displayed by the dots under the control of a signal supplied from an external letter memory. With this apparatus, however, a letter can not be formed unless the beams are deflected.

SUMMARY OF THE INVENTION

It is therefore the principal object of this invention to eliminate any and all of the problems of the prior apparatus.

Another object of this invention is to provide a novel display cathode ray tube wherein selected ones of a plurality of letters, digits, symbols and like patterns can be displayed on the display screen of the cathode ray tube without the necessity of deflecting the electron beam to form the letter, digit, symbol or pattern.

A further object of this invention is to provide a new and improved display apparatus which can display clearly and stably different types of letters.

Still another object of this invention is to provide a display apparatus capable of displaying letters of different types with a simplified circuit construction without the necessity of utilizing any digital-analogue converter.

Yet another object of this invention is to provide a novel display apparatus capable of displaying a large number of letters, digits and symbols of different type.

More specific object of this invention is to provide an improved display apparatus of compact design suitable for use in desk type electronic computers.

According to this invention, these and further objects can be accomplished by providing a display apparatus comprising a cathode ray tube including a cathode electrode, a matrix electrode, a display screen, and a deflection coil disposed between the matrix electrode and the display screen ; a plurality of discrete memories connected to the matrix electrode, the memories being provided for different groups of patterns of the letters, digits and symbols to be displayed on the screen ; address memory means for storing the positions on the screen at which the selected patterns of the letters, digits and symbols are to be displayed ; information mem-

ory means for storing the information regarding the patterns to be displayed ; means responsive to the outputs from the address memory means and the information memory means for selectively driving the plurality of memories for the groups of patterns, and means for supplying deflection signals to the deflection coil in synchronism with the outputs from the plurality of memories.

BRIEF DESCRIPTION OF THE DRAWINGS

Further objects and advantages of the invention will become apparent from the following detailed description taken in conjunction with the accompanying drawings in which :

FIG. **1** shows a block diagram showing the basic construction of the novel display apparatus utilizing the cathode ray tube embodying this invention ;

FIGS. **2***a* and **2***b* are waveforms to explain the operation of respective blocks shown in FIG. **1** ;

FIGS. **3, 4** and **5** are connection diagrams showing examples of memories of symbols of alphabets, digits, and "katakanas" (Japanese alphabets) shown in FIG. **1** ;

FIG. **6** shows one example of an electrical connection of a gate circuit shown in FIG. **1**;

FIGS. **7***a*, **7***b* and **7***c* show the patterns displayed on the screen of the cathode ray tube, and the correspondence between the positions of the patterns, and the addresses of the sub-memory ;

FIG. **8** shows a truth table showing the state of address symbols memorized in a register ;

FIG. **9** shows a construction of a dot matrix electrode utilized in the cathode ray tube shown in FIG. **1** and

FIG. **10** is an enlarged view of one example of the pattern displayed on the display screen of the cathode ray tube.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to FIG. **1** showing a general block diagram of a display apparatus utilizing the novel cathode ray tube, the output from a memory **1** is coupled to a sub-memory, whose output is coupled to a register **3.** The major portion of the outputs from register **3** is coupled to a decoder **4** which in turn is connected to a gate circuit **5** via conductors $D_1, D_2 \ldots D_n$. The remaining portion of the outputs from register **3** is directly coupled to gate circuit **5** through conductors g_1, g_2 and g_3.

A portion of the output from gate circuit **5** is coupled to an alphabet symbol memory **6** over conductors A_1, $A_2 \ldots A_n$, another portion to a digit symbol memory **7** over conductors $N_1, N_2 \ldots N_n$ whereas the remaining portion to a katakana symbol memory **8** over conductors $K_1, K_2 \ldots K_n$. The outputs from these memories **6, 7** and **8** are supplied to a dot matrix electrode portion **19**b of a cathode ray tube **18.**

A clock pulse generator **13** is connected to a counter **12.** A portion of the output from counter **12** is coupled to alphabet symbol memory **6,** digit symbol memory **7** and Katakana symbol memory **8,** another portion of the output from counter **12** is supplied to an address register **10** whereas the remaining portion is fed to a X-axis stepped wave synthesizer **15.** The output from the address counter **10** is coupled to a read out control **11,** the output thereof being coupled to the sub-memory **2.** A portion of the output from the X-axis stepped wave synthesizer **15** is supplied to the deflection coil **17** of the cathode ray tube **18** and another portion of the output from X-axis stepped wave synthesizer is coupled to a Y-axis stepped wave synthesizer **16** also comprising a deflection circuit of the cathode ray tube. Hence the output from the synthesizer **16** is also connected to the deflection coil **17.**

To the inputs of a start-stop control **9** are supplied a start signal and a stop signal generated by an external source such as an electronic computer, not shown, and the outputs from the start-stop control are supplied to X-axis stepped wave synthesizer **15,** Y-axis stepped wave synthesizer, address register **10** and counter **12,** respectively.

FIGS. **2***a* and **2***b* show output waveforms helpful to explain the operation of various components shown in FIG. **1,** wherein the abscissas represent the time and the ordinates the voltage or current, t_1, t_2, $t_3 \ldots$ show various times at which more than one waveform varies. In FIG. 2a, a reference numeral **22** represents the waveform of the output voltage of the clock pulse generator **13,** reference numerals **23** to **28** show output waveforms of counter **12, 29** the output from the X-axis stepped wave synthesizer **15,** that is the waveform of the current flowing through deflection coil **17.** In FIG. **2***b*, waveform **30** shows on a different time basis the same waveform as that shown by **29** in FIG. **2***a*, that is the waveform of the output from the X-axis stepped wave synthesizer that flows through deflection coil **17,** whereas **31** shows the waveform of the output from the Y-axis stepped wave synthesizer **16** or the waveform of the current flowing through deflection coil **17.** It should be understood that the waveforms **30** and **31** are not limited to the illustrated examples and that the number of steps of these waves varies dependent upon the number of arrays of the letter or digit symbols to be displayed on the screen of the cathode ray tube **18.** $T_0, T_1 \ldots$ on the time axis t of FIG. **2***b* represents the times at which one or both of waveforms **30** and **31** vary.

FIGS. **3, 4** and **5** show typical connection diagrams of the alphabet symbol memory **6,** the digit symbol memory **7** and the katakana symbol memory **8,** respectively shown in FIG. **1.** In these figures, y_1 through y_5, respectively corresponding to waveforms **24** through **28** shown in FIG. **2***a*, represent the same conductors. Also conductors x_1 through x_7 shown in FIGS. **3** to **5** represent the same conductors and are connected to the dot matrix electrode **19**b of cathode ray tube **18.** Conductors $A_1, A_2, A_3 \ldots A_n$ correspond to conductors $A_1, A_2, A_3 \ldots A_n$, respectively shown in FIGS. **1** and **6.** Similarly, conductors $N_1, N_2, N_3 \ldots N_n$ shown in FIG. **4** correspond, respectively to conductors $N_1, N_2, N_3 \ldots N_n$, and conductors $K_1, K_2, K_3 \ldots K_n$ shown in FIG. **5** correspond to conductors $K_1, K_2, K_3 \ldots K_n$, respectively, shown in FIGS. **1** and **6.**

As shown in FIG. **3** one end of resisters **32, 33, 34, 35** and **36** are connected to corresponding one of conductors y_1, y_2, y_3, y_4 and y_5 while the other ends of these resisters are connected to corresponding one of conductors **47, 48, 49, 50** and **51.** Of these conductors, conductor **47** is connected to the positive poles of diodes **73, 74, 75, 76** and **77,** the negative poles thereof being connected to conductors **68, 69, 70, 71** and **72,** respectively. Similarly, conductor **48** is connected to the positive poles of diodes **79** and **89,** the negative poles thereof being connected to conductors **67** and **70,** respectively. Conductor **49** is connected to the positive poles of diodes **78** and **87,** the negative poles

thereof being connected to conductors **66** and **70**, respectively. In the same manner, conductor **50** is connected to conductors **67** and **70**, respectively through diodes **80** and **86** and conductor **51** is connected to conductors **68, 69, 70, 71** and **72**, respectively through diodes **81, 82, 83, 84** and **85**. The other ends of these conductors **66** through **72** are connected to conductors x_1 through x_7, respectively through diodes **59** through **65**. Furthermore, conductors **66** through **72** are connected to the positive poles of diodes through **58**, respectively, the negative poles of these diodes being commonly connected to the output conductor A_1 of the gate circuit **5**. Such a combination of diodes means that an information of a letter "A" is stored. Elements associated with another conductors A_2 to A_n are also similarly connected. Thus, the combination of diodes associated with conductor A_2 stores the information of a letter "B" and that associated with conductor A_3 stores the information of letter "C."

Similarly, in FIG. **4**, combinations of diodes storing informations of digits "1," "2," "3" . . . . are associated with output conductors $N_1, N_2, \ldots N_n$ respectively, of gate circuit **5**.

Also, in FIG. **5**, combinations of diodes storing informations of katakana symbols *a*, *e*, *u* . . . . are associated with output conductors $K_1, K_2 \ldots K_n$, respectively of gate circuit **5**.

FIG. **6** shows a typical connection diagram of the gate circuit **5** shown in FIG. **1**, as shown the output conductors $A_1, A_2, A_3 \ldots A_n$ are connected to the positive poles of diodes **89, 90, 91, 92, 93, 94**, and **95**, respectively. Actually, although the number of diodes is equal to the number of conductors $A_1, A_2, A_3 \ldots A_n$, for the sake of simplicity, the number of the diodes is shown reduced. The negative poles of these diodes **89, 90, 91, 92, 93, 94** and **95** are commonly connected to a conductor **131**, hereinafter called g_1 conductor. Conductors $A_1, A_2, A_3 \ldots A_n$ are also connected to positive poles of diodes **96** through **102**, respectively, the negative poles of these conductors being connected to conductors **135** through **141**, respectively, hereinafter called G_1 line, G_2 line . . . . G_n line, respectively.

Other output conductors $N_1, N_2, N_3 \ldots N_n$ are similarly connected. Thus, these conductors are connected to a conductor **132** (hereinafter called g_2 line) through diodes **103** through **109**. Further, conductors N_1 through N_n are connected to conductors G_1 through G_n, respectively, through diodes **110** to **116** inclusive.

Output conductors $K_1, K_2, K_3 \ldots K_n$ of gate circuit **5** are similarly connected. More particularly, these conductors are connected to a conductor (herein termed g_3 line) respectively through diodes **117** through **123**. These conductors K_1 through K_n are also connected to conductors G_1 through G_n, respectively through diodes **124** to **130** inclusive.

FIGS. *7a*, *7b* and *7c* show patterns and the positions thereof displayed on the screen of cathode ray tube **18** as well as the correspondence between these positions and the addresses in the sub-memory **2**. Thus, FIG. *7a* shows the manner of displaying the patterns of letters, digits and the like on the screen of the cathode ray tube, FIG. *7b* shows the positions of the patterns of the letters, digits and the like to be displayed on the screen of the cathode ray tube **18**, and FIG. *7c* shows the correspondence between the address symbol numbers $B_{11} \ldots B_{mn}$ of sub-memory **2** and the symbol numbers $S_{11} \ldots S_{mn}$, shown in FIG. *7b*.

FIG. **8** shows a truth table showing the state of the address symbol numbers B_{11} through B_{1n} when they are stored in the register **3**. In this table, $D_1, D_2, D_3 \ldots D_n$ shown logical values of the contents of register **3** when they appear on respective output conductors D_1 *through* D_n after being decoded by decoder **4**, whereas g_1, g_2 and g_3 show the logical values appearing on respective output conductors g_1, g_1 and g_2 of register **3** shown in FIGS. **1** and **6**.

FIG. **9** shows a typical construction of the dot matrix electrode consisting of portions **19***a* and **19***b* of the cathode ray tube **18**, which are situated in front of the electron gun of the cathode ray tube. In this figure, y'_1, y'_2, y'_3, y'_4 and y'_5 (collectively designated **19**a) and $x'_1, x'_2, x'_3, x'_4, x'_5, x'_6$ and x'_7 (collectively designated **19**b) electrode plates respectively connected to conductors y_1 through y_5 and conductors x_1 through x_7 described above. These electrode plates comprise a matrix of 5×7. Among these electrodes, each of the electrodes y_1 through y_5 is provided with equally spaced apart five openings and each of the electrodes x'_1 through x'_7 is provided with equally spaced apart seven openings. The openings of the electrode plates y'_1 through y'_5 and the openings of the electrode plates x'_1 through x'_7 are superposed at the crossings of these electrode plates. A shield plate **142** is interposed between these groups of electrode plates or in front of electrode plates x'_1 through x'_7. Suppose now that a positive potential, for example, of 15 to 20 volts is impressed upon respective electrode plates, this positive potential attracts the electrons emitted from the cathode electrode **20** to pass them through the openings. The electrons passed through these openings are accelerated to impinge upon the screen to display **35** dots thereon. Assuming now that some of the electrode plates are connected to a source of a negative potential or the ground instead of the positive potential, the dots on the screen corresponding to the rows of openings through these grounded electrode plates would not be displayed (or luminesce). In this manner, while successively scanning the electrode plates y'_1 through y'_5 (or **19***a*) with a positive pulse, when some of the electrode plates belonging to the other group **19**b of electrode plates x_1 through x_7 necessary for displaying letter are synchronously impressed with a positive pulse, the desired pattern of a letter, digit or symbol or the like can be displayed by dots.

FIG. **10** shows one example of the pattern displayed on the screen of the cathode ray tube. In this case, a letter B is displayed.

The operation of the novel display device is generally as follows :

Upon application of a start signal pulse to start-stop control **9**, a start signal is supplied to cause to respective circuit blocks. The start-stop control **9** functions to coincide with each other the phases of the deflection signal applied to coil **17**, the information read signal for obtaining information from memories **6–8** and the scanning pulses on conductors $y_1 - y_5$ for the matrix electrode and the signal provided by the start-stop control operates address register **10** and counter **12** which have been held in their set state to transfer the information to be displayed from memory **1**. At this time, by considering the position of the letter to be displayed on the screen, the content of the memory is determined so as to coincide the positions of the position numbers $S_{11} \ldots S_{1n}$ of the screen of the cathode ray tube shown

in FIG. 7*b* and the positions of the address numbers A_{11} . . . . A_{1n} of the submemory shown in FIG. 7*c*. In response to the output from the clock pulse generator **13**, a portion of the output from counter **12** operates address register **10**. Accordingly, each time the content of the address register **10** is changed, under the control of the read out control **11**, the contents of the sub-memory **2** are successively written into register **3** according to the order of the patterns to be displayed on the screen of the cathode ray tube **18**. To this end, it is essential to write into the register without destructing the contents of the sub-memory. Three codes of the contents written in the register **3** are utilized as the gate signals for selecting the alphabet symbol memory **6**, the digit symbol memory **7** and the katakana symbol memory **8**, respectively and the remaining contents of the register are codes for selecting the patterns of the letters, digits and symbols, respectively. These codes are supplied to gate circuit **5** through decoder **4**. Consequently, one of the letter digit or katakana symbols having patterns in the memories **8**, **7** and **6** is selected and the selected pattern is applied to the matrix electrode portion **19***b* according to the memory and in synchronism with a pulse signal from counter **12** for scanning the dot matrix electrode portion **19***a* in the cathode ray tube **18** whereby the selected pattern is synthesized with the pulse signal to form the desired pattern. For the purpose of displaying the pattern at the desired position on the screen, synthesizers **15** and **16** comprising the deflection circuit pass deflection currents through the deflection coil of the cathode ray tube in synchronism with the pulse utilized to form the pattern. Upon completion of one cycle, the content of the register **3** reads out a code corresponding to the pattern of the letter and the like to be displayed next time from the sub-memory **2** and the code is applied to the matrix electrode of the cathode ray tube to display the newly selected pattern on the screen. At this time, since the deflection currents supplied by the stepped wave synthesizers **15** and **16** have been varied stepwisely, the pattern of the next letter can be displayed at the desired position. These display operations are repeated at such a period that does not cause flicker to the eyes of the viewer, so that it is possible to display a plurality of letters and the like on the screen at the same time.

The operation of respective componets and that of the entire system shown by the block diagram of FIG. **1** are described hereunder. Memory **1**, sub-memory **2**, address register **10** and read out control **11** are not limited to the particular types illustrated. Thus, for example, where the display apparatus is used for a desk type electronic computer and the like, memory **1** may be eliminated, in which case the sub-memory **2** is used as the memory of the electronic computer. It is only essential to arrange the components so that the contents of the sub-memory **2** are successively read out into register **3** at a high speed in accordance with the arrangement of the letter on the screen by a single output pulse from counter **12**. This is possible by conventional computer technique. For brevity it is asumed herein that when one output signal is provided by counter **12**, codes corresponding to the symbols of the letters, digits or the like to be displayed are sequentially read out and stored in the register **3**.

The waveform of a clock pulse generated by the clock pulse generator **13** is shown by a curve **22** in FIG. 2a. The start-stop control **9** comprises a single RS flip-flop to store start and stop signals. Assuming now that upon receival of a stop signal, the address register **10**, counter **12**, X-axis stepped wave synthesizer **15** and Y-axis stepped wave synthesizer **16** are set. Then, upon receival of a start signal at the start-stop control **9**, address register **10**, counter **12** and X and Y axis stepped wave synthesizers **15** and **16** will start under predetermined conditions, which should satisfy the following. Address register **10** should indicate an address number B_{11} shown in FIG. 7*c*, whereas counter **12** should correspond to waveforms **23**, **24**, **25**, **26**, **27** and **28** at a time to shown in FIG. 2*a*. Moreover, the wave forms of the currents passed through the deflection coil **17** of the cathode ray tube **18** by the X-axis stepped wave synthesizer **15** and the Y-axis stepped wave synthesizer **16** should correspond to the waveforms **23**, **24**, **25**, **26**, **27**, and **28** of the counter **12** at a time to and current waveforms **30** and **31** at a time T_0 in FIG. 2*b*. When these conditions are satisfied, since the content of the set address register **10** indicates the address number B_{11} of FIG. 7*c*, the content of the address number B_{11} will be stored in register **3** by read out control **11**. Three codes of the contents are applied to gate circuit **5**. Most of the codes recorded are supplied to decoder **4** and the outputs thereof are applied to gate circuit **5**. For example, the contents of address numbers B_{11} . . . . B_{mn} shown in FIG. 7*c* of sub-memory **2** are stored in register **3**. FIG. **8** shows the codes read out from register **3** which are applied directly to gate circuit **5** and the codes read out from register **3** which are applied to gate circuit **5** through decoder **4**. With reference now to FIGS. **6** and **8**, let us consider a case wherein the address number of sub-memory is B_{11}. Assume that a code of **100** as a positive voltage logical value and that the gate to the alphabet symbol memory **6** is enabled whereas the gates to the katakana symbol memory **8** and digit symbol memory **7** are disenabled, thereby selecting the alphabet symbol memory **6** alone. It is further assumed that a code " 1 " is represented by a positive voltage and a code " 0 " by a zero voltage, a positive voltage will be applied on conductor g_1 with zero voltages upon conductors g_2 and g_3 shown in FIG. **6**. When the positive potential impressed upon conductor g_1 is higher than the voltages on conductors A_1, A_2 . . . . A_n, diodes **89** through **95** connected to conductor g_1 are biased in the reverse direction so that they pass no current. However, diodes **103** through **109** connected to conductor g_2 are biased in the foreward direction to pass currents. Consequently, all conductors N_1, N_2, N_3 . . . . N_n assume a zero voltage. Similarly, as conductor g_3 is also at the zero potential, all conductors K_1, K_2, K_3 . . . . K_n assume a zero voltage. Since all of the conductors N_1 through N_n and K_1 through K_n are at the zero potential, diodes **96** through **102** are connected with polarities as shown in FIG. **6** in order to prevent conductors A_1, A_2, A_3 . . . . A_n from being affected by the zero potential. By this gate action, the alphabet symbol memory **6** is selected.

Codes on conductors D_1, D_2, D_3 . . . . D_n are supplied to conductors G_1, G_2, G_3 . . . . G_n, respectively. Again assuming positive voltage logical values for the codes on conductors D_1 through D_n, then a positive voltage will be impressed only upon conductor G_1, the potential impressed across diode **96** of the selected alphabet symbol memory **6** is a negative bias because the voltages on conductors A_1 and G_1 are equal or the voltage on conductor G_1 is higher than that impressed upon conductor A_1 whereby diode **96** does not pass current.

However, since zero voltages are impressed upon conductors G_2, $G_3 \ldots G_n$, diodes 97 through 102 will be biased forwardly, and hence conductors A_2, $A_3 \ldots A_n$ will assume zero voltages. As a result, a positive potential is applied to only conductor A_1 to select the same. Actually, however, during the intervals from t_0 to t_1 and t_{12} to t_{13}, in FIG. 2*a*, conductor A_1 does not assume the positive potential, but during these intervals, since no pattern of a letter or the like is being displayed on the screen of the cathode ray tube, no trouble results. This can be more clearly understood from the operation of the circuits shown in FIGS. 3 to 5. More particularly, voltages corresponding to the positive pulses 24 to 28 shown in FIG. 2a are sequentially applied to conductors y_1, y_2, y_3, y_4 and y_5 shown in FIGS. 3 to 5, by the operation of counter 12 whereby the matrix electrode portion 19a of the cathode ray tube 18 is scanned sequentially by these voltages. The pulse voltages applied to conductors y_1 through y_5 pass through diode matrixes for the letter, digit and the like and appear on conductors x_1 through x_7. In this manner, codes corresponding to letter or digit symbols appear on conductors x_1 through x_7 in the order of y_1, y_2, y_3, $y_4$and y_5 . As has been pointed out previously, conductors x_1 through x_7 shown in FIGS. 3 to 5 are the same conductors which are connected to the dot matrix electrode portion 19*b* of the cathode ray tube 18. Since the selected conductor A_1 is being impressed with a positive potential, diodes 52 through 58 are biased in the reverse direction and hence are non-conductive. Positive pulses 24 through 28 shown in FIG. 2*a* correspond to voltages appearing on conductors y_1 through y_5, respectively, and during the interval between t_1 to t_2, a positive potential is applied upon conductor y_1 and conductors y_2 to y_5 inclusive are at a zero voltage. This positive voltage appears on conductors x_3 through x_7 through diodes 81 through 85 and thence through diodes 61 through 65. Since conductors y_2 through y_5 are at the zero voltage, conductors x_1 and x_2 are also at the zero voltage. For the same principle, of operation, the positive potential is thereafter applied sequentially upon conductors y_2 through y_5, thus forming a series of codes on conductors x_1 through x_7. In the illustrated example, a series of codes prepared by the diode matrix connected to conductor A_1 and the voltage impressed upon conductors y_1 to y_5 inclusive are synthesized by the dot matrixes 19*a* electrode portions and 19*b* of the cathode ray tube 18 to display an alphabet "A." As above described, diodes 59 through 65 function to prevent interference with diode memory blocks of other letters and the like.

When a selected letter has been displayed on the screen in this manner, the operation for displaying the next letter or the like is commenced. A trigger pulse obtained by differentiating the buildup portion at a time t_6 of a pulse voltage 23 (FIG. 2*a*) of the output from counter 12 shown in FIG. 1 or the build-down portion of one positive pulse 28 of waveforms 24 to 28 (FIG. 2*a*) inclusive which are impressed upon conductors y_1 to y_5, functions to change the condition of the X-axis stepped wave synthesizer 15 to vary the magnitude of the current flowing through the X-axis deflection coil shown by the waveform 29 in FIG. 2*a*, at a time t_6 . Concurrently with this change in the valve of the deflection current, at time t_6, the pulse wave 23 shown in FIG. 2*a* reads out the letter or digit to be displayed subsequently from sub-memory 2, FIG. 1, and stores it in register 3. Thereafter, similar operations are repeated. When the selected letters are displayed on the predetermined positions S_{11}, $S_{12} \ldots S_{1n}$ (FIG. 7*b*) on the screen of the cathode ray tube 18 corresponding to the contents of address numbers A_{11}, $A_{12} \ldots A_{1n}$ (FIG. 7*c*) of the sub-memory 2, the content of the address number B_{21} shown in FIG. 7*c* must be displayed at the postion S_{21} shown in FIG. 7*b*. The designation of this position is done by the X-axis stepped wave synthesizer 15 and the Y-axis stepped wave synthesizer 16 comprising the deflection circuit shown in FIG. 1. At this time, a signal is applied to the Y-axis stepped wave synthesizer 16 from a counter included in the X-axis stepped wave synthesizer 15 to vary the condition of the stepped wave generated by the synthesizer 16. The counter in the X-axis stepped wave synthesizer 15 is a n step counter for the letters, digits and symbols to be formed at the sides of positions $S_{11} \ldots S_{12}$ shown in FIG. 7(*b*). Immediately after forming a letter, digit or a like symbol at position S_{1n} in FIG. 7b by the counter, a pulse signal is applied to the Y-axis stepped wave synthesizer 16 to change its state as shown in FIG. 2b. The waveform 30 shown in FIG. 2*b* shows the current passed through the deflection coil 17 of the cathode ray tube 18 by the X-axis stepped wave synthesizer 15, which is similar to the waveform 29 shown in FIG. 2*a*. As can be noted this current waveform shows a case where $n=6$ in FIG. 7*b*, that is the case wherein the number of letters to be displayed equals 6. The waveform 31 shown in FIG. 2 *b* shows a signal generated by Y-axis stepped wave synthesizer 16 under the control of an output from the counter included in the X-axis stepped wave synthesizer 15. Waveform 30 shows the horizontal deflection current through the deflection coil of the cathode ray tube 18 and as shown by FIG. 2*b*, as the value of waveform 30 varies at times T_6, T_{12}, T_{18} and T_{24}, the value of waveform 31 varies also. This example shows a case wherein 6 juxtapose letters or the like are displayed on the screen of the cathode ray tube in synchronism with waveform 30 by the counter included in the X-axis stepped wave synthesizer 15. During very short intervals or at instants T_1, T_2, $T_4 \ldots T_{24}$ on waveforms 30 and 31 provided by synthesizers 15 and 16 it is necessary to apply an elimination signal upon the cathode electrode 20 or grid electrode 21 of the cathode ray tube 18 by an elimination signal synthesizer 14. As shown in FIG. 1, timing of the elimination signal synthesizer is obtained from the counter 12. By the repetition of these operations all of the contents in the sub-memory 2 are displayed on the screen of the cathode ray tube 18. As the operations are repeated continuously at such a period (less than one-thirtieth sec.) that will not cause a flicker to the eyes of the viewer. When a stop signal is applied upon the start-stop control 9, all of the contents of the sub-memory will be displayed standstill on the screen of the cathode ray tube 18.

In the above described operation, although a single letter is displayed by 35 dots, it is to be understood that by increasing the number to dots of the dot matrix utilized in the cathode ray tube, it becomes possible to display more clearly the letters and the like. Where the nature of the letters and the like is such that it can be displayed with a lesser number of dots, it is possible to decrease the number of signals impressed upon the dot matrix electrode.

Patterns of the letters and the like to be displayed are dependent upon the contents of the register 3 which

are applied directly upon gate circuit **5** over conductors g_1, g_2 and g_3 and the contents of the register **23** which are applied to gate circuit **5** through decoder **4.** Where the number of letters and the like required to be stored in these components increases, the number of conductors D_1 through D_n also increases thus complicating the circuit arrangement of decorder **4.** In such a case, the alphabet symbol memory **6,** digit symbol memory **7** and katakana symbol memory **8** are comprised by a number of sub-divided block circuits and the number of codes corresponding to the codes on conductors g_1, g_2 and g_3 for enabling and disenabling the gate circuit is increased to the number of sub-divided blocks of the letter, digit and symbol memories, which may be constructed by a diode circuit similar to that shown in FIG. **6.** With this construction, it is possible to decrease the number of terminals G_1, G_2 . . . . G_n, thus simplifying the circuit construction of the decoder **4.** When the contents of the memory **1** are expressed by simple binary values, for example, as it is necessary to decode the codes supplied to conductors g_1, g_2 and g_3, an additional decoder must be included in these conductors. In such a case, a decoder may be connected between sub-memory **2** and register **3.**

As above described, in the case of a desk type electronic computer, memory **1** may be omitted, in which case sub-memory **2** is utilized as the memory of the computer thus providing a real time display apparatus for the computer.

As above described, the invention provides an improved display apparatus employing a novel cathode ray tube according to which letters, digits, symbols and the like can be displayed on the screen deflection of the electron beam is necessary only for suitably separating letters and the like displayed on the screen. Letters and the like are formed by the selective operation of the matrix electrode acting portions **19*a***, **19*b*** as a type of a matrix switch. For this reason the display apparatus operates very stably so that the letters and the like displayed on the screen of the cathode ray tube are more stable than in the conventional display apparatus. Moreover, as the period of the stepped waveform current flowing through the electromagnetic deflection coil of the cathode ray tube is long, it is easy to generate a stable deflection current, thus assuring stable operation of the associated circuits. In other words, it is possible to display an increased number of letters and the like. The apparatus for generating patterns of the letters and the like, gate circuit **5,** alphabet symbol memory **6,** digit symbol memory **7,** katakana symbol memory **8,** counter **12** are all comprised by flip-flop circuits or logical circuits including combinations of diodes whereby the patterns of the letters and the like are displayed on the screen without the necessity of any digital-analogue conversion. For this reason, stable display can be made with inexpensive and simple apparatus not utilizing special and complicated components. Since the clock pulses generated by the clock pulse generator **13** are distributed among various component parts through counter **12,** variations in the frequency of the clock pulse do not affect the quality of the letters and the like displayed on the screen of the cathode ray tube. Further, as the letters and the like are displayed by dots, it is possible to display a large number of letters and the like by merely increasing the contents of the memory.

While the invention has been shown and described in terms of the preferred embodiment thereof it will be clear that many changes and modifications will occur to one skilled in the art within the scope of the invention as defined in the appended claims.

What is claimed is :

1. Display apparatus comprising a cathode ray tube including a cathode electrode, a display screen, a matrix electrode disposed between said cathode electrode and display screen, said matrix electrode comprising a plurality of *y* electrode plates and a plurality of *x* electrode plates, said *y* and *x* electrode plates being arranged to form a matrix and having holes at their junctions adapted to pass electrons emitted from said cathode electrode, and a deflection coil disposed between said matrix electrode and said display screen; a plurality of discrete memories connected to control said plurality of *x* electrode plates, each of said memories being provided for a different group of patterns of the letters, digits and symbols to be displayed on said screen; address memory means for storing the positions on said screen at which the selected patterns of said letters, digits and symbols are to be displayed; information memory means for storing the information regarding the patterns to be displayed; means responsive to the outputs from said address memory means and said information memory means for selectively driving said plurality of memories to control said *x* electrode plates, means for controlling said *y* electrode plates in sequence with the control of said *x* electrode plates to cause electrons from said cathode electrode to pass through said holes in said plates toward said display screen to form the letters, digits and symbols from one of said groups of patterns; and means for supplying deflection signals to said deflection coil in synchronism with the outputs from said plurality of memories.

2. The display apparatus according to claim **1** wherein said information memory means is connected to said address memory means such that the contents of said information memory means are read out under the control of said address memory means, and said driving means includes a register connected to said information memory means for receiving said read out contents, a decoder and a gate circuit connected between the output of said register and said plurality of memories and through which said read out contents are supplied to said plurality of memories.

3. The display apparatus according to claim **2** wherein portions of the outputs from said register are supplied directly to said gate circuit and the remaining portions of the outputs from said register are supplied to said gate circuit through said decoder.

4. The display apparatus according to claim **1** wherein each one of said plurality of memories for said groups of patterns comprises a plurality of parallel connected diode matrixes, each for one pattern.

5. The display apparatus according to claim **1** wherein said means for supplying said deflection signals comprised a X-axis stepped wave synthesizer and a Y-axis stepped wave synthesizer.

6. The display apparatus according to claim **5** which further comprises a start-stop control for controlling the operations of said X-axis stepped wave synthesizer and said Y-axis stepped wave synthesizer and for controlling the operation of said address memory means.

7. The display apparatus according to claim **5** which further comprises a clock pulse generator and a

counter responsive to the output from said clock pulse generator for synchronously controlling the operations of said address memory means, said plurality of memories for said groups of patterns, said X-axis stepped wave synthesizer and said Y-axis stepped wave synthesizer.

8. The display apparatus according to claim 1 wherein said information memory means comprises a main memory and a submemory.

9. The display apparatus according to claim 1 wherein said letters, digits and symbols are displayed on said screen in discrete positions spaced across said screen by changes in said deflection signals supplied to said deflection coil, and wherein said cathode ray tube further comprises a grid electrode and an elimination synchronizer connected to said grid electrode and adapted to apply an elimination signal of a very short interval to said grid electrode while said deflection signals change causing said deflection coil to position the next letter, digit or symbol to be displayed on said screen.

10. A display apparatus for displaying letters, digits, symbols and like patterns, comprising a cathode ray tube including a cathode electrode, a control grid, a display screen, a dot matrix electrode disposed between said cathode electrode and display screen, said matrix electrode comprising a plurality of *y* electrode plates and a plurality of *x* electrode plates, said *y* and *x* electrode plates being arranged to form a matrix and having holes at their junctions adapted to pass electrons emitted from said cathode electrode, and a deflection coil disposed between said matrix electrode and said display screen; a main memory for storing information regarding the patterns to be displayed on said display screen; a register; an address register for storing the positions on said screen at which selected patterns are to be displayed; a sub-memory, responsive to said address register, connected between the output of said main memory and the input of said register for reading out the information from said main memory and storing the read out information in said register under the control of said address register; a gate circuit; a decoder; connections to supply some of the outputs from said register directly to said gate circuit and to supply others of said outputs from said register to said gate circuit through decoder; a plurality of discrete memories for different types of patterns connected between the output of said gate circuit and said dot matrix electrode of said cathode ray tube for controlling said plurality of *x* electrode plates in response to the outputs of said gate circuit, each of said discrete memories comprising a plurality of parallel connected diode matrixes, each for one pattern; a deflection circuit for said deflection coil comprising a X-axis stepped wave generator and a Y-axis stepped wave generator; an elimination signal generator connected to said control grid of said cathode ray tube; a clock pulse generator; a counter connected to and responsive to the output pulses from said clock pulse generator, said counter being connected to and adapted to synchronously control said address register, said plurality of discrete memories, said X-axis stepped wave generator, said Y-axis stepped wave generator, said *y* electrode plates and said elimination signal generator; and a start-stop control connected to and adapted to control said address register, said X-axis stepped wave generator, said Y-axis stepped wave generator and said counter, said *x* electrode plates and said *y* electrode plates being sequentially controlled by said discrete memories and said counter to cause electrons from said cathode electrode to pass through said holes in said plates toward said display screen to form letters, digits and symbols from one of said types of patterns.

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UNITED STATES PATENT OFFICE

CERTIFICATE OF CORRECTION

Patent No. 3,735,383 Dated May 22, 1973

Inventor(s) Katushi Naka

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 5, line 31, the numeral "89" should be -- 89' --;

line 35, the numeral "89" should be -- 89' --.

Signed and sealed this 27th day of November 1973.

(SEAL)
Attest:

EDWARD M.FLETCHER,JR.
Attesting Officer

RENE D. TEGTMEYR
Acting Commissioner of Patents