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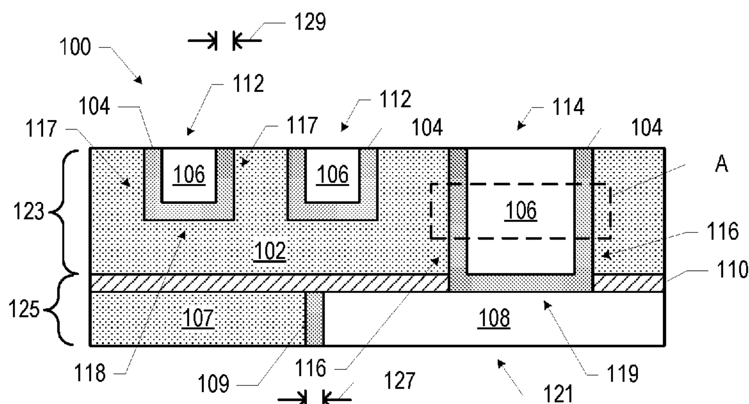

FIG. 1

(57) Abstract: Disclosed herein are graphitic liners for integrated circuit (IC) devices, as well as related devices and methods. For example, disclosed herein are liners that include graphene having a quality gradient, multi-layer liners (e.g., including metal and graphene layers), and liners that line the sidewalls of a via while leaving a bottom of the via open for direct contact with a lower conductive structure.

WO 2018/118082 A1

GRAPHITIC LINERS FOR INTEGRATED CIRCUIT DEVICES

Background

[0001] Some integrated circuit interconnect structures include a thick metal liner to mitigate diffusion of copper into nearby interlayer dielectric (ILD) and/or to improve the mechanical coupling between the copper and the ILD.

Brief Description of the Drawings

[0002] Embodiments will be readily understood by the following detailed description in conjunction with the accompanying drawings. To facilitate this description, like reference numerals designate like structural elements. Embodiments are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings.

[0003] FIG. 1 is a cross-sectional view of a portion of an integrated circuit (IC) device including conductive structures with graphitic liners, in accordance with various embodiments.

[0004] FIG. 2 is a cross-sectional view of an example embodiment of the IC device of FIG. 1.

[0005] FIG. 3 is a cross-sectional view of a portion of an IC device including conductive structures with graphitic liners, in accordance with various embodiments.

[0006] FIG. 4 is a cross-sectional view of an example embodiment of the IC device of FIG. 3.

[0007] FIGS. 5A-5F are cross-sectional views of various example stages in the manufacture of the IC device of FIG. 1, in accordance with various embodiments.

[0008] FIGS. 6A-6D are cross-sectional views of various example stages in the manufacture of the IC device of FIG. 3, in accordance with various embodiments.

[0009] FIGS. 7A-7D are cross-sectional views of some example graphitic liners that may be included in an IC device, in accordance with various embodiments.

[0010] FIG. 8 is a flow diagram of an example method of manufacturing an IC device including a graphitic liner, in accordance with various embodiments.

[0011] FIG. 9 is a flow diagram of an example method of manufacturing an IC device including a graphitic liner, in accordance with various embodiments.

[0012] FIGS. 10A and 10B are top views of a wafer and dies that include any of the graphitic liners disclosed herein.

[0013] FIG. 11 is a cross-sectional side view of an IC device that may include any of the graphitic liners disclosed herein.

[0014] FIG. 12 is a cross-sectional side view of an IC device assembly that may include any of the graphitic liners disclosed herein.

[0015] FIG. 13 is a block diagram of an example computing device that may include any of the graphitic liners disclosed herein.

Detailed Description

[0016] Disclosed herein are graphitic liners for integrated circuit (IC) devices, as well as related devices and methods. For example, disclosed herein are liners that include graphene having a quality gradient, multi-layer liners (e.g., including metal and graphene layers), and liners that line the sidewalls of a via while leaving a bottom of the via open for direct contact with a lower conductive structure.

[0017] In conventional IC devices, copper interconnects in an interlayer dielectric (ILD) may include an adhesion liner to improve the mechanical coupling between the copper and the ILD, as well as a diffusion barrier liner to limit the diffusion of copper into the ILD. Conventional adhesion/diffusion barrier liners are relatively thick, limiting the degree to which the size of a copper interconnect can be scaled down before the copper portion of the interconnect is too thin and thus resistance becomes unacceptable.

[0018] Disclosed herein are graphitic liners for conductive structures in an IC device. Various ones of the graphitic liners disclosed herein may be used with copper interconnects, and may serve as both adhesion liners and diffusion barriers with a thickness that may be substantially reduced relative to conventional liners. Various ones of the graphitic liners disclosed herein may be used with non-copper interconnects (e.g., refractory metal interconnects), and may serve as adhesion liners to improve the mechanical coupling between the non-copper metal and the ILD.

[0019] In the following detailed description, reference is made to the accompanying drawings that form a part hereof, wherein like numerals designate like parts throughout, and in which is shown, by way of illustration, embodiments that may be practiced. It is to be understood that other embodiments may be utilized and structural or logical changes may be made without departing from the scope of the present disclosure. Therefore, the following detailed description is not to be taken in a limiting sense.

[0020] Various operations may be described as multiple discrete actions or operations in turn, in a manner that is most helpful in understanding the disclosed subject matter. However, the order of description should not be construed as to imply that these operations are necessarily order dependent. In particular, these operations may not be performed in the order of presentation. Operations described may be performed in a different order from the described embodiment. Various additional operations may be performed, and/or described operations may be omitted in additional embodiments.

[0021] For the purposes of the present disclosure, the phrase "A and/or B" means (A), (B), or (A and B). For the purposes of the present disclosure, the phrase "A, B, and/or C" means (A), (B), (C), (A and B), (A and C), (B and C), or (A, B, and C). The term "between," when used with reference to

measurement ranges, is inclusive of the ends of the measurement ranges. As used herein, a "high-k dielectric material" may refer to a material having a higher dielectric constant than silicon oxide.

[0022] The description uses the phrases "in an embodiment" or "in embodiments," which may each refer to one or more of the same or different embodiments. Furthermore, the terms "comprising," "including," "having," and the like, as used with respect to embodiments of the present disclosure, are synonymous. The disclosure may use perspective-based descriptions such as "above," "below," "top," "bottom," and "side"; such descriptions are used to facilitate the discussion and are not intended to restrict the application of disclosed embodiments. The accompanying drawings are not necessarily drawn to scale. For ease of exposition, the term "FIG. 5" may be used to refer to the collection of FIGS. 5A-5F, the term "FIG. 6" may be used to refer to the collection of FIGS. 6A-6D, the term "FIG. 7" may be used to refer to the collection of FIGS. 7A-7D, and the term "FIG. 10" may be used to refer to the collection of FIGS. 10A-10B.

[0023] FIG. 1 is a cross-sectional view of a portion of an integrated circuit (IC) device 100 including conductive structures with graphitic liners 104, in accordance with various embodiments. In particular, the portion of the IC device 100 illustrated in FIG. 1 includes an insulating material 102 in which two conductive lines 112 and one conductive via 114 are disposed. The term "conductive structures" may be used herein to refer to conductive lines, conductive vias, other interconnect structures, or any other suitable conductive structures in accordance with the present disclosure. The conductive lines 112 and the conductive via 114 of the IC device 100 of FIG. 1 may include graphitic liners 104, as discussed below.

[0024] The conductive lines 112 and the conductive via 114 may be filled with an electrically conductive material 106 (e.g., a metal). In some embodiments, the conductive material 106 may include copper. In some embodiments, the conductive material 106 may include a non-copper material, such as cobalt, ruthenium, nickel, molybdenum, or tungsten. In some embodiments, the conductive material 106 may include a refractory metal, such as niobium, molybdenum, tantalum, tungsten, rhenium, titanium, vanadium, chromium, zirconium, ruthenium, rhodium, hafnium, osmium, or iridium. In some embodiments, the conductive material 106 may include multiple different conductive materials, such as multiple different ones of any of the conductive materials discussed above. In some embodiments, an IC device 100 may include copper interconnects (e.g., conductive lines 112 and conductive vias 114) and non-copper interconnects; the copper interconnects may be used for power/ground pathways, and the non-copper interconnects (which may be less resistive than the copper interconnects) may be used for signal communication pathways.

[0025] The conductive lines 112 may be arranged to route electrical signals in a direction of a plane that is substantially parallel with a surface of a substrate (not shown) of the IC device 100. For example, the conductive lines 112 may route electrical signals in a direction "in and out" of the page from the perspective of FIG. 1. The conductive vias 114 may be arranged to route electrical signals in a direction of a plane that is substantially perpendicular to the surface of a substrate of the IC device 100. For example, the conductive vias 114 may route electrical signals in a direction "up and down" in the page from the perspective of FIG. 1.

[0026] The conductive vias 114 and the conductive lines 112 illustrated in FIG. 1 may be part of a single interconnect layer 123, and in some embodiments, the conductive vias 114 may electrically couple conductive lines 112 of different interconnect layers together. For example, in the embodiment illustrated in FIG. 1, the conductive via 114 of the interconnect layer 123 may be in electrical contact with a conductive structure 121 in a different interconnect layer 125. The conductive structure 121 may include conductive material 108 and a liner 109, and may be, for example, a conductive via or a conductive line. The conductive structure 121 may be insulated from other conductive structures in the interconnect layer 125 by an insulating material 107. In some embodiments, the insulating material 107 may take the same form as the insulating material 102, while in other embodiments, the insulating material 107 may be different from the insulating material 102. Similarly, in some embodiments, the conductive material 108 may be the same material as the conductive material 106, while in other embodiments, the conductive material 108 may be a different conductive material from the conductive material 106. Additionally, the liner 109 may take the same form as the graphitic liner 104, or may be different from the graphitic liner 104. Further conductive structures, and/or other electrical components, may be disposed "above" and/or "below" the portion of the IC device 100 illustrated in FIG. 1 (e.g., as discussed below with reference to FIG. 11).

[0027] As noted above, an insulating material 102 may be disposed around the conductive lines 112 and the conductive via 114. The insulating material 102 may include one or more dielectric materials. For example, in some embodiments, the insulating material 102 may be provided by an interlayer dielectric (ILD), such as an oxide (e.g., silicon oxide or aluminum oxide), a nitride (e.g., silicon nitride), a carbide (e.g., silicon carbide), a carbonitride (e.g., silicon carbon nitride), an oxynitride (e.g., silicon oxynitride), or any combination thereof. In some embodiments, the insulating material 102 may be provided by multiple insulating materials. For example, FIG. 2 illustrates an example of the portion of the IC device 100 illustrated in FIG. 1 in which the insulating material 102 is provided by a combination of an ILD 103 and a hardmask 105 (or other etch stop material). The hardmask 105 may be used to define and pattern the conductive lines 112 and the

conductive via 114, as discussed below with reference to FIG. 5C, and in some embodiments, the hardmask 105 may remain in the IC device 100 after patterning. The hardmask 105 may be formed of silicon nitride, silicon carbide, or another suitable material. In some embodiments, the insulating material 107 of the interconnect layer 125 may be (at least partially) provided by a hardmask. Any of the other components of the embodiment of FIG. 2 may take any of the forms of those components discussed herein with reference to FIG. 1, and thus are not discussed further. In some embodiments, the insulating material 102 disposed between the conductive structures in different ones of the interconnect layers 123 and 125 may have different compositions; in other embodiments, the composition of the insulating material 102 between different interconnect layers 123 and 125 may be the same.

[0028] In some embodiments, a liner 110 may be disposed between the interconnect layers 123 and 125 to insulate portions of the interconnect layers 123 and 125 from each other. In some embodiments, the liner 110 may be a nitride material, and may insulate various conductive structures from proximate structures, and/or may serve as an etch stop during fabrication.

[0029] As noted above, the conductive lines 112 and the conductive via 114 may include a graphitic liner 104. As used herein, a "graphitic liner" may be a liner that includes graphene. In some embodiments, as discussed below with reference to FIG. 7, the graphitic liner 104 may have a homogeneous or inhomogeneous material composition, and may or may not include non-graphene materials. In some embodiments, the graphitic liner 104 may have a thickness 129 between 3 angstroms and 80 angstroms. A graphitic liner 104 having a thickness 129 of 3 angstroms may take the form of a single monolayer of graphene, while thicker graphitic liners 104 may include more than one monolayer of graphene (and/or other materials). The number of monolayers in a sample of graphene may be identified by the Raman spectrum of that sample; the shape of the 2D peak (also called the G peak) may be identified the number of monolayers, as known in the art.

[0030] Various ones of the graphitic liners 104 disclosed herein may provide a number of advantages relative to conventional adhesion/diffusion barrier liners. For example, graphitic liners 104 may be made thinner than conventional liners (e.g., a thickness 129 of 3 angstroms may provide an adequate adhesion/diffusion barrier liner for copper conductive material 106), leaving more "room" for the conductive material 106 in a conductive structure and thus decreasing the resistance of that structure. By extension, the use of various ones of the graphitic liners 104 disclosed herein may enable the size of conductive structures (e.g., conductive lines 112 and conductive vias 114) to shrink beyond what is conventionally achievable, increasing the performance density of the IC device 100. Additionally, when the conductive material 106 is copper, the interface between the graphitic liner 104 and the conductive material 106 may exhibit less specular scattering than occurs at the

interface between a conventional adhesion/diffusion barrier liner and the conductive material 106 (e.g., the interface between tantalum and copper), further reducing resistance relative to conventional interconnects. A number of embodiments of the graphitic liner 104 are discussed below with reference to FIG. 7.

[0031] As noted above, the liner 109 of the conductive structure 121 may or may not be a graphitic liner. For example, the liner 109 may not include graphene (and may instead be formed of, for example, tantalum by physical vapor deposition (PVD)). In some embodiments, a non-graphitic liner 109 may have a thickness 127 that is greater than or equal to 8 nanometers. In some embodiments, the liner 109 may be a graphitic liner, and may take the form of any of the graphitic liners 104 discussed herein.

[0032] As illustrated in FIGS. 1 and 2, a conductive line 112 may be formed in a cavity of the insulating material 102 such that the graphitic liner 104 lines the sidewalls 117 and the bottom 118 of the cavity and is disposed between the conductive material 106 and the insulating material 102 of the conductive line 112. The bottom 118 of the cavity may be spaced apart from the liner 110 by intervening insulating material 102.

[0033] The conductive via 114 may be formed in a cavity of the insulating material 102 such that the graphitic liner 104 lines the sidewalls 116 and is disposed between the insulating material 102 and the conductive material 106 of the conductive via 114. In some embodiments, the conductive via 114 may extend into an opening in the liner 110, and the graphitic liner 104 may be disposed between the liner 110 and the conductive material 106 of the conductive via 114.

[0034] In the embodiment illustrated in FIGS. 1 and 2, the bottom 119 of the cavity associated with the conductive via 114 is provided by the conductive material 108 of the conductive structure 121. Some of the graphitic liner 104 is disposed at the bottom 119 of the cavity so that the graphitic liner 104 is between the conductive material 106 of the conductive via 114 and a conductive material 108 of the conductive structure 121. Such embodiments may be particularly advantageous when the conductive material 106 is copper; the graphitic liner 104 disposed at the bottom 119 of the cavity may mitigate electromigration between the conductive material 106 and the conductive material 108 without significantly increasing the resistance of the interconnect.

[0035] FIGS. 3 and 4 illustrate embodiments of an IC device 100 in which there is no graphitic liner 104 between the conductive material 106 of the conductive via 114 and the conductive material 108 of the conductive structure 121. The graphitic liner 104 may be present only on the surface of the insulating material 102. In these embodiments, the conductive material 106 of the conductive via 114 may extend into a recess 111 in the conductive material 108. Thus, a bottom 115 of a cavity defining the conductive via 114 may be "below" the insulating material 102 of the interconnect layer

123 (and may be below the liner 110 between the interconnect layers 123 and 125). The conductive material 106 of the conductive via 114 may directly contact the conductive material 108 of the conductive structure 121.

[0036] The embodiments of FIGS. 3 and 4 may be particularly advantageous when the conductive material 106 is a non-copper material, such as any of the non-copper materials discussed above. Non-copper conductive materials 106 (e.g., tungsten) may be at a lower risk for electromigration between the conductive material 106 and the conductive material 108, and thus the performance of the IC device 100 may benefit by not having the graphitic liner 104 therebetween (e.g., by having lower resistance through the conductive via 114).

[0037] As illustrated in FIGS. 3 and 4, in some embodiments, the conductive material 106 of the conductive via 114 may extend "under" the graphitic liner 104 of the conductive via 114 so that the conductive material 106 is disposed between some of the conductive material 108 and the graphitic liner 104. As also illustrated in FIGS. 3 and 4, in some embodiments, the conductive material 106 of the conductive via 114 may extend "under" the liner 110 so that the conductive material 106 is disposed between some of the conductive material 108 and the liner 110. In other embodiments, the conductive material 106 of the conductive via 114 may not extend under the liner 110, and in some further embodiments, the conductive material 106 of the conductive via 114 may not extend under the graphitic liner 104. FIG. 4 illustrates an example of the portion of the IC device 100 illustrated in FIG. 3 in which the insulating material 102 is provided by a combination of an ILD 103 and a hardmask 105 (e.g., as discussed above with reference to FIG. 2); any of the other components of the embodiments of FIGS. 3 and 4 may take any of the forms of those components discussed herein with reference to FIGS. 1 and 2, and thus are not discussed further. In particular, any of the graphitic liners 104 discussed herein (e.g., discussed below with reference to FIG. 7) may be used in any of the IC devices 100 disclosed herein (e.g., any of the devices as discussed above with reference to FIGS. 1-4).

[0038] Any suitable techniques may be used to manufacture an IC device 100 including the conductive structures and graphitic liners 104 disclosed herein. For example, FIGS. 5A-5F are cross-sectional views of various example stages in the manufacture of the IC device 100 of FIG. 1, in accordance with various embodiments.

[0039] FIG. 5A is a cross-sectional view of an assembly 200 including the interconnect layer 125. As discussed above, the interconnect layer 125 may include an insulating material 107, a liner 110, and a conductive structure 121. The conductive structure 121 may include a conductive material 108 and a liner 109 disposed between the insulating material 107 and the conductive material 108. The components of the assembly 200 may take the form of any of the embodiments of these

components discussed herein. The assembly 200 may be formed using any suitable techniques. Examples of such techniques may include subtractive fabrication techniques, additive or semi-additive fabrication techniques, single-damascene fabrication techniques, dual-damascene fabrication techniques, or any other suitable technique.

[0040] FIG. 5B is a cross-sectional view of an assembly 202 subsequent to providing an insulating material 102 on the liner 110 of the assembly 200 (FIG. 5A). The insulating material 102 may take any of the forms disclosed herein; for example, in some embodiments, the insulating material 102 may be provided by an ILD, while in other embodiments the insulating material 102 may be provided by an ILD in conjunction with a hardmask (e.g., as discussed above with reference to FIGS. 2 and 4). The insulating material 102 may be provided on the assembly 202 using any suitable technique or techniques, such as spin coating, chemical vapor deposition (CVD), or plasma-enhanced CVD (PECVD). In some embodiments, the insulating material 102 may be polished back after deposition, and before further processing.

[0041] FIG. 5C is a cross-sectional view of an assembly 204 subsequent to forming cavities in the insulating material 102 of the assembly 202 (FIG. 5B). In particular, FIG. 5C depicts two line cavities 205 (each having sidewalls 117 and a bottom 118) and one via cavity 207. The via cavity 207 has sidewalls 116 partially provided by the insulating material 102 and partially provided by the liner 110, and also has a bottom 119 provided by the conductive material 108 of the conductive structure 121. The cavities may be formed using any suitable lithographic etching technique known in the art (e.g., applying a resist, patterning the resist using lithography, and etching the insulating material 102 using dry or wet etching), and in particular, may include one or more rounds of lithographic etching. The conductive material 108 may provide an etch stop for the via cavity 207. Although the via cavity 207 (and thus the conductive vias 114 disclosed herein) is illustrated as having a substantially rectangular profile, this is simply for ease of illustration, and in some embodiments, the via cavity 207 (and thus the conductive vias 114 disclosed herein) may have a tapered profile that narrows closer to the conductive material 108.

[0042] FIG. 5D is a cross-sectional view of an assembly 206 subsequent to conformally depositing a graphitic liner 104 on the assembly 204 (FIG. 5C). The graphitic liner 104 may cover the sidewalls 117 and bottom 118 of the cavities 205 and the sidewalls 116 and the bottom 119 of the via cavity 207, and the deposition of the graphitic liner 104 may be controlled to achieve a graphitic liner 104 of a desired thickness. The particular operations used to deposit the graphitic liner 104 on the assembly 204 will depend on the material composition of the graphitic liner 104, as discussed below with reference to FIG. 7. Generally, deposition techniques like CVD (e.g., atomic layer deposition (ALD)) may be used. In some ALD techniques, an amount of the graphitic liner 104 may be deposited

on the exposed conductive material 108 and then treated with a plasma, and this cycle may be repeated as appropriate to allow the graphitic liner 104 to "climb" the sidewalls 116 and extend over the entire assembly 204.

[0043] In some embodiments, a self-assembled monolayer (SAM) technique may be used to form the graphitic liner 104; in such embodiments, a precursor material may be deposited (instead of the graphitic liner 104 of the assembly 206, the conductive material 106 may be deposited on the precursor material (e.g., as discussed below with reference to FIG. 5E), and then the resulting assembly may be further processed to convert the precursor material into the graphitic liner 104 "under" the conductive material 106. In such embodiments, the resulting graphitic liner 104 may include some amount of the unconverted precursor material (e.g., one or more silanes, phosphonic acids, germanes, or ethylene-terminated compounds). In embodiments in which the graphitic liner 104 is formed using ALD or CVD, these unconverted precursor materials may not be present in the graphitic liner 104.

[0044] FIG. 5E is a cross-sectional view of an assembly 208 subsequent to depositing a conductive material 106 on the graphitic liner 104 of the assembly 206 (FIG. 5D). The conductive material 106 may fill the cavities 205 and 207, and in some embodiments, the conductive material 106 may extend above the graphitic liner 104, as shown. The conductive material 106 may be deposited using any suitable technique, such as ALD or CVD, and may take the form of any of the conductive materials 106 disclosed herein.

[0045] FIG. 5F is a cross-sectional view of an assembly 210 subsequent to planarizing the assembly 208 (FIG. 5E) to remove the conductive material 106 and the graphitic liner 104 above the insulating material 102. In some embodiments, the assembly 208 may be planarized using a chemical mechanical polishing (CMP) technique. The assembly 210 may take the form of the portion of the IC device 100 illustrated in FIG. 1, and may be further processed as desired (e.g., by forming additional interconnect layers on "top" of the assembly 210 by repeating the operations discussed above with reference to FIG. 5).

[0046] FIGS. 6A-6D are cross-sectional views of various example stages in the manufacture of the IC device 100 of FIG. 3, in accordance with various embodiments. The manufacture of the IC device 100 of FIG. 3 may begin as discussed above with reference to FIGS. 5A-5D.

[0047] FIG. 6A is a cross-sectional view of an assembly 212 subsequent to oxidizing a region 209 of the conductive material 108 proximate to the bottom 119 of the via cavity 207 of the assembly 206 (FIG. 5D). In some embodiments, the oxidation may occur by exposing the assembly 210 to oxygen (e.g., using a wet cleaning or plasma treatment); defects in the portion 104A of the graphitic liner 104 proximate to the conductive material 108 may allow oxygen to reach the conductive material

108 to form the oxidized region 209. Thus, the oxidized region 209 may be formed subsequent to deposition of the graphitic liner 104. In other embodiments, the oxidized region 209 may be formed prior to deposition of the graphitic liner 104; in particular, the assembly 204 of FIG. 5C may be exposed to oxygen to form the oxidized region 209, and the graphitic liner 104 may be subsequently deposited (e.g., as discussed above with reference to FIG. 5D), resulting in the assembly 212. In some embodiments, the oxidized region 209 may extend "laterally" beyond the graphitic liner 104 and "under" the liner 110. The dimensions of the oxidized region 209 may be controlled by controlling the defect level of the graphitic liner 104 and the environmental conditions around the oxygen exposure.

[0048] FIG. 6B is a cross-sectional view of an assembly 214 subsequent to removing the oxidized region 209 and the portion 104A of the graphitic liner 104 proximate to the oxidized region 209 from the assembly 212 (FIG. 6A). In some embodiments, a lift-off technique may be performed to remove the oxidized region 209 and the portion 104A. For example, lift-off may be performed by using a wet etchant to etch the oxidized region 209 selective to the conductive material 108, enabling removal of the portion 104A as well. Removing the oxidized region 209 may result in a recess 111 in the conductive material 108; the dimensions of the recess 111 may correspond to the dimensions of the oxidized region 209. The via cavity 207 may thus be "deepened," and may extend into the conductive material 108.

[0049] FIG. 6C is a cross-sectional view of an assembly 216 subsequent to depositing a conductive material 106 on the assembly 214 (FIG. 6B). The conductive material 106 may fill the cavities 205 and 207, and in some embodiments, the conductive material 106 may extend above the graphitic liner 104, as shown. The conductive material 106 may be provided in the assembly 216 in accordance with any of the embodiments discussed above with reference to FIG. 5E. In the assembly 216, the conductive material 106 may extend into the recess 111 and contact the conductive material 108.

[0050] FIG. 6D is a cross-sectional view of an assembly 218 subsequent to planarizing the assembly 216 (FIG. 6C) to remove the conductive material 106 and the graphitic liner 104 above the insulating material 102. The planarization may occur in accordance with any of the embodiments discussed above with reference to FIG. 5F. The assembly 218 may take the form of the portion of the IC device 100 illustrated in FIG. 3, and may be further processed as desired (e.g., by forming additional interconnect layers on "top" of the assembly 218 by repeating the operations discussed above with reference to FIG. 6).

[0051] FIGS. 7A-7D are cross-sectional views of some example graphitic liners 104 that may be included in an IC device 100, in accordance with various embodiments. In particular, the cross-

sectional views in FIGS. 7A-7D may represent cross-sectional views of the dashed regions A of FIGS. 1-4. Any of the graphitic liners 104 may be used in any of the IC devices 100 disclosed herein, and any suitable ones of the manufacturing techniques discussed herein may be used to form any of the graphitic liners 104.

[0052] FIG. 7A depicts an embodiment in which the graphitic liner 104 is formed entirely of a graphene liner 120. The graphene liner 120 may be deposited using ALD or CVD as discussed above, and the quality of the graphene liner 120 (inverse to the density of defects in the graphene liner 120) may depend on the deposition techniques and conditions. In some embodiments, the graphene liner 120 may be a single monolayer of graphene. In some embodiments, the graphene liner 120 may include between 1 and 10 monolayers of graphene (e.g., between 1 and 5 monolayers of graphene). In some embodiments, the graphene liner 120 may have a thickness 129 between 3 angstroms and 30 angstroms (e.g., between 3 angstroms and 15 angstroms). The thickness 129 of the graphene liner 120 may be selected based on the quality of the graphene liner 120 (e.g., based on the defect density of the graphene liner 120); for example, a graphitic liner 104 having a lower-quality graphene liner 120 may be thicker than a graphitic liner 104 having a higher-quality graphene liner 120 to provide the desired adhesion/diffusion barrier liner properties.

[0053] FIG. 7B depicts an embodiment in which the graphitic liner 104 includes defect-gradient graphene 122. As used herein, "defect-gradient graphene" may be graphene having a defect density that varies from the insulating material 102 to the conductive material 106. This gradient in the defect density may be a continuous one (e.g., resulting from relatively continuous changes in the deposition conditions during formation of the defect-gradient graphene 122) or may be stepped (e.g., when graphene of a first quality is deposited in a first deposition round, and graphene of a second different quality is deposited in a second deposition round with different deposition conditions on top of the graphene of the first quality). In a stepped gradient, the graphitic liner 104 may include two or more quality levels of graphene. The deposition conditions that may be changed to change the quality of the deposited graphene may include deposition temperature (with higher temperatures corresponding to higher-quality graphene), deposition pressure, selection of hydrocarbon precursors, hydrocarbon-to-hydrogen partial pressure ratios, and cooling rates, for example. The thickness 129 of the defect-gradient graphene 122 may take the form of any of the thicknesses 129 disclosed herein.

[0054] In some embodiments of the defect-gradient graphene 122, the graphene closer to the insulating material 102 may have more defects (and thus be of a lower quality) than the graphene closer to the conductive material 106. The "higher quality" graphene closer to the conductive material 106 may serve as a diffusion barrier to prevent migration of the conductive material 106

into the insulating material 102, and the "lower quality" graphene closer to the insulating material 102 may serve as an adhesion liner to mechanically secure the conductive material 106 to the insulating material 102 (and thus, for example, mitigate delamination or cracking during heating due to thermal mismatch). The defects present in the lower quality may improve the graphene's performance as an adhesion liner (relative to the use of higher-quality graphene). Using defect-gradient graphene 122 in the graphitic liner 104 may be particularly advantageous when the conductive material 106 is one for which an adhesion liner and a diffusion barrier is useful (e.g., copper).

[0055] The defect density in the defect-gradient graphene may be quantified in any suitable manner. For example, in some embodiments, the defect density in graphene may be quantified by comparing the amplitude of the D peak in the Raman spectrum of the graphene to the amplitude of the G peak in the Raman spectrum (referred to as a "D/G ratio"); a lower D/G ratio may be associated with a lower defect density, and vice versa.

[0056] FIG. 7C depicts an embodiment in which the graphitic liner 104 includes a metal liner 124 and a graphene liner 120. The metal liner 124 may be between the insulating material 102 and the graphene liner 120, and the graphene liner 120 may be between the metal liner 124 and the conductive material 106. The metal liner 124 may include any suitable metal, such as tantalum, titanium (e.g., titanium nitride), or ruthenium. The thickness 215 of the metal liner 124 may take any suitable value (e.g., between 0.5 nanometers and 15 nanometers, or between 0.5 nanometers and 12 nanometers). The thickness 217 of the graphene liner 120 of FIG. 7C may take any suitable value (e.g., between 3 angstroms and 80 angstroms).

[0057] During manufacture of the graphitic liner 104 of FIG. 7C, the metal liner 124 may first be conformally deposited on the insulating material 102 (e.g., using ALD), then the graphene liner 120 may be deposited on the metal liner 124. Because the metal liner 124 may serve as a catalyst for the growth of the graphene liner 120, providing the metal liner 124 first may improve the quality and ease of fabrication of the graphene liner 120.

[0058] FIG. 7D depicts another embodiment in which the graphitic liner 104 includes a metal liner 124 and a graphene liner 120, but in contrast to the embodiment of FIG. 7C, the graphene liner 120 may be between the insulating material 102 and the metal liner 124, and the metal liner 124 may be between the graphene liner 120 and the conductive material 106. The dimensions of the metal liner 124 and the graphene liner 120 of FIG. 7D may take any of the forms discussed above with reference to FIG. 7C.

[0059] FIG. 8 is a flow diagram of an example method 300 of manufacturing an IC device, in accordance with various embodiments. Although the various operations discussed with reference to

the method 300 are shown in a particular order and once each, the operations may be performed in any suitable order (e.g., in any combination of parallel or series performance), and may be repeated or omitted as suitable. Additionally, although various operations of the method 300 may be illustrated with reference to particular embodiments of the IC device 100 disclosed herein, these are simply examples, and the method 300 may be used to form any suitable IC device.

[0060] At 302, an insulating material may be provided. The insulating material may have a cavity. For example, the insulating material 102 (with the cavities 205 and 207) may be provided (e.g., as discussed above with reference to FIGS. 5B and 5C). In some embodiments, the cavity may be formed in the insulating material after the insulating material is blanket-deposited, while in other embodiments, the cavity may be formed in the insulating material as part of the deposition of the insulating material.

[0061] At 304, an inhomogeneous liner may be provided on sidewalls of the cavity. For example, the inhomogeneous liner may be provided as discussed above with reference to the provision of the graphitic liner 104 of FIG. 5D. In some embodiments, the inhomogeneous liner may include multiple layers of distinct material, such as a metal liner and a graphene liner (e.g., the metal liner 124 and the graphene liner 120 discussed above with reference to FIGS. 7C and 7D). In some embodiments, the inhomogeneous liner may include graphene with a defect gradient (e.g., the defect-gradient graphene 122 discussed above with reference to FIG. 7B).

[0062] At 306, after provision of the inhomogeneous liner, conductive material may be provided in the cavity. For example, the conductive material may be provided as discussed above with reference to the provision of the conductive material 106 of FIGS. 5E and 6A-6C).

[0063] FIG. 9 is a flow diagram of another example method 310 of manufacturing an IC device, in accordance with various embodiments. Although the various operations discussed with reference to the method 310 are shown in a particular order and once each, the operations may be performed in any suitable order (e.g., in any combination of parallel or series performance), and may be repeated or omitted as suitable. Additionally, although various operations of the method 310 may be illustrated with reference to particular embodiments of the IC devices 100 disclosed herein, these are simply examples, and the method 310 may be used to form any suitable IC device.

[0064] At 312, a via cavity may be formed in an insulating material. The via cavity may extend down to a conductive structure so that the conductive structure is at a bottom of the cavity. For example, the via cavity 207 may be formed in the insulating material 102, and may extend down to the conductive structure 121, as discussed above with reference to FIG. 5C.

[0065] At 314, a liner may be provided on the bottom and sidewalls of the via cavity. The liner may include graphene. For example, the liner may be any of the graphitic liners 104 discussed above with reference to FIG. 7, and may be provided as discussed above with reference to FIG. 5D.

[0066] At 316, a portion of the conductive structure proximate to the bottom of the cavity may be oxidized. For example, the oxidized region 209 may be formed in the conductive structure 121 proximate to the bottom 119 of the via cavity 207. In some embodiments, the portion of the conductive structure may be oxidized after the liner is provided (e.g., as discussed above with reference to FIG. 6A), while in other embodiments, the portion of the conductive structure may be oxidized before the liner is provided.

[0067] At 318, the oxidized portion and some of the liner at the bottom of the cavity may be removed. For example, the oxidized region 209 and the portion 104A of the graphitic liner 104 may be removed (e.g., as discussed above with reference to FIG. 6B).

[0068] At 320, after the oxidized portion and some of the liner at the bottom of the cavity are removed, a conductive material may be provided in the cavity. For example, the conductive material 106 may be provided in the via cavity 207 (e.g., as discussed above with reference to FIG. 6C).

[0069] The graphitic liners 104, and more generally, the IC devices 100, disclosed herein may be included in any suitable electronic device. FIGS. 10-13 illustrate various examples of apparatuses that may include any of the graphitic liners 104 disclosed herein.

[0070] FIGS. 10A-10B are top views of a wafer 5200 and dies 5202 that may include any of the graphitic liners 104 disclosed herein. The wafer 5200 may be composed of semiconductor material and may include one or more dies 5202 having IC elements formed on a surface of the wafer 5200. Each of the dies 5202 may be a repeating unit of a semiconductor product that includes any suitable IC. After the fabrication of the semiconductor product is complete, the wafer 5200 may undergo a singulation process in which each of the dies 5202 is separated from one another to provide discrete "chips" of the semiconductor product. The die 5202 may include one or more transistors (e.g., some of the transistors 5340 of FIG. 11, discussed below) and/or supporting circuitry to route electrical signals to the transistors (e.g., including any conductive interconnects or other structures that may include a graphitic liner 104), as well as any other IC components. In some embodiments, the wafer 5200 or the die 5202 may include a memory device (e.g., a static random access memory (SRAM) device), a logic device (e.g., AND, OR, NAND, or NOR gate), or any other suitable circuit element. Multiple ones of these devices may be combined on a single die 5202. For example, a memory array formed by multiple memory devices may be formed on a same die 5202 as a processing device (e.g., the processing device 5502 of FIG. 13) or other logic that is configured to store information in the memory devices or execute instructions stored in the memory array. In some embodiments, the die

5202 may include one or more conductive lines 112 and/or conductive vias 114 having any of the graphitic liners 104 disclosed herein.

[0071] FIG. 11 is a cross-sectional side view of an IC device 5300 that may include any of the graphitic liners 104 disclosed herein. Any of the IC devices 5300 discussed herein may be examples of the IC device 100. In particular, any of the conductive structures (e.g., conductive vias or lines) discussed below with reference to FIG. 11 may include any of the graphitic liners 104 disclosed herein. The IC device 5300 may be formed on a substrate 5302 (e.g., the wafer 5200 of FIG. 10A) and may be included in a die (e.g., the die 5202 of FIG. 10B). The substrate 5302 may be a semiconductor substrate composed of semiconductor material systems including, for example, N-type or P-type material systems. The substrate 5302 may include, for example, a crystalline substrate formed using a bulk silicon or a silicon-on-insulator substructure. In some embodiments, the substrate 5302 may be formed using alternative materials, which may or may not be combined with silicon, that include but are not limited to germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, or gallium antimonide. Further materials classified as group II-VI, III-V, or IV may also be used to form the substrate 5302. Although a few examples of materials from which the substrate 5302 may be formed are described here, any material that may serve as a foundation for an IC device 5300 may be used. The substrate 5302 may be part of a singulated die (e.g., the dies 5202 of FIG. 10B) or a wafer (e.g., the wafer 5200 of FIG. 10A).

[0072] The IC device 5300 may include one or more device layers 5304 disposed on the substrate 5302. The device layer 5304 may include features of one or more transistors 5340 (e.g., metal oxide semiconductor field-effect transistors (MOSFETs)) formed on the substrate 5302. The device layer 5304 may include, for example, one or more source and/or drain (S/D) regions 5320, a gate 5322 to control current flow in the transistors 5340 between the S/D regions 5320, and one or more S/D contacts 5324 to route electrical signals to/from the S/D regions 5320. The transistors 5340 may include additional features not depicted for the sake of clarity, such as device isolation regions, gate contacts, and the like. The transistors 5340 are not limited to the type and configuration depicted in FIG. 11 and may include a wide variety of other types and configurations such as, for example, planar transistors, nonplanar transistors, or a combination of both. Nonplanar transistors may include FinFET transistors, such as double-gate transistors or tri-gate transistors, and wraparound or all-around gate transistors, such as nanoribbon and nanowire transistors.

[0073] Each transistor 5340 may include a gate 5322 formed of at least two layers, a gate dielectric layer and a gate electrode layer. The gate dielectric layer may include one layer or a stack of layers. The one or more layers may include silicon oxide, silicon dioxide, and/or a high-k dielectric material.

The high-k dielectric material may include elements such as hafnium, silicon, oxygen, titanium, tantalum, lanthanum, aluminum, zirconium, barium, strontium, yttrium, lead, scandium, niobium, and zinc. Examples of high-k materials that may be used in the gate dielectric layer include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. In some embodiments, an annealing process may be carried out on the gate dielectric layer to improve its quality when a high-k material is used.

[0074] The gate electrode layer may be formed on the gate dielectric layer and may include at least one P-type work-function metal or N-type work-function metal, depending on whether the transistor 5340 is to be a PMOS or an NMOS transistor. In some implementations, the gate electrode layer may consist of a stack of two or more metal layers, where one or more metal layers are work-function metal layers and at least one metal layer is a fill metal layer. Further metal layers may be included for other purposes, such as a barrier layer. For a PMOS transistor, metals that may be used for the gate electrode include, but are not limited to, ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides (e.g., ruthenium oxide). For an NMOS transistor, metals that may be used for the gate electrode include, but are not limited to, hafnium, zirconium, titanium, tantalum, aluminum, alloys of these metals, and carbides of these metals (e.g., hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, and aluminum carbide).

[0075] In some embodiments, when viewed as a cross section of the transistor 5340 along the source-channel-drain direction, the gate electrode may consist of a U-shaped structure that includes a bottom portion substantially parallel to the surface of the substrate and two sidewall portions that are substantially perpendicular to the top surface of the substrate. In other embodiments, at least one of the metal layers that form the gate electrode may simply be a planar layer that is substantially parallel to the top surface of the substrate and does not include sidewall portions substantially perpendicular to the top surface of the substrate. In other embodiments, the gate electrode may consist of a combination of U-shaped structures and planar, non-U-shaped structures. For example, the gate electrode may consist of one or more U-shaped metal layers formed atop one or more planar, non-U-shaped layers.

[0076] In some embodiments, a pair of sidewall spacers may be formed on opposing sides of the gate stack to bracket the gate stack. The sidewall spacers may be formed from a material such as silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, and silicon oxynitride. Processes for forming sidewall spacers are well known in the art and generally include deposition and etching process steps. In some embodiments, a plurality of spacer pairs may be used; for

instance, two pairs, three pairs, or four pairs of sidewall spacers may be formed on opposing sides of the gate stack.

[0077] The S/D regions 5320 may be formed within the substrate 5302 adjacent to the gate 5322 of each transistor 5340. The S/D regions 5320 may be formed using either an implantation/diffusion process or an etching/deposition process, for example. In the former process, dopants such as boron, aluminum, antimony, phosphorous, or arsenic may be ion-implanted into the substrate 5302 to form the S/D regions 5320. An annealing process that activates the dopants and causes them to diffuse farther into the substrate 5302 may follow the ion-implantation process. In the latter process, the substrate 5302 may first be etched to form recesses at the locations of the S/D regions 5320. An epitaxial deposition process may then be carried out to fill the recesses with material that is used to fabricate the S/D regions 5320. In some implementations, the S/D regions 5320 may be fabricated using a silicon alloy such as silicon germanium or silicon carbide. In some embodiments, the epitaxially deposited silicon alloy may be doped in situ with dopants such as boron, arsenic, or phosphorous. In some embodiments, the S/D regions 5320 may be formed using one or more alternate semiconductor materials such as germanium or a group III-V material or alloy. In further embodiments, one or more layers of metal and/or metal alloys may be used to form the S/D regions 5320.

[0078] Electrical signals, such as power and/or input/output (I/O) signals, may be routed to and/or from the transistors 5340 of the device layer 5304 through one or more interconnect layers disposed on the device layer 5304 (illustrated in FIG. 11 as interconnect layers 5306-5310). For example, electrically conductive features of the device layer 5304 (e.g., the gate 5322 and the S/D contacts 5324) may be electrically coupled with the interconnect structures 5328 of the interconnect layers 5306-5310. The one or more interconnect layers 5306-5310 may form an interlayer dielectric (ILD) stack 5319 of the IC device 5300. Any of the interconnect structures 5328 in the interconnect layers 5306-5310 may include any of the graphitic liners 104 disclosed herein.

[0079] The interconnect structures 5328 may be arranged within the interconnect layers 5306-5310 to route electrical signals according to a wide variety of designs (in particular, the arrangement is not limited to the particular configuration of interconnect structures 5328 depicted in FIG. 11). Although a particular number of interconnect layers 5306-5310 is depicted in FIG. 11, embodiments of the present disclosure include IC devices having more or fewer interconnect layers than depicted.

[0080] In some embodiments, the interconnect structures 5328 may include conductive lines 5328a and/or conductive vias 5328b filled with an electrically conductive material such as a metal (e.g., the conductive material 106). In some embodiments, the conductive lines 5328a may take the form of any of the conductive lines 112 discussed above, and the conductive vias 5328b may take the form

of any of the conductive vias 114 discussed above. The conductive lines 5328a may be arranged to route electrical signals in a direction of a plane that is substantially parallel with a surface of the substrate 5302 upon which the device layer 5304 is formed. For example, the conductive lines 5328a may route electrical signals in a direction in and out of the page from the perspective of FIG. 11. The conductive vias 5328b may be arranged to route electrical signals in a direction of a plane that is substantially perpendicular to the surface of the substrate 5302 upon which the device layer 5304 is formed.

[0081] The interconnect layers 5306-5310 may include a dielectric material 5326 disposed between the interconnect structures 5328, as shown in FIG. 11. In some embodiments, the dielectric material 5326 disposed between the interconnect structures 5328 in different ones of the interconnect layers 5306-5310 may have different compositions; in other embodiments, the composition of the dielectric material 5326 between different interconnect layers 5306-5310 may be the same. The dielectric material 5326 may take the form of any of the embodiments of the insulating material 102 discussed above. In some embodiments, the conductive material of the interconnect structures 5328 may be spaced apart from the dielectric material 5326 by any of the graphitic liners 104 disclosed herein. In some embodiments, no graphitic liner 104 may be disposed between a conductive via 5328b and the interconnect structure 5328 directly "below" the conductive via 5328b (e.g., as discussed above with reference to FIGS. 3-4).

[0082] A first interconnect layer 5306 (referred to as Metal 1 or "M1") may be formed directly on the device layer 5304. In some embodiments, the first interconnect layer 5306 may include conductive lines 5328a and/or conductive vias 5328b, as shown. The conductive lines 5328a of the first interconnect layer 5306 may be coupled with contacts (e.g., the S/D contacts 5324) of the device layer 5304.

[0083] A second interconnect layer 5308 (referred to as Metal 2 or "M2") may be formed directly on the first interconnect layer 5306. In some embodiments, the second interconnect layer 5308 may include conductive vias 5328b to couple the conductive lines 5328a of the second interconnect layer 5308 with the conductive lines 5328a of the first interconnect layer 5306. Although the conductive lines 5328a and the conductive vias 5328b are structurally delineated with a line within each interconnect layer (e.g., within the second interconnect layer 5308) for the sake of clarity, the conductive lines 5328a and the conductive vias 5328b may be structurally and/or materially contiguous (e.g., simultaneously filled during a dual-damascene process) in some embodiments.

[0084] A third interconnect layer 5310 (referred to as Metal 3 or "M3") (and additional interconnect layers, as desired) may be formed in succession on the second interconnect layer 5308 according to

similar techniques and configurations described in connection with the second interconnect layer 5308 or the first interconnect layer 5306.

[0085] The IC device 5300 may include a solder resist material 5334 (e.g., polyimide or similar material) and one or more bond pads 5336 formed on the interconnect layers 5306-5310. The bond pads 5336 may be electrically coupled with the interconnect structures 5328 and configured to route the electrical signals of the transistor(s) 5340 to other external devices. For example, solder bonds may be formed on the one or more bond pads 5336 to mechanically and/or electrically couple a chip including the IC device 5300 with another component (e.g., a circuit board). The IC device 5300 may have other alternative configurations to route the electrical signals from the interconnect layers 5306-5310 than depicted in other embodiments. For example, the bond pads 5336 may be replaced by or may further include other analogous features (e.g., posts) that route the electrical signals to external components.

[0086] FIG. 12 is a cross-sectional side view of an IC device assembly 5400 that may include any of the graphitic liners 104 disclosed herein. The IC device assembly 5400 includes a number of components disposed on a circuit board 5402. The IC device assembly 5400 may include components disposed on a first face 5440 of the circuit board 5402 and an opposing second face 5442 of the circuit board 5402; generally, components may be disposed on one or both faces 5440 and 5442.

[0087] In some embodiments, the circuit board 5402 may be a printed circuit board (PCB) including multiple metal layers separated from one another by layers of dielectric material and interconnected by electrically conductive vias. Any one or more of the metal layers may be formed in a desired circuit pattern to route electrical signals (optionally in conjunction with other metal layers) between the components coupled to the circuit board 5402. In other embodiments, the circuit board 5402 may be a non-PCB substrate.

[0088] The IC device assembly 5400 illustrated in FIG. 12 includes a package-on-interposer structure 5436 coupled to the first face 5440 of the circuit board 5402 by coupling components 5416. The coupling components 5416 may electrically and mechanically couple the package-on-interposer structure 5436 to the circuit board 5402, and may include solder balls (as shown in FIG. 12), male and female portions of a socket, an adhesive, an underfill material, and/or any other suitable electrical and/or mechanical coupling structure.

[0089] The package-on-interposer structure 5436 may include an IC package 5420 coupled to an interposer 5404 by coupling components 5418. The coupling components 5418 may take any suitable form for the application, such as the forms discussed above with reference to the coupling components 5416. Although a single IC package 5420 is shown in FIG. 12, multiple IC packages may

be coupled to the interposer 5404; indeed, additional interposers may be coupled to the interposer 5404. The interposer 5404 may provide an intervening substrate used to bridge the circuit board 5402 and the IC package 5420. The IC package 5420 may be or include, for example, a die (the die 5202 of FIG. 10B), an IC device (e.g., the IC device 5300 of FIG. 11 or any of the IC devices 100 disclosed herein), or any other suitable component. Generally, the interposer 5404 may spread a connection to a wider pitch or reroute a connection to a different connection. For example, the interposer 5404 may couple the IC package 5420 (e.g., a die) to a ball grid array (BGA) of the coupling components 5416 for coupling to the circuit board 5402. In the embodiment illustrated in FIG. 12, the IC package 5420 and the circuit board 5402 are attached to opposing sides of the interposer 5404; in other embodiments, the IC package 5420 and the circuit board 5402 may be attached to a same side of the interposer 5404. In some embodiments, three or more components may be interconnected by way of the interposer 5404.

[0090] The interposer 5404 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In some embodiments, the interposer 5404 may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials. The interposer 5404 may include metal interconnects 5408 and vias 5410, including but not limited to through-silicon vias (TSVs) 5406. The interposer 5404 may further include embedded devices 5414, including both passive and active devices. Such devices may include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, electrostatic discharge (ESD) devices, and memory devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and microelectromechanical systems (MEMS) devices may also be formed on the interposer 5404. The package-on-interposer structure 5436 may take the form of any of the package-on-interposer structures known in the art.

[0091] The IC device assembly 5400 may include an IC package 5424 coupled to the first face 5440 of the circuit board 5402 by coupling components 5422. The coupling components 5422 may take the form of any of the embodiments discussed above with reference to the coupling components 5416, and the IC package 5424 may take the form of any of the embodiments discussed above with reference to the IC package 5420.

[0092] The IC device assembly 5400 illustrated in FIG. 12 includes a package-on-package structure 5434 coupled to the second face 5442 of the circuit board 5402 by coupling components 5428. The package-on-package structure 5434 may include an IC package 5426 and an IC package 5432 coupled together by coupling components 5430 such that the IC package 5426 is disposed between the

circuit board 5402 and the IC package 5432. The coupling components 5428 and 5430 may take the form of any of the embodiments of the coupling components 5416 discussed above, and the IC packages 5426 and 5432 may take the form of any of the embodiments of the IC package 5420 discussed above.

[0093] FIG. 13 is a block diagram of an example computing device 5500 that may include any of the graphitic liners 104 disclosed herein. For example, any suitable ones of the components of the computing device 5500 may include, or be included in, a die including one or more graphitic liners 104 in accordance with any of the embodiments disclosed herein. A number of components are illustrated in FIG. 13 as included in the computing device 5500, but any one or more of these components may be omitted or duplicated, as suitable for the application. In some embodiments, some or all of the components included in the computing device 5500 may be attached to one or more motherboards. In some embodiments, some or all of these components are fabricated onto a single system-on-a-chip (SoC) die.

[0094] Additionally, in various embodiments, the computing device 5500 may not include one or more of the components illustrated in FIG. 13, but the computing device 5500 may include interface circuitry for coupling to the one or more components. For example, the computing device 5500 may not include a display device 5506, but may include display device interface circuitry (e.g., a connector and driver circuitry) to which a display device 5506 may be coupled. In another set of examples, the computing device 5500 may not include an audio input device 5524 or an audio output device 5508, but may include audio input or output device interface circuitry (e.g., connectors and supporting circuitry) to which an audio input device 5524 or audio output device 5508 may be coupled.

[0095] The computing device 5500 may include a processing device 5502 (e.g., one or more processing devices). As used herein, the term "processing device" or "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory. The processing device 5502 may include one or more digital signal processors (DSPs), application-specific integrated circuits (ASICs), central processing units (CPUs), graphics processing units (GPUs), cryptoprocessors (specialized processors that execute cryptographic algorithms within hardware), server processors, or any other suitable processing devices. The computing device 5500 may include a memory 5504, which may itself include one or more memory devices such as volatile memory (e.g., dynamic random access memory (DRAM)), nonvolatile memory (e.g., read-only memory (ROM)), flash memory, solid state memory, and/or a hard drive. In some embodiments, the memory 5504 may include memory that shares a die with the processing device 5502. This memory

may be used as cache memory and may include embedded dynamic random access memory (eDRAM) or spin transfer torque magnetic random-access memory (STT-MRAM). In some embodiments, the processing device 5502 and/or the memory 5504 may include one or more of the graphitic liners 104 disclosed herein.

[0096] In some embodiments, the computing device 5500 may include a communication chip 5512 (e.g., one or more communication chips). For example, the communication chip 5512 may be configured for managing wireless communications for the transfer of data to and from the computing device 5500. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a nonsolid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. In some embodiments, the communication chip 5512 may include one or more of the graphitic liners 104 disclosed herein.

[0097] The communication chip 5512 may implement any of a number of wireless standards or protocols, including but not limited to Institute for Electrical and Electronic Engineers (IEEE) standards including Wi-Fi (IEEE 802.11 family), IEEE 802.16 standards (e.g., IEEE 802.16-2005 Amendment), Long-Term Evolution (LTE) project along with any amendments, updates, and/or revisions (e.g., advanced LTE project, ultra-mobile broadband (UMB) project (also referred to as "3GPP2"), etc.). IEEE 802.16 compatible Broadband Wireless Access (BWA) networks are generally referred to as WiMAX networks, an acronym that stands for Worldwide Interoperability for Microwave Access, which is a certification mark for products that pass conformity and interoperability tests for the IEEE 802.16 standards. The communication chip 5512 may operate in accordance with a Global System for Mobile Communication (GSM), General Packet Radio Service (GPRS), Universal Mobile Telecommunications System (UMTS), High Speed Packet Access (HSPA), Evolved HSPA (E-HSPA), or LTE network. The communication chip 5512 may operate in accordance with Enhanced Data for GSM Evolution (EDGE), GSM EDGE Radio Access Network (GERAN), Universal Terrestrial Radio Access Network (UTRAN), or Evolved UTRAN (E-UTRAN). The communication chip 5512 may operate in accordance with Code Division Multiple Access (CDMA), Time Division Multiple Access (TDMA), Digital Enhanced Cordless Telecommunications (DECT), Evolution-Data Optimized (EV-DO), and derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The communication chip 5512 may operate in accordance with other wireless protocols in other embodiments. The computing device 5500 may include an antenna 5522 to facilitate wireless communications and/or to receive other wireless communications (such as AM or FM radio transmissions).

[0098] In some embodiments, the communication chip 5512 may manage wired communications, such as electrical, optical, or any other suitable communication protocols (e.g., the Ethernet). As noted above, the communication chip 5512 may include multiple communication chips. For instance, a first communication chip 5512 may be dedicated to shorter-range wireless communications such as Wi-Fi or Bluetooth, and a second communication chip 5512 may be dedicated to longer-range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, EV-DO, or others. In some embodiments, a first communication chip 5512 may be dedicated to wireless communications, and a second communication chip 5512 may be dedicated to wired communications.

[0099] The computing device 5500 may include battery/power circuitry 5514. The battery/power circuitry 5514 may include one or more energy storage devices (e.g., batteries or capacitors) and/or circuitry for coupling components of the computing device 5500 to an energy source separate from the computing device 5500 (e.g., AC line power).

[0100] The computing device 5500 may include a display device 5506 (or corresponding interface circuitry, as discussed above). The display device 5506 may include any visual indicators, such as a heads-up display, a computer monitor, a projector, a touchscreen display, a liquid crystal display (LCD), a light-emitting diode display, or a flat panel display, for example.

[0101] The computing device 5500 may include an audio output device 5508 (or corresponding interface circuitry, as discussed above). The audio output device 5508 may include any device that generates an audible indicator, such as speakers, headsets, or earbuds, for example.

[0102] The computing device 5500 may include an audio input device 5524 (or corresponding interface circuitry, as discussed above). The audio input device 5524 may include any device that generates a signal representative of a sound, such as microphones, microphone arrays, or digital instruments (e.g., instruments having a musical instrument digital interface (MIDI) output).

[0103] The computing device 5500 may include a global positioning system (GPS) device 5518 (or corresponding interface circuitry, as discussed above). The GPS device 5518 may be in communication with a satellite-based system and may receive a location of the computing device 5500, as known in the art.

[0104] The computing device 5500 may include an other output device 5510 (or corresponding interface circuitry, as discussed above). Examples of the other output device 5510 may include an audio codec, a video codec, a printer, a wired or wireless transmitter for providing information to other devices, or an additional storage device.

[0105] The computing device 5500 may include an other input device 5520 (or corresponding interface circuitry, as discussed above). Examples of the other input device 5520 may include an

accelerometer, a gyroscope, a compass, an image capture device, a keyboard, a cursor control device such as a mouse, a stylus, a touchpad, a bar code reader, a Quick Response (QR) code reader, any sensor, or a radio frequency identification (RFID) reader.

[0106] The computing device 5500 may have any desired form factor, such as a hand-held or mobile computing device (e.g., a cell phone, a smart phone, a mobile internet device, a music player, a tablet computer, a laptop computer, a netbook computer, an ultrabook computer, a personal digital assistant (PDA), an ultra-mobile personal computer, etc.), a desktop computing device, a server or other networked computing component, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a vehicle control unit, a digital camera, a digital video recorder, or a wearable computing device. In some embodiments, the computing device 5500 may be any other electronic device that processes data.

[0107] The following paragraphs provide various examples of the embodiments disclosed herein.

[0108] Example A1 is an integrated circuit (IC) device, including: an insulating material; a conductive structure in the insulating material, wherein the conductive structure includes a conductive material; a first liner between the conductive material and the insulating material, wherein the first liner includes metal; and a second liner between the conductive material and the first liner, wherein the second liner includes graphene.

[0109] Example A2 may include the subject matter of Example A1, and may further specify that the first liner includes tantalum, titanium, or ruthenium.

[0110] Example A3 may include the subject matter of any of Examples A1-2, and may further specify that the first liner has a thickness between 0.5 nanometers and 12 nanometers.

[0111] Example A4 may include the subject matter of any of Examples A1-3, and may further specify that the second liner includes between 1 and 10 graphene monolayers.

[0112] Example A5 may include the subject matter of any of Examples A1-4, and may further specify that the second liner has a thickness between 3 and 80 nanometers.

[0113] Example A6 may include the subject matter of any of Examples A1-5, and may further specify that the graphene of the second liner has a defect gradient between the insulating material and the conductive material.

[0114] Example A7 may include the subject matter of Example A6, and may further specify that the defect gradient is such that the graphene closer to the insulating material has more defects than the graphene closer to the conductive material.

[0115] Example A8 may include the subject matter of any of Examples A6-7, and may further specify that the graphene with more defects has a higher ratio between an amplitude of a D peak

and an amplitude of a G peak in a Raman spectrum (D/G ratio) than the graphene with fewer defects.

[0116] Example A9 may include the subject matter of any of Examples A1-8, and may further specify that the second liner does not include a silane, a phosphonic acid, a germane, or an ethylene-terminated compound.

[0117] Example A10 may include the subject matter of any of Examples A1-9, and may further specify that the conductive structure is a conductive via or a conductive line.

[0118] Example A11 may include the subject matter of any of Examples A1-10, and may further specify that the conductive material includes copper.

[0119] Example A12 may include the subject matter of any of Examples A1-11, and may further specify that the insulating material includes an interlayer dielectric (ILD), and the first liner is in contact with the ILD.

[0120] Example A13 may include the subject matter of any of Examples A1-12, and may further specify that the second liner is in contact with the conductive material.

[0121] Example A14 may include the subject matter of any of Examples A1-13, and may further specify that the first liner is in contact with the second liner.

[0122] Example A15 is an integrated circuit (IC) device, including: an insulating material; a conductive structure in the insulating material, wherein the conductive structure includes a conductive material; and a liner between the conductive material and the insulating material, wherein the liner includes graphene having a defect gradient between the insulating material and the conductive material.

[0123] Example A16 may include the subject matter of Example A15, and may further specify that the defect gradient is such that the graphene closer to the insulating material has more defects than the graphene closer to the conductive material.

[0124] Example A17 may include the subject matter of Example A16, and may further specify that the graphene with more defects has a higher ratio between an amplitude of a D peak and an amplitude of a G peak in a Raman spectrum (D/G ratio) than the graphene with fewer defects.

[0125] Example A18 may include the subject matter of any of Examples A15-17, and may further specify that the liner includes between 1 and 10 graphene monolayers.

[0126] Example A19 may include the subject matter of any of Examples A15-18, and may further specify that the liner has a thickness between 3 and 80 nanometers.

[0127] Example A20 may include the subject matter of any of Examples A15-19, and may further specify that the liner does not include a silane, a phosphonic acid, a germane, or an ethylene-terminated compound.

[0128] Example A21 may include the subject matter of any of Examples A15-20, and may further specify that the conductive structure is a conductive via or a conductive line.

[0129] Example A22 may include the subject matter of any of Examples A15-21, and may further specify that the conductive material includes copper.

[0130] Example A23 may include the subject matter of any of Examples A15-22, and may further specify that the insulating material includes an interlayer dielectric (ILD), and the liner is in contact with the ILD.

[0131] Example A24 may include the subject matter of any of Examples A15-23, and may further specify that the liner is in contact with the conductive material.

[0132] Example A25 is a method of manufacturing an integrated circuit (IC) device, including: providing an insulating material having a cavity; providing a first liner on sidewalls of the cavity, wherein the first liner includes a metal; providing a second liner on the first liner, wherein the second liner includes graphene; and after providing the second liner, providing a conductive material in the cavity, wherein the first liner is disposed between a sidewall of the cavity and the second liner, and the second liner is disposed between the conductive material and the first liner.

[0133] Example A26 may include the subject matter of Example A25, and may further specify that providing the first liner includes atomic layer deposition (ALD) or chemical vapor deposition (CVD) of the metal.

[0134] Example A27 may include the subject matter of any of Examples A25-26, and may further specify that providing the second liner on the first liner includes atomic layer deposition (ALD) or chemical vapor deposition (CVD) of the graphene.

[0135] Example A28 may include the subject matter of any of Examples A25-27, and may further specify that the cavity extends down to a conductive line or via in the insulating material.

[0136] Example A29 may include the subject matter of any of Examples A25-28, and may further specify that the second liner includes graphene having a defect gradient between the insulating material and the conductive material.

[0137] Example A30 may include the subject matter of Example A29, and may further specify that the defect gradient is such that the graphene closer to the insulating material has more defects than the graphene closer to the conductive material.

[0138] Example A31 may include the subject matter of any of Examples A29-30, and may further specify that providing the second liner on the first liner includes providing the second liner at progressively higher temperatures.

[0139] Example A32 is a method of manufacturing an integrated circuit (IC) device, including: providing an insulating material having a cavity; providing a liner on sidewalls of the cavity, wherein

the liner includes graphene having a defect gradient in which a defect density of the graphene increases farther away from the sidewalls of the cavity; and after providing the liner, providing a conductive material in the cavity, wherein the liner is disposed between a sidewall of the cavity and the conductive material.

[0140] Example A33 may include the subject matter of Example A32, and may further specify that providing the liner includes atomic layer deposition (ALD) or chemical vapor deposition (CVD) of the graphene.

[0141] Example A34 may include the subject matter of any of Examples A32-33, and may further specify that the defect gradient is a stepped gradient having two or more defect levels.

[0142] Example A35 may include the subject matter of any of Examples A32-33, and may further specify that the defect gradient is a continuous gradient.

[0143] Example A36 may include the subject matter of any of Examples A32-35, and may further specify that providing the insulating material having the cavity includes removing some of the insulating material to form the cavity.

[0144] Example A37 may include the subject matter of any of Examples A32-36, and may further specify that the liner is provided at progressively higher temperatures.

[0145] Example A38 may include the subject matter of any of Examples A32-37, and may further specify that the liner has a thickness between 3 and 80 angstroms.

[0146] Example A39 is a computing device, including: a processing device including an interlayer dielectric (ILD), a conductive via in the ILD, wherein the conductive via includes a conductive material, a first liner between the conductive material and the ILD, wherein the first liner includes metal, and a second liner between the conductive material and the first liner, wherein the second liner includes graphene; and a memory device, communicatively coupled to the processing device.

[0147] Example A40 may include the subject matter of Example A39, and may further specify that the graphene of the second liner has a defect gradient between the ILD and the conductive material.

[0148] Example A41 may include the subject matter of any of Examples A39-40, and may further specify that the computing device is a mobile computing device.

[0149] Example A42 may include the subject matter of any of Examples A39-41, and may further include one or more communication chips.

[0150] Example A43 may include the subject matter of any of Examples A39-42, and may further specify that the processing device is included in an integrated circuit (IC) die.

[0151] Example A44 is a computing device, including: a processing device including an interlayer dielectric (ILD), a conductive via in the ILD, wherein the conductive via includes a conductive material, a liner between the conductive material and the ILD, wherein the liner includes graphene

having a defect gradient between the ILD and the conductive material; and a memory device, communicatively coupled to the processing device.

[0152] Example A45 may include the subject matter of Example A44, and may further specify that, in the liner, graphene with fewer defects is proximate to the conductive material and graphene with more defects is proximate to the ILD.

[0153] Example A46 may include the subject matter of any of Examples A44-45, and may further specify that the computing device is a mobile computing device.

[0154] Example A47 may include the subject matter of any of Examples A44-46, and may further include one or more communication chips.

[0155] Example A48 may include the subject matter of any of Examples A44-47, and may further specify that the processing device is included in an integrated circuit (IC) die.

[0156] Example A49 is an integrated circuit (IC) device manufactured by the method of any of Examples A25-38.

[0157] Example A50 is a computing device including the integrated circuit (IC) device of any of Examples A1-24.

[0158] Example B1 is an integrated circuit (IC) device, including: an insulating material; a conductive via in the insulating material, wherein the conductive via includes a conductive material, and the conductive material extends down to contact a conductive structure; and a liner between the conductive material and the insulating material, wherein the liner includes graphene.

[0159] Example B2 may include the subject matter of Example B1, and may further specify that the conductive structure includes a recess, and the conductive material of the conductive via extends into the recess to contact the conductive structure.

[0160] Example B3 may include the subject matter of Example B2, and may further specify that the recess extends under the liner.

[0161] Example B4 may include the subject matter of Example B3, and may further specify that the recess extends under the insulating material.

[0162] Example B5 may include the subject matter of any of Examples B1-4, and may further specify that the conductive material includes cobalt, ruthenium, nickel, molybdenum, or tungsten.

[0163] Example B6 may include the subject matter of any of Examples B1-5, and may further specify that the conductive material includes a refractory metal.

[0164] Example B7 may include the subject matter of any of Examples B1-6, and may further specify that the liner includes between 1 and 10 graphene monolayers.

[0165] Example B8 may include the subject matter of any of Examples B1-7, and may further specify that the liner has a thickness between 3 and 80 nanometers.

[0166] Example B9 may include the subject matter of any of Examples B1-8, and may further specify that the liner does not include a silane, a phosphonic acid, a germane, or an ethylene-terminated compound.

[0167] Example B10 may include the subject matter of any of Examples B1-9, and may further specify that the conductive structure is a conductive via or a conductive line.

[0168] Example B11 may include the subject matter of any of Examples B1-10, and may further specify that the liner is in contact with the insulating material.

[0169] Example B12 may include the subject matter of any of Examples B1-11, and may further specify that the insulating material includes an interlayer dielectric (ILD).

[0170] Example B13 may include the subject matter of any of Examples B1-12, and may further specify that the liner is in contact with the conductive material.

[0171] Example B14 is a method of manufacturing an integrated circuit (IC) device, including: forming a via cavity in an insulating material, wherein the via cavity extends down to a conductive structure so that the conductive structure is at a bottom of the cavity; providing a liner on the bottom and sidewalls of the via cavity, wherein the liner includes graphene; oxidizing a portion of the conductive structure proximate to the bottom of the via cavity; removing the oxidized portion and some of the liner at the bottom of the via cavity; and after removing the oxidized portion and some of the liner at the bottom of the via cavity, providing a conductive material in the via cavity.

[0172] Example B15 may include the subject matter of Example B14, and may further specify that providing the liner includes atomic layer deposition (ALD) or chemical vapor deposition (CVD) of the graphene.

[0173] Example B16 may include the subject matter of any of Examples B14-15, and may further specify that removing the oxidized portion and some of the liner includes lift-off of the oxidized portion.

[0174] Example B17 may include the subject matter of any of Examples B14-16, and may further specify that the liner includes defects, and oxidizing the portion of the conductive structure includes oxidizing the portion of the conductive structure through the defects.

[0175] Example B18 may include the subject matter of any of Examples B14-17, and may further specify that the portion of the conductive structure proximate to the bottom of the via cavity is oxidized after the liner is provided.

[0176] Example B19 may include the subject matter of any of Examples B14-18, and may further specify that the conductive structure includes a conductive via or a conductive line.

[0177] Example B20 may include the subject matter of any of Examples B14-1819 wherein the liner has a thickness between 3 and 80 angstroms.

[0178] Example B21 is a computing device, including: a processing device including an interlayer dielectric (ILD), a conductive via in the ILD, wherein the conductive via includes a conductive material, and the conductive via is in electrical contact with a conductive structure below the conductive via, a liner between the conductive material and the ILD, wherein the liner includes graphene; and a memory device, communicatively coupled to the processing device.

[0179] Example B22 may include the subject matter of Example B21, and may further specify that no graphene is between the conductive structure and the conductive material of the conductive via.

[0180] Example B23 may include the subject matter of any of Examples B21-22, and may further specify that the conductive material of the conductive via extends into a recess in the conductive structure.

[0181] Example B24 may include the subject matter of any of Examples B21-23, and may further specify that the conductive structure includes a conductive via or a conductive line.

[0182] Example B25 may include the subject matter of any of Examples B21-24, and may further specify that the computing device is a mobile computing device.

[0183] Example B26 may include the subject matter of any of Examples B21-25, and may further include one or more communication chips.

[0184] Example B27 may include the subject matter of any of Examples B21-26, and may further specify that the processing device is included in an integrated circuit (IC) die.

[0185] Example B28 is an integrated circuit (IC) device manufactured by the method of any of Examples B14-20.

[0186] Example B29 is a computing device including the integrated circuit (IC) device of any of Examples B1-13.

Claims:

1. An integrated circuit (IC) device, comprising:
an insulating material;
a conductive structure in the insulating material, wherein the conductive structure includes a conductive material;
a first liner between the conductive material and the insulating material, wherein the first liner includes metal; and
a second liner between the conductive material and the first liner, wherein the second liner includes graphene.

2. The IC device of claim 1, wherein the first liner includes tantalum, titanium, or ruthenium.

3. The IC device of claim 1, wherein the first liner has a thickness between 0.5 nanometers and 12 nanometers.

4. The IC device of claim 1, wherein the second liner has a thickness between 3 and 80 nanometers.

5. The IC device of claim 1, wherein the graphene of the second liner has a defect gradient between the insulating material and the conductive material.

6. The IC device of any of claims 1-5, wherein the second liner does not include a silane, a phosphonic acid, a germane, or an ethylene-terminated compound.

7. The IC device of any of claims 1-5, wherein the conductive structure is a conductive via or a conductive line.

8. The IC device of any of claims 1-5, wherein the conductive material includes copper.

9. The IC device of any of claims 1-5, wherein the first liner is in contact with the second liner.

10. An integrated circuit (IC) device, comprising:
an insulating material;

a conductive structure in the insulating material, wherein the conductive structure includes a conductive material; and
a liner between the conductive material and the insulating material, wherein the liner includes graphene having a defect gradient between the insulating material and the conductive material.

11. The IC device of claim 10, wherein the defect gradient is such that the graphene closer to the insulating material has more defects than the graphene closer to the conductive material.

12. The IC device of claim 11, wherein the graphene with more defects has a higher ratio between an amplitude of a D peak and an amplitude of a G peak in a Raman spectrum (D/G ratio) than the graphene with fewer defects.

13. The IC device of claim 10, wherein the liner includes between 1 and 10 graphene monolayers.

14. The IC device of any of claims 10-13, wherein the conductive material includes copper.

15. The IC device of any of claims 10-13, wherein the insulating material includes an interlayer dielectric (ILD), and the liner is in contact with the ILD.

16. The IC device of any of claims 10-13, wherein the liner is in contact with the conductive material.

17. A method of manufacturing an integrated circuit (IC) device, comprising:
providing an insulating material having a cavity;
providing a first liner on sidewalls of the cavity, wherein the first liner includes a metal;
providing a second liner on the first liner, wherein the second liner includes graphene; and
after providing the second liner, providing a conductive material in the cavity, wherein the first liner is disposed between a sidewall of the cavity and the second liner, and the second liner is disposed between the conductive material and the first liner.

18. The method of claim 17, wherein providing the first liner includes atomic layer deposition (ALD) or chemical vapor deposition (CVD) of the metal.

19. The method of claim 17, wherein providing the second liner on the first liner includes atomic layer deposition (ALD) or chemical vapor deposition (CVD) of the graphene.

20. The method of any of claims 17-19, wherein the cavity extends down to a conductive line or via in the insulating material.

21. The method of any of claims 17-19, wherein the second liner includes graphene having a defect gradient between the insulating material and the conductive material.

22. A method of manufacturing an integrated circuit (IC) device, comprising:
providing an insulating material having a cavity;
providing a liner on sidewalls of the cavity, wherein the liner includes graphene having a defect gradient in which a defect density of the graphene increases farther away from the sidewalls of the cavity; and
after providing the liner, providing a conductive material in the cavity, wherein the liner is disposed between a sidewall of the cavity and the conductive material.

23. The method of claim 22, wherein providing the liner includes atomic layer deposition (ALD) or chemical vapor deposition (CVD) of the graphene.

24. The method of any of claims 22-23, wherein the defect gradient is a stepped gradient having two or more defect levels.

25. The method of any of claims 22-23, wherein the defect gradient is a continuous gradient.

FIG. 1

FIG. 2

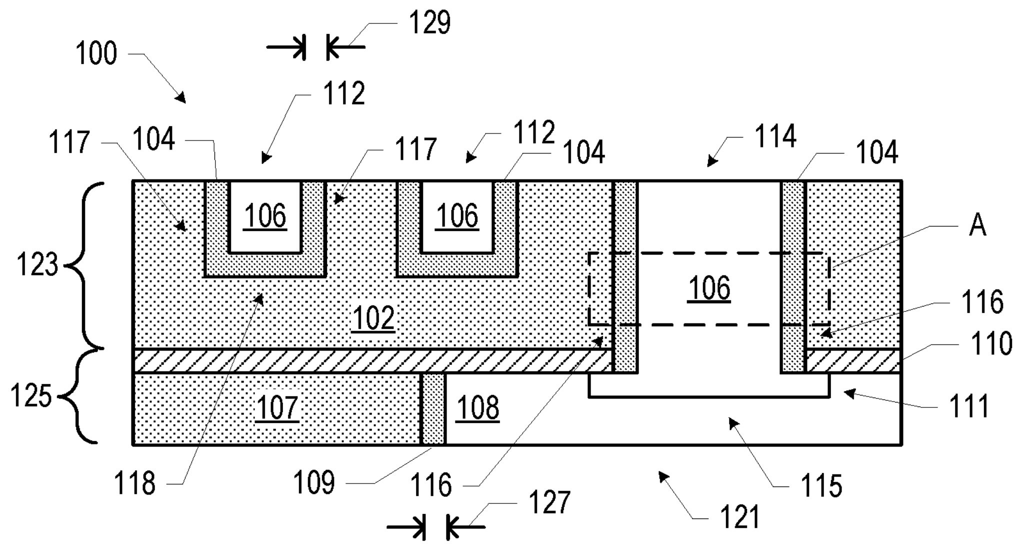

FIG. 3

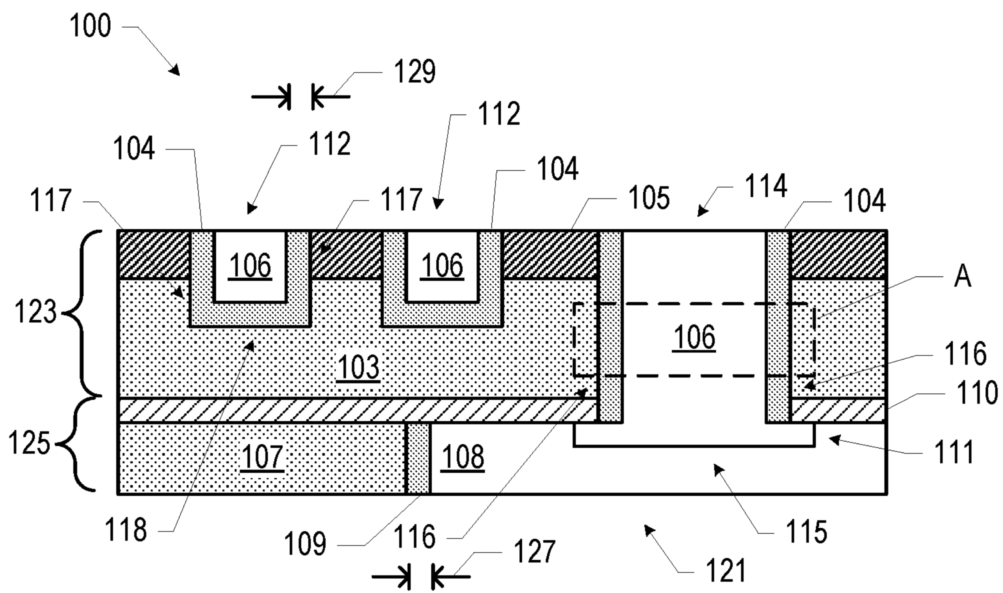

FIG. 4

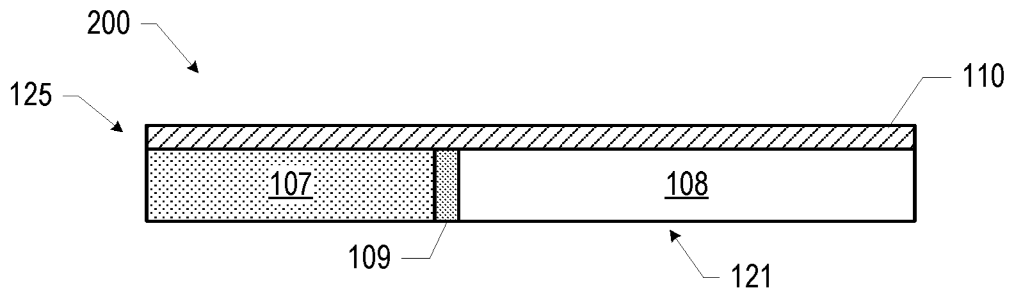

FIG. 5A

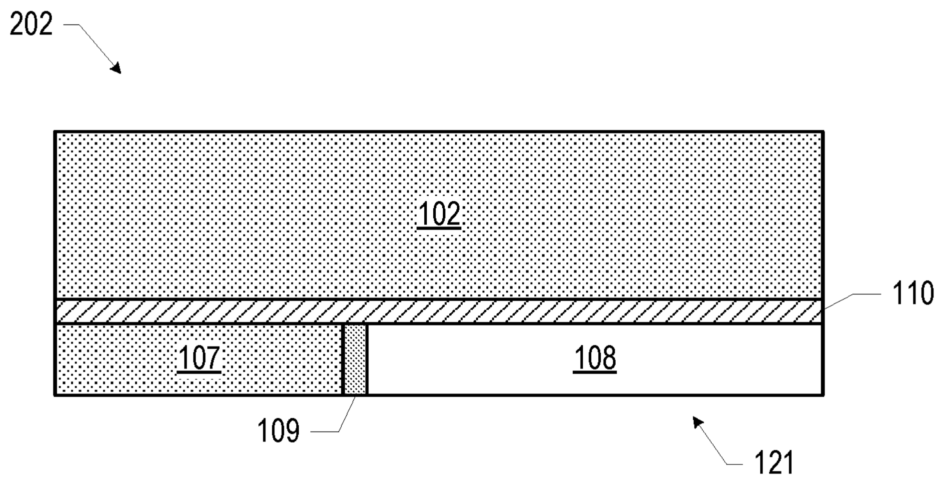

FIG. 5B

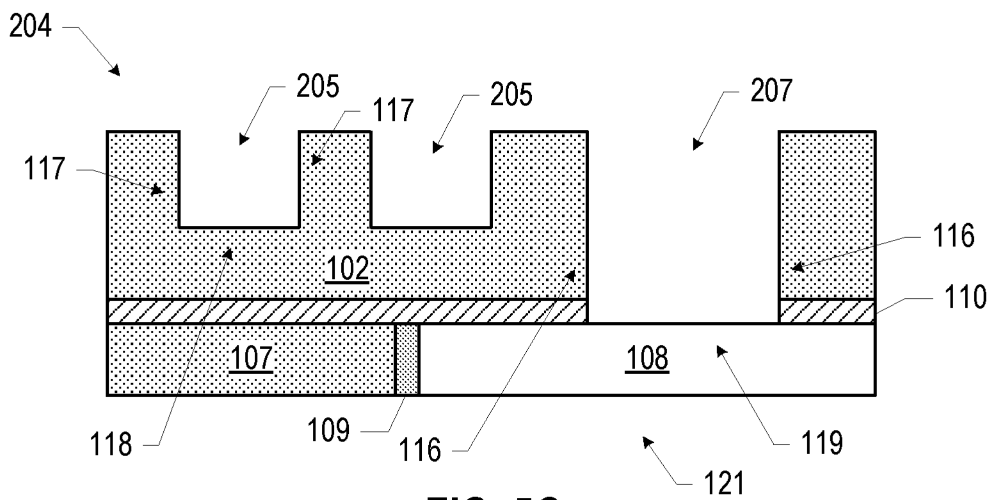

FIG. 5C

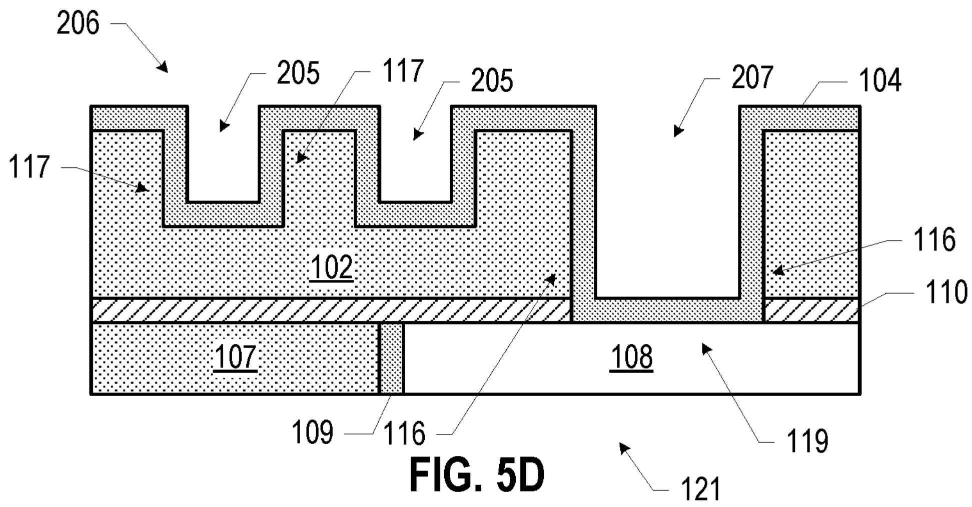

FIG. 5D

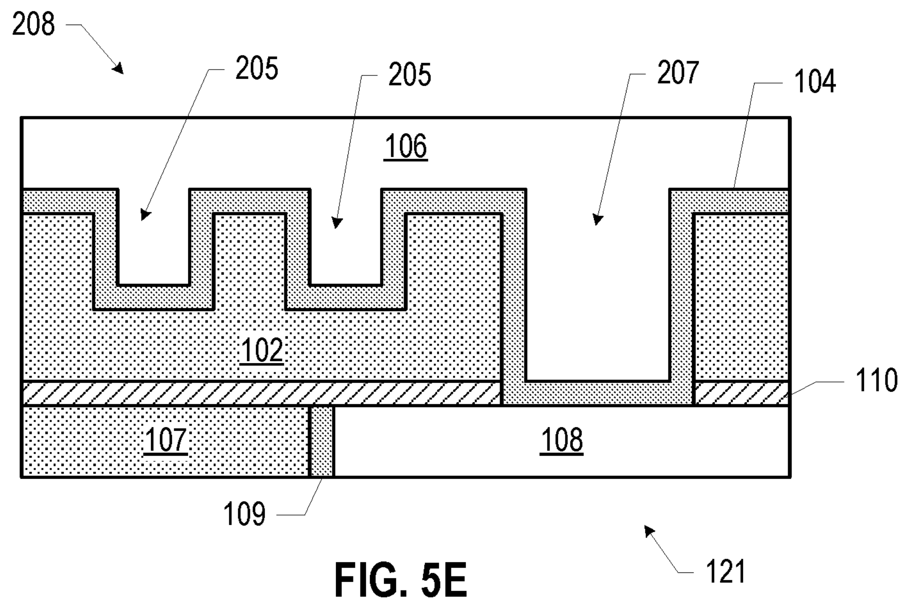

FIG. 5E

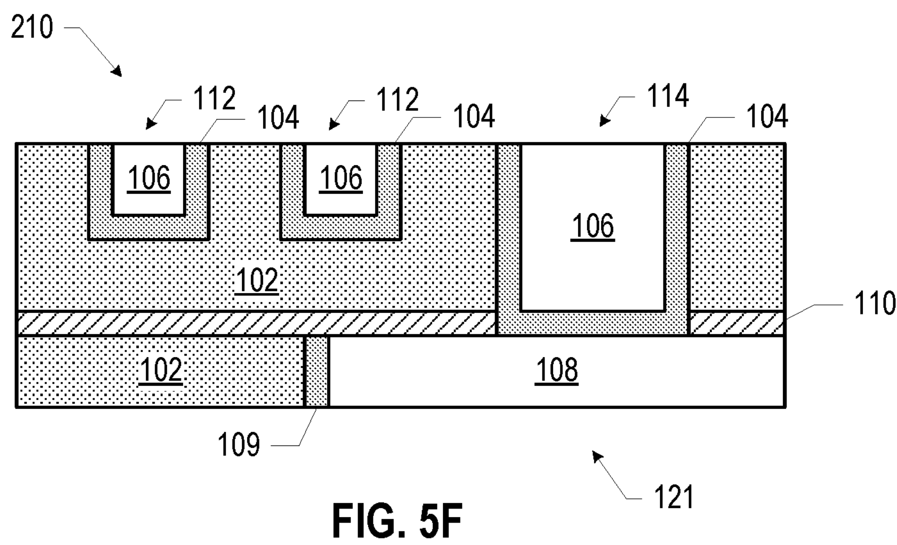

FIG. 5F

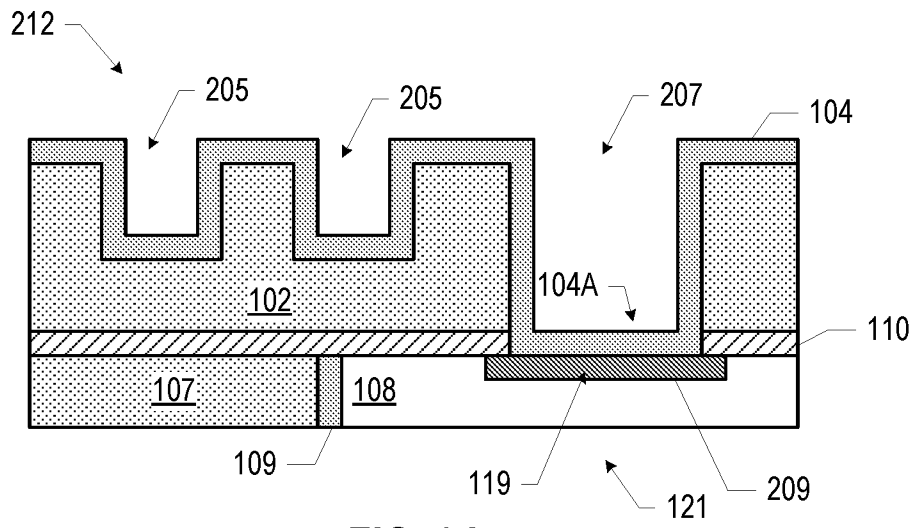

FIG. 6A

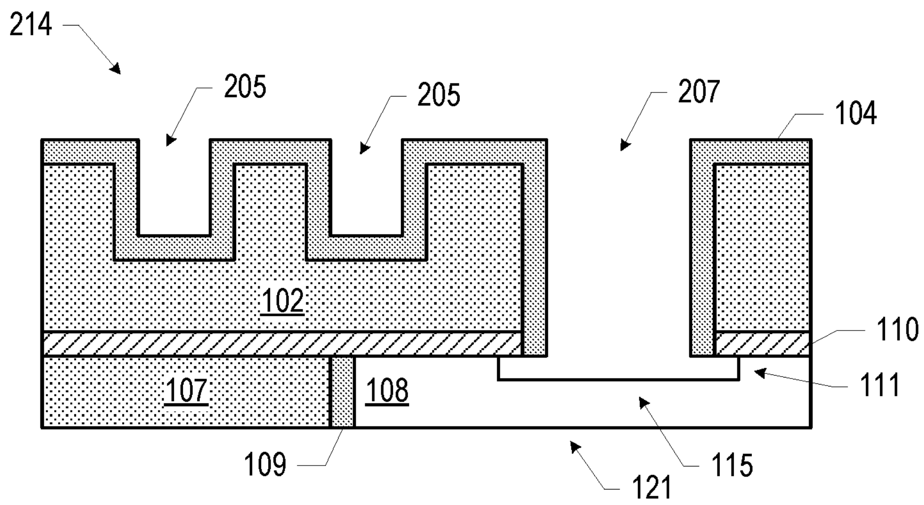

FIG. 6B

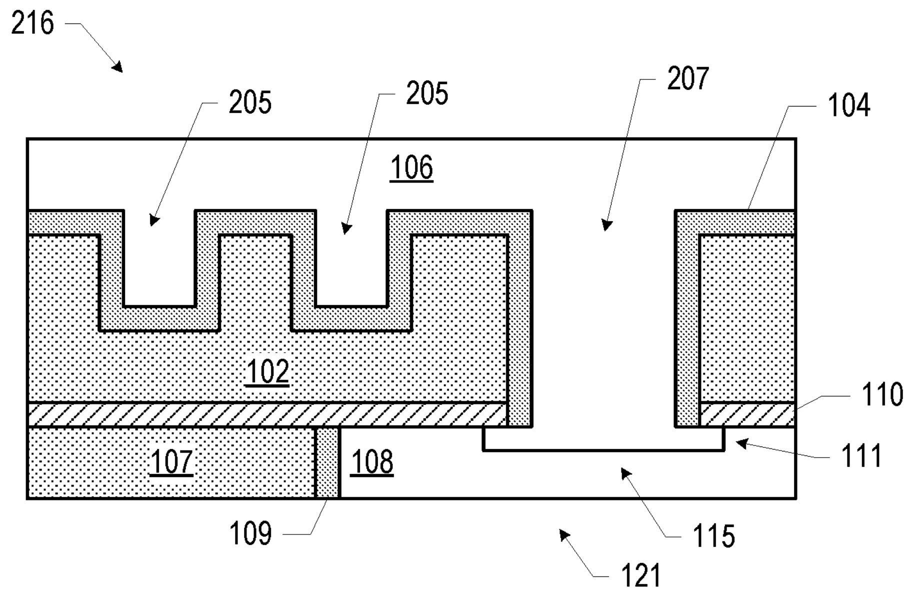

FIG. 6C

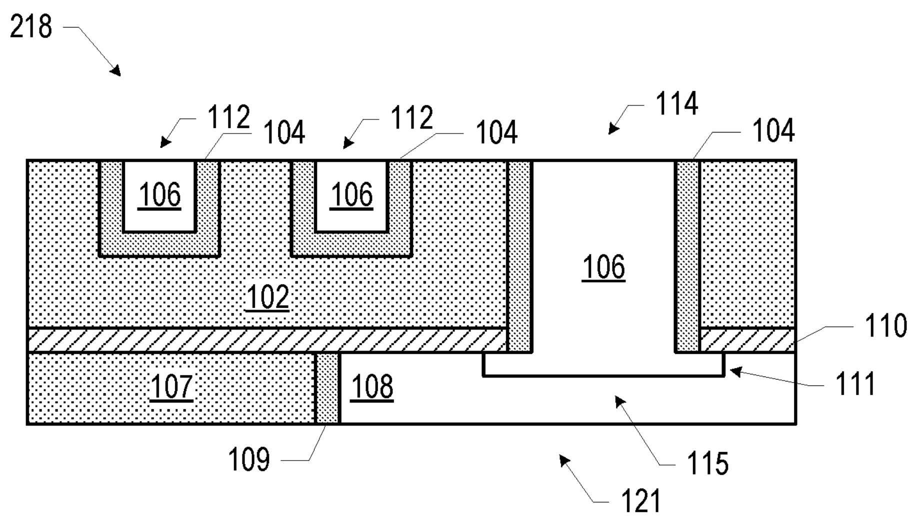

FIG. 6D

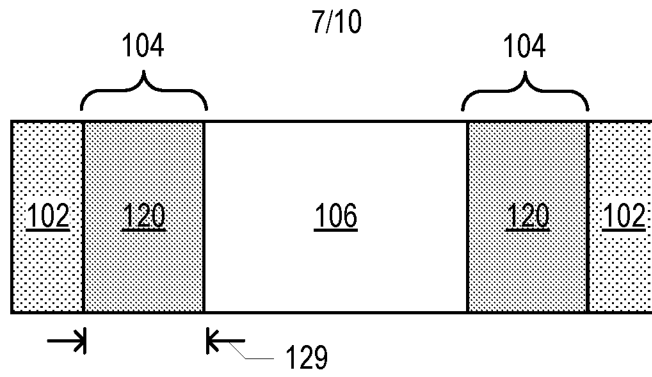

FIG. 7A

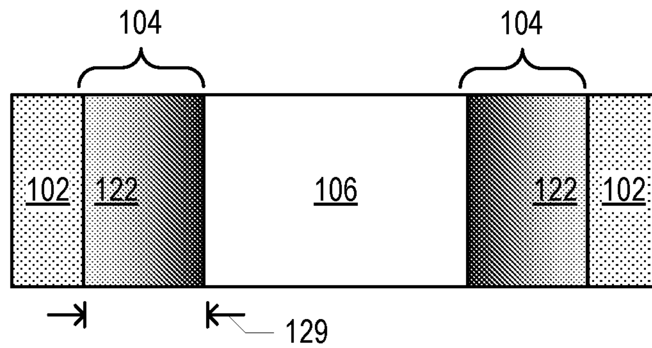

FIG. 7B

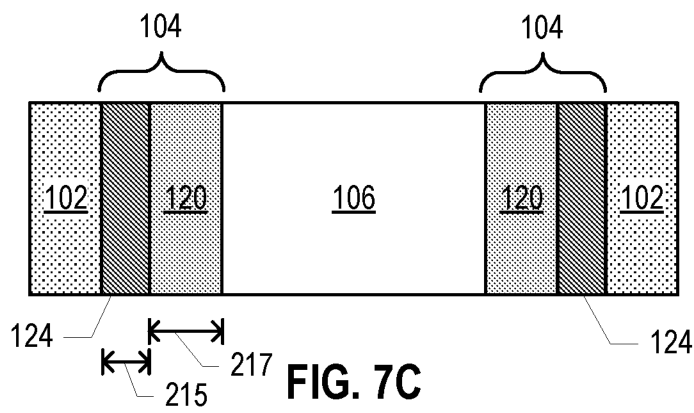

FIG. 7C

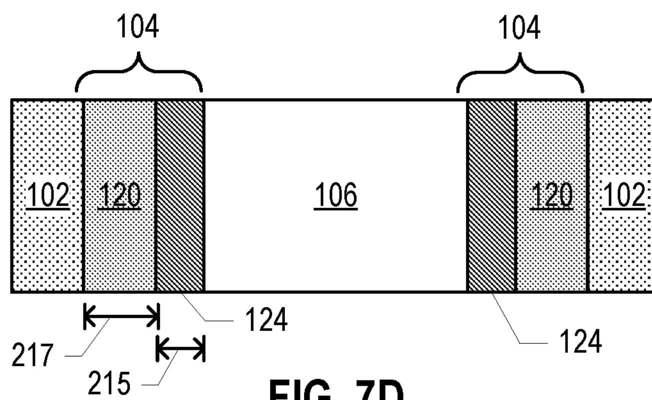

FIG. 7D

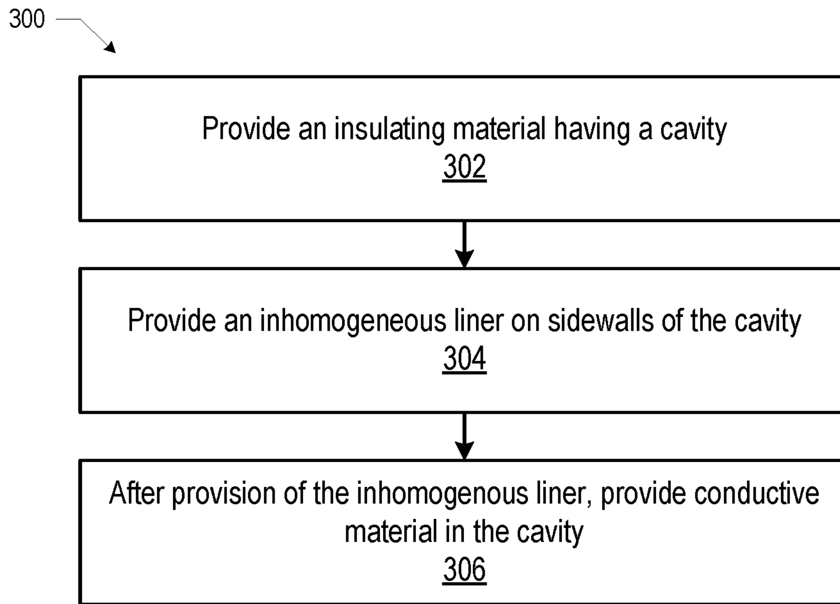

FIG. 8

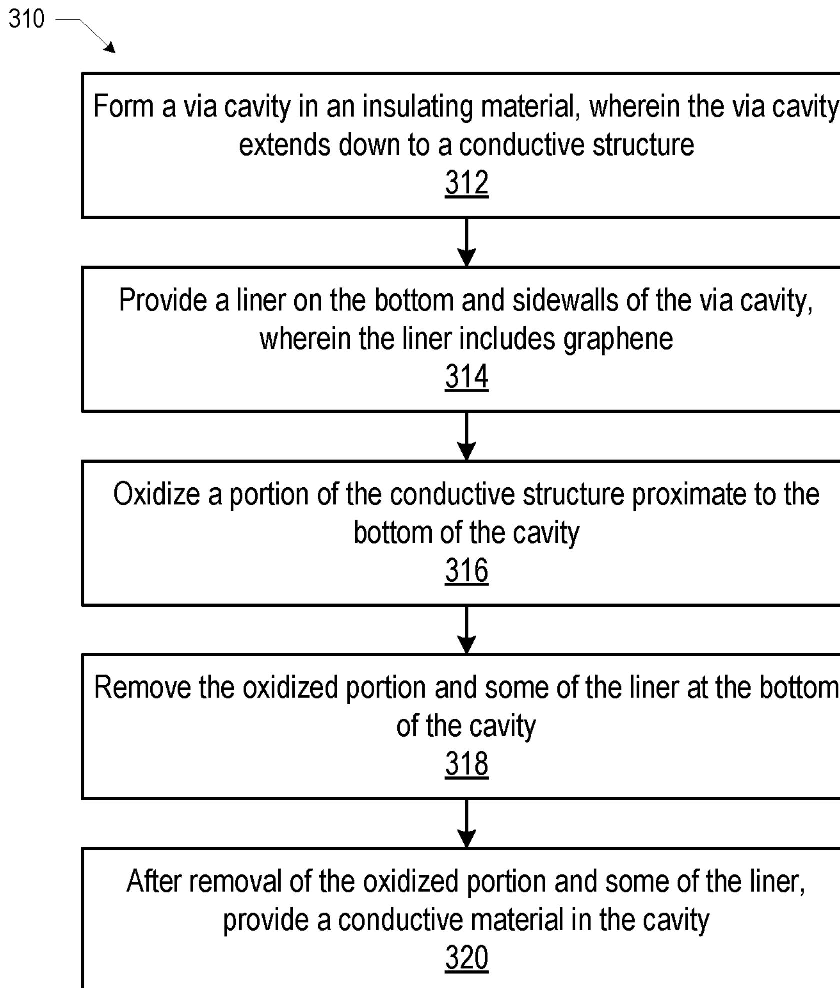

FIG. 9

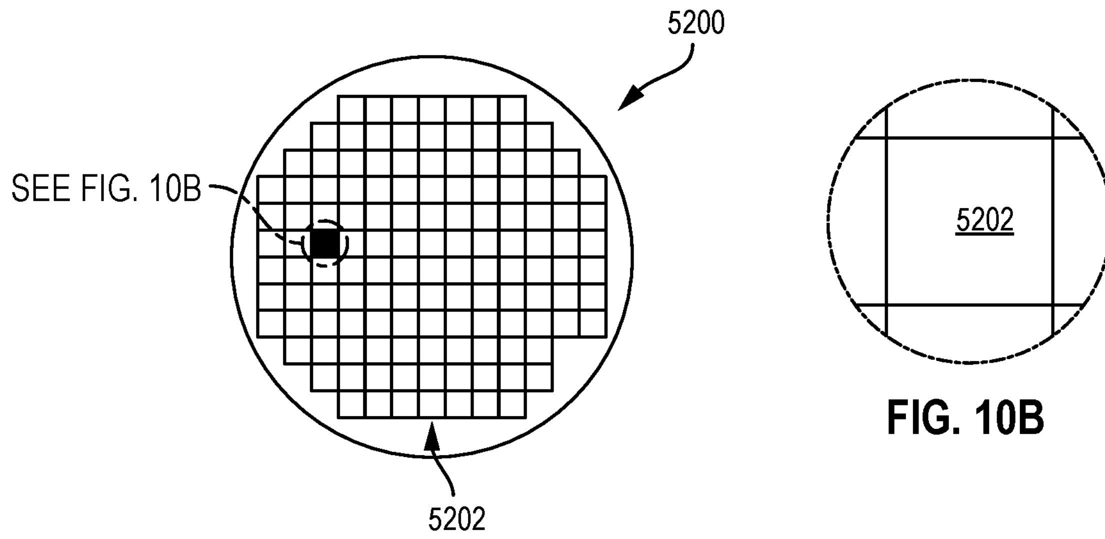

FIG. 10B

FIG. 10A

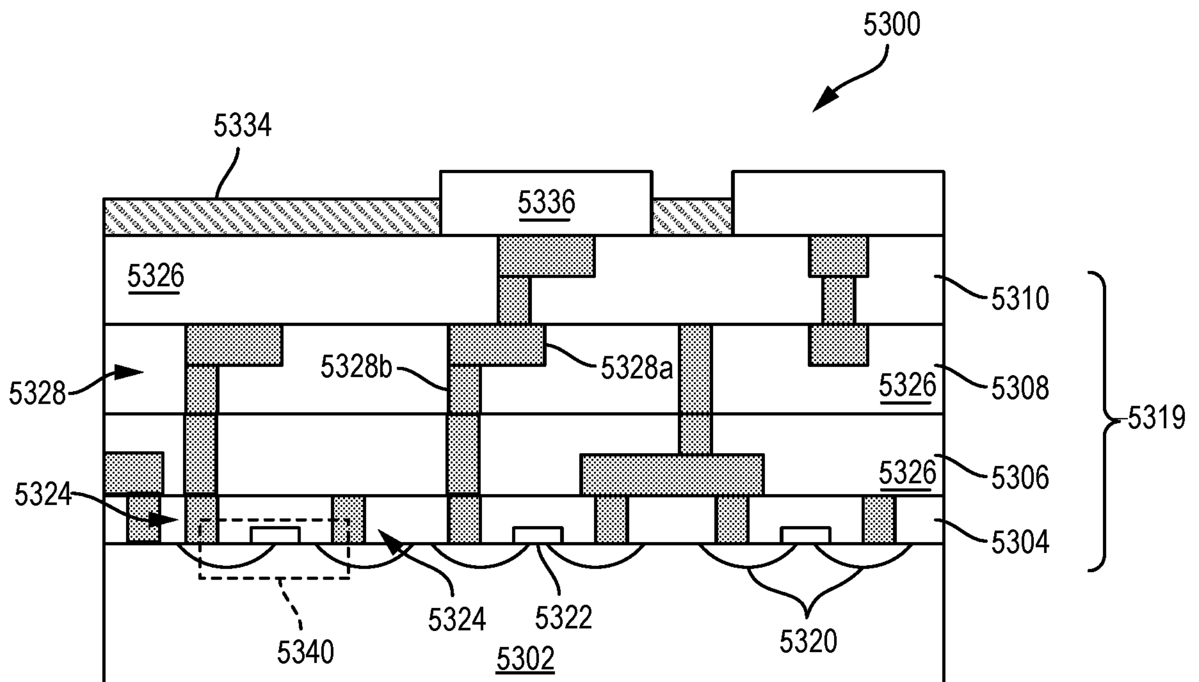

FIG. 11

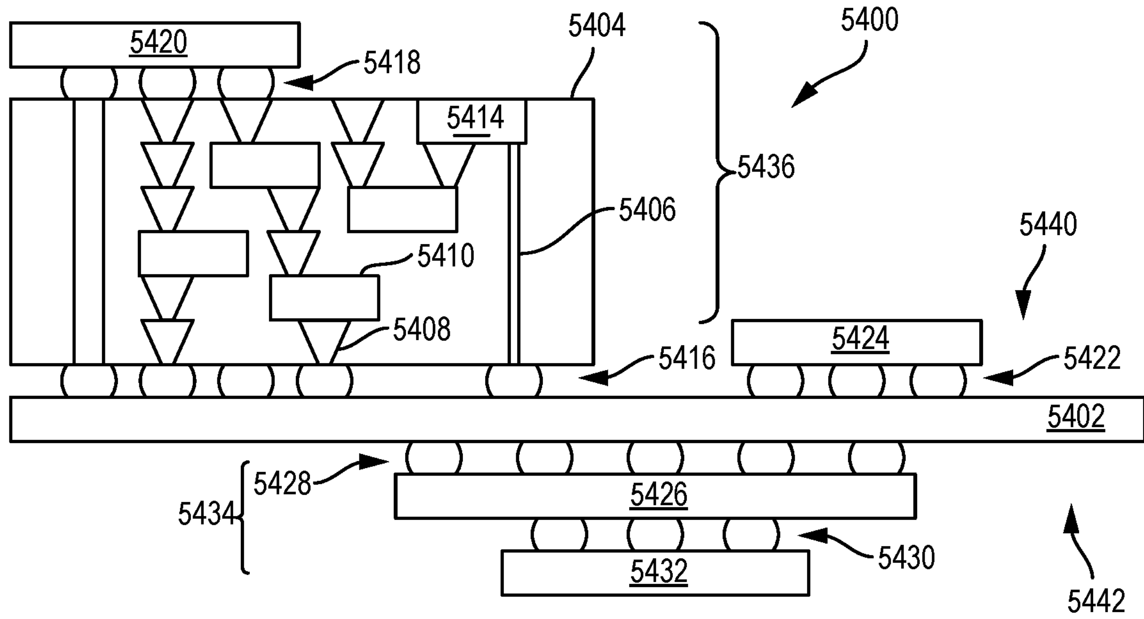

FIG. 12

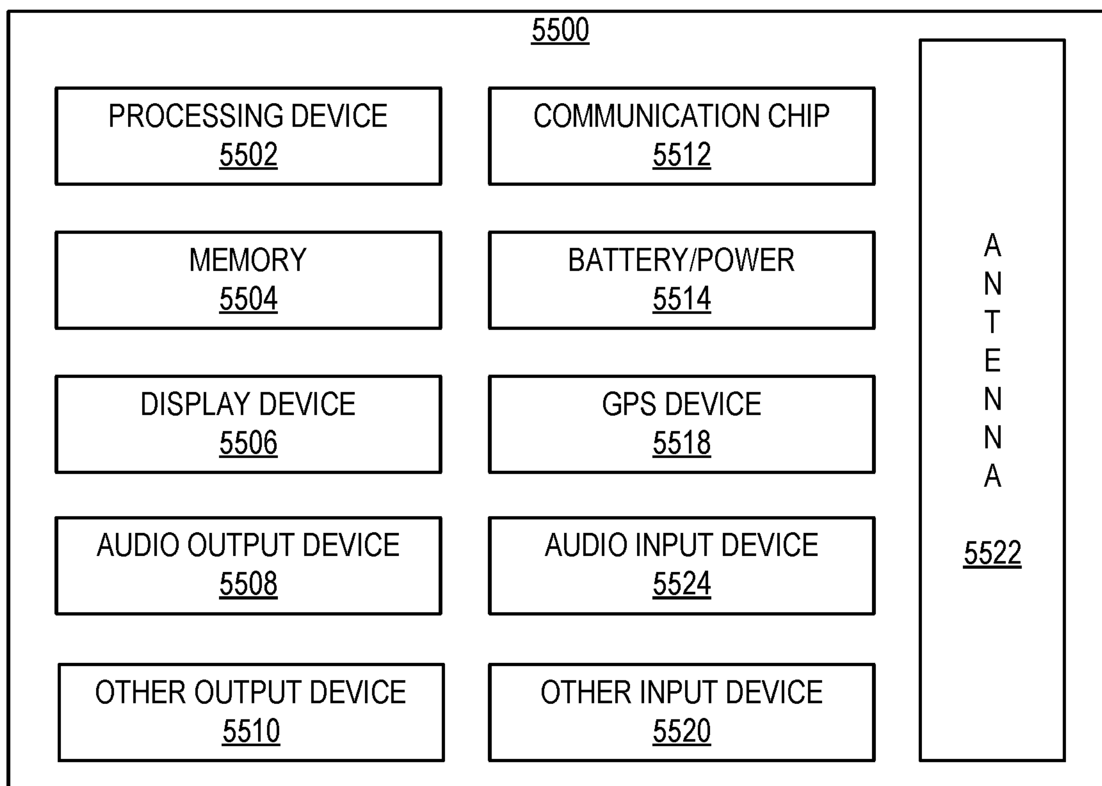

FIG. 13

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/068512

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/768(2006.01)i, H01L 29/16(2006.01)i, H01L 21/02(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/768; H01L 21/4763; H01L 23/48; H01L 29/40; B01J 10/00; B32B 5/02; H01L 23/538; H01L 29/16; H01L 21/02

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: insulating, conductive via, liner, graphene, interconnect

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2014-0145332 A1 (GLOBALFOUNDRIES INC.) 29 May 2014 See paragraphs [0020]-[0027], claims 1-4 and figures 1A-3.	1-4,6-9,17-20
A		5,10-16,21-25
A	US 2003-0129826 A1 (CHRISTIAAN J. WERKHOVEN et al.) 10 July 2003 See claim 1 and figures 9-10.	1-25
A	US 2004-0014320 A1 (LING CHEN et al.) 22 January 2004 See claim 21 and figure 1.	1-25
A	US 2013-0015581 A1 (HSINGJEN WANN et al.) 17 January 2013 See claim 1 and figure 9.	1-25
A	US 2013-0113102 A1 (JUNJING BAO et al.) 09 May 2013 See claim 1 and figures 3-6.	1-25

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
30 August 2017 (30.08.2017)	**31 August 2017 (31.08.2017)**

Name and mailing address of the ISA/KR

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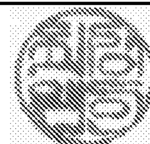
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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/US2016/068512

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