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Clark

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[54] **HIGH-RESOLUTION DIGITAL GENERATOR OF GRAPHIC SYMBOLS WITH EDGING**

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[52] **U.S. Cl.** ..... **340/324 AD;** 178/7.5 D

[51] **Int. Cl.²** **G06F 3/14**

[58] **Field of Search** ..... 340/324 AD; 178/7.5 D, 178/DIG. 22

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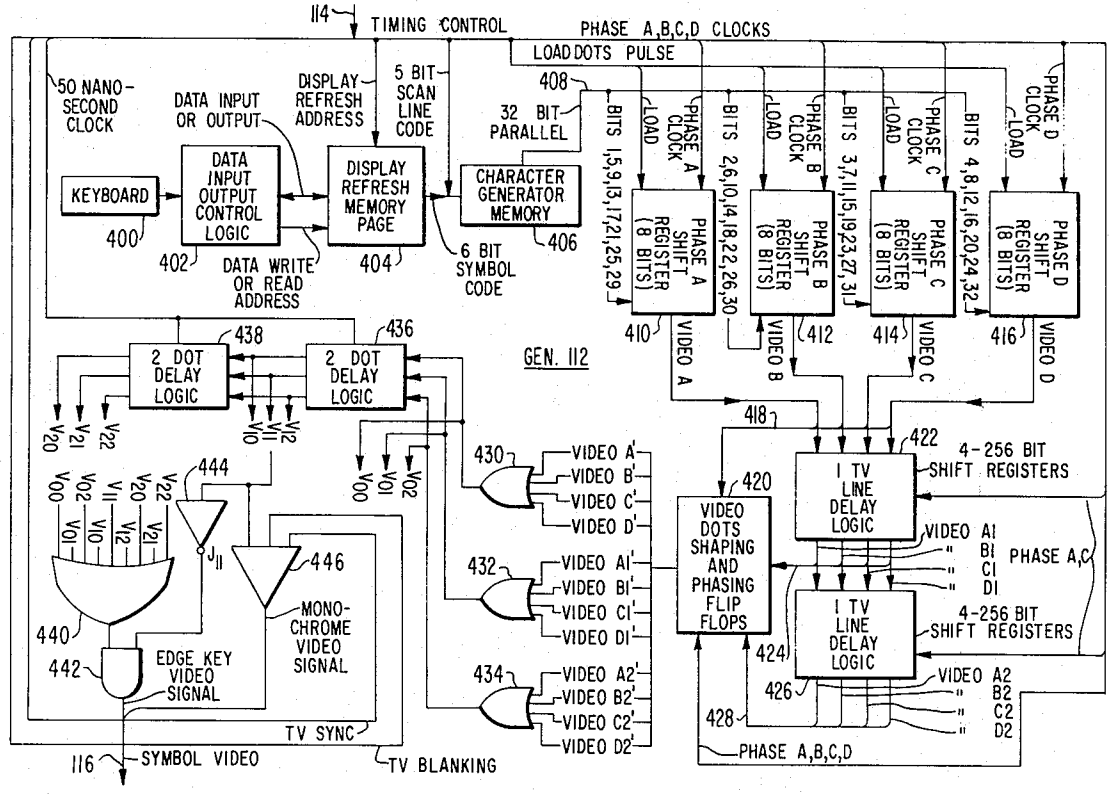
Attorney, Agent, or Firm—Edward J. Norton; George J. Seligsohn

[57] **ABSTRACT**

A graphic symbol, completely digital, video signal generator, suitable for use in a television broadcast display control system, derives high resolution (50 nanosecond video dot period) symbols with edging employing off-the-shelf low resolution (200 nanosecond period) shift registers. This is accomplished by employing four different phase clocks each having a low repetition rate (5 MHz). Separate independent edge key and monochrome video signals are derived as the symbol video output of the generator.

6 Claims, 9 Drawing Figures



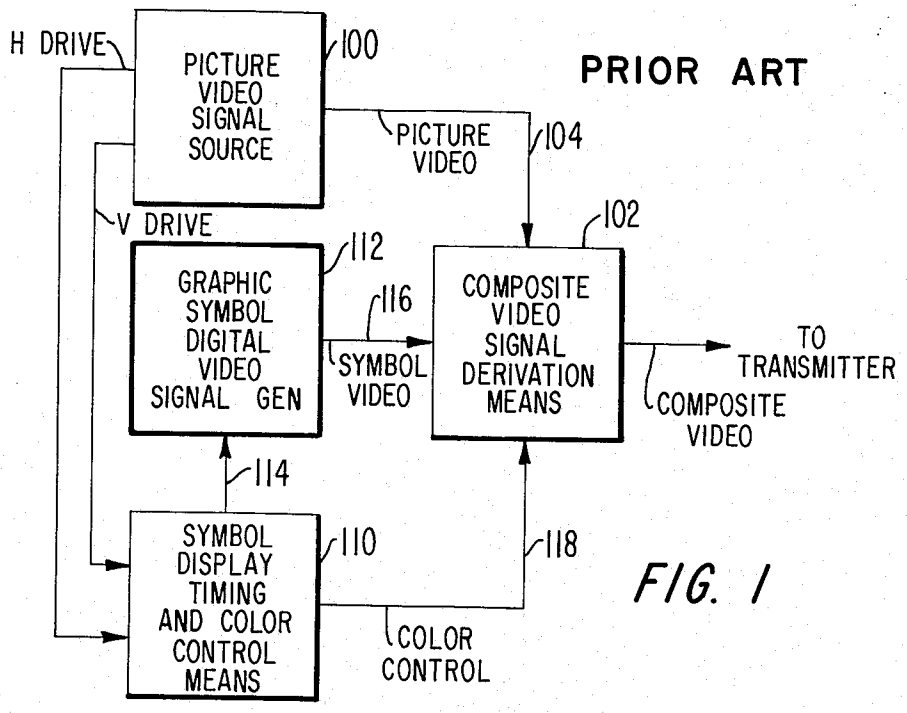
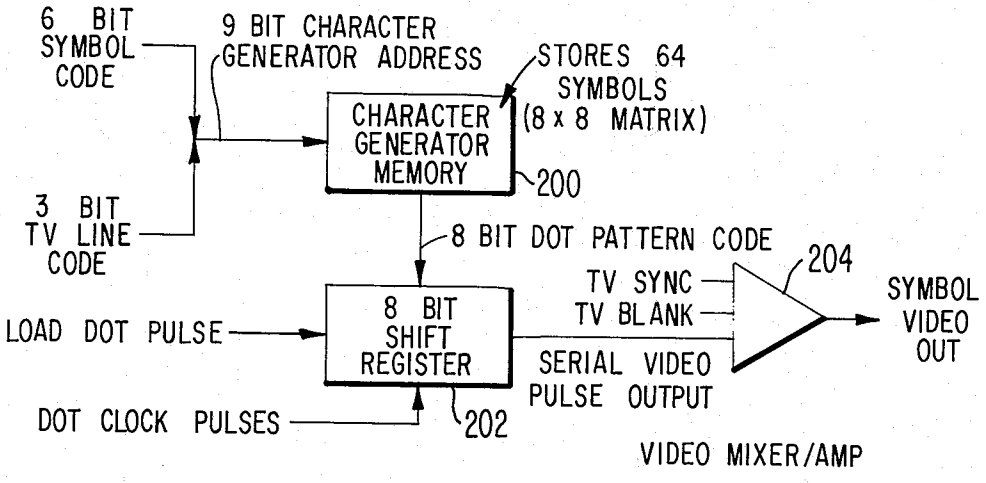


FIG. 1

TELEVISION BROADCAST DISPLAY CONTROL SYSTEM



LOW RESOLUTION PRIOR ART CHARACTER GENERATOR

FIG. 2A

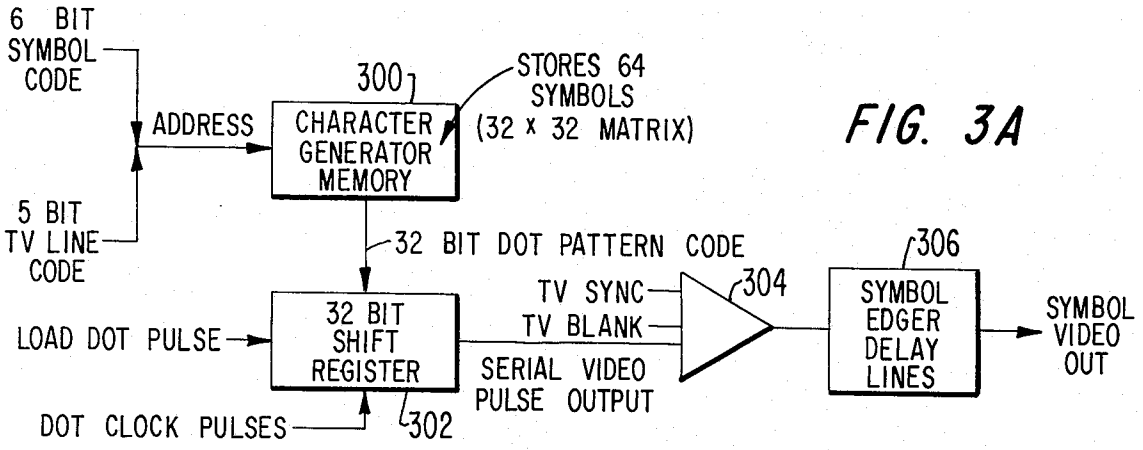


FIG. 3A

HIGH RESOLUTION PRIOR ART CHARACTER GENERATOR WITH SYMBOL EDGING DEVICE

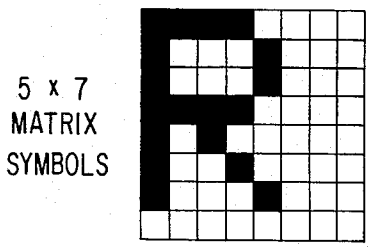


FIG. 2B

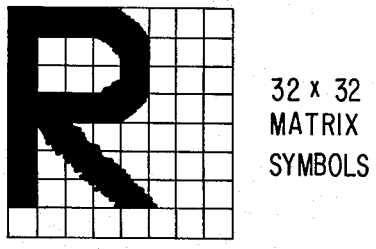
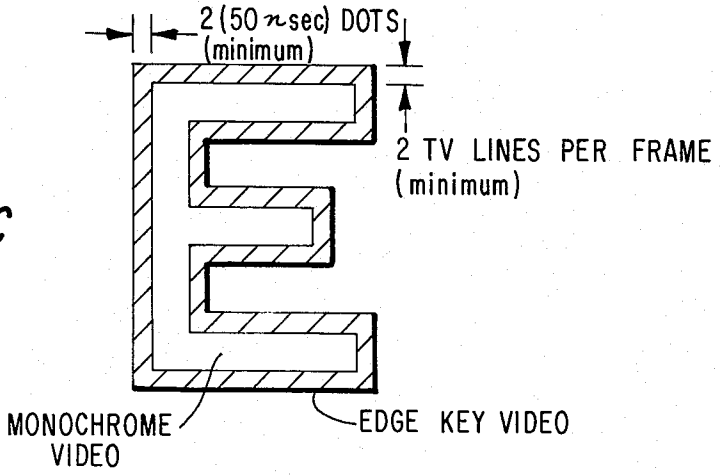


FIG. 3B

FIG. 3C



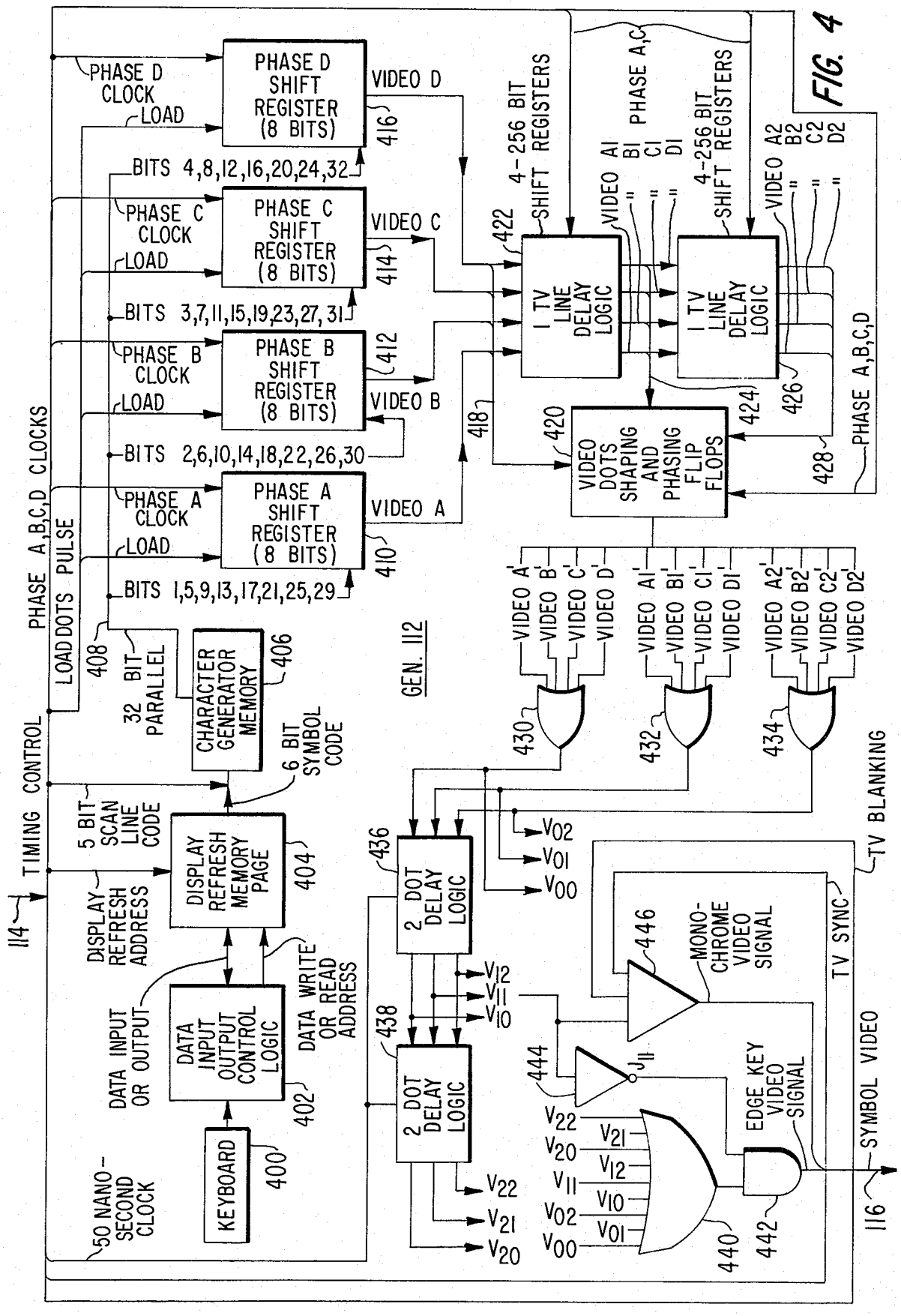

PHASE D SHIFT REGISTER (8 BITS)
PHASE C SHIFT REGISTER (8 BITS)
PHASE B SHIFT REGISTER (8 BITS)
PHASE A SHIFT REGISTER (8 BITS)
PHASE D CLOCK
PHASE C CLOCK
PHASE B CLOCK
PHASE A CLOCK
LOAD
BITS 4,8,12,16,20,24,32
BITS 3,7,11,15,19,23,27,31
BITS 2,6,10,14,18,22,26,30
BITS 1,5,9,13,17,21,25,29
VIDEO D
VIDEO C
VIDEO B
VIDEO A
416
414
412
410
PHASE A,B,C,D CLOCKS
LOAD DOTS PULSE
408
32 BIT PARALLEL
CHARACTER GENERATOR MEMORY
406
6 BIT SYMBOL CODE
GEN. 112
TIMING CONTROL
114
5 BIT SCAN LINE CODE
DISPLAY REFRESH ADDRESS
DISPLAY REFRESH MEMORY PAGE
404
DATA INPUT OR OUTPUT
DATA INPUT OUTPUT CONTROL LOGIC
402
DATA WRITE OR READ ADDRESS
KEYBOARD
400
50 NANO-SECOND CLOCK
4-256 BIT SHIFT REGISTERS
VIDEO AI BI CI DI
PHASE A,C
4-256 BIT SHIFT REGISTERS
VIDEO A2 B2 C2 D2
422
1 TV LINE DELAY LOGIC
1 TV LINE DELAY LOGIC
418
424
426
420
VIDEO DOTS SHAPING AND PHASING FLIP FLOPS
428
PHASE A,B,C,D
VIDEO A' VIDEO B' VIDEO C' VIDEO D'
VIDEO AI' VIDEO BI' VIDEO CI' VIDEO DI'
VIDEO A2' VIDEO B2' VIDEO C2' VIDEO D2'
430
432
434
436
2 DOT DELAY LOGIC
438
2 DOT DELAY LOGIC
V_{02} V_{01} V_{00}
V_{12} V_{11} V_{10}
V_{22} V_{21} V_{20}
TV BLANKING
TV SYNC
446
MONO-CHROME VIDEO SIGNAL
444
J_{11}
EDGE KEY VIDEO SIGNAL
SYMBOL VIDEO
116
440
442

FIG. 4

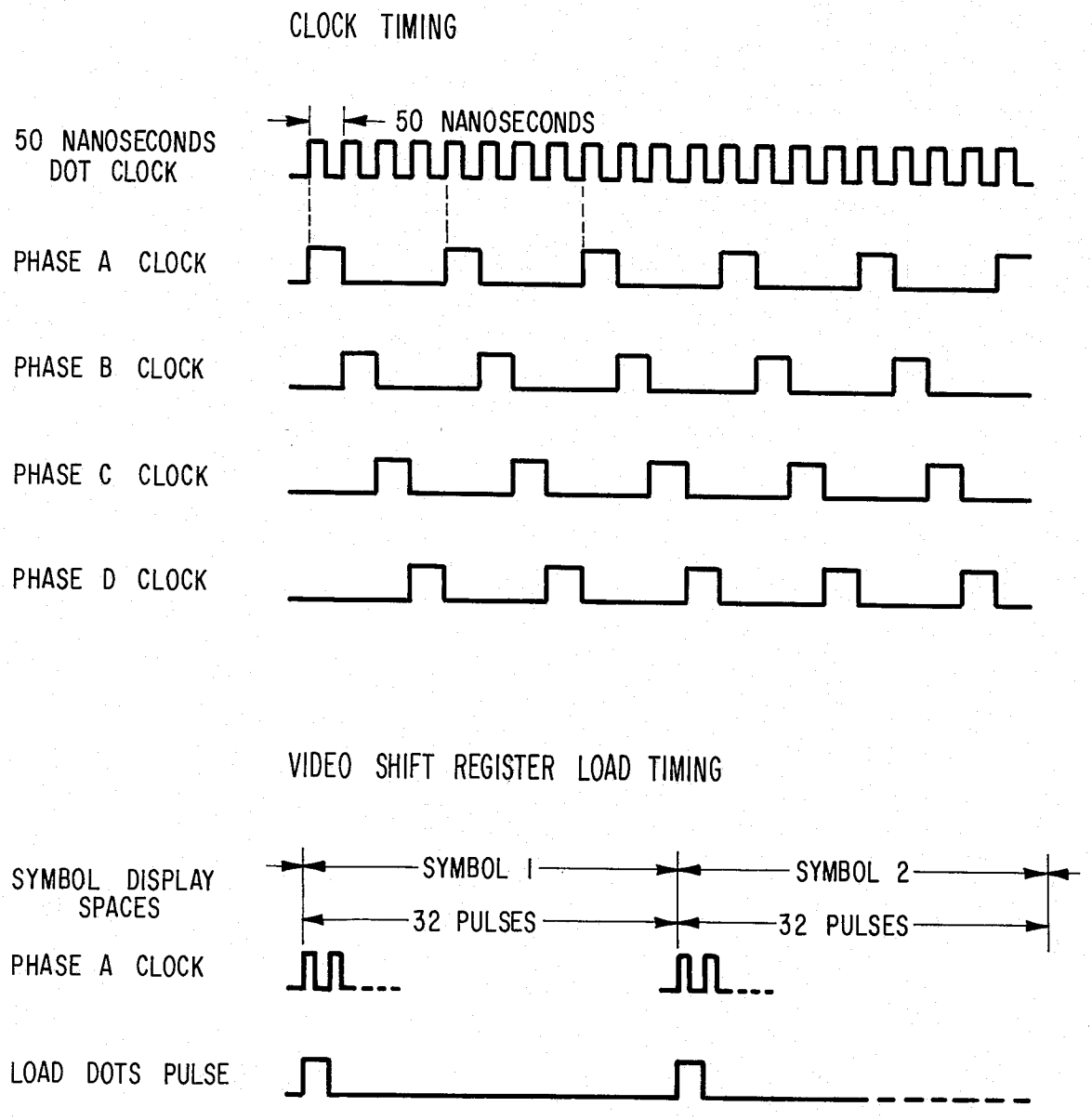
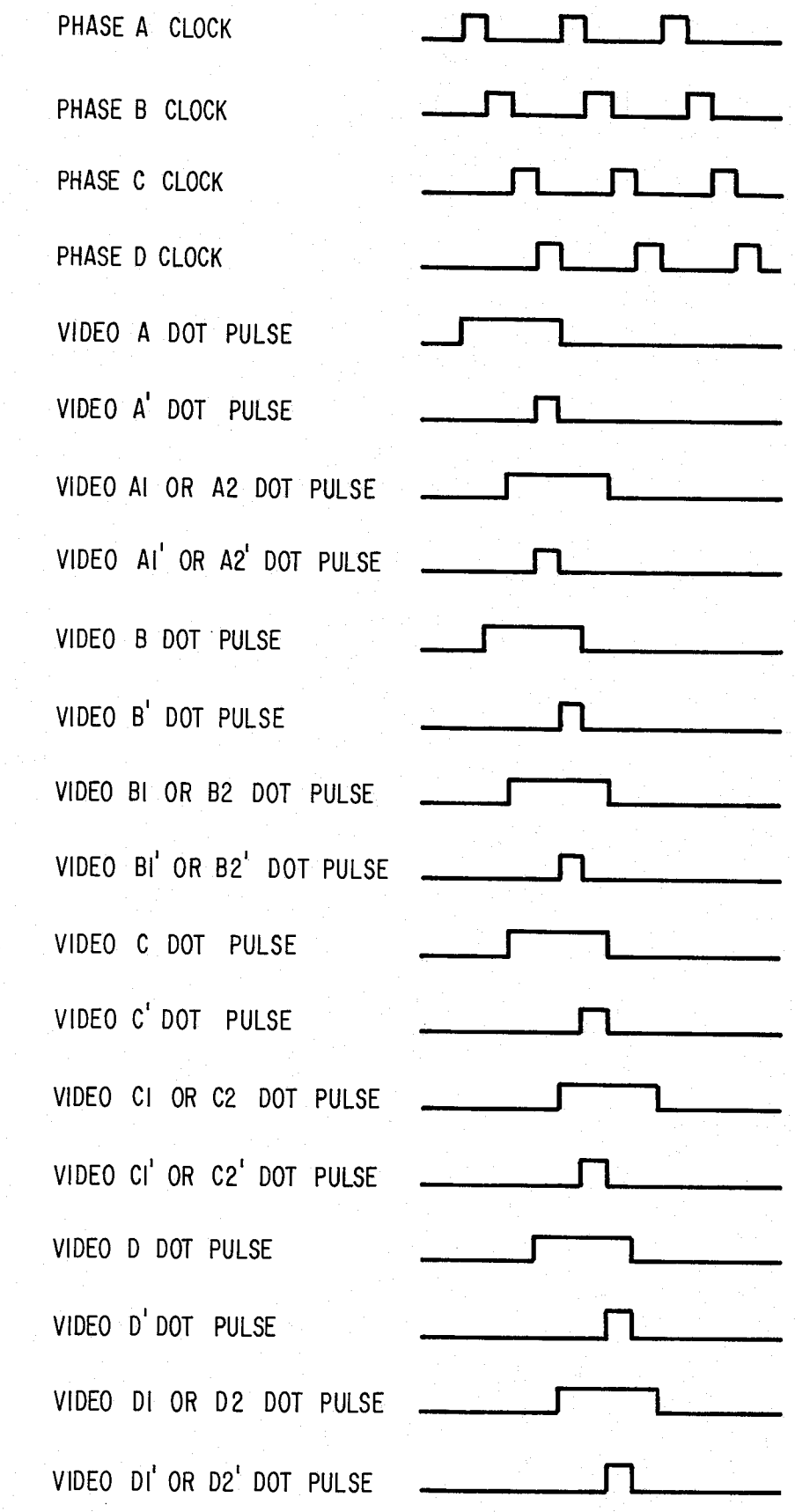

CLOCK TIMING
50 NANOSECONDS
50 NANOSECONDS DOT CLOCK
PHASE A CLOCK
PHASE B CLOCK
PHASE C CLOCK
PHASE D CLOCK
VIDEO SHIFT REGISTER LOAD TIMING
SYMBOL DISPLAY SPACES
SYMBOL 1
SYMBOL 2
32 PULSES
32 PULSES
PHASE A CLOCK
LOAD DOTS PULSE

FIG. 5



TIMING DIAGRAM - VIDEO OUTPUT PULSES

FIG. 6

HIGH-RESOLUTION DIGITAL GENERATOR OF GRAPHIC SYMBOLS WITH EDGING

This invention relates to the digital generation of video signals manifesting characters or other graphic symbols and, more particularly, the digital generation, in a manner suitable for television broadcasting, of video signals manifesting high resolution graphic symbols with edging.

For many purposes, such as in a conventional video terminal, the display on a television monitor of relatively low resolution graphic symbols without edging is perfectly acceptable. By way of example, in most video terminals, each symbol is composed of a dot matrix of only 5 ×7 dots. While this resolution is sufficient to provide intelligibility of a displayed message composed of such character symbols, it is insufficient to meet the high resolution requirements of broadcast television. To provide the high resolution which is most desirable in broadcast television, each character or other graphic symbol should be composed of a much larger dot matrix, such as a 32 ×32 dot matrix for example.

The clock rate, (in the order of 5 MHz) required for the digital generation of low resolution graphic symbols without edging (such as employed in conventional video terminals) is compatible with the switching speeds of standardly available shift registers and the other standard elements of video-signal digital generators. Further, 5 MHz is compatible with the video passbands of television monitors and standard television sets. However, the clock rate (in the order of 20 MHz) required for the digital generation of high resolution graphic symbols with edging is higher than the switching rates of standard shift registers and the other standard elements of a digital generator of high resolution graphic symbols with edging. In addition, a 20 MHz clock rate provides a dot duration of only 50 nanoseconds which, due to the video bandwidth and response time of a standard television set, is much below the approximately 150 nanosecond minimum required to maintain symbol brightness in both black-and-white and color television sets, and is even further below the minimum of approximately 200 nanoseconds required to obtain satisfactory symbol color saturation in color television sets. For these reasons, in the past, generators of high resolution graphic symbols with edging for use in television broadcasting were not completely digital in construction, but required expensive analog elements which were capable of operating effectively at a high clock rate (in the order of 20 MHz).

In accordance with the principles of the present invention, there is disclosed and claimed a completely digital generator of high resolution graphic symbols with edging. This is accomplished by providing four-phase television video signals, each at a relatively low clock rate and then using these four-phase TV video signals for deriving the required high-clock rate output video signals from the digital generators.

These and other features of the present invention will become more apparent from the following detailed description taken together with the accompanying drawing, in which:

FIG. 1 is a block diagram of a typical prior art television broadcast display control system, of a type which provides the display of graphic symbols.

FIG. 2*a* is a block diagram of a typical low resolution prior art digital character generator, and FIG. 2*b* illustrates a typical low resolution character generated by the generator of the type shown in FIG. 2*a*;

FIG. 3*a* is a block diagram of a typical high resolution prior art character generator with a symbol edging device, FIG. 3*b* is a dot matrix of a high resolution character without edging, and FIG. 3*c* shows a typical high resolution character with edging;

FIG. 4 is a block diagram of a graphic symbol digital video signal generator embodying the present invention;

FIG. 5 is a timing diagram of the clock and load pulses employed in FIG. 4, and

FIG. 6 is a timing diagram of the video output pulses derived by the video signal generator of FIG. 4.

Referring now to FIG. 1, there is shown, in generalized form, a television broadcasting display control system of the type which includes a graphic symbol digital video signal generator. Specifically, as shown in FIG. 1, picture video signal source **100** applies one or more picture video signals as one or more inputs to composite video signal derivation means **102** over picture video connection **104.** The picture video signals may be generated locally from one or more television cameras, video recorders, etc. or, as in the case of a network program, one or more of the picture video signals may originate at a distant point. In any case, any and all of these picture video signals may be applied as inputs to composite video signal derivation means **102** over connection **104** at the same time.

Horizontal drive and vertical drive signals from picture video source **100** are applied over respective connections **106** and **108** as sync inputs to symbol display timing and color control means **110.** Symbol display timing and color control means **110** applies timing control signals to a plurality of inputs of graphic symbol digital signal generator **112** over timing control connection **114.** Graphic symbol digital video signal generator **112** applies one or more symbol video signals as an input to composite video signal derivation means **102** over connection **116.** If the television broadcast is in color, symbol display timing and color control means **110** applies color control signals to composite video signal derivation means **102** over connection **118.** Of course, if the television broadcast is to be in black-and-white, both the color control portion of **110** and color control connection **118** may be omitted.

As is known in the television broadcast art, each of the blocks **100, 102, 110** and **112** may include the various switches and control means which are manually operated to provide the desired picture video, symbol video and color control input to composite video derivation means **102** and to provide the desired composite video signal output from composite video signal derivation means **102.** For instance, as is known in the television broadcast art, composite video signal derivation means **102** may include suitable video keyers and mixers for selectively combining the video signal input thereto over connection **104** and **116** in any desired manner to provide the television frame format manifested by the composite video signal output therefrom. For example, picture video signals may be selectively combined to provide a so-called "split screen" format, or symbol video signals may be superimposed on top of a picture video signal or, in the alternative, a video may be employed to "key out" from the picture the area in a television frame in which a symbol is located. Thus, a television broadcast display control system provides great versatility in forming the composite video signal

which actually is broadcast by the television transmitter.

Referring now to FIG. 2*a*, there is shown certain elements of the low resolution prior art character generator of the type employed in video terminals. Character generator memory **200** typically stores **64** different alphanumeric symbols. Each symbol may be stored in a dot matrix having an overall size of 8×8, of which the symbol itself occupies a 5×7 portion. This is exemplified for the symbol R, illustrated in FIG. 2*b*. It will be noted that the low resolution of 5×7 dots for the symbol itself greatly affects the appearance of diagonal portions of the symbol.

As shown in FIG. 2*a*, character generator memory **200,** which is usually a ROM, receives a 9 bit character generator address, which is composed of a 6 bit symbol code (such as the ASCII code) and a three bit TV scan line code. The **6** bit symbol code defines the particular one of the **64** storage symbols, such as the symbol R, to be read out, while the three bit TV scan-line code defines the particular one of the eight consecutive raster scan lines occupied by a row of characters then being scanned. In response thereto, character generator memory **200** loads eight-bit shift register **202** (which serves as a parallel-to-serial converter) with an appropriate group of eight binary bits. More specifically, if the symbol being read out is an R and the TV scan line designated by the three bit code is either the first or fourth scan line, the eight bit dot pattern code for the symbol R which loads eight bit shift register **202** is 11110000, as shown in FIG. 2*b*. Similarly, as shown in FIG. 2*b*, this eight bit dot pattern code for the symbol R is 10001000 for each of the second, third and seventh TV scan lines; while this eight bit pattern code is 10100000 for the fifth TV scan line and is 10010000 for the sixth TV scan line. To provide a space between wymbols occupying different rows of symbols on the television display, the eight bit dot pattern code for the eighth TV scan line is always 00000000.

Eight-bit shift register **202** is loaded in response to the receipt of a load dot pulse input from an associated timing control means. The loaded eight bit dot pattern code in eight-bit shift register **202** is then read out serially in response to applied dot clock shift pulses. The rate of these dot clock pulses is normally in the order of 5 MHz, so that each successive dot has a duration in the order of 200 nanoseconds, which is within the video bandwidth capabilities of standard commercial television sets. As further shown in FIG. 2*a*, the serial video pulse output from eight-bit shift register **202** is added to TV horizontal and vertical sync signals and a TV blanking signal in video mixer amplifier **204,** from which the symbol video output of the character generator is obtained.

For television broadcast purposes, the relatively low resolution provided by 5×7 matrix symbols, shown in FIG. 2*b*, is insufficient. Instead, relatively high resolution 32×32 matrix symbols, such as shown in FIG. 3*b*, are required for broadcast television. In FIG. 3*b*, the width of each line of the symbol R still has a duration of 200 nanoseconds, so that it is within the video bandwidth capabilities of a standard television set. However, as shown in FIG. 3*b*, the high resolution capability is achieved by employing a dot duration for the dot matrix of only 50 nanoseconds, so that the 200 nanosecond width of each line of the symbol R in FIG. 3*b* is provided by four consecutive 50 nanosecond dots (rather than a single 200 nanosecond dot as in FIG. 2*b*).

Furthermore, in the case of broadcast television, it is often desired to display a high resolution symbol with edging, in the manner shown for the symbol E in FIG. 3*c*. As indicated in FIG. 3*c*, the minimum width of the edging may be only 100 nanoseconds, i.e. 2 consecutive dots of 50 nanoseconds each. In the past, in order to provide symbols with edging, such as shown in FIG. 3*c*, required high resolution character generators with an analog symbol edging device of the type shown in FIG. 3*a*.

Referring now to FIG. 3*a*, character generator memory **300,** which like character generator memory **200** may be ROM, stores each of 64 symbols in a 32×32 dot matrix. Each of the 64 symbols is selected by the binary address of a six-bit symbol code applied as an input to character generator memory **300.** Character generator memory **300** is further addressed by a five-bit TV scan line code applied as an input thereto for the purpose of selecting the particular one of the 32 rows of the selected dot matrix in accordance with the particular one of 32 consecutive TV scan lines then being scanned. In response thereto, character generator memory **300** derives as an output a 32 bit dot pattern code defining the symbol dot pattern of the selected row for the selected symbol. In response to a load dot pulse applied to 32 bit shift register **302,** the 32 bit dot pattern code from character generator memory **300** is loaded in parallel into 32-bit shift register **302.** In response to dot clock pulses applied as shift pulses 32-bit shift register **302** at a relatively high rate of about 20 MHz, a serial video pulse output is obtained from 32 bit shift register **32.** This serial video pulse output is added to TV horizontal and vertical sync signals and a TV blanking signal in mixer **304.** Although, as so far described, the high resolution prior art character generator of FIG. 3*a* is digital in construction, it requires a more expensive nonstandard shift register capable of operating at 20 MHz, rather than a relatively inexpensive standardly available shift register operating at 5 MHz employed in the low resolution prior art character generator of FIG. 2*a*. Furthermore, if symbol edging of the type shown in FIG. 3*c* is desired, the output from mixer **304** must be passed through an edging device, such as symbol edger delay lines **306,** to produce the symbol video outputs. Due to the high frequency (20 MHz) requirement of the final video output stages, symbol edging, as shown in FIG. 3*c*, is performed by symbol edger **306** using expensive analog circuitry, which includes delay lines.

The present invention, embodied in the graphic symbol digital video signal generator of FIG. **4,** provides a technique for generating high resolution digital symbols with edging, which does not require a 32 bit, **20** MHz output shift register and in which it is possible to provide an inexpensive digital (rather than analog) symbol edging using off-the-shelf 5 MHz digital shift registers instead of analog circuitry including delay lines.

FIG. **4** illustrates an embodiment of graphic symbol digital video generator **112** of FIG. **1,** which incorporates the present invention. As is conventional in graphic symbol digital video signal generators, there is included keyboard **400,** data input output control logic **402** and display refresh memory **404.** Block **400, 402,** and **404** cooperate in a manner known in the art to store in display refresh memory **404** the characters making up the message to be displayed. Specifically,

each character of the message is manifested by a six-bit word symbol code. This six-bit word symbol code corresponding to each character in the message is stored within display refresh memory page **404** at a location thereof which corresponds to the display position of that character in the format of the displayed message, as is conventional.

In a manner known in the art, the readout of memory page **404** is synchronized by a display refresh address word timing control signal applied thereto over connection **114** to read out in sequence the entire stored page of six-bit word symbol codes in synchronism with the raster scan of each successive television frame.

The six-bit word symbol code output from display refresh memory **404** and a five-bit television scan line code applied from timing control connection **114** are applied as inputs to character generator memory **406,** which is identical in all respects to character generator memory **300** of FIG. **3***a*.

The output from character generator memory **406** consists of a 32-bit parallel dot pattern, each bit of which appears on a separate lead of connection **408.** In response to a load dot pulse from timing control connection **114,** bits **1, 5, 9, 13, 17, 21, 25** and **29** of the **32**-bit parallel dot pattern carried by the corresponding leads of connection **408** are loaded into eight-bit phase A shift register **410.** In a similar manner, bits **2, 6, 10, 14, 18, 22, 26** and **30** are loaded into eight-bit phase B shift register **412,** bits **3, 7, 11, 15, 19, 23, 27** and **31** are loaded into eight-bit phase C shift register **414,** and bits **4, 8, 12, 16, 20, 26, 28** and **32** are loaded into eight-bit phase D shift register **416.**

Phase A shift register **410** receives phase A clock pulses from timing control connection **114,** which occur at a given relatively slow rate, such as 5 MHz. In a similar manner, phase B shift register **412** receives phase B clock pulses, phase C shift register **414** receives phase C clock pulses and phase D shift register **416** receives phase D clock pulses. Each of phase B, D and D clock pulses occur at the same relatively slow given rate, such as 5 MHz, as the phase A clock pulses. However, as shown in FIG. **5,** the respective phase A, phase B, phase C and phase D clock pulses (which are each 50 nanoseconds in duration) are phase delayed with respect to each other. Specifically, the leading edge of phase D clock pulse occurs coincidentally with the lagging edge of the preceding phase A clock pulse; the leading edge of a phase C clock pulse occurs coincidentally with the lagging edge of preceding phase C clock pulse; the leading edge of a phase D clock pulse occurs coincidentally with the lagging edge of the preceding phase C clock pulse and the leading edge of a phase A clock pulse occurs coincidentally with the lagging edge of the preceding phase D clock pulse. Thus, the durations between the leading edges of two successive pulses of the same phase is 200 nanoseconds (i.e., the clock pulses occur at a frequency of 5 MHz.).

The respective video A, video B, video C and video D output from respective shift register **410, 412, 414,** and **416,** in response to being shifted by the respective phase A, B, C and D clock pulses applied thereto, are applied over connection **418** as respective inputs to video dots shaping and phasing flip flops **420.** In addition, the respective video A, video B, video C and video D signals are applied as inputs to **1** TV line delay logic **422** (which consists of four shift registers, each having a capacity of 256 bits). Block **422** also receives phase A and phase C clock shift pulses, which operate in a manner to be described below in connection with FIG. **6.**

The output from **1** TV line delay logic **422,** which consists of video signals **A1, B1, C1** and **D1,** is applied as second inputs to video dot shaping and phasing flip flops **420** over connection **424,** and is also applied as inputs to **1** TV line delay logic **426.** Block **426,** like block **422,** comprises four **256** bit shift registers, which have phase A and phase C clocks applied as shift pulses thereto. The function performed by delay logic **426** also will be described below in connection with FIG. **6.**

The outputs from one TV line delay logic **426,** which consists of video signals **A2, B2, C2** and **D2,** are applied as third inputs to video dot shaping and phasing flip flops **420** over connection **428.** Video dot shaping and phasing flip flops **420** also has phase A, B, C and D clocks applied as inputs thereto, as shown.

Delay logic **422,** delay logic **426** and video dot shaping and phasing flip flops **420** cooperate to effectively convert the relatively low resolution (5 MHz) video signals A, B, C and D appearing at the respective outputs of shift registers **410, 412, 414** and **416** into relatively high resolution (20 MHz) video signals appearing at the output of video dot shaping and phasing flip flops **420.** More specifically, referring to the timing diagram shown in FIG. **6,** each video A dot pulse has a duration of 200 nanoseconds and has its leading edge in time coincidence with the leading edge of the phase A clock. In video dot shaping and phasing flip flops **420,** each video A dot pulse is sampled during the occurrence of a phase-D clock pulse, to provide a 50 nanosecond video A′ dot pulse which occurs in time coincidence with a phase D clock. In a similar manner, each 200 nanosecond video B dot pulse is sampled during the occurrence of a phase A clock to provide a 50 nanosecond video B′ dot pulse in time coincidence with the the phase A clock; each 200 nanosecond video C dot pulse is sampled during the occurrence of a phase B clock to provide a 50 nanosecond video C′ dot pulse in time coincidence with the phase B clock, and each 200 nanosecond video D dot pulse is sampled during the occurrence of a phase C clock to provide a 50 nanosecond video D′ dot pulse in time coincidence with the phase C clock.

Essentially, one TV line delay logic **422** and one TV line delay logic **426** together form a center-tapped delay means which provides an overall delay of **512** successive shift pulses for each respective one of the video A, video B, video C and video D signals loaded into the input of **1** TV line delay logic **422.** Furthermore, since logic **422** cannot be loaded and shifted at the same time, there is provided a phase delay between the loading of the first stage of the four shift registers of delay logic **422** and the shifting of both these four shift registers and the corresponding four shift registers of delay logic **426.** Specifically, both the A and B shift registers of both blocks **422** and **426** are shifted in response to a phase C clock applied thereto, while both the C and D shift registers of both block **422** and **426** are shifted in response to a phase A clock applied thereto. This is illustrated in the timing diagram of FIG. **6,** wherein the leading edge of the video **A1, A2, B1,** and B2 200 nanosecond dot pulses occur in time coincidence with the leading edge of a phase C clock, although the leading edge of the video A dot pulse itself occurs in time coincidence with the leading edge of the preceding phase A clock and the leading edge of the video B dot pulse itself occurs in time coincidence with

the preceding phase B clock. In a similar manner, the leading edge of the C1, C2, D1 and D2 dot pulses occur in time coincidence with a phase A clock, although the leading edge of the video C dot pulse itself occurs in time coincidence with the preceding phase C clock and the leading edge of the D dot pulse itself occurs in time coincidence with the preceding phase D clock.

Thus, the overall delay between the occurrence of an A1 or C1 200 nanosecond dot pulse on connection **424** with respect to the occurrence of the corresponding video A and video C dot pulses on connection **418** is actually 100 nanoseconds greater than one TV line delay, while in the case of the video B1 and video D1 dot pulses this delay is actually 50 nanoseconds greater than one TV line delay. In a similar manner, the actual delay of the A2, B2, C2 and D2 video dot pulses on connection **428** is either 50 or 100 nanoseconds greater than a two TV line delay with respect to the corresponding video A, video B, video C and Video D dot pulses applied to connection **418.**

Despite the 50 or 100 nanosecond phase delay of the 200 nanosecond video dot pulses appearing on connections **424** and **428** with respect to the corresponding 200 nanosecond dot pulses appearing on conductor **418,** the sampling of these video dot pulses in video dot shaping and phasing flip flops **420** is such that the 50 nanosecond video A1′ and A2′ dot pulses occur in time coincidence with a video A′ dot pulse, the 50 nanosecond video B1′ and B2′ dot pulses occur in time coincidence with a video B′ dot pulse, the 50 nanosecond video C1′ and C2′ dot pulses occur in time coincidence with a video C′ dot pulse and the 50 nanosecond video D1′ and D2′ dot pulses occur in time coincidence with a video D′ dot pulse. This is illustrated in the timing diagram of FIG. **6,** which shows that the 200 nanosecond video A1 or A2 dot pulse, as well as the 200 nanosecond video A dot pulse, is sampled by a phase D clock; the 200 nanosecond B1 and B2 dot pulses, as well as the 200 nanosecond video B dot pulse, is sampled by a phase A clock; the 200 nanosecond video C1 and C2 dot pulses, as well as the 200 nanosecond video C dot pulse, is sampled by a phase B clock, and the 200 nanosecond video D1 and D2 dot pulses, as well as the 200 nanosecond video D pulses, is sampled by a phase C clock.

As further shown in FIG. **4,** all the video A′, B′, C′ and D′ signals are applied through OR gate **430** as a first input to **2** dot delay logic **436.** Similarly, all the video A1′, B1′, C1′ and D1′ signals are applied through OR gate **432** as a second input to **2** dot delay **436** and all of the video A2′, video B2′, video C2′ and video D2′ signals are applied through OR gate **434** as a third input to **2** dot delay logic **436.** In addition, the output from OR gate **430** represents the V_{00} signal (the video signal with no dot delay and no TV line delay). In a similar manner, the output from OR gate **432** represents the V_{01} signal (the video signal with no dot delay and one TV line delay) and the output from OR gate **434** represents the V_{02} signal (the video signal with no dot delay and two TV line delay).

2 dot delay logic **436,** in response to a 50 nanosecond clock applied thereto, provides a two dot (100 nanosecond) delay in each of its three inputs to thereby provide three corresponding outputs represented by the V_{10}, V_{11} and V_{12} signals. The three output signals from **2** dot delay logic **436** are also applied as inputs to **2** dot delay logic **438,** which, in response to 50 nanosecond clock pulses applied thereto, provides an additional two dot (100 nanosecond) delay. This results in corresponding output signals represented by output V_{20}, V_{21}, V_{22} appearing at the output of **2** dot delay logic **438.**

As further shown in FIG. **4,** eight of the nine output signals from OR gates **430, 432** and **434** and **2** dot delay logic blocks **436** and **438** are applied as inputs to OR gate **440.** In particular, signals V_{00}, V_{01}, V_{02}, V_{10}, V_{12}, V_{20}, V_{21} and V_{22} are applied as inputs to OR gate **440,** while the remaining one of these nine signals, V_{11}, is applied as an input to an inverter **444** and as an input to signal mixer **446.** Horizontal and vertical TV sync signals and a TV blanking signal are applied as additional inputs to signal mixer **446.**

The output of OR gate **440** is applied as a first input to AND gate **442,** while the output from inverter **444,** manifesting V_{11}, is applied as a second input to AND gate **442.**

The symbol video present on connection **116** consists of two separate component video signals. The first of these two separate component video signals is the edge key video signal which appears at the output from AND gate **442** and the second of these separate component video signals is the monochrome video signal which appears at the output of signal mixer **446.** As shown in FIG. **1,** the edge key video signal and the monochrome video signal, which together form the symbol video output present on connection **116,** are applied as control inputs to composite video signal derivation means **102.**

It will be seen that the edge key video signal is derived in response to the presence of any one or more of the eight signal inputs to OR gate **440,** if and only if signal V_{11} is then absent.

As is known, each frame of a television picture is made up of two interlaced raster-scan fields. When the video signal A, B, C and D present on connection **418** correspond to the first (top) television scan line of a row of symbols to be displayed during a given raster-scan field, no signal is present on connection **424** and, hence, output signal V_{11} (along with output signals V_{01} and V_{21}) is absent. Similarly, two TV scan lines after the video A, B, C and D signals corresponding to the last (bottom) television scan line of a row of symbols to be displayed during a given raster-scan field, video A2, B2, C2 and D2 signals are present on connection **428,** but no video signals are present on either connection **418** or connection **424.** Therefore, in this case, signals V_{02}, V_{12} and V_{22} are applied to OR gate **440,** but signal V_{11} is absent. During all intermediate scan lines of a display signal, the V_{11} signal is present, except for the first two dot periods (100 nanoseconds) of the scan of that symbol, when none of the output signals V_{10}, V_{11}, V_{12}, V_{20}, V_{21} nor V_{22} is present, and during the last two dot periods (100 nanoseconds) of the scan of that symbol, when none of output signals V_{00}, V_{01}, V_{02}, V_{10}, V_{11} nor V_{12} is present. Thus, because of the fact that a television frame is made of two interlaced raster-scanned fields, the generation of the edge key video signal corresponds to the edge key video portion of FIG. **3***c*, while the generation of the monochrome video signal corresponds to the monochrome video portion of FIG. **3***c*.

The edge key video signal and/or the monochrome video signal component of the symbol video may be made use of in various ways within composite video signal derivation means **102.** For instance, the edge key video signal alone may be used to "key out" the picture video. In this case, the picture video would appear both outside the symbol and within the "monochrome"

video portion of the symbol. A second example would be to OR together the monochrome video signal and the edge key video signal to "key out" the picture video. In this case, the symbols would appear as "black" block symbols within the picture field. However, if the monochrome video signal, besides being combined with the edge key video signal for "keying out" purposes, is also employed to gate in a selected color into the mixed composite video signal, the monochrome video portion of the symbol will appear in the selected color within a "black" edging. Further, the combined edge key video signal and monochrome video signal, beside being used for "key out" purposes, may also be used for selecting a second color, In this later case, the monochrome video portion of the symbol will appear in the first color within an edging having the second color. Besides these various examples, other ways of using either or both the edge key video signal and the monochrome video signal may occur to the controller of a television broadcast display control system. In any case, it is the generation of the separate edge key video signal and monochrome video signal by the techniques embodied in generator **112** of FIG. **4**, and not the various ways of employing these two components of the symbol video within composite video signal derivation means **102**, which forms the novel subject matter of the present invention.

What is claimed is:

1. In a digital generator of graphic symbols with edging for display on a display device exhibiting a television raster scan, said generator being of the type which includes a character generator memory responsive to the application thereto of a first multibit symbol code and a second multibit scan line per symbol height code for deriving an m bit parallel dot pattern manifesting a selected scan-line portion of a selected symbol to be displayed; the improvement therein comprising:

a. a set of n shift registers each having k stages, wherein both n and k are plural integers and m is equal to the produce of n times k;

b. means for loading said k stages of each ordinal one of said n shift registers with the i, $n+i$, $2n+i$, . . . $m-n+i$ ordinal ones of said m bits, where i is the ordinal value of that ordinal one of said n shift registers;

c. means for applying as shift pulses to each respective one of said n shift registers a corresponding one of a set of n clocks, each of said n clocks consisting of a series of pulses each having a duration of t which occur at a repetition frequency substantially equal to $1/nt$, and each ordinal one of said set of n clocks being phase delayed by a time interval substantially equal to t with respect to the preceding one of said set of n clocks, to thereby produce a set of respective outputs of said n shift registers each pulse of which has a duration substantially equal to nt,

d. first and second serially connected 1 television scan line delay logic means having the set of respective outputs of said n shift registers applied as respective inputs to said first line delay logic means for producing a first set of corresponding outputs from said first line delay logic means and a second set of corresponding outputs from said second line delay logic means,

e. video dots shaping and phasing flip flops having said set of respective outputs of said n shift registers applied as first inputs thereto, said first set of corresponding outputs applied as second inputs thereto, said second set of corresponding outputs applied as third inputs thereto, and said set of n clocks as fourth inputs thereto for sampling all of each separate group of corresponding ones of said first, second and third inputs with a different respective predetermined one of said set of n clocks, whereby said video dots shaping and phasing flip flops derives first, second and third output dot samples corresponding respectively to said first, second and third inputs thereto, with each dot sample having a duration t;

f. first and second serially connected dot delay logic means, each of which provides a delay substantially equal to a predetermined integral multiple of t, said first, second and third output dot samples being applied as inputs to said first dot delay logic means for producing a first set of corresponding outputs from said first dot delay logic means and a second set of corresponding outputs from said second dot delay logic means, and

g. output means including first means responsive to the presence of that given particular one of said first set of outputs from said first dot delay logic corresponding to said second output dot samples for deriving a monochrome video signal, and second means responsive to the absence of said given particular one of said first set together with the presence of at least another of said first set, any of said first, second and third output dot samples, or any of said second set of corresponding outputs from said second dot delay logic means for deriving an edge key video signal.

2. The generator defined in claim **1**, wherein m is 32, n is four, k is eight, and t is 50 nanoseconds, whereby $1/nt$ is five megahertz and nt is 200 nanoseconds.

3. The generator defined in claim **2**, wherein said graphic symbols are for display on a display device exhibiting a television raster scan for a frame consisting of two interlaced raster-scan fields, and wherein said predetermined integral multiple of t is two, whereby each of said first and second dot delay logic means provides a delay of one-hundred nanoseconds.

4. The generator defined in claim **1**, wherein each of said first and second serially connected 1 television scan line delay logic means includes a second set of n shift registers individually corresponding to each of the n shift registers of said first-mentioned set, each of said second set of n shift registers having a given number of stages which is equal to the number of pulses in the series of any one of said n clocks which occur during any one complete television scan line, means for loading the first stage of each of the n shift registers of said first 1 television scan line delay logic means with the output of the corresponding one of the n shift registers of said first-mentioned set, and means for applying as shift pulses to each respective one of said n shift registers of said second set of both said first and second 1 television scan line delay logic means a preselected one of said n clocks which is different from the clock applied as shift pulses to the corresponding one of the first-mentioned set of n shift registers, but which results in the respective outputs from the corresponding shift registers of said first-mentioned set and said second set of both said first and second serially connected 1 television scan line delay logic means all being simultaneously present during the occurrence of the sampling of the respective outputs of these corresponding shift registers by said

different respective predetermined ones of said set of n clocks in said video dots shaping and phasing flip-flops.

5. The generator defined in claim **1**, wherein said first means of said output means comprises a signal mixer for mixing said given particular one of said first set of outputs with television sync signals and television blanking signals.

6. The generator defined in claim **1**, wherein said second means of said output means comprises an OR gate for combining said first, second and third output dot samples, each of said others of said first set and all of said second set, an AND gate having the output of said OR gate applied as a first input thereto, and an inverter for applying said given particular one of said first set of outputs as a second input to said AND gate, the output from said AND gate constituting said edge key video signal.

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