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(56) Documents Cited:
GB 2361123 A **US 8243855 B2**
US 6909886 B2

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Other: **WPI,EPODOC, TXTE**

(54) Title of the Invention: **IQ signal generator system and method**
Abstract Title: **An IQ signal generator comprising a quadrature coupler merged into an amplifier**

(57) An IQ signal generator comprising a quadrature coupler merged into an amplifier An IQ generator, which may be used in a vector modulator, comprises a quadrature coupler merged into an amplifier. I and Q signals of equal magnitude are derived from ports 2 and 3 when the single-ended input Vin is applied to the gate of the common source input transistor M1. The quadrature coupler may comprise a lumped element configuration L,C/2, which provides a compact circuit design, or an equivalent distributed component configuration such as a branch line coupler (figure 4). The circuit provides good IQ amplitude matching, less I/Q imbalance, no losses, and less noise than prior art IQ generators. The optical common-gate output transistors M3,M4 provide configuration which improves isolation of the generator outputs.

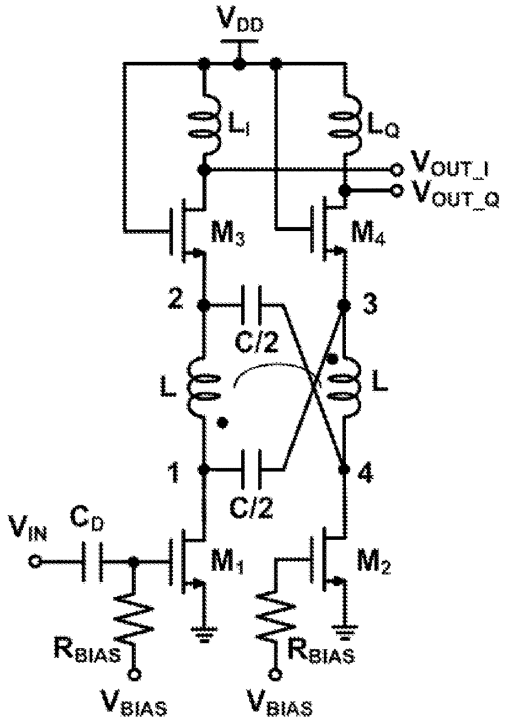

Figure 2

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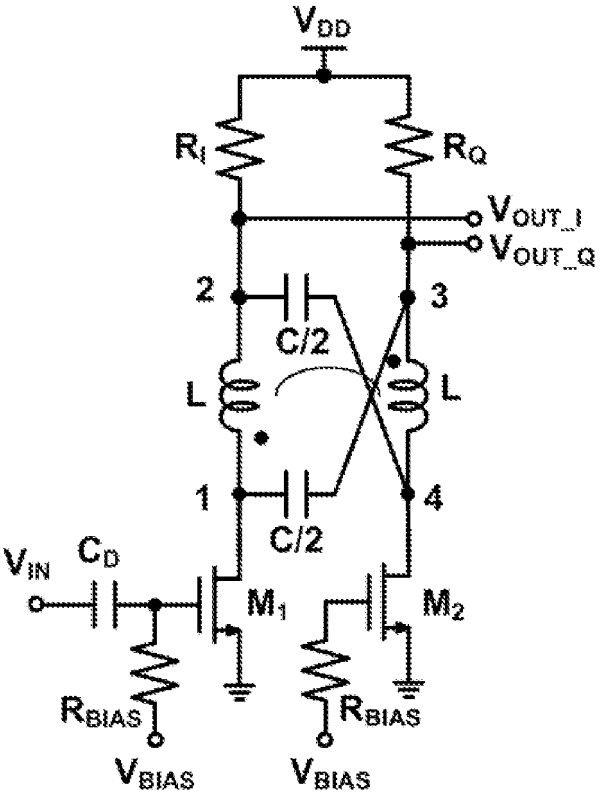

VDD
RI
RQ
VOUT_I
VOUT_Q
2
3
C/2
L
L
1
4
C/2
VIN
CD
M1
M2
RBIAS
RBIAS
VBIAS
VBIAS

Figure 1

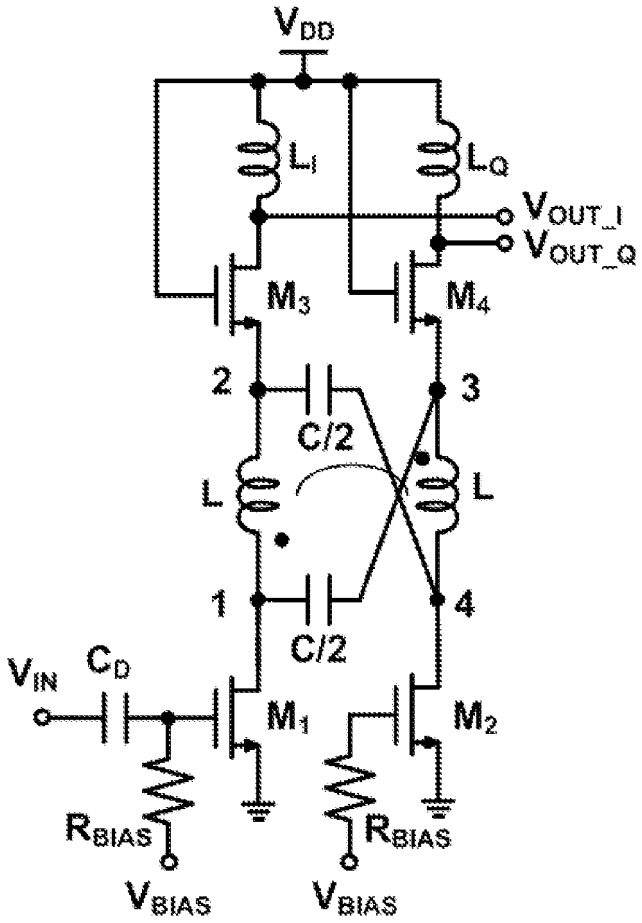

VDD
LI
LQ
VOUT_I
VOUT_Q
M3
M4
2
3
C/2
L
L
1
4
C/2
VIN
CD
M1
M2
RBIAS
RBIAS
VBIAS
VBIAS

Figure 2

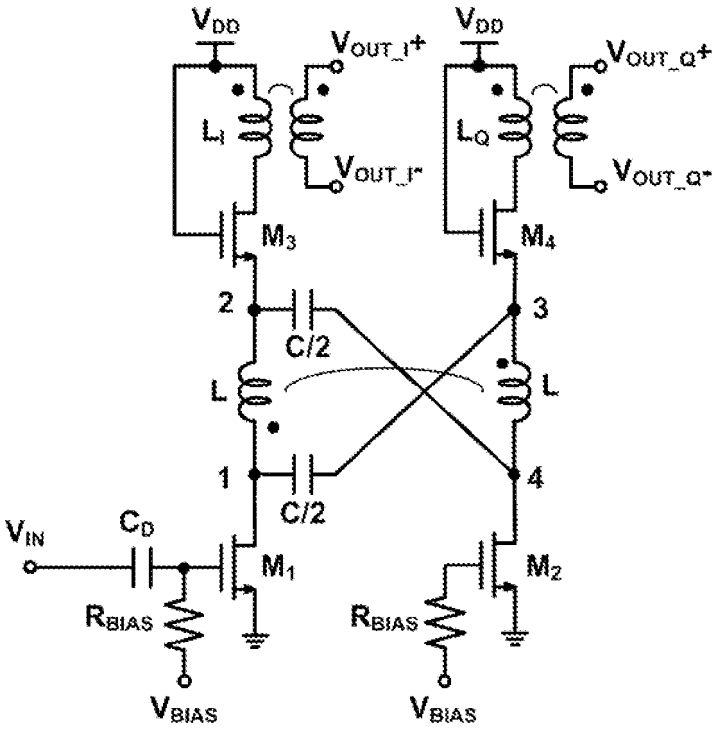
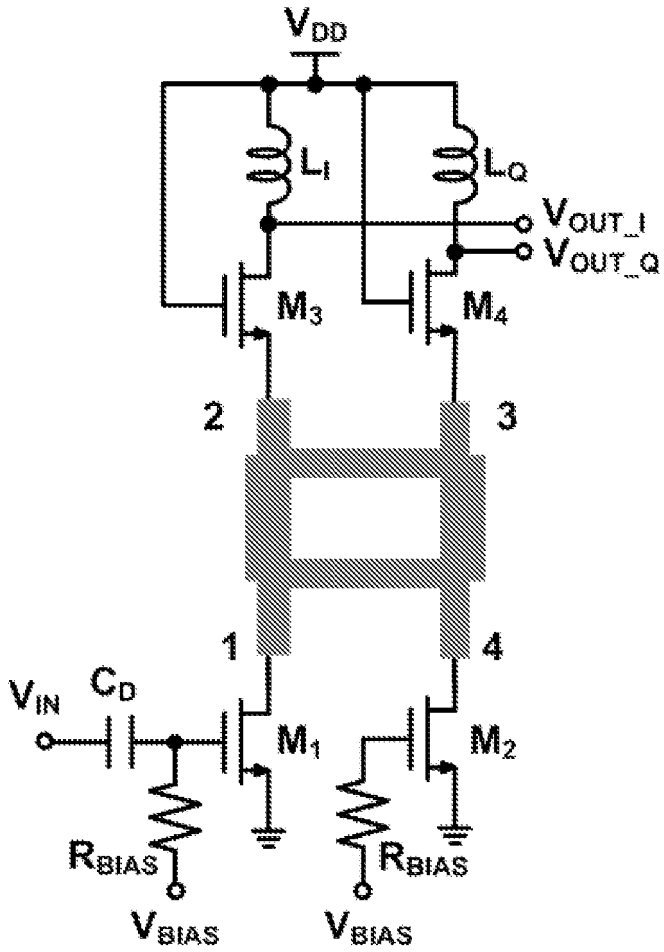

VDD
VOUT_I+
VOUT_I-
LI
VDD
VOUT_Q+
VOUT_Q-
LQ
M3
M4
2
C/2
3
L
L
1
C/2
4
VIN
CD
M1
M2
RBIAS
RBIAS
VBIAS
VBIAS

Figure 3


VDD
LI
LQ
VOUT_I
VOUT_Q
M3
M4
2
3
1
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VIN
CD
M1
M2
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VBIAS
VBIAS

Figure 4

Title

IQ signal generator System and Method

Field

The present invention is concerned with providing an IQ signal generator. More particularly, the invention is concerned with providing an IQ signal generator for a vector modulator phase shifter.

Background

A common design requirement in electronic circuits is to provide two signals with a 90 degree phase shift, commonly referred as in-phase (I) and in-quadrature (Q) signals. There are a number of methods typically used to obtain such a 90 degree phase shift. These include the use of delay lines and polyphase filters.

All-pass polyphase filters usually result in losses which impair the Noise Figure (NF) of the receiver. Delay lines generally introduce fewer losses than polyphase filters. However, delay lines present a small but unavoidable attenuation in the delayed path. This attenuation can lead to an imbalance of the in-phase (I) and quadrature (Q), components of the output signal. For particular applications, such as for example, but not limited to, passive imaging, the minimization of losses and NF contribution in the receiver chain can be an imperative requirement.

In order to minimize the losses associated with such phase shifters, it is known to integrate delay lines or polyphase filters into a common-source or a cascode amplifier. For example, a solution incorporating polyphase filters has the 0º and 180º nodes connected to the load and the drain of the common source transistors, and the 90º and 270º nodes connected to the load only. This connection makes the node impedances equal only if the drain impedance of the common source transistors tends to infinite. However, this occurs only at lower frequencies and for long-channel devices.

Moreover, this circuitry may only be realized by means of a differential topology.

It is an object of the present invention to provide a phase shifter which overcomes at least some of the above mentioned problems and weaknesses of solutions currently available.

Summary

According to the invention there is provided, as set out in the appended claims, a IQ generator for a vector modulator phase shifter comprising:

an amplifier comprising an integrated quadrature coupler, the quadrature coupler comprising an input port and an isolated port and a first and a second output port;

wherein the first output port of the quadrature coupler is adapted to generate an in-phase component of an output signal of the amplifier and the second output port of the quadrature coupler is adapted to generate a quadrature component of an output signal of the amplifier.

In one embodiment the quadrature coupler comprises a coupled line quadrature coupler.

In one embodiment the coupled line quadrature coupler comprises a plurality of lumped circuit components.

In one embodiment the coupled line quadrature coupler further comprises an input port and an isolated port, a first and a second output port, and wherein the lumped circuit components comprise a first and a second inductor forming a transformer and a first and a second capacitor; wherein the first inductor is connected between the input port and the first output port and the second inductor is connected between the isolated port and the second output port, and the first capacitor is coupled between the input port and the second output port and the second capacitor is connected between the isolated port and the first output port.

In one embodiment the quadrature coupler comprises a branch line coupler.

In one embodiment the branch line quadrature coupler comprises a plurality of distributed circuit components.

In one embodiment the first and the second output ports are connected to the same load impedance.

In one embodiment the amplifier comprises a cascode amplifier.

In one embodiment the cascode amplifier comprises a first transistor, a second transistor, a third transistor and a fourth transistor, wherein the input port is connected to the drain of the first transistor and the isolated port is connected to the drain of the second transistor, and the first output port is connected to the source of the third transistor and the second output port is connected to the source of the fourth transistor.

In one embodiment the amplifier comprises a common-source amplifier.

In one embodiment the common-source amplifier comprises a first and a second transistor and a first and a second resistor, wherein the input port is connected to the drain of the first transistor and the isolated port is connected to the drain of the second transistor, and the first output port is connected to the first resistor and the second output port is connected to the second resistor.

In one embodiment the amplifier is a single-ended amplifier.

In one embodiment the amplifier is a differential amplifier.

According to another embodiment there is provided a method of generating an IQ signal comprising:

configuring an amplifier with an integrated quadrature coupler, the quadrature coupler comprising an input port and an isolated port and a first and a second output port;

generating an in-phase component of an output signal of the amplifier from the first output port of the quadrature coupler; and

generating a quadrature component of an output signal of the amplifier at the second output port.

Brief Description of the Drawings

The invention will be more clearly understood from the following description of embodiments thereof, given by way of example only, with reference to the accompanying drawings, in which:-

Figure 1 discloses one embodiment of the IQ generator of the present invention when integrated into a common-source amplifier;

Figure 2 discloses another embodiment of the IQ generator of the invention when integrated into a cascode amplifier with single-ended I and Q outputs;

Figure 3 discloses yet another embodiment of the IQ generator of the invention when integrated into a cascode amplifier with differential I and Q outputs; and

Figure 4 discloses yet another embodiment of the IQ generator of the present invention when integrated into a cascode amplifier when the quadrature coupler is a branch line hybrid coupler.

Detailed Description of the Drawings

The IQ generator of the present invention comprises an amplifier comprising an integrated quadrature coupler, wherein a first output port of the quadrature coupler is adapted to generate the in-phase component of the output signal of the amplifier and a second output port of the quadrature coupler is adapted to generate the quadrature component of the output signal of the amplifier.

The IQ generator of the present invention may be provided by many different implementations of a quadrature coupler integrated into an amplifier. For example, the quadrature coupler can be implemented through either lumped components or distributed components. In addition, the quadrature coupler can be integrated into any type of amplifier, such as, but not limited to, a common source amplifier or a cascode amplifier.

Figures 1 to 4 illustrate four exemplary implementations of the IQ generator of the invention. However, it will be appreciated that the invention could equally well be applied to many other amplifier and quadrature coupler arrangements.

Figure 1 shows an embodiment of the invention where the quadrature coupler is implemented with lumped circuit components and is integrated into the circuitry of a common-source amplifier.

As shown in the figure, the quadrature coupler comprises a port 1 (input port) and a port 4 (isolated port) and a port 2 (first output port) and a port 3 (second output port). The lumped circuit components within the ports comprise a first and a second inductor of value L forming a transformer, and a first and a second capacitor of value C/2.The circuit components are sized as follows: $L=Z_0/\omega_0$; $C=1/(Z_0\omega_0)$; $Z_0=(LC)^{1/2}$; $\omega_0=2\pi f_0$; where f_0 is the central frequency of operation. The first inductor is connected between the input port 1 and the output port 2. The first inductor is magnetically coupled with the second inductor connected between the port 4 and the output port 3. The first capacitor is connected between the input port 1 and the output port 3, and the second capacitor is connected between the port 4 and the output port 2.

The common-source amplifier comprises a first transistor M1 and a second transistor M2 and load impedances R_I and R_Q. R_I and R_Q are sized as follows: $R_I=R_Q=Z_0$. The sources of transistors M1 and M2 are connected to ground. The input port 1 of the quadrature coupler is connected to the drain of the first transistor M1 and the port 4 is connected to the drain of the second transistor

M2. The gate of transistor M1 is connected to an input voltage V_{in}, with or without a dc decoupling capacitor C_D. The gates of both transistors M1 and M2 are biased by a voltage V_{bias} via resistance R_{bias}. Alternatively, M1 and M2 could be biased through other common techniques, for example, through current mirrors. The first output port 2 of the quadrature coupler is connected to the resistor R_I and the second output port 3 is connected to the resistor R_Q. The other end of resistors R_I and R_Q are connected to a supply voltage V_{DD}.

In operation, the in-phase component of the output signal of the amplifier, V_{out_I}, is obtained at the first output port 2 of the quadrature coupler (the I output node), and the quadrature component of the output signal of the amplifier V_{out_Q} is obtained at the second output port 3 (the Q output node). At the operating frequency f_0, the input signal power is equally split by the coupler into two signal paths, one towards the port 2 and one towards the port 3. As an effect of the lumped component quadrature coupler, the output signal at the port 2 is delayed by 45º with respect to the input signal; whereas the output signal at the port 3 is anticipated by 45º with respect to the input signal. Overall, the output signals at the port 2 and port 3 are shifted by 90º.

Figure 2 shows an alternative embodiment of the invention where the quadrature coupler is integrated into a cascode amplifier. It can be seen that the circuit of Figure 2 is similar to the circuit of Figure 1, in that the input port 1 and the port 4 are connected to the same components as those of Figure 1. However, the first output port 2 of the quadrature coupler is now connected to the source of the transistor M3 of the cascode amplifier, while the second output port 3 is connected to the source of a fourth transistor M4. The drain of transistor M3 is connected to the supply voltage V_{DD} via inductor L_1, whereas the drain of transistor M4 is connected to the supply voltage V_{DD} via inductor L_Q. The gates of both transistors M3 and M4 are also connected to the supply voltage V_{DD}.

In operation, the in-phase component of the output signal of the amplifier, V_{out_I}, is obtained at the drain of transistor M3 and the quadrature component of the

output signal of the amplifier, V_{out_Q}, is obtained at the drain of the transistor M4. As explained for the circuit in Figure 1, at the operating frequency f_0, the input signal power is equally split by the coupler into two signal paths, one towards the port 2 and one towards the port 3. Overall, the output signals at the port 2 and port 3 are shifted by 90º. With respect to the circuit in Figure 1, the circuit in Figure 2 provides better isolations from the output of the amplifier to the input terminal of the amplifier, as well as to the output terminals (ports) of the quadrature coupler.

Figure 3 shows an alternative embodiment of the invention where the quadrature coupler is integrated into a cascode amplifier. It can be seen that this circuit is the same as the circuit of Figure 2, except that the inductors L_I and L_Q now provide differential I components, V_{out_I+} and V_{out_I-}, and differential Q components, V_{out_Q+} and V_{out_Q-}, respectively. The functionality is the same as described for the circuit in Figure 2, with the difference that output differential signals I and Q are provided in the case of the circuit in Figure 3.

Figure 4 shows an alternative embodiment of the invention where the quadrature coupler is implemented through distributed components and integrated into a cascode amplifier. It can be seen that this circuit is the same as the circuit of Figure 2, except that the quadrature coupler is now implemented through a branch-line quadrature coupler realized with distributed components such as transmission lines, rather than lumped components. The functionality is the same as described for the circuit in Figure 2, with the difference that output signals I and Q are obtained as an effect of the quadrature coupler implemented via a branch-line directional coupler with distributed components such as transmission lines.

The present invention has a number of advantages when compared to prior art phase shifter implementations. Firstly, the IQ generator of the present invention enables I and Q output components of exactly the same amplitude to be generated. It can also provide for the generation of I and Q signal components

having less I/Q imbalance, no losses and less noise when compared with prior art phase shifters.

In the present invention, the I and Q output nodes of the coupler are connected to loads of equal impedance. Moreover, the spirals of the transformer are connected in series between the common-source and common-gate transistors, allowing a compensation of the parasitic capacitances at those nodes. As a result, the present invention is also suitable for operation at extremely high frequencies.

In addition, the present invention can be realized in both single-ended and differential topologies, in a more compact circuit design.

As the present invention can be implemented with lumped components, it also allows a great area saving on silicon compared to delay line implementations.

It will be appreciated that IQ generator of the present invention can be used for phase shifting in the RF path, baseband path and Local Oscillator (LO) path. The IQ generator can be exploited in a vector modulator phase shifter in an integrated circuit, and, in general in any application in which IQ generation is needed. Examples of applications are, but not limited to, the emerging mm-wave wireless applications for communication and sensing, where a phased array approach is required, such as 60 GHz multi-gigabit-per-second wireless communications, 77 and 79 GHz automotive radars, and W-band imagers. It will be appreciated that the selection of the particular embodiment of IQ generator circuitry to use is thus dependent on the application in which it is to be used.

The embodiments in the invention described with reference to the drawings comprise a computer apparatus and/or processes performed in a computer apparatus. However, the invention also extends to computer programs, particularly computer programs stored on or in a carrier adapted to bring the invention into practice. The program may be in the form of source code, object code, or a code intermediate source and object code, such as in partially

compiled form or in any other form suitable for use in the implementation of the method according to the invention. The carrier may comprise a storage medium such as ROM, e.g. CD ROM, or magnetic recording medium, e.g. a floppy disk or hard disk. The carrier may be an electrical or optical signal which may be transmitted via an electrical or an optical cable or by radio or other means.

In the specification the terms "comprise, comprises, comprised and comprising" or any variation thereof and the terms include, includes, included and including" or any variation thereof are considered to be totally interchangeable and they should all be afforded the widest possible interpretation and vice versa.

The invention is not limited to the embodiments hereinbefore described but may be varied in both construction and detail.

Claims

1. An IQ generator for a vector modulator phase shifter comprising:
an amplifier comprising an integrated quadrature coupler, the quadrature coupler comprising an input port and an isolated port and a first and a second output port;
wherein the first output port of the quadrature coupler is adapted to generate an in-phase component of an output signal of the amplifier and the second output port of the quadrature coupler is adapted to generate a quadrature component of an output signal of the amplifier.

2. The IQ generator of Claim 1, wherein the quadrature coupler comprises a coupled line quadrature coupler.

3. The IQ generator of Claim 2, where the coupled line quadrature coupler comprises a plurality of lumped circuit components.

4. The IQ generator of Claim 3, where the coupled line quadrature coupler further comprises an input port and an isolated port, a first and a second output port, and wherein the lumped circuit components comprise a first and a second inductor forming a transformer and a first and a second capacitor; wherein the first inductor is connected between the input port and the first output port and the second inductor is connected between the isolated port and the second output port, and the first capacitor is coupled between the input port and the second output port and the second capacitor is connected between the isolated port and the first output port.

5. The IQ generator of Claim 1, wherein the quadrature coupler comprises a branch line coupler.

6. The IQ generator of Claim 5, wherein the branch line quadrature coupler comprises a plurality of distributed circuit components.

7. The IQ generator of any of the previous claims, wherein the first and the second output ports are connected to the same load impedance.

8. The IQ generator of any of the previous claims, wherein the amplifier comprises a cascode amplifier.

9. The IQ generator of Claim 7, wherein the cascode amplifier comprises a first transistor, a second transistor, a third transistor and a fourth transistor, wherein the input port is connected to the drain of the first transistor and the isolated port is connected to the drain of the second transistor, and the first output port is connected to the source of the third transistor and the second output port is connected to the source of the fourth transistor.

10. The IQ generator of any of Claims 1 to 7, wherein the amplifier comprises a common-source amplifier.

11. The IQ generator of Claim 10, wherein the common-source amplifier comprises a first and a second transistor and a first and a second resistor, wherein the input port is connected to the drain of the first transistor and the isolated port is connected to the drain of the second transistor, and the first output port is connected to the first resistor and the second output port is connected to the second resistor.

12. The IQ generator of any of the previous claims wherein the amplifier is a single-ended amplifier.

13. The IQ generator of any of Claims 1 to 11, wherein the amplifier is a differential amplifier.

14. A method of generating an IQ signal comprising:

configuring an amplifier with an integrated quadrature coupler, the quadrature coupler comprising an input port and an isolated port and a first and a second output port;

generating an in-phase component of an output signal of the amplifier from the first output port of the quadrature coupler; and

generating a quadrature component of an output signal of the amplifier at the second output port.

Intellectual Property Office

Application No:	GB1415851.3	**Examiner:**	Mr K Sylvan
Claims searched:	1-14	**Date of search:**	6 March 2015

Patents Act 1977: Search Report under Section 17

Documents considered to be relevant:

Category	Relevant to claims	Identity of document and passage or figure of particular relevance
A	-	US8243855 B2 Zarei. See figure 4 and column 5 lines 13-15.
A	-	US6909886 B2 Magnusen. See figure 1.
A	-	GB2361123 A Nokia. See figure 2.

Categories:

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.

Field of Search:

Search of GB, EP, WO & US patent documents classified in the following areas of the UKC^{X} :

Worldwide search of patent documents classified in the following areas of the IPC

H03D; H03H; H04L

The following online and other databases have been used in the preparation of this search report

WPI,EPODOC,TXTE

International Classification:

Subclass	Subgroup	Valid From
H03H	0011/22	01/01/2006