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EP 0600184 A WO 94/17554 A US 5506816 A
US 5148401 A US 4554646 A

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(54) Abstract Title
A semiconductor memory device

(57) A semiconductor memory device includes a cell array formed of a plurality of rows and columns, a row decoder 200 and a column decoder for respectively selecting rows and columns in accordance with addresses. The memory device has a hierarchical word line structure in which sub word line driving circuits MN1, MN2 numbering 2^m per sub word line group are obtained by classifying respective cell arrays into n sub cell blocks in the column direction, and classifying sub word lines of respective sub cell blocks by 2^m, and a main word line MWL is provided in the row direction. The semiconductor memory device comprising the row decoder 200 for providing said main word line MWL by receiving the row address of one portion. Word line boosting signal generating means 100 receive the remaining row addresses numbering m as an input for producing word line boosting signal and word line boosting signal bar by 2^m. A plurality of sub word line driving means MN1, MN2 drive said sub word lines in accordance with said word line boosting signal and word line boosting signal bar.

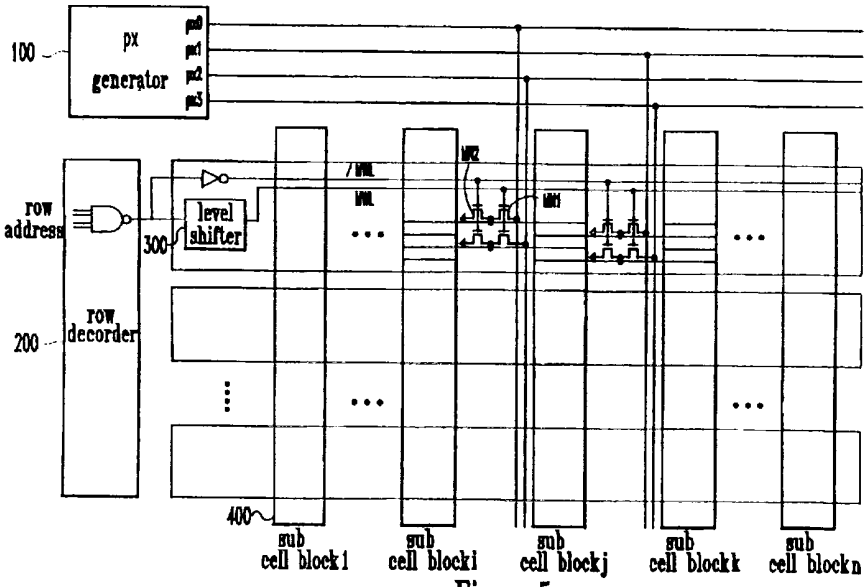

Fig . 5

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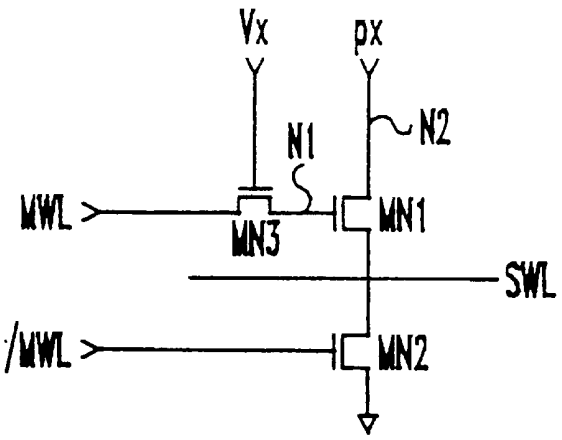


Fig . 1
(Prior Art)

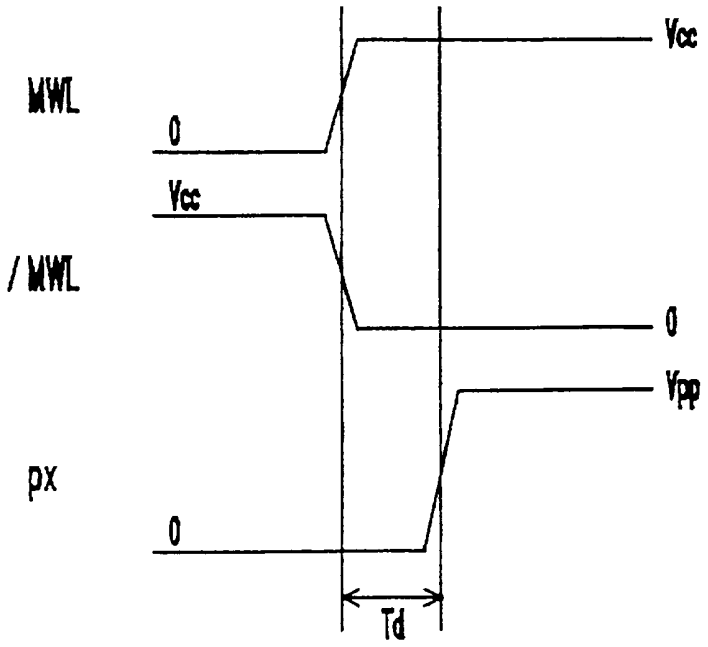


Fig . 2
(Prior Art)

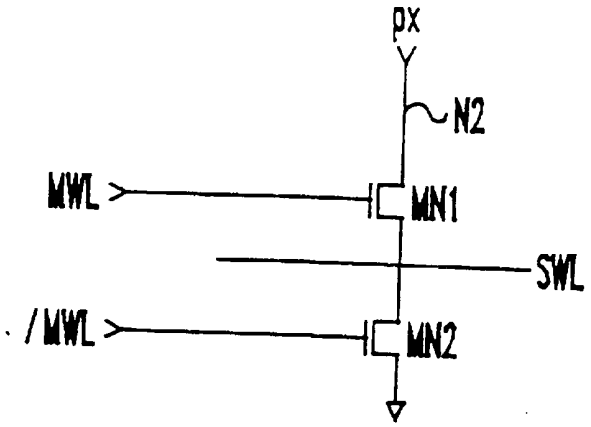


Fig . 3

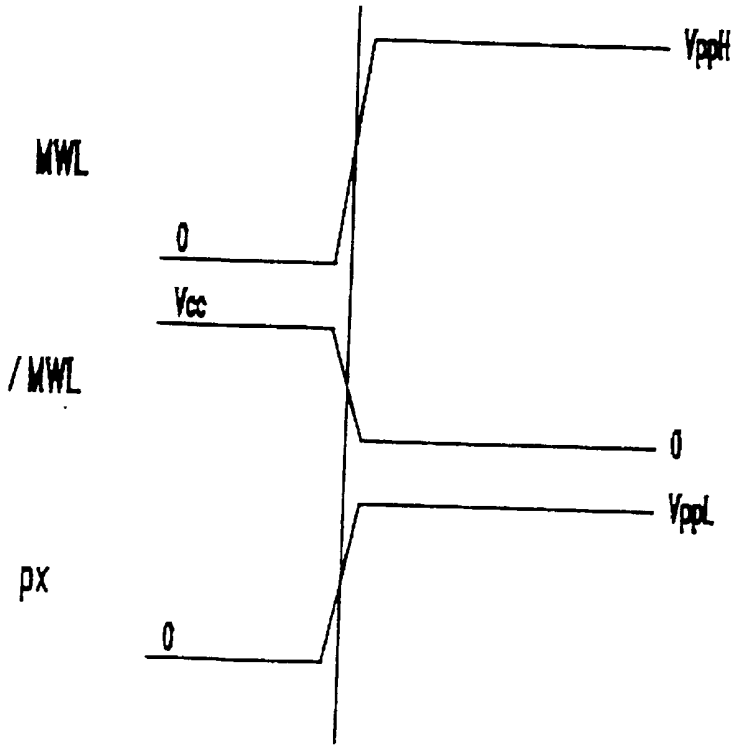
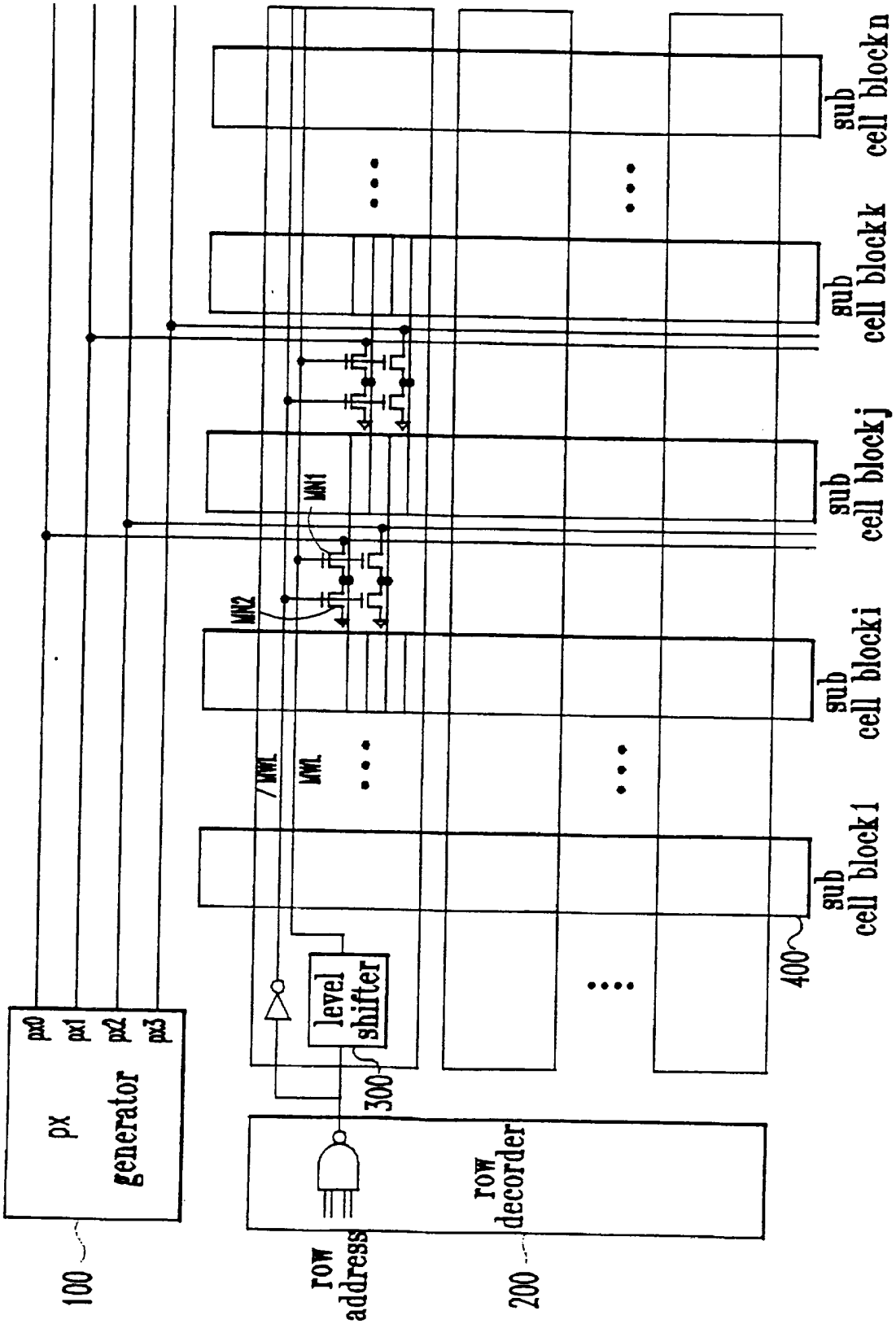


Fig . 4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px1
px2
px3
px
generator
100
level
shifter
300
/MWL
MWL
MW1
MW2
row
address
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200
400
sub
cell block1
sub
cell blocki
sub
cell blockj
sub
cell blockk
sub
cell blockn

Fig. 5

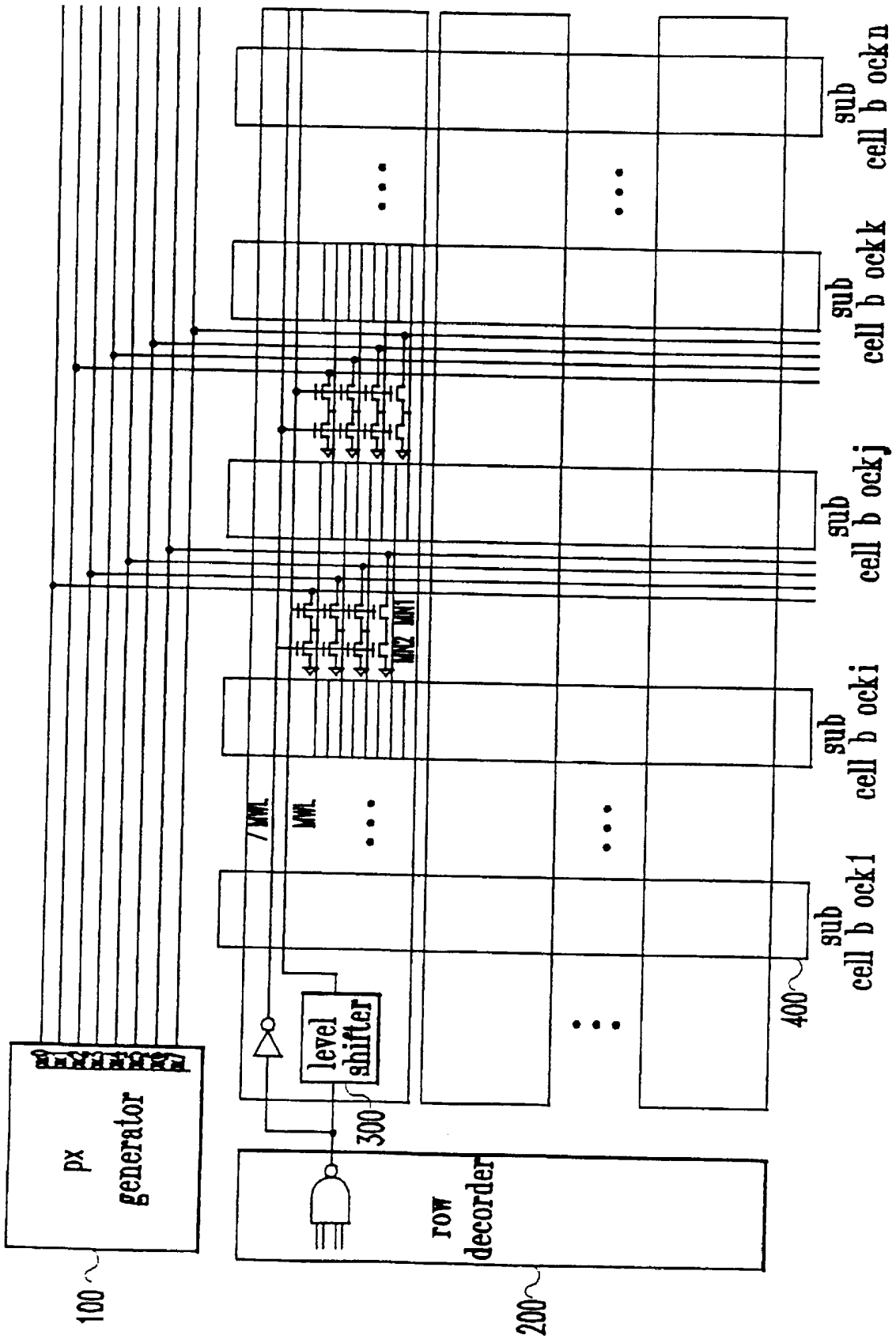
px
generator
100
level
shifter
300
row
decorder
200
/WWL
WWL
WWL WWL
sub
cell b ock1
sub
cell b ocki
sub
cell b ockj
sub
cell b ockk
sub
cell b ockn
400

Fig. 6

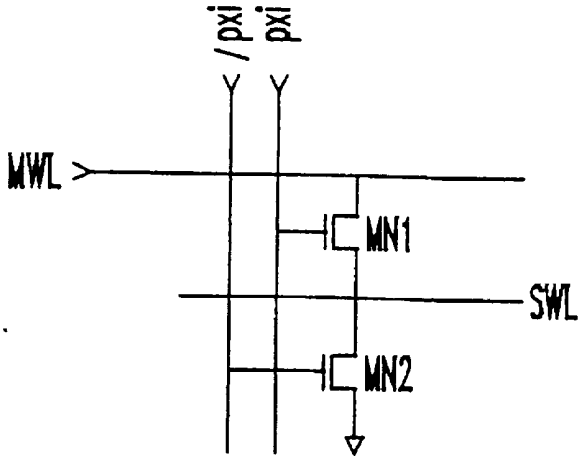

Fig . 7

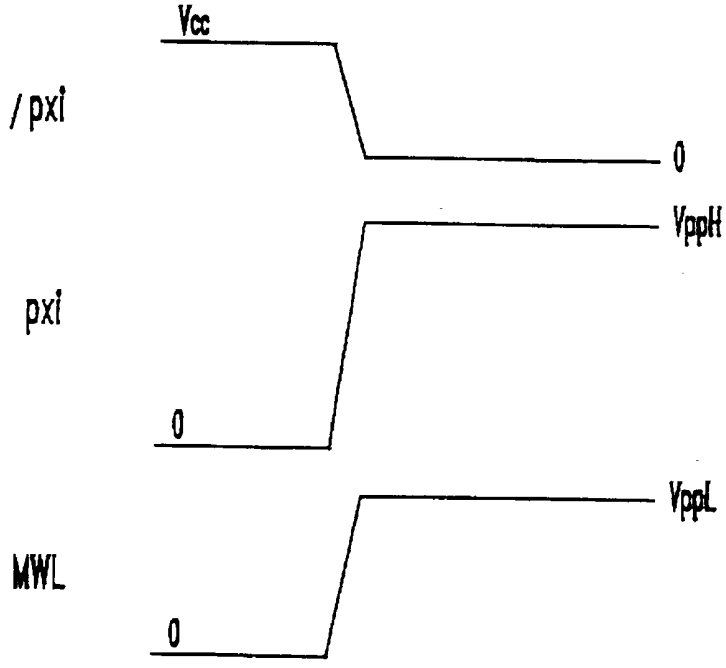

Fig . 8

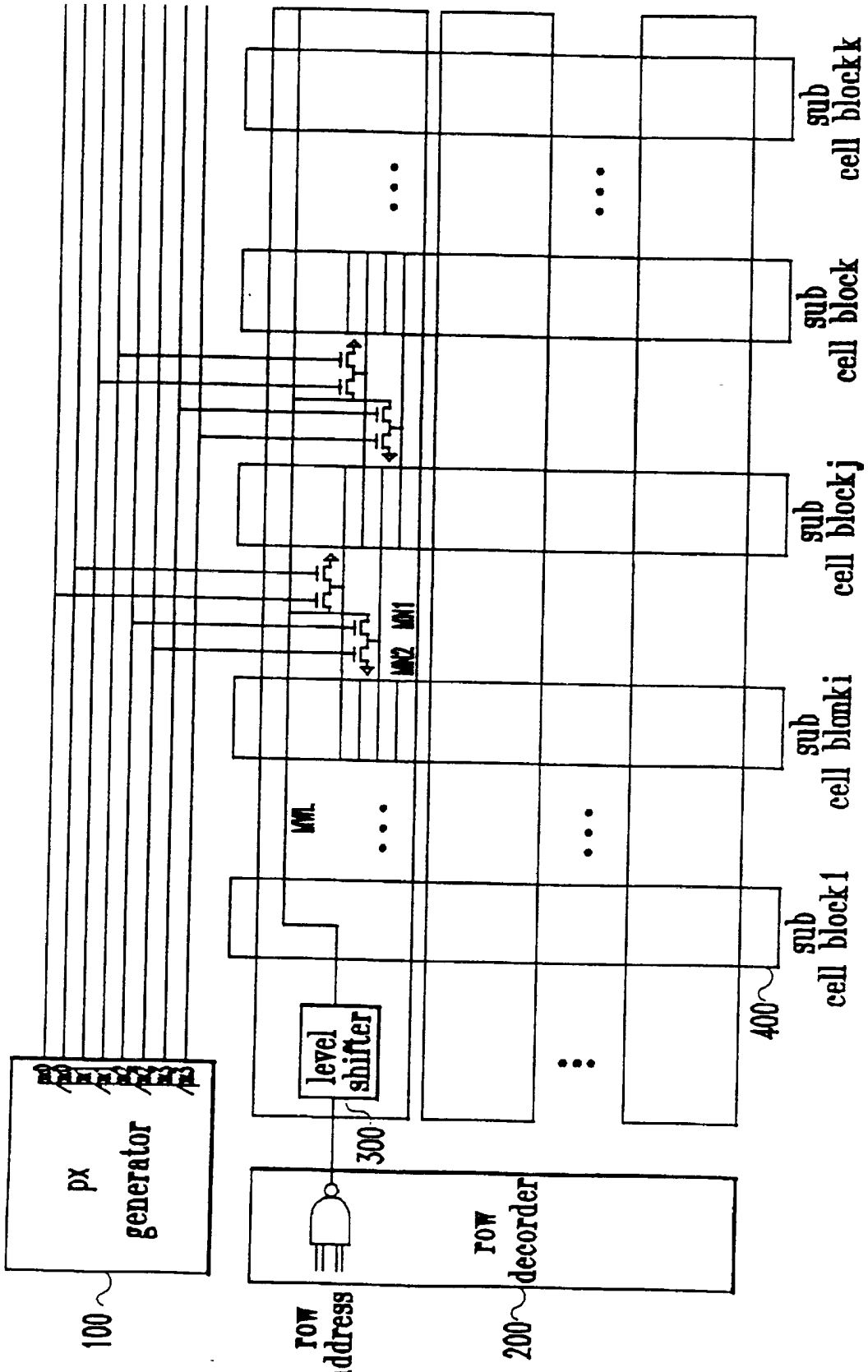
px generator
100
level shifter
300
row address
row decorder
200
400
sub cell block1
sub cell blockki
sub cell blockj
sub cell block
sub cell blockk
WL
WL2
WL1

FIG. 9

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A SEMICONDUCTOR MEMORY DEVICE

The present invention relates to a semiconductor memory device.

A hierarchical word line structure is generally used in semiconductor memory devices for relieving a strict metal design rule originated from a metal strapping of a word line. The metal strapping is performed such that, in order to reduce resistance of a word line formed of a poly-silicon, a metal line is arranged onto an upper portion of a cell array in a word line pitch and is then coupled to the word line of poly-silicon, thereby reducing the resistance of the word line to speed up driving time. (Here, the pitch refers the sum of a line width and a space in the regularly arranged lines.) In the metal strapping method, since the word line pitch is decreased along with the increase of the packing density of a memory device, a failure rate of the metal process is increased to thus reduce yield. Therefore, the hierarchical word line structure is necessarily applied from the class of 16M DRAM products.

A conventional sub word line driving circuit employed for the hierarchical word line structure is generally formed by three NMOS transistors, and the sub word line is driven by a high potential Vpp which is a boosted voltage level via a double bootstrapping process. This double bootstrapping process has a node applied with a considerably high voltage to adversely affect the reliability of the device. In addition, the delay required between driving signals lengthens the driving time. Furthermore, since the layout area of the sub word line driving circuit has a great influence upon the overall memory device, the layout is required to be as small as possible.

Figure 1 is a detailed circuit diagram showing the conventional sub word line driving circuit which includes a NMOS transistor MN3 coupled between a main word line MWL and a node N1 and supplied with a potential signal Vx (which is a DC voltage that typically equals Vcc) via a gate thereof. Also, a NMOS transistor MN1 coupled between a node N2 for receiving an operating signal px and a sub word line SWL has a gate coupled to node N1, and a NMOS transistor MN2 coupled between sub word line SWL and a ground voltage Vss has a gate coupled to a complement main word line /MWL.

Main pull-up transistor MN1 functions by pulling up sub word line SWL to the Vpp level (which is higher than a power source voltage within a memory chip), and pull-down transistor MN2 pulls it down to 0V (ground voltage). Also, NMOS transistor MN3 serves as a switch for maintaining the potential after node N1 is precharged and bootstrapped. That is, in almost all cases, Vx=Vcc and node N1 is precharged by V_x-V_t (where V_t is a threshold voltage) prior to activating px to Vpp after elapsing a predetermined time Td. Thus, node N1 is bootstrapped by a voltage more than Vpp-Vt, so that voltage Vpp of a signal px for selectively operating sub word line SWL is transferred to the sub word line unchanged via pull-up transistor MN1.

Figure 2 is a timing chart applied for driving the sub word line shown in Figure 1.

The conventional sub word line driving circuit has as much time as the predetermined time Td delay, and exerts a bad influence upon the reliability of pull-up transistor MN1 due to node N1 under transition to the higher voltage.

It is an object of the present invention to reduce some of the limitations and disadvantages of the known devices.

According to the present invention there is provided a semiconductor memory device including a cell array formed of a plurality of rows and columns, a row decoder and a column decoder for respectively selecting rows and columns in accordance with addresses,

with respect to a hierarchical word line structure having sub word line driving circuits numbering 2^m per sub word line group obtained by classifying respective cell arrays into n sub cell blocks in the column direction and classifying sub word lines of respective sub cell blocks 2^m, and main word line provided in the row direction,

wherein said semiconductor memory device comprises:

the row decoder for providing said main word line by receiving the row address of one portion;

word line boosting signal generating for receiving remaining row addresses numbering m as an input for producing word line boosting signal and word line boosting signal bar by 2^m; and

a plurality of sub word line driving means for driving said sub word lines in accordance with said word line boosting signal and word line boosting signal bar.

Embodiments of the present invention will hereinafter be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a detailed circuit diagram showing a conventional sub word line driving circuit;

Figure 2 is an operational timing chart of the sub word line driving circuit shown in Figure 1;

Figure 3 is a detailed circuit diagram showing a sub word line driving circuit of an embodiment of the present invention;

Figure 4 is an operational timing chart of the sub word line driving circuit shown in Figure 3;

Figure 5 shows an embodiment in which the sub word line driving circuit of Figure 3 is applied to the overall cell array;

Figure 6 shows a further embodiment in which the sub word line driving circuit of Figure 3 is applied to the overall cell array;

Figure 7 is a detailed circuit diagram showing a second embodiment of a sub word line driving circuit;

Figure 8 is an operational timing chart of the sub word line driving circuit of Figure 7; and

Figure 9 shows a further embodiment of the application of the sub word line driving circuit of Figure 7 to an overall cell array.

Figure 3 is a detailed circuit diagram showing a first embodiment of a sub word line driving circuit. Here, the circuit includes a NMOS transistor MN1 coupled between a node N2 for receiving a px potential and a sub word line SWL and having a gate coupled to a main word line MWL. Also, a NMOS transistor MN2 coupled between sub word line SWL and a ground voltage Vss has a gate coupled to a complement main word line /MWL.

The sub word line driving circuit is formed by two NMOS transistors MN1 and MN2, in which pull-up transistor MN1 serves the pull-up function for transmitting a voltage level of Vpp low VppL to sub word line SWL, and pull-down transistor MN2 pulls down sub word line SWL to 0V of ground voltage.

Figure 4 is an operational timing chart applied for driving the sub word line driving circuit shown in Figure 3. Different from the conventional sub word line driving circuit, there is no time delay between main word line MWL and complement main word line /MWL and signal px. In order to operate the circuit, boosted voltage levels of VppH and VppL are required. At this time, VppH is a voltage level required for activating the sub word line, and VppL is a voltage supplied to the gate of pull-up transistor MN1 for transmitting the VppL voltage of px to the sub word line unchanged (i.e. VppH > VppL + Vt).

Figure 5 shows the application of the sub word line driving circuit of Figure 3 to an overall cell array. Here, sub word lines SWL are classified as respective groups by four. In addition, since two main word lines MWL and complement word line /MWL metal line pass over the group of four sub word lines of poly-silicon, metal pitch is increased twice as compared with the conventional metal strapping method. A row decoder 200 receives a row address of one portion as an input for activating main word line MWL corresponding to the address signal. Main word line MWL selected in accordance with the row address is driven by VppH at 0V via a level shifter 300, and a px generator 100 receives two row addresses as inputs for driving only pxi (where i is a constant and $0 \le i \le 3$) of the corresponding address with VppL at 0V. Sub word line driving circuits 400 are placed on both sides of respective sub cell blocks i ($1 \le i \le n$).

Figure 6 shows an alternative embodiment in which the sub word line driving circuit of Figure 3 is applied to the overall cell array. In this arrangement, the metal pitch is increased four times over the conventional metal strapping method since every eight sub word lines SWL are classified as respective groups and two main lines MWL and complement main word line /MWL metal line pass over the eight sub word line groups of poly-silicon. Row decoder 200 receives the row address of one portion as an input for activating the main word line MWL corresponding to the address signal.

Main word line MWL selected in accordance with the row address is driven by VppH at 0V via level shifter 300, and px generator 100 receives three row addresses as inputs for driving only pxi (where i is a constant, and $0 \le i \le 7$) of

corresponding address with VppL at 0V. The sub word line driving circuits 400 are placed on both sides of respective sub cell blocks i (where $1 \leq i \leq n$).

Figure 7 is a detailed circuit diagram showing an embodiment of a sub word line driving circuit which includes a NMOS transistor MN1 coupled between main word line MWL and sub word line SWL and having a gate coupled to a true pxi potential line, and a NMOS transistor MN2 coupled between sub word line SWL and ground voltage Vss and having a gate coupled to complement /pxi potential line. Different from the circuit of the first embodiment, the circuit has no complement main word line /MWL signal, and the sub word line is driven by main word line MWL and two signals pxi and /pxi.

Figure 8 is an operational timing chart of the sub word line driving circuit shown in Figure 7. This circuit includes two NMOS transistors MN1 and MN2 as the first embodiment, in which pull-up transistor MN1 is on/off by the pxi signal, and serves the pull-up function for transmitting the VppL voltage of main word line MWL to sub word line SWL. Meantime, pull-down transistor MN2 is on/off by the /pxi signal, and pulls down the sub word line to 0V. The pxi signal has the voltage level of VppH on 0V when it is not activated, and main word line MWL has the voltage level of VppL on 0V.

Figure 9 shows a third embodiment in which the sub word line driving circuit of Figure 7 is applied to the overall cell array. Here, the metal pitch is increased four times over the conventional metal strapping method since four sub word lines are classified as respective groups, and a single main word line MWL metal line passes over four sub word lines of poly-silicon. Row decoder 200 receives a row address of one portion as an input to activate main word line MWL corresponding to the address signal.

Main word line MWL selected by the row address is driven by VppL at 0V via level shifter 300, and px generator 100 receives two row addresses for driving only pxi and /pxi (where i is a constant, and $0 \leq i \leq 3$) of corresponding address. At this time, pxi becomes VppH at 0V and /pxi becomes 0V at Vcc. Sub word line driving circuits 400 are placed on both sides of respective sub cell blocks i.

When a sub word line driving circuit as described above is embodied into VLSI products of Gigabit class, the sub word line is driven only by two NMOS transistors to decrease the overall area of the memory device. Furthermore, there is no time loss caused by delay between the driving signals which has been heretofore required in the bootstrapping process to involve high operating speed and to be favourable for a reliability aspect of the device.

Whilst the invention has been illustrated and described with reference to particular embodiments, it will be appreciated that various changes may be effected therein without departing from the scope of the invention as defined by the appended claims.

A sub word line driving circuit as described herein is described and claimed in our copending application No. 2307998 from which the present application was divided.

CLAIMS

1. A semiconductor memory device including a cell array formed of a plurality of rows and columns, a row decoder and a column decoder for respectively selecting rows and columns in accordance with addresses,

with respect to a hierarchical word line structure having sub word line driving circuits numbering 2^m per sub word line group obtained by classifying respective cell arrays into n sub cell blocks in the column direction and classifying sub word lines of respective sub cell blocks 2^m, and main word line provided in the row direction,

wherein said semiconductor memory device comprises:

the row decoder for providing said main word line by receiving the row address of one portion;

word line boosting signal generating for receiving remaining row addresses numbering m as an input for producing word line boosting signal and word line boosting signal bar by 2^m; and

a plurality of sub word line driving means for driving said sub word lines in accordance with said word line boosting signal and word line boosting signal bar.

2. A semiconductor memory device as claimed in Claim 1, wherein the references n and m signify natural numbers.

3. A semiconductor memory device as claimed in Claim 1 or Claim 2, wherein said main word line is driven by a ground potential and a low logic level of high potential, and

said word line boosting signal is driven by said ground potential and a high logic level of high potential.

4. A semiconductor memory device as claimed in any preceding claim, wherein said 2^m word line boosting signal and word line boosting signal bar are commonly shared by said plurality of word line driving means.

5. A semiconductor memory device as claimed in any preceding claim, wherein said sub word line driving means comprises:

pull-up driver coupled between said main word line and sub word line, and having a gate coupled to said word line boosting signal potential; and

pull-down driver coupled between said sub word line and ground voltage, and having a gate coupled to said word line boosting signal bar potential.

6. A semiconductor memory device as claimed in Claim 5, wherein said pull-up driver and pull-down driver are comprised of MOS transistor.

7. A semiconductor memory device as claimed in Claim 6, wherein said MOS transistor is a NMOS transistor.

8. A semiconductor memory device as claimed in Claim 6 or Claim 7, wherein said pull-up driver is comprised of a transistor having a threshold voltage smaller than a threshold voltage of another transistor.

Application No: GB 0015127.4 **Examiner:** Brian Ede
Claims searched: 1-8 **Date of search:** 1 August 2000

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.R): G4C(C800C, C800L, C11408C)

Int Cl (Ed.7): G11C 8/08 8/14 11/4094

Other: Online: EPODOC, JAPIO, WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
A	EP 0600184 A1	(NIPPON ELECTRIC) see Fig 1	
A	WO94/17554A1	(OKI ELECTRIC) see Figure 4	
AP	US 5506816	(NVX CORPORATION) 9.4.96 see Figures 6 and 7	
A	US 5148401	(OKI ELECTRIC) see 20-11, 20-12 Figure 3	
A	US 4554646	(MITSUBISHI) see 15, 21, 22 Figures 7 and 8	

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