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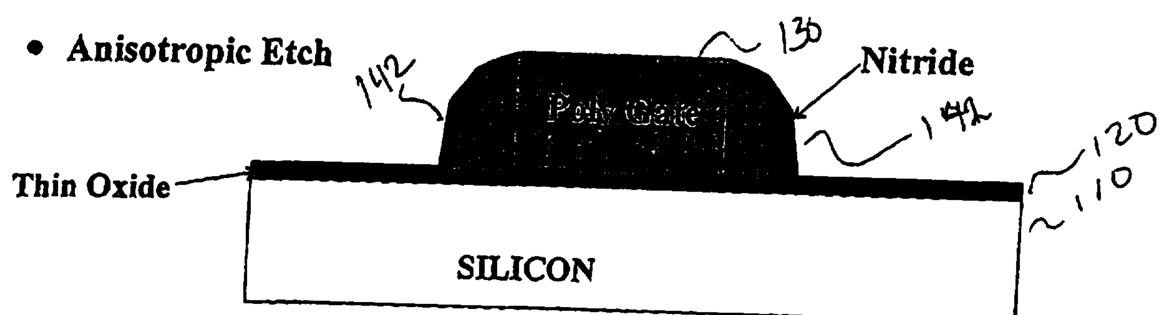

(57) Abstract

In a method for anisotropically and selectively etching a nitride layer in a semiconductor device having a layer of nitride overlying a layer of oxide on a silicon substrate, first, the substrate is placed between the upper electrode and the lower electrode of a reactive ion etching device. Then, the etching process is commenced. The endpoint of the etch is determined by measuring the change in voltage between the upper and lower electrodes. The etching process is terminated some time after determining that the chaange in the measured voltage is approximately equal to zero. The change in the measured voltage is approximately equal to zero when the layer of nitride is completely etched from the layer of oxide.

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PROCESS FOR THE ANISOTROPIC AND SELECTIVE DRY ETCHING OF NITRIDE OVER THIN OXIDES

Field of the Invention

5 The present invention relates to semiconductor devices and, in particular, to integrated circuit fabrication processes in which selective etching of nitride over oxide is needed to form transistors.

Background of the Invention

It is known in the prior art to provide layers of oxide and nitride over silicon substrates to act as insulators. It is also known in the prior art to selectively etch certain portions of the nitride and oxide 10 layer in order to provide contact openings for the formation of transistors and for the formation of spacers.

An example of a process known in the prior art will be described in connection with Figures 1 and 2. As shown in Figure 1, a silicon substrate 10 is covered with a layer of thin oxide 20, according to processes well known in the art. Similarly, a polysilicon gate 40 is formed on top of the thin oxide layer 15 20. A layer of silicon dioxide (SiO_2) 30 is deposited conformally over gate 40 and thin oxide layer 20. SiO_2 layer 40 is then anisotropically etched, using methods known in the prior art for endpoint detection, to form the spacers shown in Figure 2.

As shown in Figure 2, thin oxide layer 20 is completely removed during the step of etching the spacers. As a result, damage often occurs to the silicon contact area and to the gate oxide due to 20 overetching.

The damage to silicon occurs because of the etching processes used to selectively etch oxide on silicon. The etching processes must use gas chemistries which selectively etch oxide on silicon. To achieve a high oxide etch rate and a low silicon etch rate, the following gas mixtures are typically used: $CF_4 + H_2$, $CHF_3 + O_2$, and $CHF_3 + C_2F_6$. The etch selectivity is achieved by the creation of polymers 25 on the bare silicon surfaces which result from the presence of hydrogen. The silicon areas are damaged by surface contamination due to the presence of the polymers. There is also physical damage extending up to several hundred angstroms from the surface. Finally, the presence of hydrogen can often lead to boron (B) neutralization. Boron neutralization in turn negatively affects silicon resistivity, thereby making it more susceptible to damage. The damage to the gate oxide occurs for many of the same 30 reasons (physically and by contamination).

Summary of the Invention

The present invention is directed to an improved method for realizing spacers and contacts for MOS and bipolar devices. The problems associated with the prior art are overcome by providing a layer of nitride over a layer of oxide and then anisotropically etching the nitride selectively to oxide. The 35 process used is characterized by its manufacturability and by the low damage that results.

According to the present invention, in a semiconductor device having a layer of nitride overlying a layer of oxide on a silicon substrate, the nitride layer is anisotropically and selectively etched as follows. The substrate is placed between an upper and a lower electrode of a reactive ion etching device. An etching process is then commenced using chlorine gas. The voltage present at the lower electrode after a 40 first predetermined time following the commencing of the etching process is measured. Finally, the etching process is stopped after a second predetermined period of time passes after determining when a

change in the measured voltage is approximately equal to zero (ie., the slope of a curve plotting voltage to time is approximately equal to zero). The change in the measured voltage is approximately equal to zero when the layer of nitride is completely etched from the layer of oxide.

5 These and other aspects and advantages of the present invention will become apparent in view of the Figures and the detailed description of the preferred embodiments.

Brief Description of the Drawings

Figures 1 and 2 illustrate examples of structures known in the prior art resulting from processes practiced in the prior art.

Figure 3 illustrates a block diagram of a device used according to a preferred embodiment of the
10 present invention.

Figure 4 illustrates a structure formed, at an intermediate step, according to a first embodiment of the present invention.

Figure 5 illustrates a structure formed, after an anisotropic etching step, according to a first embodiment of the present invention.

15 Figure 6 illustrates a structure formed according to a second embodiment of the present invention.

Figure 7 illustrates an endpoint trace of nitride on oxide showing voltage plotted as a function of time.

Detailed Description of the Preferred Embodiments

The present invention is directed to a method for reliably fabricating self-aligned nitride spacers for
20 the realization of advanced devices. Such devices include complementary bipolar and complementary BiCMOS technologies as well as MOS transistors with elevated sources and drains. Nitride spacers are preferred to oxide spacers for a number of reasons. First, there is no spacer thinning during a post spacer formation step of wet cleaning using hydrogen fluoride (HF). Second, there is no risk of overetching because the etch is stopped on the underlying silicon oxide. Third, there is no need for a
25 polymerizing etch process which can introduce contaminants onto the surface of the substrate. Finally, there is no need to use etching chemistries having hydrogen, which causes boron neutralization, silicon damage and increases silicon contact resistance.

The key process requirements satisfied by the present invention are now discussed. First, anisotropic etching is required for self-aligned vertical spacers. Second, selectivity of the etching process
30 to thin oxides is required to minimize device damage and to eliminate the risk of underlying silicon over-etching. Preferably, a minimum 2:1 selectivity is achieved for Si_3N_4:SiO_2, with loss of oxide being less than 150 angstroms. Third, manufacturability must be provided by a high throughput of greater than 20 wafers/hour, and with better than 5% uniformity. Fourth, the process must be simple so that complex gas mixtures and custom equipment are not required. Fifth, there must be low damage, so low frequency
35 plasmas and magnetic fields must be avoided. Finally, the process must be scalable to any wafer size so ECR plasma sources must be avoided so that different size magnets need not constantly be inserted for different size wafers.

A first embodiment of the present invention is illustrated by Figures 4 and 5. This embodiment will now be discussed in detail.

40 As shown in Figure 4, a silicon substrate 110 is covered by a thin oxide layer 120. A gate electrode 130 is formed on top of the thin oxide by using a photoresist layer (not shown). Finally, a layer of silicon nitride 140 is conformally deposited over the gate 130 and the thin oxide layer 120. The

silicon nitride layer 140 is subsequently etched in a novel manner according to the present invention, thereby resulting in the structure shown in Figure 5.

As shown in Figure 5, silicon nitride layer 140 has been selectively and anisotropically etched to result in spacers (shown as 142) which surround the gate electrode 130. By using the novel etching method of the present invention, the thin oxide is left intact and any overetching into the thin oxide is controlled.

The novel etching method with endpoint detection according to the present invention will now be described in conjunction with Figure 3. Figure 3 illustrates an overall block diagram 50 of the etching process using an etching apparatus manufactured by Drytek (now owned by LAM Research, Inc.), and known as the TRIODE 384T. Preferably, this etching apparatus is operated by a 13.56 MHz single power source at 300 watts. Although this particular etching apparatus is disclosed, other equivalent etching apparatuses may be used along with the novel method disclosed herein. The etching apparatus is provided with a lower electrode 60, a grounded electrode 62 and an upper electrode 64. A wafer (or substrate) 55 is placed upon the lower electrode 60 so that the selective, anisotropic etching of the silicon nitride (ie. layer 140 of Figure 4) may be performed. In operation, a plasma is generated between the upper and lower electrodes 64 and 60. The grounded electrode 62 is provided with holes (not shown) so that the plasma may freely pass through the electrode. The portion of the plasma above grounded electrode 62 is referred to in Figure 3 as remote plasma 70, while the portion of the plasma below grounded electrode 62 is referred to as reactive ion etching (RIE) plasma 72.

The etching is manufacturably performed using only one gas, chlorine (Cl_2). This is possible because only one film, nitride, is being etched. One advantage of using only Cl_2 gas is that no polymers are created because only the nitride layer is being etched and no photoresist is being used. Another advantage is that only one flow needs to be controlled, as opposed to most etching processes in which a plurality of gases are simultaneously used. The Cl_2 gas is used at 100 sccm (standard cubic centimeters per minute). The anisotropic etching process operates at 90 mTorr (this refers to the pressure of a gas inside a chamber in which the etching takes place).

A voltmeter 80 is coupled with the lower electrode 60 and measures the DC bias between lower electrode 60 and grounded electrode 62. The voltage measured is a function of the gas used as well as the species that are present in RIE plasma 72. During the etching process, the content of the different species within the RIE plasma 72 changes. This changes the conductance of the plasma. Since the power is constant, the voltage measured by voltmeter 80 also changes.

The inventors of the presently disclosed subject matter have discovered that the DC bias voltage measured during the etching process changes significantly once the thin oxide layer 120 is reached. Figure 7 graphically illustrates this relationship. The voltage proportional to DC bias is plotted on the horizontal axis and time is plotted on the vertical axis. As shown in Figure 7, voltmeter 80 is not turned on until a certain time period has passed (namely, t_1-t_0). This time period is variable and is provided mainly to permit the RIE plasma 72 to stabilize. Once voltmeter 80 begins taking measurements (ie., at time t_1), it can be seen that, as the silicon nitride layer 140 is being etched, the voltage is increasing. At time t_2, nitride layer 140 has been completely etched away from the substrate, except for spacers 142. As the etching process is continued, the voltage decreases from time t_2.

Therefore, by monitoring the voltage, endpoint detection can be simply and reliably accomplished. For example, the etching may be discontinued once the slope of curve 300 is equal to zero (ie. at time t_2, and at voltage V_1). Or, if desired, a controlled amount of overetching can be performed until a time such as t_3 to ensure complete removal of unwanted nitride.

The graph depicted in Figure 7 shows the results of a test performed on a wafer having a layer of oxide 300 angstroms thick. A layer of nitride was deposited using low pressure chemical vapor deposition (LPCVD) to a thickness of 3500 angstroms. The etching process is shown with a 10% overetch. The "10% overetch" refers to a 10% increase in the etching time as calculated from the overall
5 time used in the etching process to remove the nitride layer.

A second embodiment of a structure resulting from practicing the above-mentioned endpoint detection process is shown in Figure 6. This embodiment entails the formation of contact portions on a substrate. As shown in Figure 6, a layer of thin oxide 220 and a layer of silicon nitride 230 are deposited over a silicon substrate 210. Unlike the embodiment of Figures 4 and 5, a photoresist layer
10 240 is used to define contact portion 250. However, the same endpoint detection process can be used to etch the silicon nitride layer 230 until thin oxide layer 220 is reached. Thus, etching of the underlying silicon substrate 210 is minimized or avoided entirely.

Although the present invention has been described with particular reference to the preferred embodiments, one of ordinary skill in the art would be enabled by this disclosure to make various
15 modifications and still be within the scope and spirit of the present invention as defined in the appended claims.

What is Claimed is:

1. A method of anisotropically and selectively etching a nitride layer overlying a layer of oxide formed on a silicon substrate, the method comprising the steps of:
placing the substrate between an upper and a lower electrode of a reactive ion etching device;
5 commencing an etching process;
measuring a voltage present at the lower electrode at predetermined increments of time after a first predetermined time following the commencing of the etching process; and
stopping the etching process a second predetermined period of time after determining when the endpoint is reached, wherein it is determined that the endpoint has been reached when a change in the
10 measured voltage between two of the predetermined increments of time is approximately equal to zero, and wherein the change in the measured voltage is approximately equal to zero when the layer of nitride is completely etched from the layer of oxide.

2. The method according to claim 1, wherein the first predetermined period of time is dependent upon how much time is needed for plasma used in the etching process to stabilize.

15 3. The method according to claim 2, wherein the second predetermined period of time is dependent upon how much overetching is desired.

4. The method according to claim 1, wherein the etching process is carried out using chlorine gas.

5. A method of forming a nitride spacer around a gate electrode comprising the following sequence of steps:
20 providing a layer of oxide on a silicon substrate;
forming a gate electrode over the layer of oxide;
depositing a layer of silicon nitride over the entire substrate using low pressure chemical vapor deposition; and
performing an anisotropic etch of the layer of silicon nitride with an endpoint on the layer of oxide
25 to form the nitride spacer around the gate electrode, wherein the anisotropic etch is performed within an etching apparatus having at least two electrodes and wherein the endpoint is determined by evaluating a change in voltage as measured between the two electrodes.

6. The method according to claim 5, further comprising the step of performing an overetch for a predetermined period of time after the endpoint has been determined.

30 7. The method according to claim 6, wherein the anisotropic etch is performed in the presence of chlorine gas.

8. A method of anisotropically and selectively etching a nitride layer overlying a layer of oxide formed on a silicon substrate, the method comprising the steps of:
forming the oxide layer on the silicon substrate;
35 forming the nitride layer on the oxide layer;
forming a layer of photoresist on the nitride layer;
patterning the photoresist to expose selected surface regions of the nitride layer;

placing the structure defined by the preceding steps between an upper and a lower electrode of a reactive ion etching chamber;

commencing an etching process in the reactive ion etching chamber;

measuring voltage present at the lower electrode at predetermined increments of time after a first
5 predetermined period of time following commencement of the etching process;

determining that an endpoint has been reached when a change in the measured voltage between two of the predetermined increments of time is approximately equal to zero; and

stopping the etching process a second predetermined period of time after it has been determined that the end point has been reached.

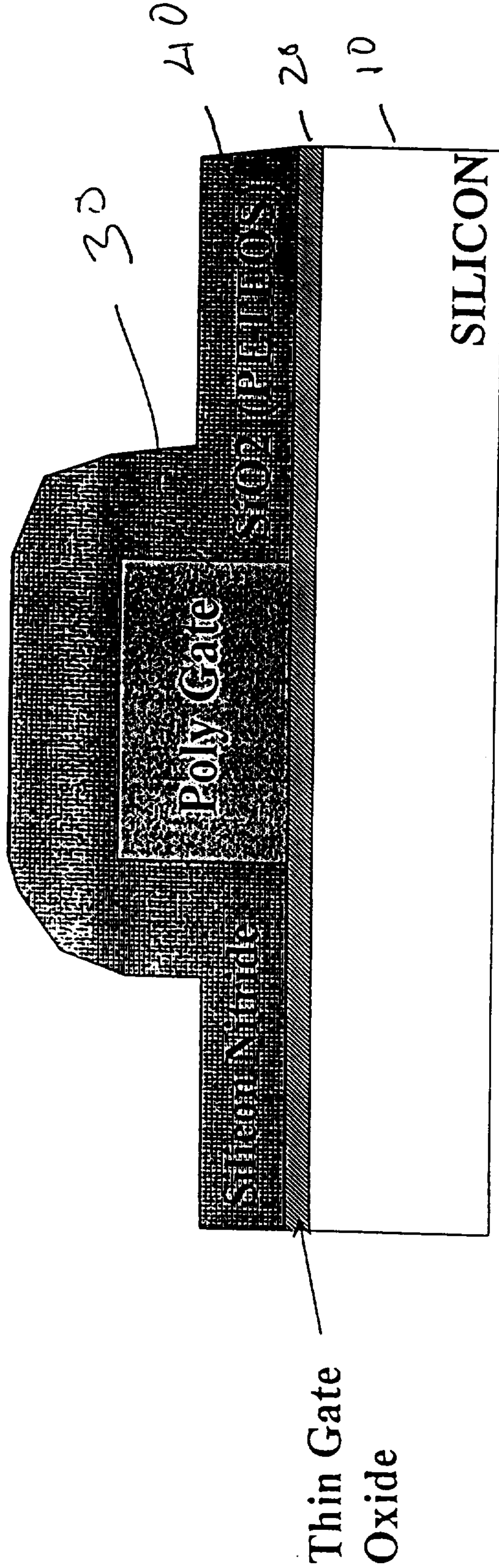


FIG. 1

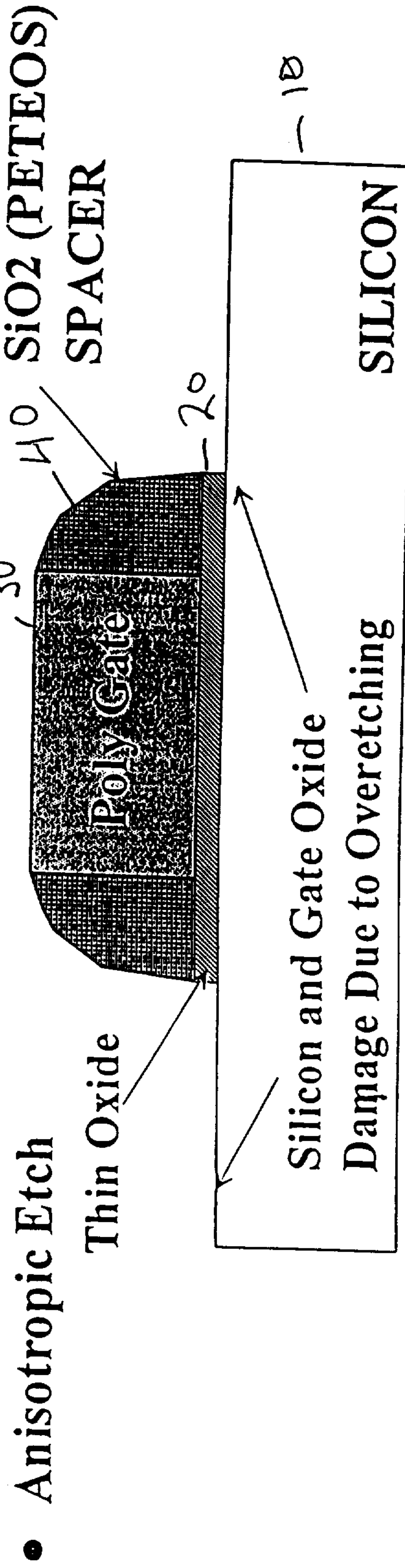


FIG. 2

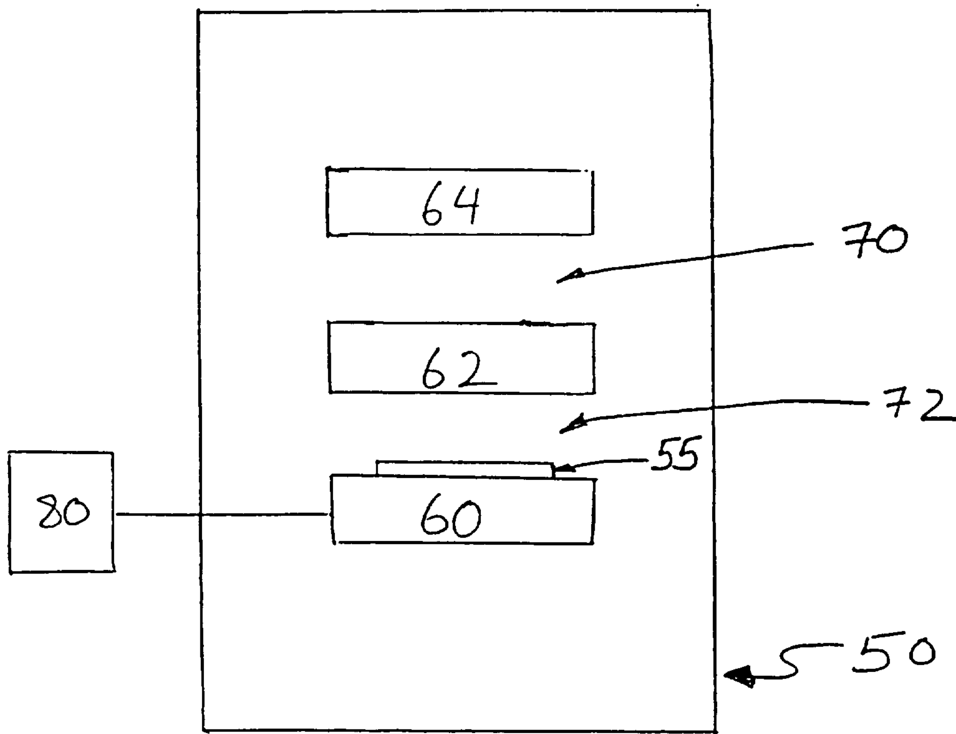
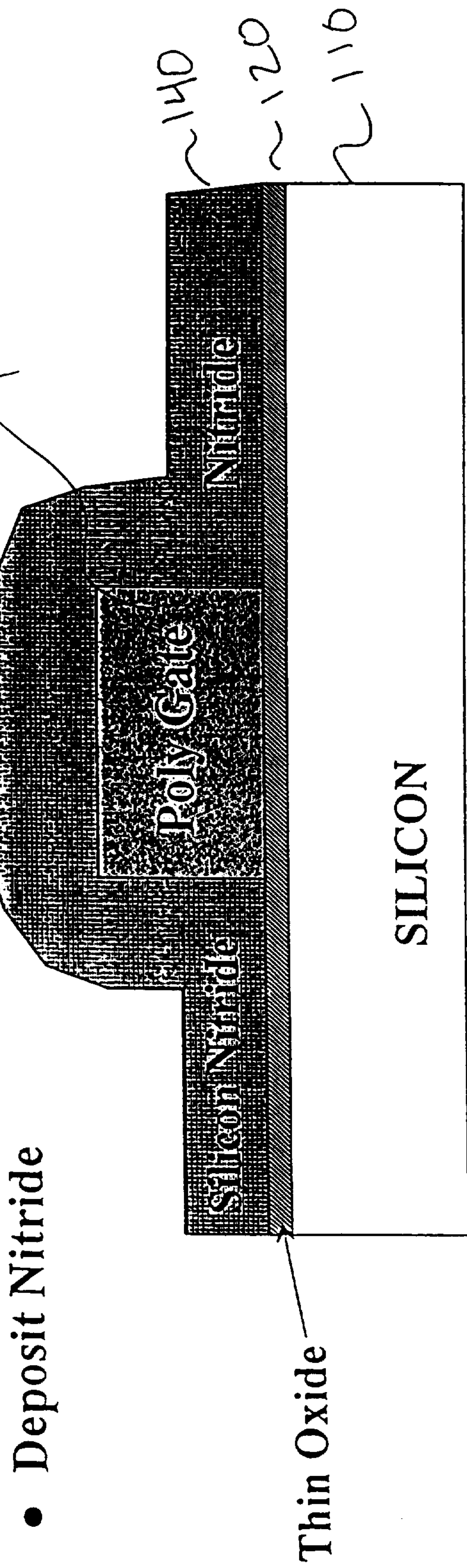
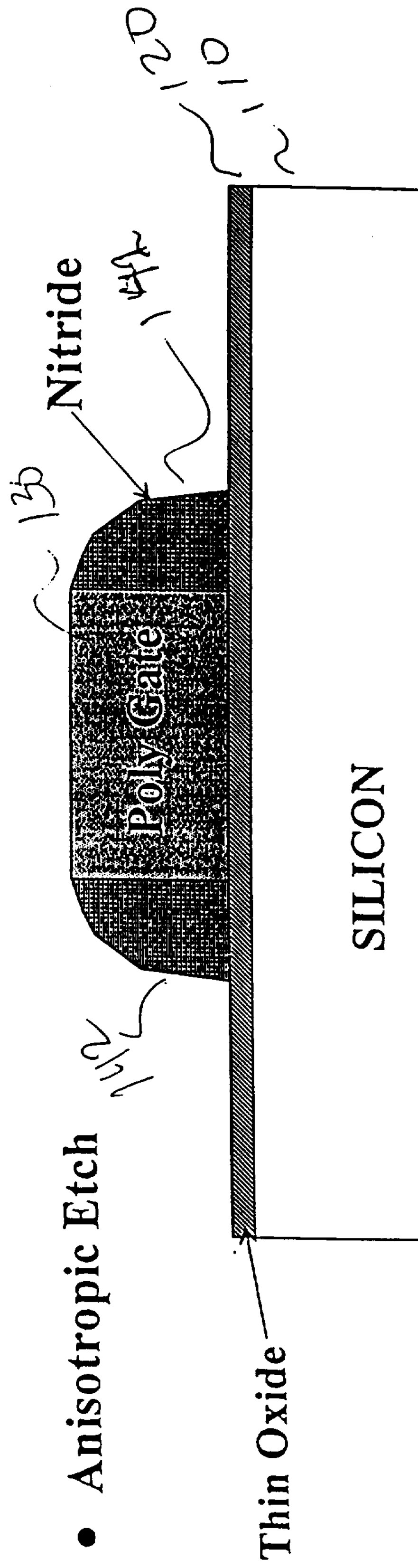


FIG. 3


• Deposit Nitride
Silicon Nitride
Poly Gate
Nitride
SILICON
Thin Oxide
140
120
110
130
FIG. 4


• Anisotropic Etch
Nitride
Poly Gate
SILICON
Thin Oxide
142
130
120
110
FIG. 5

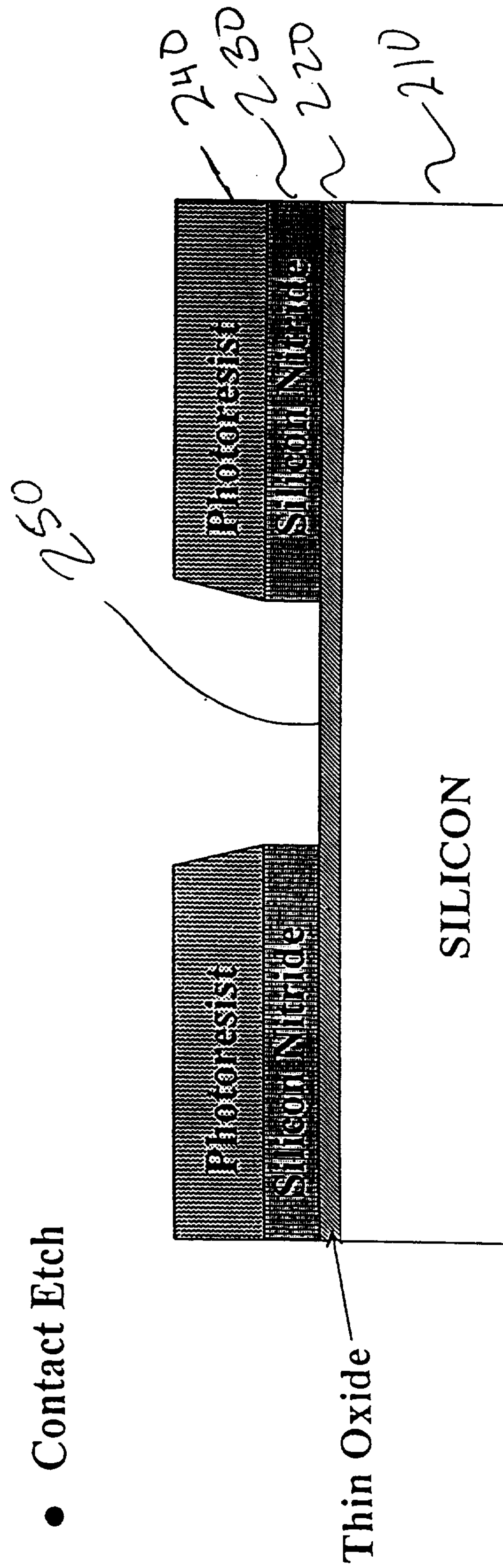


FIG. 6

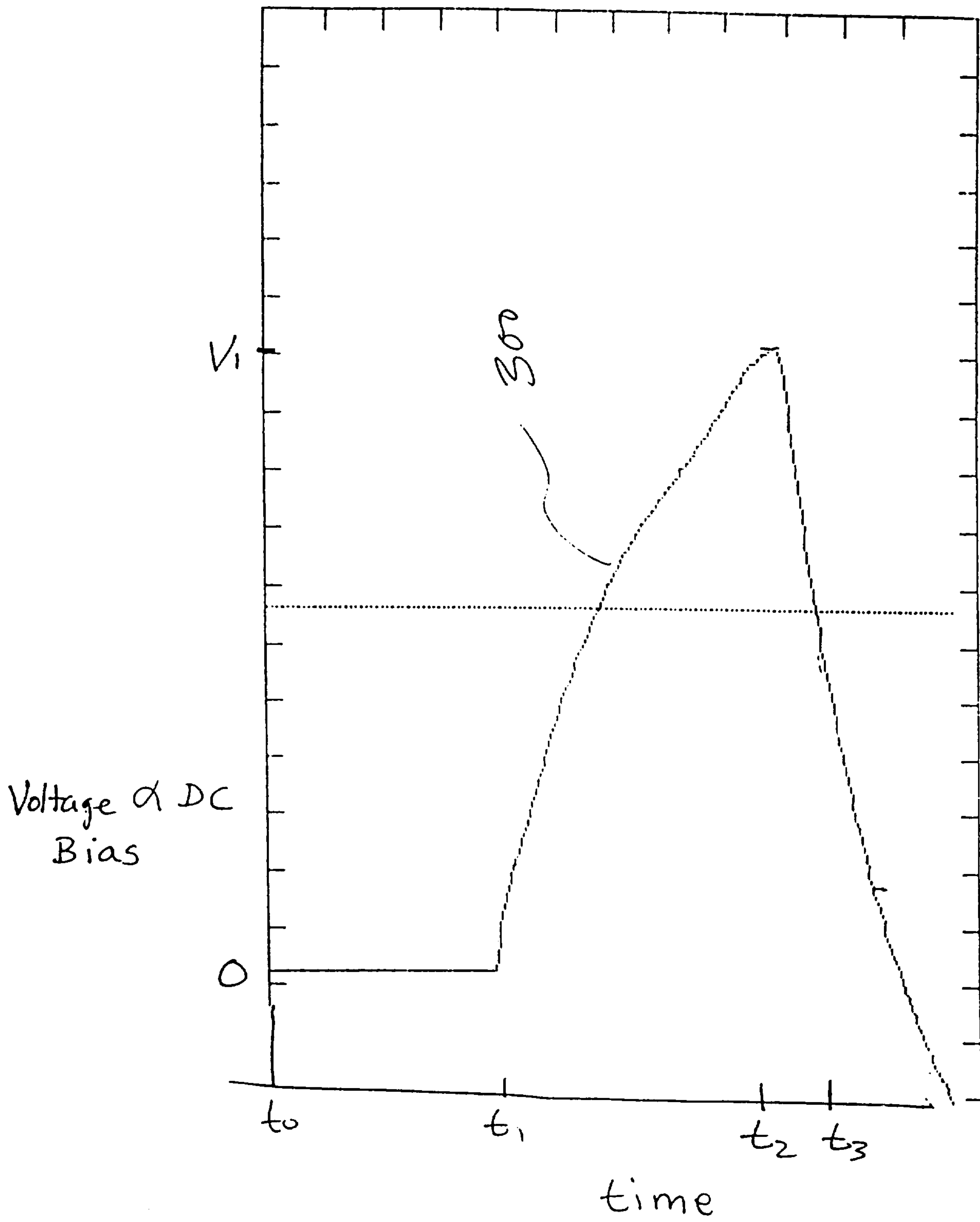


FIG. 7