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(71) Applicant
The Marconi Company Limited, Marconi House, New Street, Chelmsford, Essex CM1 1PL
(72) Inventors
Gyöngyver Claydon,
Gordon David Iles
(74) Agents
Roger Tolfree

(54) Apparatus and Method for Processing Television Picture Signals and Other Information

(57) Information is written into and read from a buffer memory 16 in response to independent write C and read D signals respectively, the write signals being selectively delayed to prevent them coinciding with the read signals.

Video signals are converted 2 to digital and passed through a serial-to-parallel converter 17 to the memory 16, the write signals C being derived from the video signal. Read signals D from a local source read data from the memory 16 through a parallel-to-serial converter 18 and digital-to-analogue converter 19. The write signal delay 9A, 11A is variable so as to position each write signal midway between adjacent read signals. An additional fixed delay may operate on the write signals following each blanking period. The video signals may also be delayed 9B, 11B, by the same amount as the write signals.

The drawings originally filed were informal and the print here reproduced is taken from a later filed formal copy.

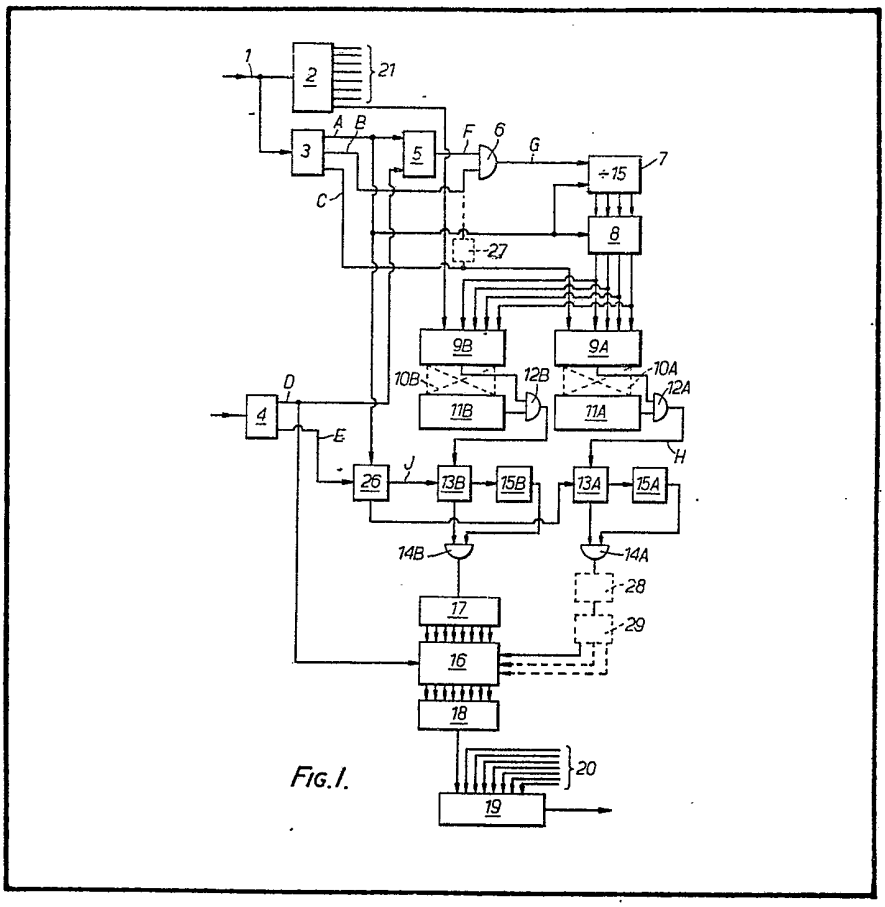

FIG. 1.

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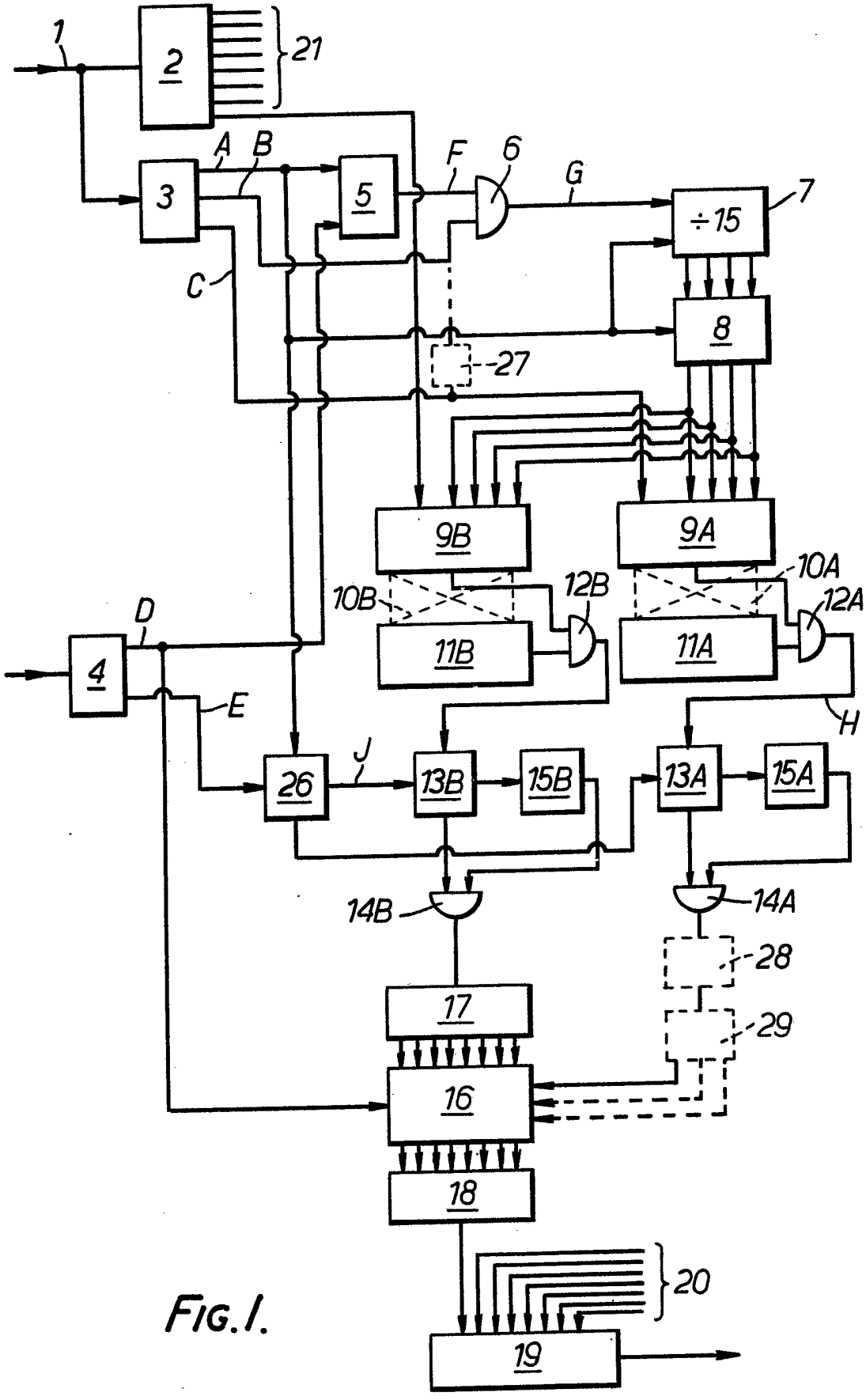
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E
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14A
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FIG. 1.

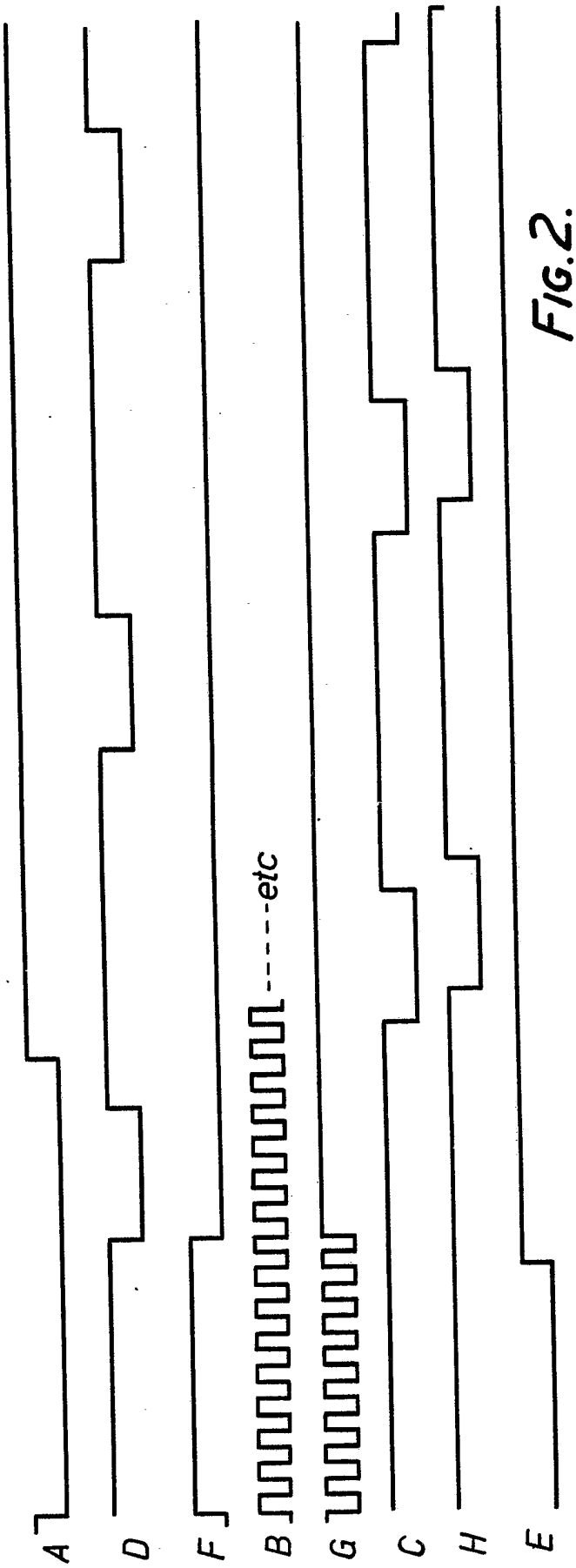

FIG. 2.

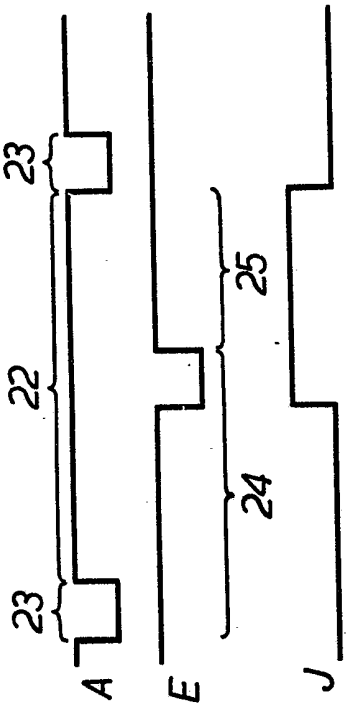

FIG. 3.

SPECIFICATION

Apparatus and Method for Processing Television Picture Signals and Other Information

This invention relates to apparatus for processing information and was conceived when designing a picture synchronisation system for television signals.

Many forms of television picture processing depend for their operation upon the storage of one or more fields of the signal. Examples of types of picture processing which employ storage are: standards conversion; picture synchronisation; noise reduction; and picture size reduction and expansion.

Picture storage can be carried out using analogue methods, the use of quartz delay lines being an example of this type of storage. However, digital memories are cheaper, more reliable and more compact and most equipment employing picture storage now uses digital semiconductor memory chips with the television signal being converted from analogue-to-digital form at the input of the equipment and back to analogue at the output.

This invention is particularly, although not exclusively, applicable for use in a picture synchroniser. The purpose of a synchroniser is to re-time a television signal, e.g. one arriving from an outside broadcast, so that its subcarrier, line and field frequencies are identical to some local reference, e.g. the studio camera pictures. At the output of the synchroniser the remote signal can be treated as if it were generated locally and can be mixed, faded, and inserted into local pictures without causing timing disturbance to the transmitted signal.

A typical known synchroniser works by writing the incoming signal into the memory at a rate determined by the incoming signal and then reading the signal out of the memory at the rate fixed by a local reference signal. Since there is no frequency or phase relationship between the reading and writing operations, there will be occasions when the reading will overtake the writing or vice-versa. Also there will be occasions when reading and writing operations coincide.

It is a feature of most random access memory systems that, at any instant, only one memory location may be addressed, and that information may be written into or read from the chosen location, but not both together. One known method of overcoming the need for simultaneous writing and reading within a memory chip is to provide storage additional to that strictly needed for one field of the picture. In this way, when an attempt is made to read from and write into the memory at the same time; one of the operations, e.g. writing, is transferred to an additional memory. This known method suffers from the disadvantage that substantial additional memory is required.

This invention provides an information processing apparatus comprising a memory, means for writing information into the memory at times depending on first timing signals, means for reading the information out of the memory at times depending on second timing signals whose timing may be the same as or different to the first signals, and delay means for delaying at least some of the writing times so that they do not coincide with the reading times.

The invention also provides a method of processing information comprising writing the information into a memory at times depending on first timing signals, reading the information out of the memory at times depending on second timing signals whose timing may be the same as or different to the first signals, and delaying at least some of the writing times so that they do not coincide with the reading times.

Thus, the read and write operations are 'interleaved', i.e. the memory is addressed in a read-write-read etc. sequence and no additional memory is required.

In systems where the first and second timing signals have different timings, the writing times are preferably delayed by varying amounts, chosen so that each writing time is approximately mid-way between reading times.

Since it may be necessary to write information into and read information from the memory at a very fast rate it is preferable to include a serial-to-parallel converter at the input to the memory and a parallel-to-serial converter at the output. This allows the memory sufficient time to register each bit.

When the invention is used in a synchroniser for television signals, the said 'first' timing signals are preferably generated from the line synchronising pulses, the field synchronising pulses and the first of the signals to be processed, whereas the 'second' timing signals are generated similarly from an independent source. In this particular application of the invention the frequencies of the first and second timing signals are marginally different. This means that they drift into and out of phase with each other. When they are in phase the delay produced in accordance with the invention avoids the memory being instructed to read and write simultaneously. When they are 180° out of phase there is no need for delay.

The change in phase of the 'first' and 'second' timing signals in a television sychroniser is very small during any given line. It is, therefore, satisfactory to set a delay time which remains constant during any given line of the signal to be processed.

The blanking periods, between lines of the video information being read out of the memory are not normally equal to a multiple of the period between reading times. This means that the delay, fixed for a given line of the signal to be processed is inappropriate after the blanking period of the signal being read out of the memory. This problem can be overcome by delaying the writing times by a further fixed amount after the blanking period.

In some other applications of the invention the first and second timing signals can be the same in which case the delay will be a fixed value, permanently present. Such would be the case for example in picture size reduction systems and noise reduction systems for television signals.

A particular embodiment of the invention will now be described, by way of example, with reference to the accompanying drawings in which:—

Figure 1 is a block diagram showing, in full lines, a television picture synchronisation device designed to synchronise television signals derived from somewhere outside a studio with signals generated locally, i.e. in the studio; and, in broken lines, a modification applicable when the memory requires more than one write clock.

Figure 2 shows waveforms A, B, C, D, E, F, G and H which are generated at various positions, also indicated on Figure 1 by the same reference letters; and

Figure 3 shows waveform A of Figure 2 but on a smaller time scale, and also waveforms E and J on the same (smaller) time scale.

The circuit of Figure 1 is designed for use in a television studio and the object is to synchronise a video television signal derived from a remote source with timing signals produced locally in the studio.

The remote signal is received by an input 1 and is digitised by an analogue-to-digital converter 2 into 8-bit parallel form, samples being taken at a frequency of three times the frequency of the subcarrier (3 fsc). This video input 1 also drives a timing generator 3 that produces first timing signals constituting line frequency pulses A, 3fsc clocks B, and write clock pulses C. The write clock pulses C are started by line pulses A and have a period of repetition which is a predetermined number of periods of the 3fsc clocks B. In the described embodiment this is fifteen times the period of the 3fsc clocks. Local pulses generated within the studio pass through a second timing generator 4, similar to generator 3. The generator 4 produces second timing signals constituting line pulses E and read clock pulses D. These are similar to A and C respectively, but are not locked to the remote signal.

A comparator 5 compares the phase of the remote line pulses A relative to local read clock pulses D and produces a signal F which opens a NAND gate 6 to pass 3fsc clock pulses B during a period between the beginning of a pulse A and the beginning of the next pulse D. The number of clock pulses B passed by the gate 6 during this period is a measure of the relative timing of pulses A and D. A divide-by-fifteen counter 7 counts the clock pulses G passed by the gate 6 and the number contained in the counter when the clocks stop is stored in a latch 8 for the duration of a television line. The counter 7 is cleared on each line just before the gate 6 is enabled. Figure 2 shows a situation where the time difference between the beginning of a pulse A and the beginning of the next pulse D is such that nine clock pulses G are passed to the counter 7. The output of the counter 7, which is in four-bit parallel form, is held for one line period in the latch circuit 8, and the output of the latch circuit is fed to two identical selectors 9A and 9B.

The selector 9A feeds each write clock pulse C to a selected one of fifteen output connections 10A. These connections 10A are connected to respective inputs of a fourteen-bit shift register 11A so as to produce pulses H which are similar to pulses C, but are delayed in accordance with the following table:—

Count held by latch circuit 8	*Delay produced by shift register (No. of periods of clock signal B)*
0	7
1	8
2	9
3	10
4	11
5	12
6	13
7	14
9	1
10	2
11	3
12	4
13	5
14	6

When a count of eight is held by the latch circuit 8 the selector 9A feeds the pulses C to one particular output which is connected directly to an OR gate 12A. This means that the pulse H is produced simultaneously with a pulse C; i.e. there is no delay.

The effect of the delays caused by the circuits 7, 8, 9A, 10A, 11A and 12A is to delay the write pulses C by a time such that the leading edges of the delayed write pulses H are approximately half-way between the leading edges of the read clock pulse D. The delay is reset for each line of the remote video signals but, except for a fixed adjustment produced by circuits 13A, 14A and 15A to be described later, remains constant during each line.

The delayed write pulses from the gate 14A are fed to the "write clock" input of a random access memory circuit 16. The circuits 28 and 29, shown in broken lines, are not included in this particular embodiment of the invention. They will be referred to later in relation to a modification. Each write pulse enables the memory to receive video information from a serial-to-parallel converter 17.

The video information from one output of the analogue-to-digital converter 2 is delayed in exactly the same way as the "write pulses", but by separate circuits 10B, 11B, 12B, 13B, 14B and 15B. These are identical to circuits 10A, 11A, 12A, 13A, 14A and 15A.

The delayed signals, representing one output of the analogue-to-digital converter 2 cannot be fed directly to the memory 16 since they occur at a

frequency of 3fsc which is too fast to register in the memory. They are, therefore, converted by circuit 17 into 15-bit parallel form before being entered in the memory 16.

The remote video information stored in the memory 16 is read out by the read clock signal D derived from the local video signal and, therefore, the output from memory 16 is synchronised with the local video signal. Because of the delay introduced by the circuitry, the memory is never required to read and write simultaneously.

The output from the memory is passed to a parallel-to-serial converter 18 and thence to a digital-to-analogue converter 19. The latter also receives, through inputs 20, the outputs from seven other circuits, identical to that illustrated, which process signals from the seven other outputs 21 of the analogue-to-digital converter 2.

The output of the digital-to-analogue converter 19 represents the remote picture signal synchronised with the locally generated signal.

Figure 3 shows at A and E respectively the blanking periods of a line of the remote video signal (before the delay) and of a line of the local video signal. It should be noted that the blanking period shown at E of the local video signal is exactly the same as the blanking period of the remote signal withdrawn after processing from the memory 19. The picture signals of the remote signal occupy a part 22 of the line during which 765 samples are taken from the analogue-to-digital converter 2. The blanking period 23 occupies 86.25 sample periods. The signal E is similar, but its blanking period may, and normally will, occur during the picture part of the remote signal. Since the delay to the individual samples of the remote signal is set by the latch circuit 8 for a whole line period, this will be correct only for a time interval indicated at 24. It will be wrong during the time interval 25. This can be corrected by introducing an additional delay during the interval 25. Since the read and write clocks occur every 15 samples, the correct delay is equal to the remainder of 86.25/15 sample periods; i.e. 11.25 sample periods. Thus, an additional delay of this amount is introduced to the remote video signals during the interval 25. This is done by the circuits 26, 13A, 13B, 14A, 14B, 15A and 15B shown in Figure 1. The comparator 26 receives the remote line pulses A from the timing generator 3 and the local line pulses E from the timing generator 4 to produce an output as shown at J on Figure 3. When the waveform J is at the low level it sets the switches 13A and 13B in conditions where they connect the outputs of gates 12A and 12B directly to the OR gates 14A and 14B respectively. When the waveform J is at the high level, the switches 13A and 13B are set in conditions such that the outputs of gates 12A and 12B are connected to delay circuits in the form of 11-bit serial registers 15A and 15B. The outputs of these registers are connected to the OR gates 14A and 14B. Thus, during the appropriate interval an additional delay of 11 periods of the waveform B is introduced. This is close enough to the required delay of 11.5 periods to ensure that the read signals at the input to the memory are approximately mid-way between the write signals.

If the memory 16 requires more than one write clock, all these must be delayed by the same amount. A simpler solution is to modify the circuit of Figure 2 so as to delay the 3fsc clocks B, instead of the write clocks C. Delayed write clocks can then be generated from the delayed 3fsc clocks. The necessary additions to the circuit are indicated in broken lines in Figure 4. Also, the lowermost output of the timing generator 3, as shown in Figure 1, must be disconnected.

In this modified circuit the input to the selector 9A is connected, through a divide-by-two circuit 27 to receive the 3fsc pulses B instead of clock pulses C. The divide-by-two circuit 27 is needed simply to enable identical delay circuits to be used to delay the video signals and the clock signals. A multiply-by-two circuit 28 is included to bring the frequency of the delayed signals back to 3fsc. The output of the circuit 28 drives a clock generator 29 which produces as many clock signals as may be required and feeds them to the memory 16.

Claims

1. Information processing apparatus comprising a memory, means for writing information into the memory at times depending on first timing signals, means for reading the information out of the memory at times depending on second timing signals whose timing may be the same as or different to the first signals, and delay means for delaying at least some of the writing times so that they do not coincide with the reading times.

2. Apparatus according to claim 2 including means for producing differently timed first and second timing signals.

3. An apparatus according to claim 2 in which the delay means is connected to receive the first and second timing signals and is designed to delay the writing times by varying amounts so as to position each writing time approximately mid-way between reading times.

4. An apparatus according to claim 3 in which the delay means includes a counter arranged to count during a period between a first and a second timing signal, the delay produced by the delay means being related to the count accommodated by the counter.

5. An apparatus according to any preceding claim including a serial-to-parallel converter at the input to the memory and a parallel-to-serial converter at the output from the memory.

6. An apparatus according to any preceding claim for processing video signals comprising means for generating the said first timing signals from the video signals to be processed.

7. An apparatus according to claim 6 in which the delay means is arranged so that the delay produced by it is reset by line synchronising pulses of the video signals to be processed.

8. An apparatus according to claim 6 or 7 including a fixed delay circuit for further delaying

the writing times when they occur during a period after a blanking period of the processed video signal and before the next blanking period of the signal to be processed; this further delay being such that the writing and reading times do not coincide with each other during said period.

9. An apparatus according to claim 5, 6, 7, or 8 comprising an analogue-to-digital converter for converting the video signals into digital form, the memory being connected to receive the digital output of the converter and the output of the memory being connected to a digital-to-analogue converter.

10. An apparatus according to claim 9 in which the delay means is arranged to delay by equal amounts (a) the times when digital codes produced by the analogue-to-digital converter are fed to the memory and (b) the first timing signals which dictate the times at which the digital codes are written into the memory.

11. An apparatus for processing video signals comprising an analogue-to-digital converter for encoding the signals into parallel digital form, each output of the analogue-to-digital converter being connected to a circuit constructed in accordance with any preceding claim, the apparatus also including a digital-to-analogue converter for converting the outputs from the memories back to analogue form.

12. An apparatus for processing television signals substantially as described with reference to the accompanying drawings.

13. A method of processing information comprising writing the information into a memory at times depending on first timing signals, reading the information out of the memory at times depending on second timing signals whose timing may be the same as or different to the first signals, and delaying at least some of the writing times so that they do not coincide with the reading times.

14. A method according to claim 13 in which the signals on which the writing times depend and the signals on which the reading times depend have different timings.

15. A method according to claim 14 in which the writing times are delayed by varying amounts chosen so that each writing time is approximately between reading times.

16. A method according to claim 15 in which a counter is clocked during a period between one of said first timing signals and one of said second timing signals and in which the delay is fixed according to the count at the end of said period.

17. A method according to claim, 13, 14, 15 or 16 in which the information is converted from serial-to-parallel.

18. A method according to claim 13, 14, 15, 16 or 17 in which the information to be processed is in the form of video signals and in which the said first timing signals are derived from the said video signals to be processed.

19. Method according to claim 18 in which the writing times are delayed by a period which is reset by line synchronising pulses of the video signals to be processed.

20. A method according to claim 18 or 19 in which the writing times are further delayed when they occur after a blanking period of the processed video signal and before the next blanking period of the signal to be processed this further delay being chosen so that the reading and writing times do not coincide with each other during said period.

21. A method according to claim 17, 18, 19 or 20 in which the video signals are converted into digital codes which are fed to the memory and in which the digital output of the memory is converted into analogue form.

22. A method according to claim 21 in which the digital codes are delayed by the same amount as the timing signals.

23. A method of processing video signals in which they are first converted to parallel digital form; each parallel output is processed by a method in accordance with any of claims 13 to 22, and the information read out of the memories is then converted back to analogue form.

24. A method in accordance with any of claims 14 to 25 of synchronising video signals with synchronising pulses derived independently of the said video signals, the first timing signals being derived from synchronising pulses belonging to the signal being processed and the second timing signals being derived from the said independently derived synchronising pulses.

25. A method of synchronising video signals substantially as described with reference to the accompanying drawings and substantially as illustrated therein.

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