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(54) Title: ADVANCED TRANSISTORS WITH PUNCH THROUGH SUPPRESSION

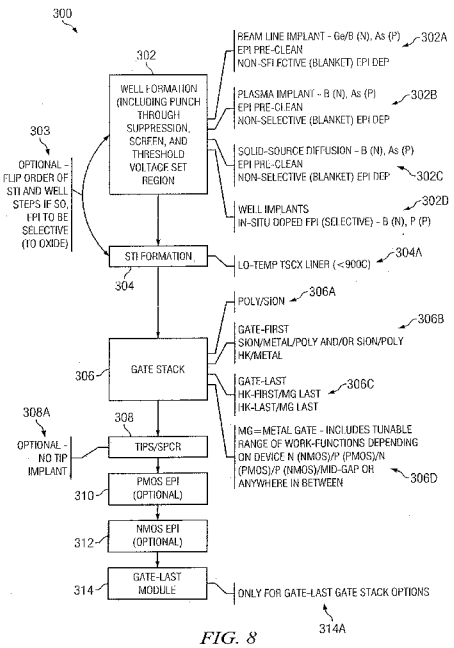

FIG. 8

(57) Abstract: An advanced transistor with punch through suppression includes a gate with length Lg, a well doped to have a first concentration of a dopant, and a screening region positioned under the gate and having a second concentration of dopant. The second concentration of dopant may be greater than 5 x 10 dopant atoms per cm. At least one punch through suppression region is disposed under the gate between the screening region and the well. The punch through suppression region has a third concentration of a dopant intermediate between the first concentration and the second concentration of dopant. A bias voltage may be applied to the well region to adjust a threshold voltage of the transistor.

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Title

Advanced transistors with punch through suppression

Related Applications

This application claims the benefit of U.S. Provisional Application No.61/247,300, filed September 30, 2009, the disclosure of which is incorporated by reference herein. This application also claims the benefit of U.S. Provisional Application No.61/262,122, filed November 17, 2009, the disclosure of which is incorporated by reference herein, and US Patent Application No.12/708,497 , titled "Electronic Devices and Systems, and Methods for Making and Using the Same", filed February 18, 2010, the disclosure of which is incorporated by reference herein. This application also claims the benefit of U.S. Provisional Application No.61/357,492, filed June 22, 2010, the disclosure of which is incorporated by reference herein.

Field of the Invention: This disclosure relates to structures and processes for forming advanced transistors with improved operational characteristics, including enhanced punch through suppression.

Background of the Invention:

Fitting more transistors onto a single die is desirable to reduce cost of electronics and improve their functional capability. A common strategy employed by semiconductor manufacturers is to simply reduce gate size of a field effect transistor (FET), and proportionally shrink area of the transistor source, drain, and required interconnects between transistors. However, a simple proportional shrink is not always possible because of what are known as "short channel effects". Short channel effects are particularly acute when channel length under a transistor gate is comparable in magnitude to depletion depth of an operating transistor, and include reduction in threshold voltage,

severe surface scattering, drain induced barrier lowering (DIBL), source-drain punch through, and electron mobility issues.

Conventional solutions to mitigate some short channel effects can involve implantation of pocket or halo implants around the source and the drain. Halo implants can be symmetrical or asymmetrical with respect to a transistor source and drain, and typically provide a smoother dopant gradient between a transistor well and the source and drains. Unfortunately, while such implants improve some electrical characteristics such as threshold voltage rolloff and drain induced barrier lowering, the resultant increased channel doping adversely affects electron mobility, primarily because of the increased dopant scattering in the channel.

Many semiconductor manufacturers have attempted to reduce short channel effects by employing new transistor types, including fully or partially depleted silicon on insulator (SOI) transistors. SOI transistors are built on a thin layer of silicon that overlies an insulator layer, have an undoped or low doped channel that minimizes short channel effects, and do not require either deep well implants or halo implants for operation. Unfortunately, creating a suitable insulator layer is expensive and difficult to accomplish. Early SOI devices were built on insulative sapphire wafers instead of silicon wafers, and are typically only used in specialty applications (e.g. military avionics or satellite) because of the high costs. Modern SOI technology can use silicon wafers, but require require expensive and time consuming additional wafer processing steps to make an insulative silicon oxide layer that extends across the entire wafer below a surface layer of device-quality single-crystal silicon.

One common approach to making such a silicon oxide layer on a silicon wafer requires high dose ion implantation of oxygen and high temperature annealing to form a buried oxide (BOX) layer in a bulk silicon wafer. Alternatively, SOI wafers can be fabricated by bonding a silicon wafer to another silicon wafer (a "handle" wafer) that has an oxide layer on its surface. The pair of wafers are split apart, using a process that leaves a thin

transistor quality layer of single crystal silicon on top of the BOX layer on the handle wafer. This is called the "layer transfer" technique, because it transfers a thin layer of silicon onto a thermally grown oxide layer of the handle wafer.

As would be expected, both BOX formation or layer transfer are costly manufacturing techniques with a relatively high failure rate. Accordingly, manufacture of SOI transistors not an economically attractive solution for many leading manufacturers. When cost of transistor redesign to cope with "floating body" effects, the need to develop new SOI specific transistor processes, and other circuit changes is added to SOI wafer costs, it is clear that other solutions are needed.

Another possible advanced transistor that has been investigated uses multiple gate transistors that, like SOI transistors, minimize short channel effects by having little or no doping in the channel. Commonly known as a finFET (due to a fin-like shaped channel partially surrounded by gates), use of finFET transistors has been proposed for transistors having 28 nanometer or lower transistor gate size. But again, like SOI transistors, while moving to a radically new transistor architecture solves some short channel effect issues, it creates others, requiring even more significant transistor layout redesign than SOI. Considering the likely need for complex non-planar transistor manufacturing techniques to make a finFET, and the unknown difficulty in creating a new process flow for finFET, manufacturers have been reluctant to invest in semiconductor fabrication facilities capable of making finFETs.

Brief Description of the Drawings:

Fig. 1 illustrates a DDC transistor with a punch through suppression;

Fig. 2 illustrates a dopant profile of a DDC transistor with enhanced punch through suppression;

Figs. 3-7 illustrate alternative useful dopant profiles; and

Fig. 8 is a flow diagram illustrating one exemplary process for forming a DDC transistor with a punch through suppression.

Detailed Description:

Unlike silicon on insulator (SOI) transistors, nanoscale bulk CMOS transistors (those typically having a gate length less than 100 nanometers) are subject to significant adverse short channel effects, including body leakage through both drain induced barrier lowering (DIBL) and source drain punch through. Punch through is associated with the merging of source and drain depletion layers, causing the drain depletion layer to extend across a doped substrate and reach the source depletion layer, creating a conduction path or leakage current between the source and drain. This results in a substantial increase in required transistor electrical power, along with a consequent increase in transistor heat output and decrease in operational lifetime for portable or battery powered devices using such transistors.

An improved transistor manufacturable on bulk CMOS substrates is seen in Fig. 1. A Field Effect Transistor (FET) 100 is configured to have greatly reduced short channel effects, along with enhanced punch through suppression according to certain described embodiments. The FET 100 includes a gate electrode 102, source 104, drain 106, and a gate dielectric 108 positioned over a channel 110. In operation, the channel 110 is deeply depleted, forming what can be described as deeply depleted channel (DDC) as compared to conventional transistors, with depletion depth set in part by a highly doped screening region 112. While the channel 110 is substantially undoped, and positioned as illustrated above a highly doped screening region 112, it may include simple or complex layering with different dopant concentrations. This doped layering can include a threshold voltage set region 111 with a dopant concentration less than screening region 112, optionally positioned between the gate dielectric 108 and the screening region 112 in the channel 110. A threshold voltage set region 111 permits small adjustments in operational threshold voltage of the FET 100, while leaving the bulk of the channel 110 substantially undoped. In particular, that portion of the channel 110 adjacent to the gate dielectric 108 should remain undoped. Additionally, a punch through suppression region 113 is formed beneath the screening region 112. Like the threshold voltage set region 111, the punch through suppression region 113 has a dopant concentration less than screening region

112, while being higher than the overall dopant concentration of a lightly doped well substrate 114.

In operation, a bias voltage 122 V_{BS} may be applied to source 104 to further modify operational threshold voltage, and P+ terminal 126 can be connected to P-well 114 at connection 124 to close the circuit. The gate stack includes a gate electrode 102, gate contact 118 and a gate dielectric 108. Gate spacers 130 are included to separate the gate from the source and drain, and optional Source/Drain Extensions (SDE) 132, or "tips" extend the source and drain under the gate spacers and gate dielectric 108, somewhat reducing the gate length and improving electrical characteristics of FET 100.

In this exemplary embodiment, the FET 100 is shown as an N-channel transistor having a source and drain made of N-type dopant material, formed upon a substrate as P-type doped silicon substrate providing a P-well 114 formed on a substrate 116. However, it will be understood that, with appropriate change to substrate or dopant material, a non-silicon P-type semiconductor transistor formed from other suitable substrates such as Gallium Arsenide based materials may be substituted. The source 104 and drain 106 can be formed using conventional dopant implant processes and materials, and may include, for example, modifications such as stress inducing source/drain structures, raised and/or recessed source/drains, asymmetrically doped, counter-doped or crystal structure modified source/drains, or implant doping of source/drain extension regions according to LDD (low doped drain) techniques. Various other techniques to modify source/drain operational characteristics can also be used, including, in certain embodiments, use of heterogeneous dopant materials as compensation dopants to modify electrical characteristics.

The gate electrode 102 can be formed from conventional materials, preferably including, but not limited to, metals, metal alloys, metal nitrides and metal silicides, as well as laminates thereof and composites thereof. In certain embodiments the gate electrode 102 may also be formed from polysilicon, including, for example, highly doped polysilicon and polysilicon-germanium alloy. Metals or metal alloys may include those containing

aluminum, titanium, tantalum, or nitrides thereof, including titanium containing compounds such as titanium nitride. Formation of the gate electrode 102 can include silicide methods, chemical vapor deposition methods and physical vapor deposition methods, such as, but not limited to, evaporative methods and sputtering methods. Typically, the gate electrode 102 has an overall thickness from about 1 to about 500 nanometers.

The gate dielectric 108 may include conventional dielectric materials such as oxides, nitrides and oxynitrides. Alternatively, the gate dielectric 108 may include generally higher dielectric constant dielectric materials including, but not limited to hafnium oxides, hafnium silicates, zirconium oxides, lanthanum oxides, titanium oxides, barium-strontium-titanates and lead-zirconate-titanates, metal based dielectric materials, and other materials having dielectric properties. Preferred hafnium-containing oxides include HfO_2, $HfZrO_x$, $HfSiO_x$, $HfTiO_x$, $HfAlO_x$, and the like. Depending on composition and available deposition processing equipment, the gate dielectric 108 may be formed by such methods as thermal or plasma oxidation, nitridation methods, chemical vapor deposition methods (including atomic layer deposition methods) and physical vapor deposition methods. In some embodiments, multiple or composite layers, laminates, and compositional mixtures of dielectric materials can be used. For example, a gate dielectric can be formed from a SiO_2-based insulator having a thickness between about 0.3 and 1 nm and the hafnium oxide based insulator having a thickness between 0.5 and 4nm. Typically, the gate dielectric has an overall thickness from about 0.5 to about 5 nanometers.

The channel region 110 is formed below the gate dielectric 108 and above the highly doped screening region 112. The channel region 110 also contacts and extends between, the source 104 and the drain 106. Preferably, the channel region includes substantially undoped silicon having a dopant concentration less than 5×10^{17} dopant atoms per cm^3 adjacent or near the gate dielectric 108. Channel thickness can typically range from 5 to 50 nanometers. In certain embodiments the channel region 110 is formed by epitaxial growth of pure or substantially pure silicon on the screening region.

As disclosed, the threshold voltage set region 111 is positioned above screening region 112, and is typically formed as a thin doped layer. Suitably varying dopant concentration, thickness, and separation from the gate dielectric and the screening region allows for controlled slight adjustments of threshold voltage in the operating FET 100. In certain embodiments, the threshold voltage set region 111 is doped to have a concentration between about 1×10^{18} dopant atoms per cm^3 and about 1×10^{19} dopant atoms per cm^3. The threshold voltage set region 111 can be formed by several different processes, including 1) in-situ epitaxial doping, 2) epitaxial growth of a thin layer of silicon followed by a tightly controlled dopant implant, 3) epitaxial growth of a thin layer of silicon followed by dopant diffusion of atoms from the screening region 112, or 4) by any combination of these processes (e.g. epitaxial growth of silicon followed by both dopant implant and diffusion from the screening layer 112) .

Position of a highly doped screening region 112 typically sets depth of the depletion zone of an operating FET 100. Advantageously, the screening region 112 (and associated depletion depth) are set at a depth that ranges from one comparable to the gate length (Lg/1) to a depth that is a large fraction of the gate length (Lg/5). In preferred embodiments, the typical range is between Lg/3 to Lg/1.5. Devices having an Lg/2 or greater are preferred for extremely low power operation, while digital or analog devices operating at higher voltages can often be formed with a screening region between Lg/5 and Lg/2. For example, a transistor having a gate length of 32 nanometers could be formed to have a screening region that has a peak dopant density at a depth below the gate dielectric of about 16 nanometers (Lg/2), along with a threshold voltage set region at peak dopant density at a depth of 8 nanometers (Lg/4).

In certain embodiments, the screening region 112 is doped to have a concentration between about 5×10^{18} dopant atoms per cm^3 and about 1×10^{20} dopant atoms per cm^3, significantly more than the dopant concentration of the undoped channel, and at least slightly greater than the dopant concentration of the optional threshold voltage set region 111. As will be appreciated, exact dopant concentrations and screening region

depths can be modified to improve desired operating characteristics of FET 100, or to take in to account available transistor manufacturing processes and process conditions.

To help control leakage, the punch through suppression region 113 is formed beneath the screening region 112. Typically, the punch through suppression region 113 is formed by direct implant into a lightly doped well, but it be formed by out-diffusion from the screening region, in-situ growth, or other known process. Like the threshold voltage set region 111, the punch through suppression region 113 has a dopant concentration less than the screening region 122, typically set between about 1×10^{18} dopant atoms per cm^3 and about 1×10^{19} dopant atoms per cm^3. In addition, the punch through suppression region 113 dopant concentration is set higher than the overall dopant concentration of the well substrate. As will be appreciated, exact dopant concentrations and depths can be modified to improve desired operating characteristics of FET 100, or to take in to account available transistor manufacturing processes and process conditions.

Forming such a FET 100 is relatively simple compared to SOI or finFET transistors, since well developed and long used planar CMOS processing techniques can be readily adapted.

Together, the structures and the methods of making the structures allow for FET transistors having both a low operating voltage and a low threshold voltage as compared to conventional nanoscale devices. Furthermore, DDC transistors can be configured to allow for the threshold voltage to be statically set with the aid of a voltage body bias generator. In some embodiments the threshold voltage can even be dynamically controlled, allowing the transistor leakage currents to be greatly reduced (by setting the voltage bias to upwardly adjust the V_T for low leakage, low speed operation), or increased (by downwardly adjusting the V_T for high leakage, high speed operation). Ultimately, these structures and the methods of making structures provide for designing integrated circuits having FET devices that can be dynamically adjusted while the circuit is in operation. Thus, transistors in an integrated circuit can be designed with nominally identical structure, and can be controlled, modulated or programmed to operate at

different operating voltages in response to different bias voltages, or to operate in different operating modes in response to different bias voltages and operating voltages. In addition, these can be configured post-fabrication for different applications within a circuit.

As will be appreciated, concentrations of atoms implanted or otherwise present in a substrate or crystalline layers of a semiconductor to modify physical and electrical characteristics of a semiconductor are be described in terms of physical and functional regions or layers. These may be understood by those skilled in the art as three-dimensional masses of material that have particular averages of concentrations. Or, they may be understood as sub-regions or sub-layers with different or spatially varying concentrations. They may also exist as small groups of dopant atoms, regions of substantially similar dopant atoms or the like, or other physical embodiments. Descriptions of the regions based on these properties are not intended to limit the shape, exact location or orientation. They are also not intended to limit these regions or layers to any particular type or number of process steps, type or numbers of layers (e.g., composite or unitary), semiconductor deposition, etch techniques, or growth techniques utilized. These processes may include epitaxially formed regions or atomic layer deposition, dopant implant methodologies or particular vertical or lateral dopant profiles, including linear, monotonically increasing, retrograde, or other suitable spatially varying dopant concentration. To ensure that desired dopant concentrations are maintained, various dopant anti-migration techniques, are contemplated, including low temperature processing, carbon doping, in-situ dopant deposition, and advanced flash or other annealing techniques. The resultant dopant profile may have one or more regions or layers with different dopant concentrations, and the variations in concentrations and how the regions or layers are defined, regardless of process, may or may not be detectable via techniques including infrared spectroscopy, Rutherford Back Scattering (RBS), Secondary Ion Mass Spectroscopy (SIMS), or other dopant analysis tools using different qualitative or quantitative dopant concentration determination methodologies.

To better appreciate one possible transistor structure, Fig. 2 illustrates a dopant profile 202 of a deeply depleted transistor taken at midline between a source and drain, and extending downward from a gate dielectric toward a well. Concentration is measured in number of dopant atoms per cubic centimeter, and downward depth is measured as a ratio of gate length Lg. Measuring as a ratio rather than absolute depth in nanometers better allows cross comparison between transistors manufactured at different nodes (e.g 45nm, 32 nm, 22 nm, or 15 nm) where nodes are commonly defined in term of minimum gate lengths.

As seen in Fig. 2, the region of the channel 210 adjacent to the gate dielectric is substantially free of dopants, having less than 5×10^{17} dopant atoms per cm^3 to a depth of nearly Lg/4. A threshold voltage set region 211 increases the dopant concentration to about 3×10^{18} dopant atoms per cm^3, and the concentration increases another order of magnitude to about 3×10^{19} dopant atoms per cm^3 to form the screening region 212 that sets the base of the depletion zone in an operating transistor. A punch through suppression region 213 region having a dopant concentration of about 1×10^{19} dopant atoms per cm^3 at a depth of about Lg/1 is intermediate between the screening region and the lightly doped well 214. Without the punch through suppression region, a transistor constructed to have, for example, an 30 nm gate length and an operating voltage of 1.0 volts would be expected to have significantly greater leakage. When the disclosed punch through suppression 213 is implanted, punch through leakage is reduced, making the transistor more power efficient, and better able to tolerate process variations in transistor structure without punch through failure.

This is better seen with respect to the following Table 1, which indicates expected performance improvements for a range of punch through dosage and threshold voltage:

TABLE 1

	Ioff (nA/um)	Idsat (mA/um)	Vt (V)
Target Punchthrough layer	2	0.89	0.31
No Punchthrough layer	70	1	0.199
Higher Dose Punchthrough	0.9	0.54	0.488
Very deep Punchthrough	15	1	0.237

Alternative dopant profiles are contemplated. As seen in Fig. 3, an alternative dopant profile that includes a slightly increased depth for the low doped channel is shown. In contrast to the embodiments of Fig. 3, the threshold voltage set region 211 is a shallow notch primarily formed by out-diffusion into an epitaxially deposited layer of silicon from the screening region 212. The screening region 212 itself is set to have a dopant concentration greater than 3×10^{19} dopant atoms per cm^3. The punch through suppression region 213 has a dopant concentration of about 8×10^{18} dopant atoms per cm^3, provided by a combination of out-diffusion from the screening region 212 and a separate low energy implant.

As seen in Fig. 4, an alternative dopant profile that includes a greatly increased depth for the low doped channel is shown. In contrast to the embodiments of Fig. 2 and 3, there is no distinct notch, plane or layer to aid in threshold voltage setting. The screening region 212 is set to be greater than 3×10^{19} dopant atoms per cm^3 and the punch through suppression region 213 has a similarly high, yet narrowly defined dopant concentration of about 8×10^{18} dopant atoms per cm^3, provided by with a separate low energy implant.

Yet another variation in dopant profile is seen in Fig. 5, which illustrates a transistor dopant profile 205 for a transistor structure that includes a very low doped channel 210. The threshold voltage set region 211 is precisely formed by in-situ or well controlled implant doping of thin epitaxial layer grown on the screening region. The screening region 212 is set to be about 1×10^{19} dopant atoms per cm^3 and the punch through suppression region 213 also has narrowly defined dopant concentration of about 8×10^{18} dopant atoms per cm^3, provided by with a separate low energy implant. The well implant 214 concentration is gradually reduced to about 5×10^{17} dopant atoms per cm^3 .

As seen in Fig. 6, a dopant profile 206 includes a low doped channel 210 adjacent to the gate dielectric, and a narrowly defined threshold voltage set region211. The screening region 212 increases to a narrow peak set to be about 1 x 10^{19} dopant atoms per cm^3 and the punch through suppression region 213 also has broadly peak dopant concentration of about 5 x 10^{18} dopant atoms per cm^3, provided by with a separate low energy implant. The well implant 214 concentration is high to improve bias coefficient of the transistor, with a concentration of about 8 x 10^{17} dopant atoms per cm^3 .

In contrast to the narrow screen region peak dopant concentration of Fig. 6, the dopant profile 207 of Fig. 7 has a broad peak 212. In addition to a narrow undoped channel 210, the transistor structure includes a well defined partially retrograde threshold set 211, and a distinct separate punch through suppression peak 213. The well 214 doping concentration is relatively low, less than about 5 x 10^{17} dopant atoms per cm^3 .

Fig. 8 is a schematic process flow diagram 300 illustrating one exemplary process for forming a transistor with a punch through suppression region and a screening region suitable for different types of FET structures, including both analog and digital transistors. The process illustrated here is intended to be general and broad in its description in order not to obscure the inventive concepts, and more detailed embodiments and examples are set forth below. These along with other process steps allow for the processing and manufacture of integrated circuits that include DDC structured devices together with legacy devices, allowing for designs to cover a full range of analog and digital devices with improved performance and lower power.

In Step 302, the process begins at the well formation, which may be one of many different processes according to different embodiments and examples. As indicated in 303, the well formation may be before or after STI (shallow trench isolation) formation 304, depending on the application and results desired. Boron (B), indium (I) or other P-type materials may be used for P-type implants, and arsenic (As) or phosphorous (P) and other N-type materials may be used for N-type implants. For the PMOS well implants, the P+ implant may be implanted within a range from 10 to 80keV, and at

NMOS well implants, the boron implant B+ implant may be within a range of 0.5 to 5keV, and within a concentration range of 1 x 10^{13} to 8 x $10^{13}/cm^2$. A germanium implant Ge+, may be performed within a range of 10 to 60keV, and at a concentration of 1 x 10^{14} to 5x10^{14} /cm^2. To reduce dopant migration, a carbon implant, C+ may be performed at a range of 0.5 to 5keV, and at a concentration of 1 x 10^{13} to 8 x $10^{13}/cm^2$. Well implants may include sequential implant, and/or epitaxial growth and implant, of punch through suppression regions, screen regions having a higher dopant density than the punch through suppression region, and threshold voltage set regions (which previously discussed are typically formed by implant or diffusion of dopants into a grown epitaxial layer on the screening region).

In some embodiments the well formation 302 may include a beam line implant of Ge/B (N), As (P), followed by an epitaxial (EPI) pre-clean process, and followed finally non-selective blanket EPI deposition, as shown in 302A. Alternatively, the well may be formed using a plasma implant of B (N), As (P), followed by an EPI pre-clean, then finally a non-selective (blanket) EPI deposition, 302B. The well formation may alternatively include a solid-source diffusion of B(N), As(P), followed by an EPI pre-clean, and followed finally by a non-selective (blanket) EPI deposition, 302C. The well formation may alternatively include a solid-source diffusion of B(N), As(P), followed by an EPI pre-clean, and followed finally by a non-selective (blanket) EPI deposition, 302D. As yet another alternative, well formation may simply include well implants, followed by in-situ doped selective EPI of B (N), P (P). Embodiments described herein allow for any one of a number of devices configured on a common substrate with different well structures and according to different parameters.

Shallow trench isolation (STI) formation 304, which, again, may occur before or after well formation 302, may include a low temperature trench sacrificial oxide (TSOX) liner at a temperature lower than 900^{0}C. The gate stack 306 may be formed or otherwise constructed in a number of different ways, from different materials, and of different work functions. One option is a poly/SiON gate stack 306A. Another option is a gate-first process 306B that includes SiON/Metal/Poly and/or SiON/Poly, followed by High-K/Metal Gate. Another option, a gate-last process 306C includes a high-K/metal gate stack wherein the the gate stack can either be formed with "Hi-K first-Metal gate last" flow or and "Hi-K last-Metal gate last" flow. Yet another

option, 306D is a metal gate that includes a tunable range of work functions depending on the device construction, N(NMOS)/P(PMOS)/N(PMOS)/P(NMOS) /Mid-gap or anywhere in between. In one example, N has a work function (WF) of 4.05V ±200mV, and P has a WF of 5.01V ±200mV.

Next, in Step 308, Source/Drain tips may be implanted, or optionally may not be implanted depending on the application. The dimensions of the tips can be varied as required, and will depend in part on whether gate spacers (SPCR) are used. In one option, there may be no tip implant in 308A. Next, in optional steps 310 and 312, PMOS or NMOS EPI layers may be formed in the source and drain regions as performance enhancers for creating strained channels. For gate-last gate stack options, in Step 314, a Gate-last module is formed. This may be only for gate-last processes 314A.

Die supporting multiple transistor types, including those with and without a punch through suppression, those having different threshold voltages, and with and without static or dynamic biasing are contemplated. Systems on a chip (SoC), advanced microprocessors, radio frequency, memory, and other die with one or more digital and analog transistor configurations can be incorporated into a device using the methods described herein. According to the methods and processes discussed herein, a system having a variety of combinations of DDC and/or transistor devices and structures with or without punch through suppression can be produced on silicon using bulk CMOS. In different embodiments, the die may be divided into one or more areas where dynamic bias structures, static bias structures or no-bias structures exist separately or in some combination. In a dynamic bias section, for example, dynamically adjustable devices may exist along with high and low V_T devices and possibly DDC logic devices.

While certain exemplary embodiments have been described and shown in the accompanying drawings, it is to be understood that such embodiments are merely illustrative of and not restrictive on the broad invention, and that this invention not be limited to the specific constructions and arrangements shown and described, since various other modifications may occur to those ordinarily skilled in the art.

Accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense.

1. A field effect transistor structure, comprising:

a well doped to have a first concentration of a dopant;

a screening layer implanted into the well and having a second concentration of dopant greater than 5×10^{18} dopant atoms per cm^3; and

at least one punch through suppression region having a third concentration of a dopant intermediate between the first concentration and the second concentration of dopant, with the punch through suppression region positioned under the gate and between the screening region and the well.

2. The field effect transistor structure of claim 1, wherein a blanket epitaxial layer is grown on the screening region.

3. The field effect transistor structure of claim 2, further comprising a threshold voltage set layer defined in the blanket epitaxial layer and having a fourth dopant concentration intermediate between the second concentration and 5×10^{17} dopant atoms per cm^3.

4. The field effect transistor structure of claim 1, wherein the screening region is formed to out-diffuse dopants into the at least one punchthrough suppression region.

5. The field effect transistor structure of claim 1, wherein the at least one punchthrough suppression region is formed at least in part by direct implant into the well.

6. A method for forming a field effect transistor structure that reduces adverse punch through effects, comprising:

forming a well doped to have a first concentration of a dopant;

implanting a screening region having a dopant concentration of greater than 5 x 10^{18} dopant atoms per cm^3; and

forming a punch through suppression region in the well.

7. The method of Claim 6, further comprising:

growing a blanket epitaxial layer on top of the screening region.

8. The method of Claim 7, wherein growing a blanket epitaxial layer on top of the screening region includes doping a portion of the blanket epitaxial layer adjacent to the screening region by one or more of direct implant, diffusion from the screening region, or in-situ deposition of dopants to form a threshold voltage set layer.

9. The method of Claim 6, further comprising isolating the field effect transistor using shallow trench isolation after growing an epitaxial blanket layer on top of the screening region.

10. The method of Claim 6, wherein forming a punch through suppression region further comprises doping a portion of the layer adjacent to the screening region by direct implant and/or diffusion from the screening region.

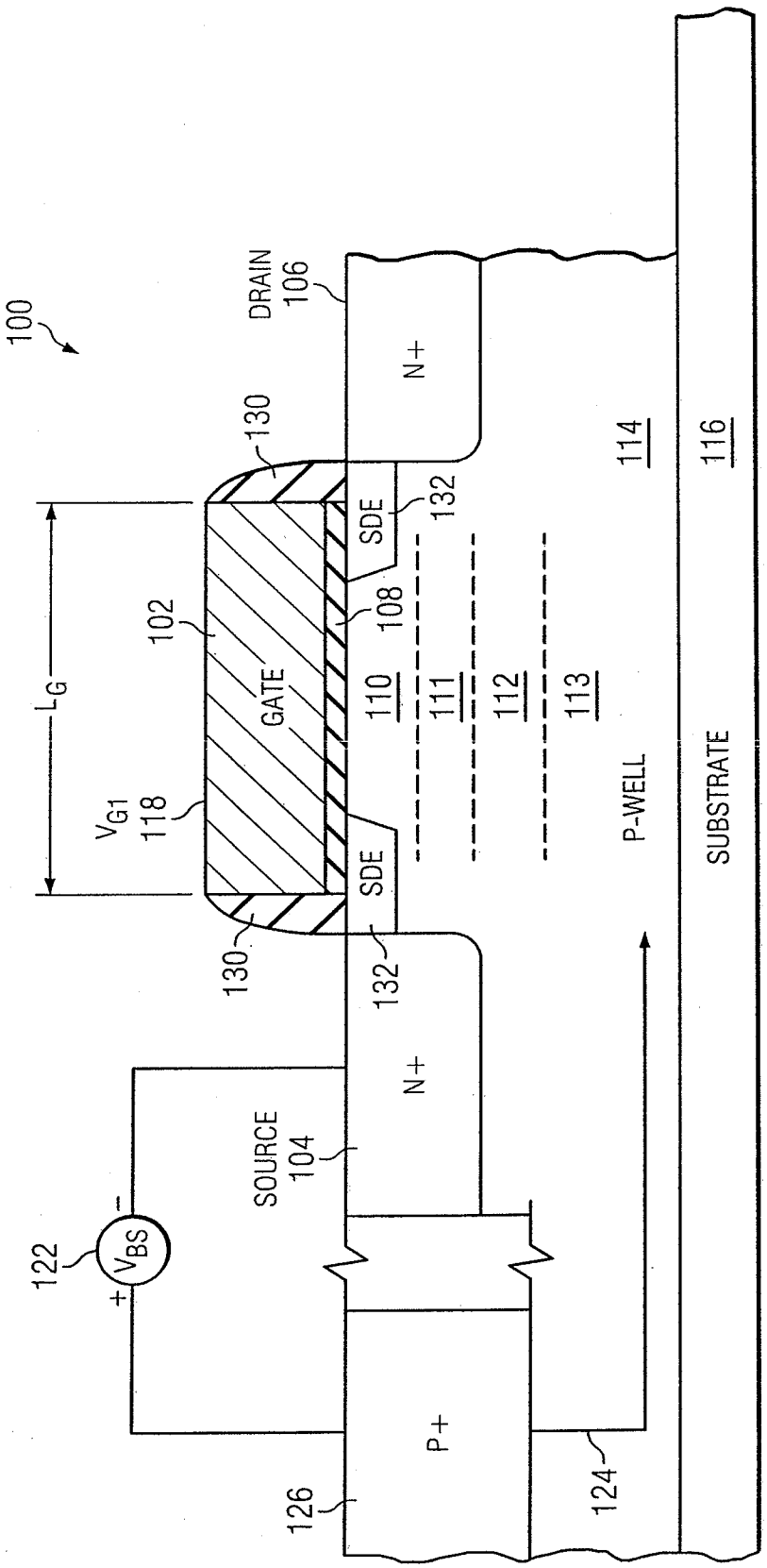
100
DRAIN
106
N+
130
SDE
132
102
108
GATE
110
111
112
113
114
116
L_G
V_{G1}
118
P-WELL
SUBSTRATE
SDE
130
132
N+
SOURCE
104
122
V_{BS}
P+
126
124

FIG. 1

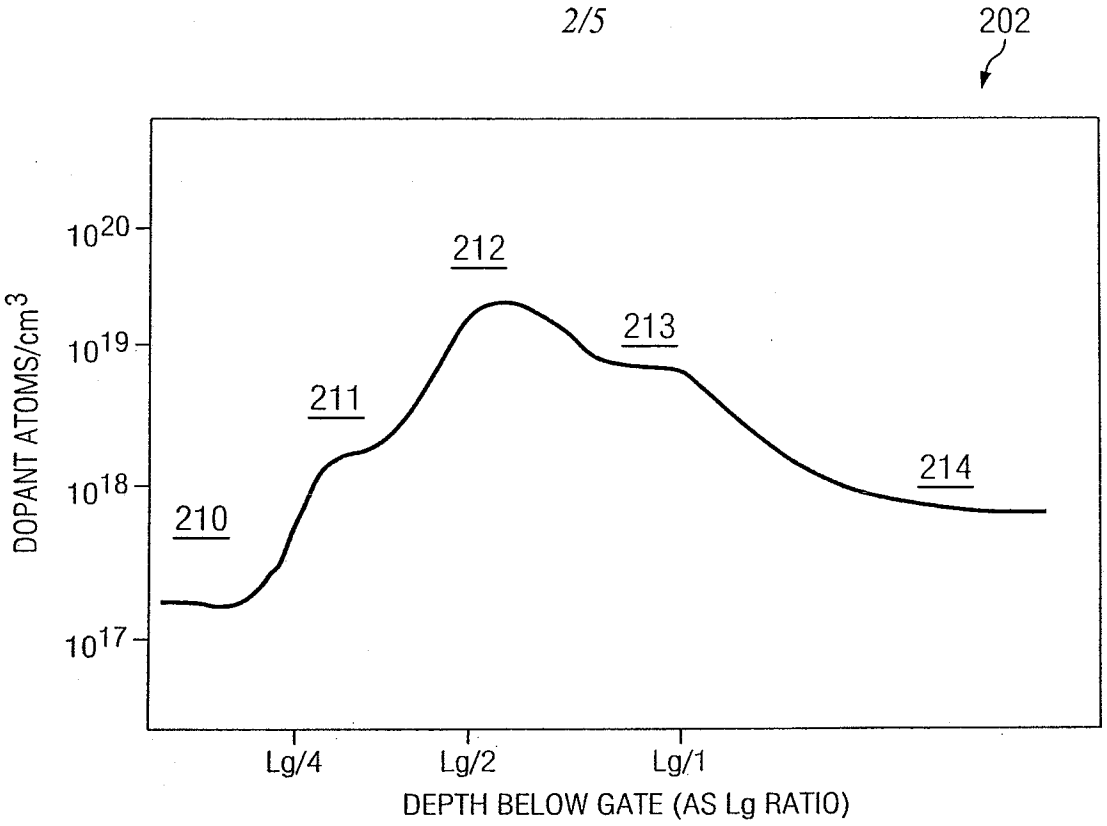
202
10^{20}
10^{19}
10^{18}
10^{17}
DOPANT ATOMS/cm^3
210
211
212
213
214
Lg/4
Lg/2
Lg/1
DEPTH BELOW GATE (AS Lg RATIO)

FIG. 2

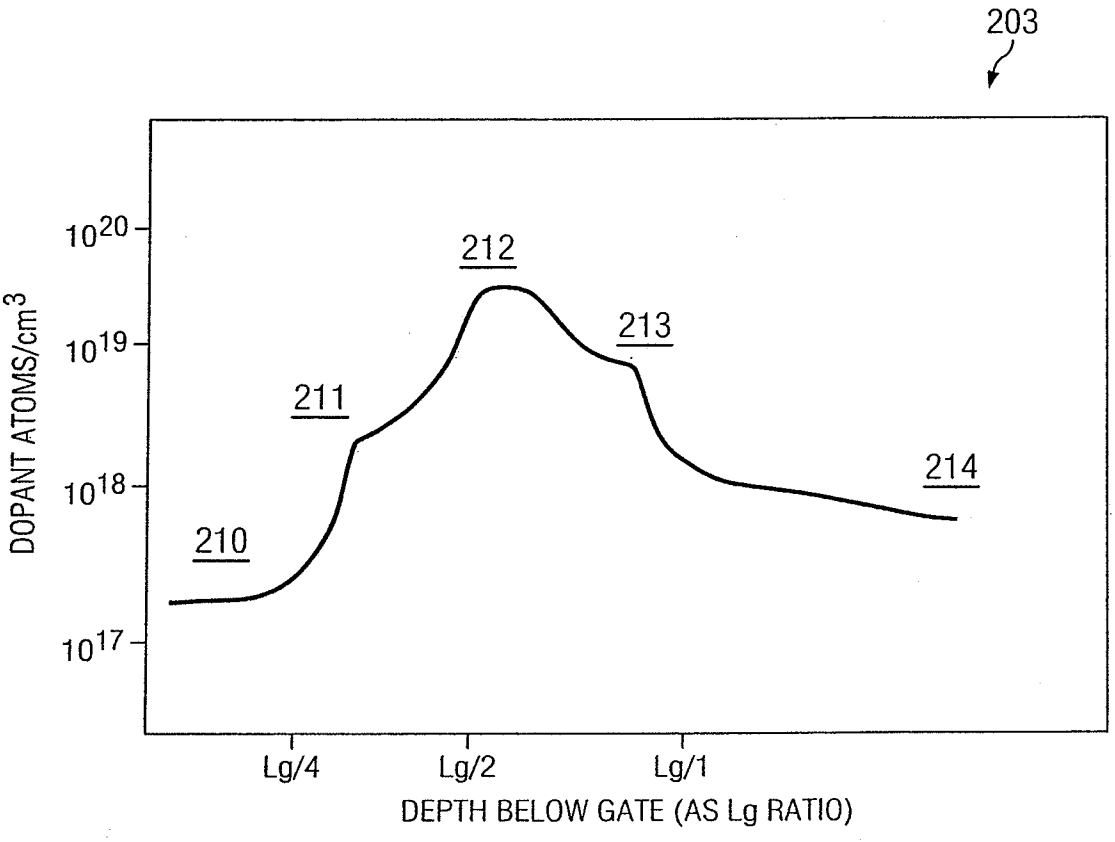
203
10^{20}
10^{19}
10^{18}
10^{17}
DOPANT ATOMS/cm^3
210
211
212
213
214
Lg/4
Lg/2
Lg/1
DEPTH BELOW GATE (AS Lg RATIO)

FIG. 3

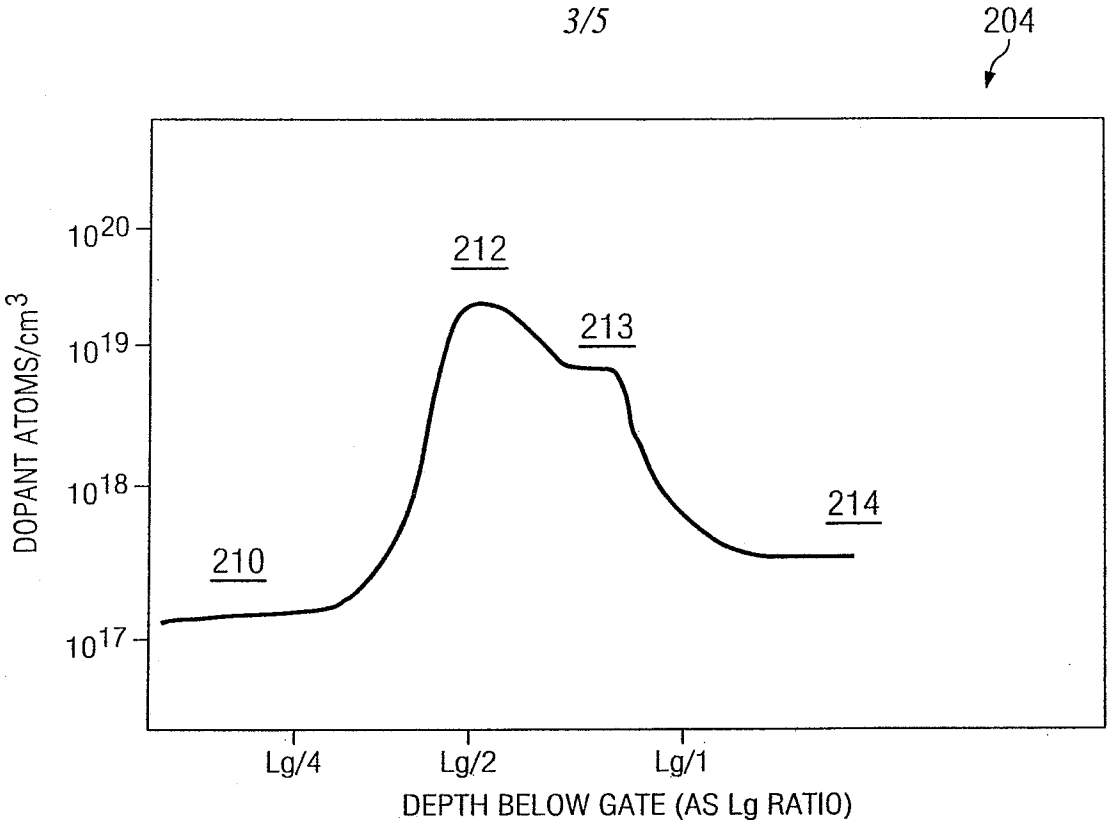
204
10^{20}
10^{19}
10^{18}
10^{17}
DOPANT ATOMS/cm^3
212
213
214
210
Lg/4
Lg/2
Lg/1
DEPTH BELOW GATE (AS Lg RATIO)

FIG. 4

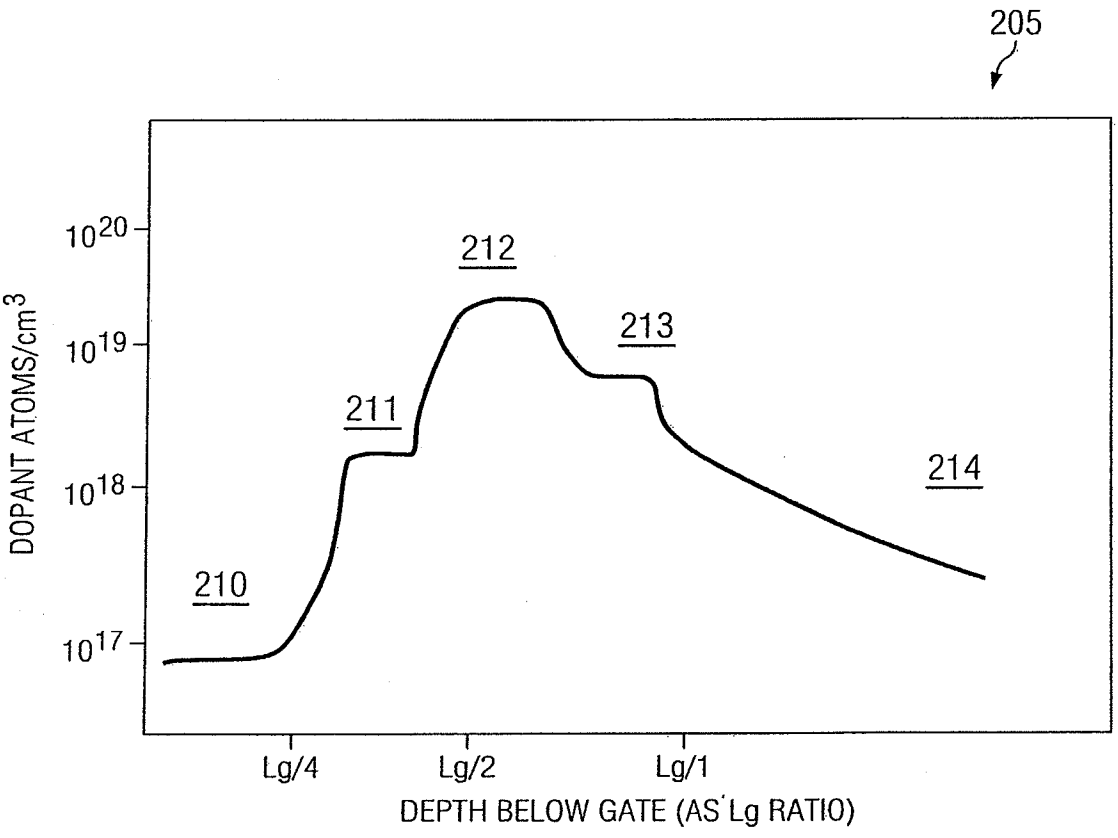
205
10^{20}
10^{19}
10^{18}
10^{17}
DOPANT ATOMS/cm^3
212
213
211
214
210
Lg/4
Lg/2
Lg/1
DEPTH BELOW GATE (AS Lg RATIO)

FIG. 5

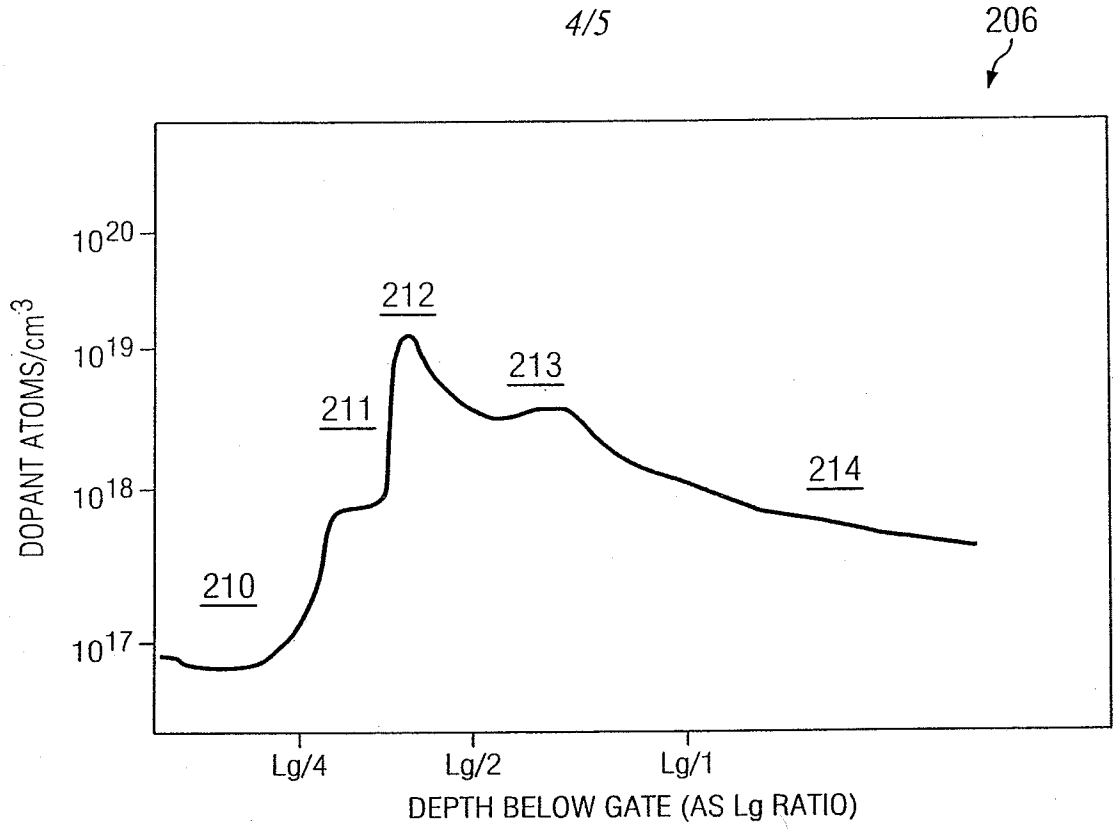
206
10^{20}
10^{19}
10^{18}
10^{17}
DOPANT ATOMS/cm^3
210
211
212
213
214
Lg/4
Lg/2
Lg/1
DEPTH BELOW GATE (AS Lg RATIO)

FIG. 6

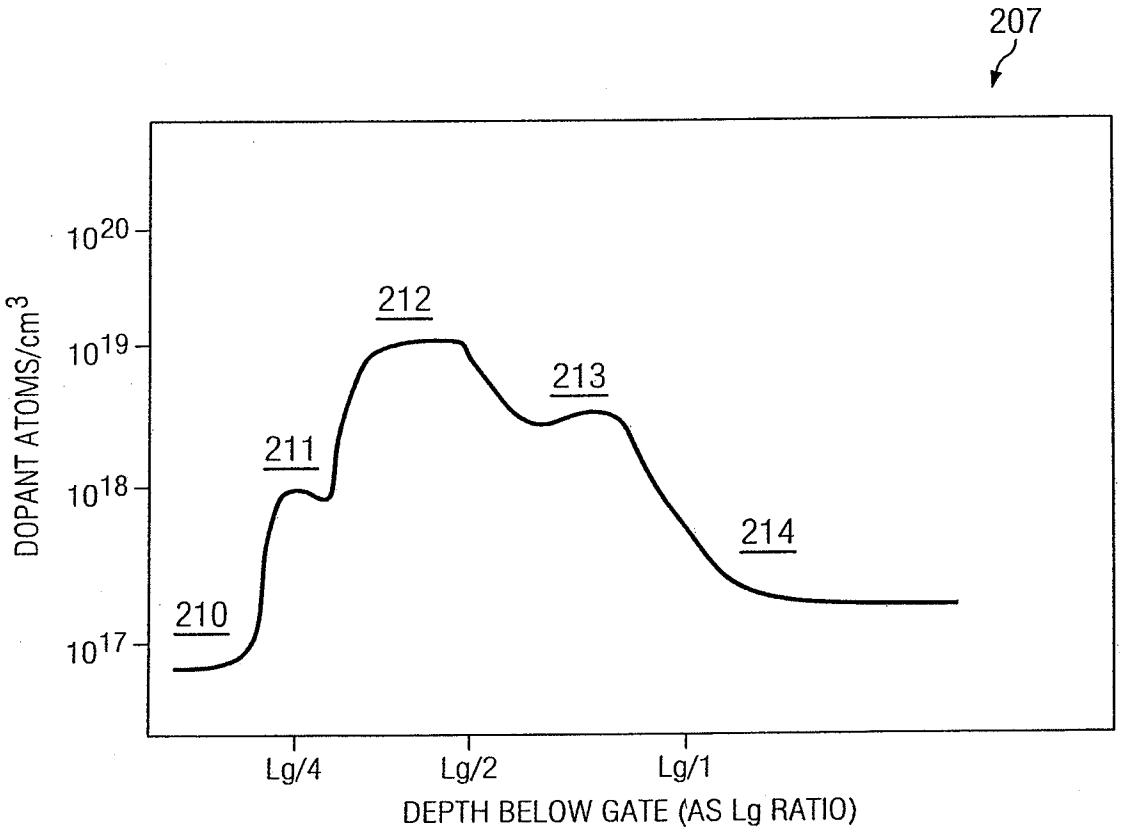
207
10^{20}
10^{19}
10^{18}
10^{17}
DOPANT ATOMS/cm^3
210
211
212
213
214
Lg/4
Lg/2
Lg/1
DEPTH BELOW GATE (AS Lg RATIO)

FIG. 7

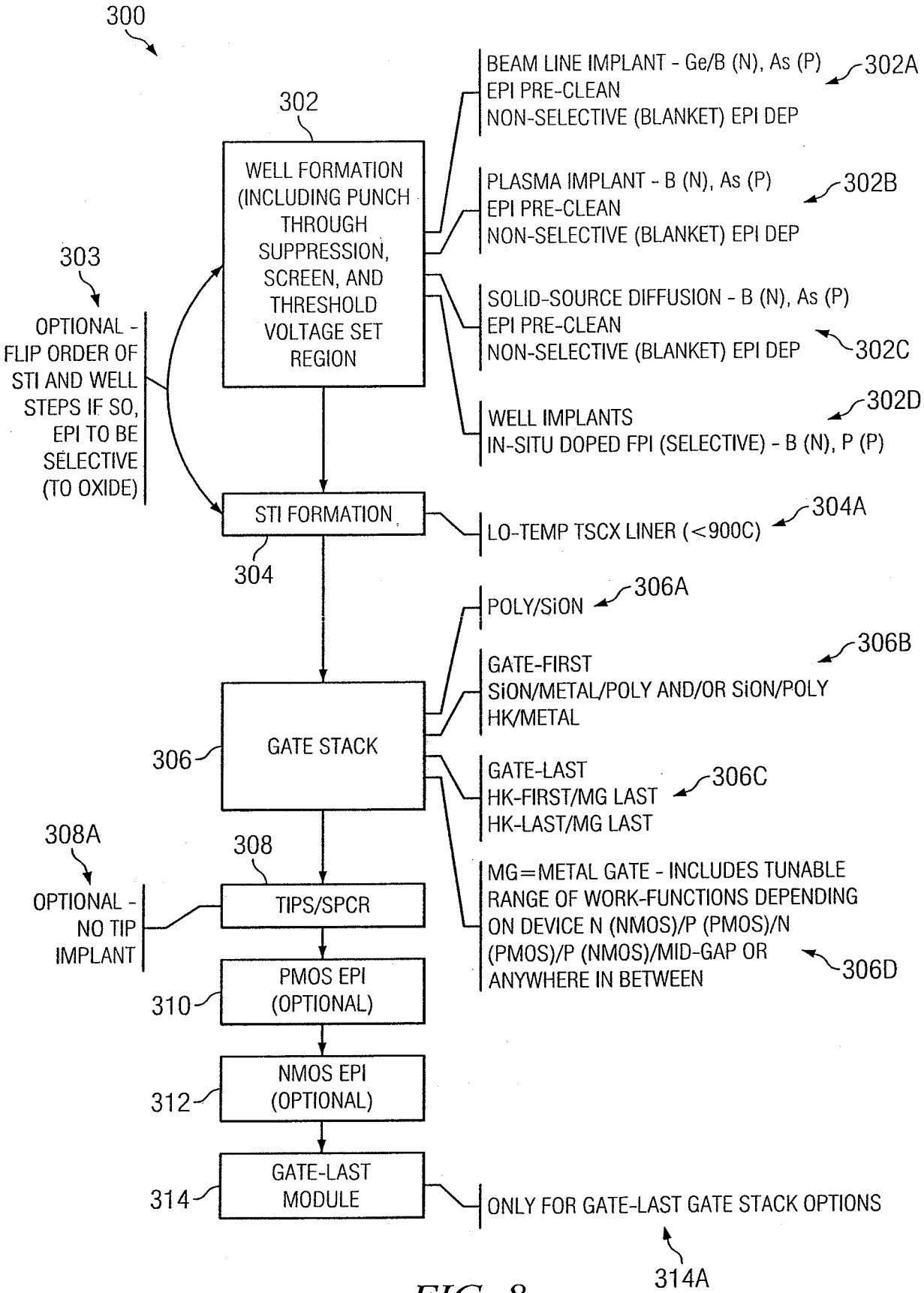
300
302
WELL FORMATION (INCLUDING PUNCH THROUGH SUPPRESSION, SCREEN, AND THRESHOLD VOLTAGE SET REGION
BEAM LINE IMPLANT - Ge/B (N), As (P)
EPI PRE-CLEAN
NON-SELECTIVE (BLANKET) EPI DEP
302A
PLASMA IMPLANT - B (N), As (P)
EPI PRE-CLEAN
NON-SELECTIVE (BLANKET) EPI DEP
302B
SOLID-SOURCE DIFFUSION - B (N), As (P)
EPI PRE-CLEAN
NON-SELECTIVE (BLANKET) EPI DEP
302C
WELL IMPLANTS
IN-SITU DOPED FPI (SELECTIVE) - B (N), P (P)
302D
303
OPTIONAL - FLIP ORDER OF STI AND WELL STEPS IF SO, EPI TO BE SELECTIVE (TO OXIDE)
STI FORMATION
304
LO-TEMP TSCX LINER (<900C)
304A
306
GATE STACK
POLY/SiON
306A
GATE-FIRST
SiON/METAL/POLY AND/OR SiON/POLY
HK/METAL
306B
GATE-LAST
HK-FIRST/MG LAST
HK-LAST/MG LAST
306C
MG=METAL GATE - INCLUDES TUNABLE RANGE OF WORK-FUNCTIONS DEPENDING ON DEVICE N (NMOS)/P (PMOS)/N (PMOS)/P (NMOS)/MID-GAP OR ANYWHERE IN BETWEEN
306D
308A
OPTIONAL - NO TIP IMPLANT
308
TIPS/SPCR
310
PMOS EPI (OPTIONAL)
312
NMOS EPI (OPTIONAL)
314
GATE-LAST MODULE
ONLY FOR GATE-LAST GATE STACK OPTIONS
314A

FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 11/41165

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - G05F 1/10; H01L 29/78 (2011.01)
USPC - 327/543; 257/392; 257/402; 257/407; 257/E21.409
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC (8) - G05F 1/10; H01L 29/78 (2011.01)
USPC - 327/543; 257/392; 257/402; 257/407; 257/E21.409

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
IPC (8) - G05F 1/10; H01L 29/78 (2011.01)
USPC - 327/543; 257/392; 257/402; 257/407; 257/E21.409 (keyword delimited)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PubWEST (PGPB,USPT,USOC,EPAB,JPAB) Terms - MOS punch punch-through punchthrough suppression well gradient inverted dopant layers short channel depleted screening SuVolta Shifren Ranade
Google - CMOS transistors punch-through dopant-gradient well reverse-short-channel

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 6,221,724 B1 (YU, ET AL.) 24 April 2001 (24.04.2001),	1-10
Y	US 5,444,008 A (HAN, ET AL.) 22 August 1995 (22.08.1995), col 5, ln 3-42; FIG. 1	1-10
Y	US 6,503,805 B2 (WANG, ET AL.) 07 January 2003 (07.01.2003), col 4, ln 42-48	9
A	US 2010/0149854 A1 (VORA) 17 June 2010 (17.06.2010), entire document	1-10
A	US 2004/0075143 A1 (BAE, ET AL.) 22 April 2004 (22.04.2004), entire document	1-10
A	US 2009/0302388 A1 (CAI, ET AL.) 10 December 2009 (10.12.2009), entire document	1-10
A	US 7,122,411 B2 (MOULI) 17 October 2006 (17.10.2006), entire document	1-10
A	US 5,622,880 A (BURR, ET AL.) 22 April 1997 (22.04.1997), entire document	1-10
A	US 6,503,805 B2 (WANG, ET AL.) 07 January 2003 (07.01.2003), entire document	1-10
A	US 5,166,765 A (LEE, ET AL.) 24 November 1992 (24.11.1992), entire document	1-10
A	US 7,566,600 B2 (MOULI) 29 July 2009 (28.07.2009), entire document	1-10
A	US 4,908,681 A (NISHIDA, ET AL.) 13 March 1990 (13.03.1990), entire document	1-10

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 October 2011 (17.10.2011)	02 NOV 2011
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (July 2009)