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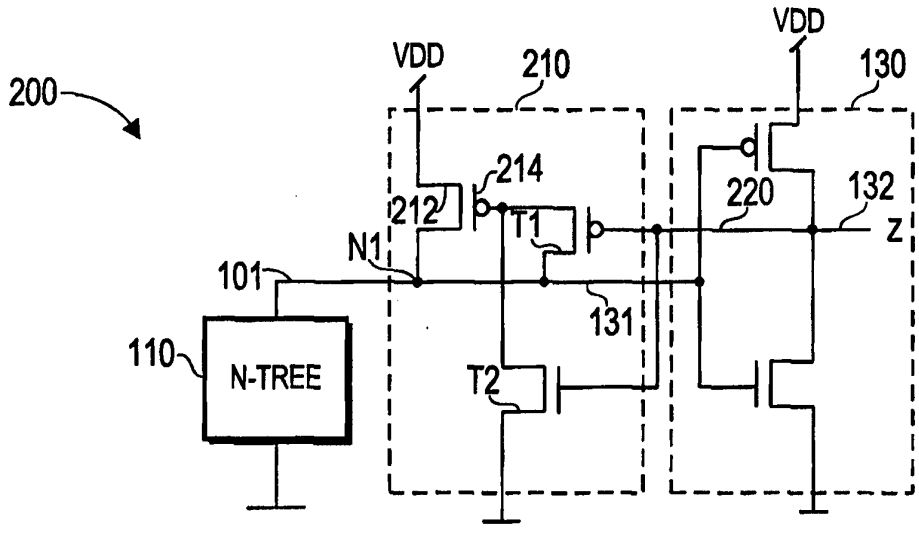

(57) Abstract

A pullup circuit (200) having a limited voltage swing and fast pullup and pulldown times comprises a pullup structure (210) and an internal node (N1). The pullup circuit (200) operates to limit the current of the pullup structure (210) before the N-tree (110) discharges the internal node (N1), thereby reducing the pullup effect of the pullup structure (210) to reduce fall time and power consumption. Then the pullup circuit (200) maximizes the current of the pullup structure (210) after the N-tree (110) has pulled down the internal node (N1) to increase the pullup effect of the pullup structure (210) to reduce rise time. As a result, the voltage of the internal node (N1) both charges more quickly when the N-tree (110) becomes inactive and discharges more quickly when the N-tree (110) becomes active.

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A FAST SWING-LIMITED PULLUP CIRCUIT

FIELD OF THE INVENTION

This invention relates to pullup circuits and, more particularly, to static pullup circuits for use with CMOS circuits.

BACKGROUND INFORMATION

FIG. 1 shows a diagram of a conventional static pullup circuit 100 commonly used in CMOS integrated circuits for high speed applications. The term CMOS is also used herein to refer to complementary MOS structures using silicon gate technologies. An N-tree 110 operates to pull down the voltage at an output line 101 when active and stops pulling down the voltage at output line 101 when not active. Output line 101 is coupled to pullup circuit 100 at an internal node 120. Internal node 120 is connected to CMOS inverter 130 by an input lead 131. Thus, the logic level on internal node 120 is inverted by inverter 130 at an output lead 132. Output lead 132 is connected to the gate of pulldown P-channel field effect transistor (FET) 140 via feed back line 141. P-channel FET 140 has a source connected to internal node 120 and a drain held at ground potential. Thus, the output signal generated by inverter 130 feeds back to the gate of P-channel FET 140, thereby turning P-channel FET 140 on or off.

A P-channel FET 150, having a source connected to a Vdd voltage source and a drain connected to internal node 120 serves as a pullup device. P-channel FET 150 receives a signal PWR_BYPASS on a gate 151. In normal operation, signal PWR_BYPASS is kept at a logic low level (i.e., deasserted) by mode control circuitry (not shown), thereby causing P-channel FET to turn on. Consequently, a voltage divider is formed by pullup P-channel FET 150 and pulldown P-channel FET 140 through internal node 120, which determines the voltage at

which node 120 is held when N-tree 110 is not active.

The PWR_BYPASS signal is used to place pullup circuit 100 in a power bypass mode, which stops all power consumption by pullup circuit 100. Thus, when pullup circuit 100 is not in operation (e.g., during testing) the PWR_BYPASS signal can be asserted (i.e., driven to a logic high level) to enter the power bypass mode. When the PWR_BYPASS signal is asserted, pullup P-channel FET 150 is turned off, thereby cutting off any DC current path through node 120 from the voltage Vdd source and the source of ground potential. As a result, substantially no power is consumed by pullup circuit 100. Further, an N-channel FET 160, having a drain connected to node 120 and a source held at ground potential, receives the PWR_BYPASS signal at a gate 161. Thus, when the PWR_BYPASS signal is asserted, pull-down N-channel FET 160 is activated, thereby pulling down the voltage at internal node 120 to a logic low level. The logic low voltage level at internal node 120 causes inverter 130 to output a logic high output signal on output lead 132, thereby providing a deterministic high output state for pullup circuit 100 when in the power bypass mode.

Pullup circuit 100 operates as follows. When inverter 130 is generating a logic high signal on output lead 132 (i.e, N-tree 110 is pulling down the voltage at internal node 120), the gate of pulldown P-channel FET 140 receives the logic high signal via line 141 and is turned off. The "low" voltage at node 120 is determined by the device ratio of pullup FET 150 to N-tree 110, which is designed to be below the threshold voltage of inverter 130 (i.e., the voltage above which inverter 130 generates a logic low output signal and below which inverter 130 generates a logic high output signal).

Then, when N-tree 110 is not active (i.e., N-tree

110 no longer pulls down the voltage at internal node 120), pullup FET 150, begins to pull up the voltage at internal node 120. Once the voltage of internal node 120 rises above the threshold voltage of inverter 130, inverter 130 generates a logic low signal, which causes pulldown FET 140 to become relatively more conductive (i.e., able to conduct more current). As a result, pulldown FET 140 begins to reduce the pull up effect of pullup FET 150, causing the voltage at node 120 to only rise slightly above the threshold voltage of inverter 130. Thus, when N-tree 110 later receives an input signal or signals (not shown) causing N-tree 110 to pull down the voltage at internal node 120, N-tree 110 does not have as much voltage to pull down, thereby reducing the pulldown time.

Consequently, the ratio of the sizes of P-channel FETs 140 and 150 directly determines the "high" voltage level of internal node 120. The designer can attempt to optimize the pulldown and pullup speeds by adjusting the size ratio of P-channel FETs 140 and 150, basically "trading off" pullup speed for pulldown speed.

SUMMARY

In accordance with the present invention, a pullup circuit is provided having a limited voltage swing and fast pullup and pulldown times. According to one embodiment of the present invention, a pullup circuit comprises a pullup structure, a pulldown structure and an internal node. The internal node is coupled to an output lead of an N-tree. When active, the N-tree discharges the internal node to a source of ground potential and when inactive, disconnects the internal node from the source of ground potential.

The pullup circuit operates to limit the current of the pullup structure before the N-tree discharges the internal node, thereby reducing the pullup effect

of the pullup structure to reduce fall time and power consumption. Then the pullup circuit maximizes the current of the pullup structure after the N-tree has pulled down the internal node, thereby increasing the pullup effect of the pullup structure to reduce rise time. As a result, the voltage of the internal node both charges more quickly when the N-tree becomes inactive and discharges more quickly when the N-tree becomes active.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 (Prior Art) shows a schematic diagram of a conventional static pullup circuit.

FIG. 2 shows a schematic diagram of a pullup circuit according to one embodiment of the present invention.

FIG. 3 illustrates the voltage characteristics of the pullup circuit depicted in FIG. 2.

FIG. 4 shows a schematic diagram of a pullup circuit according to another embodiment of the present invention.

DETAILED DESCRIPTION

FIG. 2 shows static pullup circuit 200 according to one embodiment of the present invention. The same reference numbers are used between drawings when referring to elements having substantially identical structure and function. Pullup circuit 200 includes inverter 130 and a pullup structure 210 coupled to an internal node N1. Pullup structure 210 reduces the pull up effect of the pullup circuit, as compared to circuit 100 (FIG. 1), when internal node N1 is at the "high" voltage level. Therefore, pullup circuit 200 has a faster pullup speed for a given static power dissipation, or a lower static power dissipation for a given pullup speed.

Pullup structure 210 includes P-channel FETs 212 and T1 and N-channel FET T2. P-channel FET 212 has a source connected to the Vdd source and a drain connected to internal node N1 and serves as a pullup device for pulling up node N1. In this embodiment, voltage Vdd is approximately 3.3V. P-channel FET T1 has a gate coupled to output lead 132 via line 220, a drain coupled to the gate of P-channel FET 212 and a source coupled to internal node N1. N-channel FET T2 has a gate coupled to output lead 132 via line 220, a source held at ground potential, and a drain connected to gate 214 of FET 212.

Pullup circuit 200 operates as follows. When inverter 130 outputs a logic low signal (i.e., pullup transistor 212 has pulled up the voltage of internal node N1 to a logic high level), the gates of P-channel FET T1 and N-channel FET T2 receive the logic low signal via line 220. As a result, P-channel FET T1 becomes more conductive, whereas N-channel FET T2 becomes less conductive. Thus, P-channel FET T1 pulls up the voltage of gate 214 to be substantially equal to the voltage at internal node N1. Because the voltage at gate 214 is increased, pullup FET 212 becomes less conductive, thereby limiting the amount of current pullup FET 212 can conduct if N-tree 110 begins to pull down the voltage at internal node N1. Thus, N-tree 110 discharges the internal node more quickly because N-tree 110 is "pulling down" against the reduced pullup effect of pullup FET 212.

When N-tree 110 is active and pulls down the voltage at internal node N1 to below the threshold voltage of inverter 130, inverter 130 transitions to output a logic high signal on output lead 132. The gates of P-channel FET T1 and N-channel FET T2 receive the logic high signal via line 220. As a result, P-channel FET T1 becomes less conductive, whereas N-

channel FET T2 becomes more conductive. Thus, N-channel FET T2 pulls down the voltage of gate 214 to be substantially equal to ground potential, thereby increasing the current that pullup FET 212 can conduct. Accordingly, the current conducted by pullup FET 212 from the Vdd voltage source is now maximized to enable the fastest charge time for internal node N1 after N-tree 110 stops discharging internal node N1. Further, the voltage at internal node N1 is pulled up closer to the threshold voltage of inverter 130, thereby reducing the time needed for pullup FET 212 to pull the voltage at internal node N1 above the threshold voltage of inverter 130 after N-tree 110 stops discharging internal node N1.

After N-tree 110 stops discharging internal node N1 pullup FET 212 cannot pull up the voltage at internal node N1 any higher than a threshold voltage of pullup FET 212 (Vt) below voltage Vdd because otherwise pullup FET 212 will simply turn off. Accordingly, the voltage at internal node N1 has an upper limit of Vdd-Vt. Pullup circuit 200 is an improvement over pullup circuit 100 (FIG. 1) because pullup circuit 200 controls the current conducted by pullup FET 212 allowing the current to be a maximum during pullup and a minimum during pulldown.

FIG. 3 illustrates the voltage characteristics of pullup circuit 200. The x-axis is the voltage of an input signal received by N-tree 110 (not shown). When the input signal is asserted, N-tree 110 discharges internal node N1. The y-axis measures the voltage at either internal node N1 or output lead 132.

Curve 310 illustrates the voltage at internal node N1 as a function of voltage of the input signal to N-tree 110. Segment 311 of curve 310 illustrates the voltage of internal node N1 when the input signal to N-tree 110 is low. This low input voltage causes the N-

channel transistors in N-tree 110 to turn off, thereby allowing pullup FET 212 to pull up the voltage at internal node N1. As described above, the voltage at internal node N1 is limited to approximately 2.7V, which is approximately one Vt below the Vdd voltage of 3.3V. Section 312 of curve 310 illustrates the voltage at internal node N1 when the input voltage to N-tree 110 is high. This high input voltage causes the N-channel transistors in N-tree 110 to turn on, thereby discharging internal node N1. The voltage at internal node N1 at this point is determined by the device ratio of P-channel FET T1 and N-tree 110. The upper limit of the voltage swing of internal node N1 is unaffected by this ratio, but instead depends on the Vt of pullup FET 212, as described above.

Curve 320 illustrates the voltage at output lead 132 as a function of voltage of the input signal to N-tree 110. Segment 321 of curve 320 illustrates the voltage of output lead 132 when the input signal to N-tree 110 is low. This low input voltage causes the voltage of internal node N1 to be high as shown by segment 311, which causes inverter 130 to output a logic low signal at output lead 132. Section 322 of curve 320 illustrates the voltage at output lead 132 when the input voltage to N-tree 110 is high. This high input voltage causes the voltage at internal node N1 to be low, which causes inverter 130 to output a logic high signal at output lead 132.

FIG. 4 shows a schematic diagram of a pullup circuit 400 according to another embodiment of the present invention having a power bypass mode similar to pullup circuit 100 (FIG. 1). Pullup circuit 400 is substantially identical to pullup circuit 200 (FIG. 2), except that: N-channel FET T2 has its source connected to the source of ground potential through a N-channel FET T4; gate 214 is coupled to the Vdd source through a

P-channel FET T3; internal node N1 is coupled to the source of ground potential through a N-channel FET T5; and the addition of an inverter 410 coupled to receive the PWR_BYPASS signal and provide an inverted PWR_BYPASS signal to the gates of FETs T3 and T4.

In this embodiment, N-tree 110 comprises N-channel FETs 420 and 430. Of course, other embodiments of the N-tree are possible. N-channel FET 420 has a drain connected to internal node N1, a source coupled to a drain of N-channel FET 430 and a gate coupled to receive a S signal. N-channel FET 430 has a source coupled to a source of ground potential and a gate coupled to receive a Q signal. When signals S and Q are both asserted (i.e., at a logic high level), N-channel FETs 420 and 430 are both turned on, thereby pulling down the voltage at internal node N1. However, when one or both of signals S and Q are deasserted (i.e., at a logic low level), N-tree 110 no longer pulls down the voltage at internal node N1.

During normal operation, the PWR_BYPASS signal is deasserted (i.e., held to a logic low), thereby turning on N-channel FET T4 and turning off N-channel FET T5 and P-channel FET T3 through inverter 410. Because N-channel FET T4 is on, N-channel FET T2 is coupled to the source of ground potential just as in pullup circuit 200 (FIG. 2). Further, because P-channel FET T3 and N-channel FET T5 are off, these FETs have substantially no effect on pullup circuit 400. Accordingly, when the PWR_BYPASS signal is deasserted, pullup circuit 400 operates in substantially the same manner as pullup circuit 200 (FIG. 2).

The PWR_BYPASS signal is asserted (i.e., set to a logic high level) to enter the power bypass mode. The asserted PWR_BYPASS signal is inverted by inverter 410, causing P-channel FET T3 to become conductive and pull up the voltage at gate 214, thereby causing pullup FET

212 to turn off. Further, the inverted asserted PWR_BYPASS signal also turns off N-channel FET T4, thereby causing an open circuit in the DC current path from Vdd power source to the source of ground potential through P-channel FET T3 and N-channel FET T2. However, the asserted PWR_BYPASS signal turns on N-channel FET T5, thereby discharging internal node N1 to a logic low level. As a result, inverter 130 outputs a logic high signal on output lead 132, thereby providing a deterministic high output state for pullup circuit 400 when in the power bypass mode. The logic high signal on output lead 132 is also received at the gate of P-channel FET T1 via line 220, which turns off P-channel FET T1, thereby providing another open circuit in the DC current path between Vdd voltage source and the source of ground potential.

The foregoing has described the principles and preferred embodiments of the present invention. However, the invention should not be construed as being limited to the particular embodiments described. For example, different implementations of the N-tree may used. In addition, although the described embodiments are used in 3.3V circuits, other embodiments may be adapted for use in 5V circuits. Further, other embodiments may omit the inverter used to invert the PWR_BYPASS signal and use a N-channel FET for FET T3 and a P-channel FET for FET T4. Still further, embodiments may be adapted for implementation in different transistor technologies, such as JFETs, BiCMOS or bipolar technologies. Thus, the above-described embodiments should be regarded as illustrative rather than restrictive. Variations can be made to those embodiments by workers skilled in the art without departing from the scope of the present invention as defined by the following claims.

CLAIMS

We claim:

1. A method for decreasing the rise time and fall time of a pullup circuit, said method comprising the steps of:

limiting an amount of current a pullup structure can conduct to a first current value before an internal node in said pullup circuit is discharged including the step of coupling a voltage at said internal node to a gate of a transistor in said pullup structure; and

increasing the amount of current said pullup structure can conduct to a second current value after said internal node is discharged including the step of uncoupling said voltage at said internal node to said gate, wherein said second current value is greater than said first current value.

2. The method of claim 1 wherein said step of limiting said amount of current comprises the step of limiting said voltage at said internal node to a first voltage, wherein said first voltage is less than a supply voltage supplied to said pullup circuit.

3. The method of claim 2 wherein said first voltage is equal to said supply voltage less a threshold voltage of said transistor.

4. The method of claim 1 wherein said transistor is a P-channel transistor, whereby said step of coupling provides said voltage at said internal node to said gate thereby reducing the amount of current said P-channel transistor is capable of conducting.

5. The method of claim 1 wherein said step of

increasing the amount of current further comprises the step of coupling a source of a second voltage to said gate.

6. The method of claim 5 wherein said second voltage is ground potential.

7. The method of claim 6 wherein said transistor is a P-channel transistor, whereby said step of coupling a source of a second voltage increases the amount of current said P-channel transistor is capable of conducting.

8. A structure for decreasing the rise time and fall time of a circuit, said structure comprising:

a pullup structure;

means for limiting a current said pullup structure can conduct to a first current value before an internal node in said structure is discharged; and

means for increasing the current said pullup structure can conduct to a second current value after said internal node is discharged, wherein said second current value is greater than said first current value.

9. The structure of claim 8 wherein said means for limiting a current comprises means for limiting a voltage at said internal node to a first voltage, wherein said first voltage is less a supply voltage supplied to said circuit.

10. The structure of claim 9 wherein said first voltage is substantially equal to said supply voltage minus a threshold voltage of a transistor.

11. The structure of claim 8 wherein said means for limiting a current comprises means for coupling said internal node to said pullup structure.

12. The structure of claim 11 wherein said means for coupling comprises means for coupling said internal node to a gate of a P-channel transistor, whereby a voltage of said internal node is provided to said gate, thereby reducing the amount of current said P-channel transistor is capable of conducting.

13. The structure of claim 8 wherein said means for increasing the current comprises means for coupling a source of a second voltage to said pullup structure.

14. The structure of claim 13 wherein said second voltage is ground potential.

15. The structure of claim 14 wherein said means for coupling a source of a second voltage comprises means for applying ground potential voltage to a gate of a P-channel transistor, thereby increasing the amount of current said P-channel transistor is capable of conducting.

16. A pullup circuit comprising:

an internal node;

an inverter having an input lead coupled to said internal node;

a pullup structure comprising a first transistor having a first current handling terminal coupled to a first voltage source and a second current handling terminal coupled to said internal node and a second transistor having a gate coupled to an output lead of said inverter and a first current handling terminal coupled to a

gate of said first transistor and a second current handling terminal coupled to said internal node.

17. The pullup circuit of claim 16 wherein said pullup structure further comprises:

a third transistor having a gate coupled to said output lead of said inverter, a first current handling terminal coupled to said gate of said first transistor and a second current handling terminal coupled to a second voltage source.

18. The pullup circuit of claim 16 wherein said pullup structure is capable of alternately forming a first current path between said gate of said first transistor and said internal node and a second current path between said gate of said first transistor and a second voltage source.

19. The pullup circuit of claim 16 wherein the amount of current said first transistor conducts has a first current value when a voltage at said internal node is greater than a threshold voltage of said inverter and wherein the amount of current said first transistor conducts has a second current value when said voltage at said internal node is less than said threshold voltage, said second current value being greater than said first current value.

20. The pullup circuit of claim 16 wherein said first transistor turns off when said internal node reaches a particular voltage, thereby limiting said internal node to said particular voltage, said particular voltage being less than a voltage of said first voltage source.

21. The pullup circuit of claim 20 wherein said

particular voltage is equal to said voltage of said first voltage source less a threshold voltage of said first transistor.

22. The pullup circuit of claim 16 wherein said first transistor is a P-channel transistor whereby a voltage at said internal node is provided to said gate of said P-channel transistor thereby reducing the amount of current said P-channel transistor conducts when said voltage at said internal node is greater than a threshold voltage of said inverter.

23. The pullup circuit of claim 17 wherein said second voltage source provides a ground potential and wherein said first transistor is a P-channel transistor whereby said ground potential is provided to said gate of said P-channel transistor thereby increasing the amount of current said P-channel transistor conducts when a voltage at said internal node is less than a threshold voltage of said inverter.

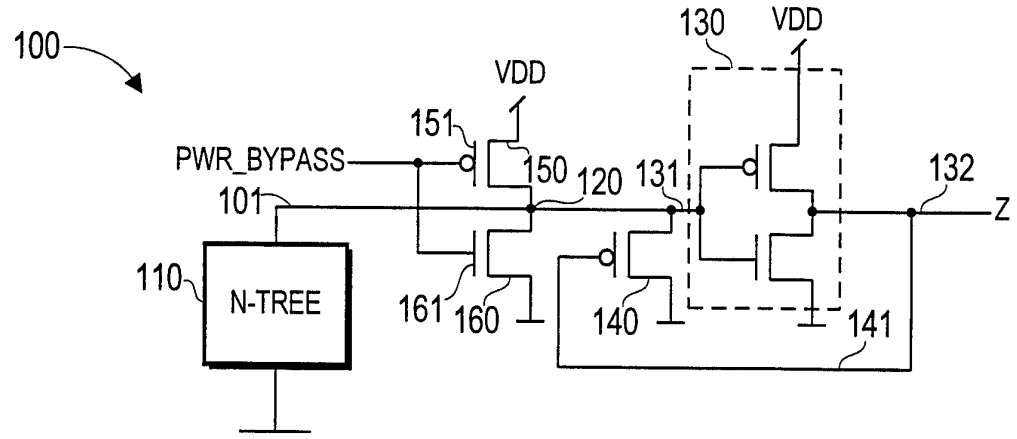


FIG. 1
PRIOR ART

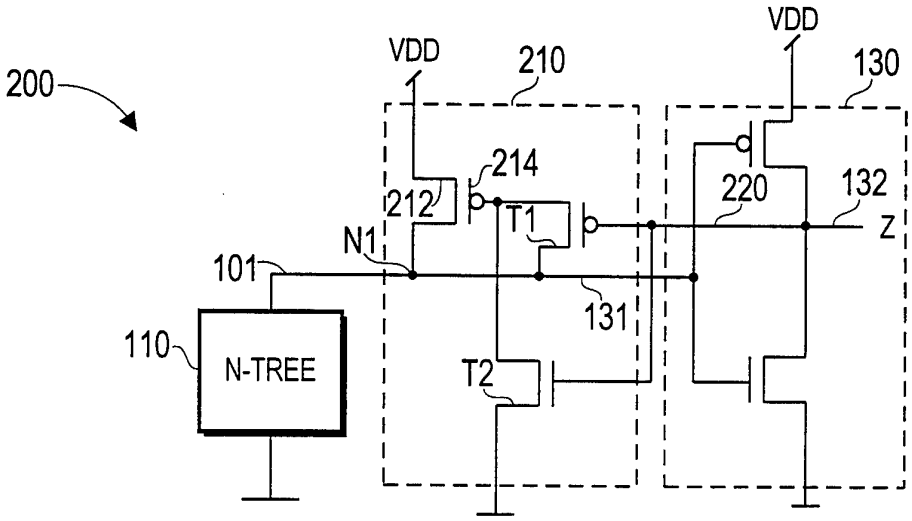
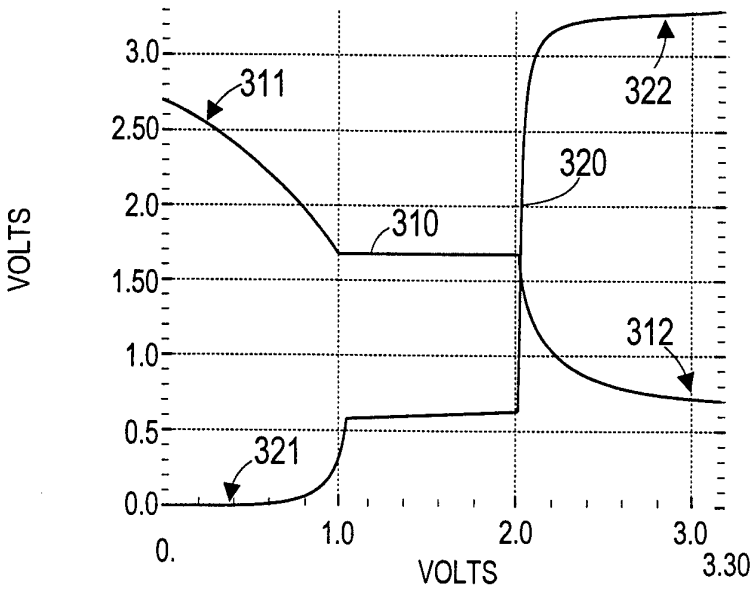


FIG. 2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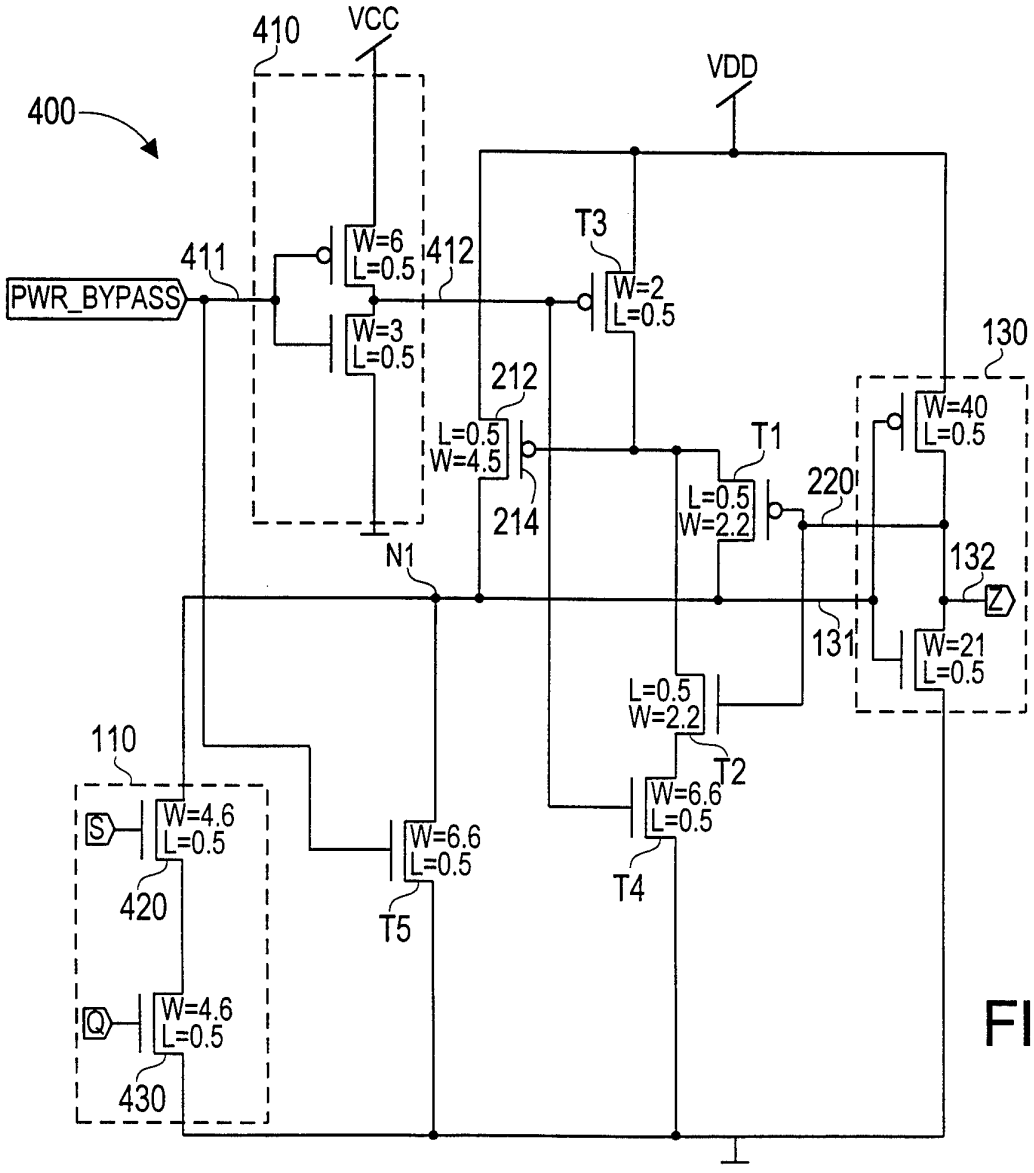
2.0
3.0
3.30
VOLTS

FIG. 3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VCC
VDD
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PWR_BYPASS
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Z
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T2
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L=0.5
T4
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W=6.6
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T5
Q
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430

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/10480

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H03K 19/094, 19/0948.
US CL :327/112, 374, 391, 437.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 327/108, 112, 313, 374, 375, 376, 377, 391, 434, 437, 483.

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

N/A

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS: CMOS, PULL UP, PULL DOWN, LIMIT? (5A) CURRENT?, LIMIT? VOLTAGE SWING?.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A ,P	US, A, 5,450,356 (MILLER) 12 September 1995, col. 1.	1-23
A, P	US, A, 5,430,335 (TANOI) 04 July 1995.	1-23
A	US, A, 5,426,385 (LAI) 20 June 1995, Fig. 3.	1-23
Y	US, A, 5,404,051 (KOBAYASHI) 04 April 1995, Fig. 7.	16, 18-22.
A	US, A, 4,985,644 (OKIHARA ET AL) 15 January 1991.	1-23
X	US, A, 4,918,341 (GALBRAITH ET AL) 17 April 1990, Fig. 3.	1-15.
A	US, A, 4,883,975 (ENOMOTO ET AL) 28 November 1989.	1-23

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 308-7722	Authorized officer MYTRANG TON Telephone No. (703) 308-4868

Form PCT/ISA/210 (second sheet)(July 1992)*

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PCT/US96/10480

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US, A, 4,806,787 (KATO ET AL) 21 February 1989.	1-23
A	US, A, 4,542,310 (ELLIS ET AL) 17 September 1985.	1-23