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(54) **SUBSTRATE COMPRISING DIFFERENT TYPES OF SURFACES AND METHOD FOR OBTAINING SUCH SUBSTRATES**

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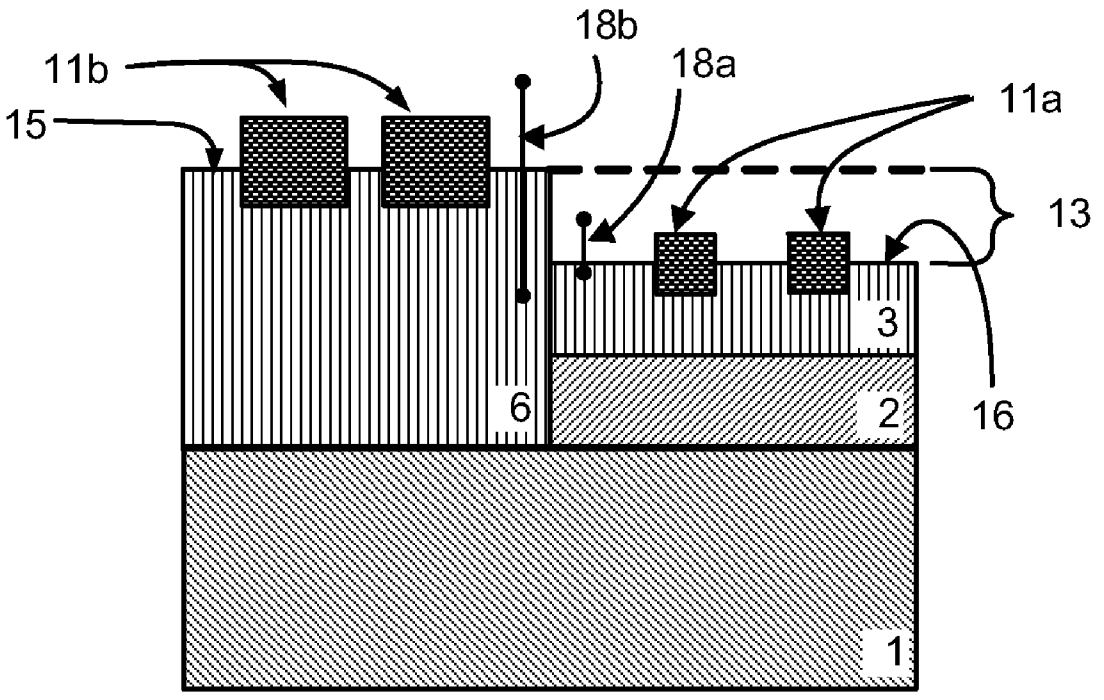
(57) **ABSTRACT**

A support having a larger density of crystalline defects, an insulating layer disposed on a first region of a front face of the support, and a superficial layer disposed on the insulating layer. An additional layer can be disposed at least on a second region of the front face of the support has a thickness sufficient to bury crystalline defects of the support. A substrate can also include an epitaxial layer arranged at least over the first region of the front face of the support, between the support and the insulation layer. Also, a method of making the substrate by forming a masking layer on the first region of the superficial layer and removing the superficial layer and the insulating layer in the second region uncovered by the masking layer. The additional layer is formed in the second region and then planarized.



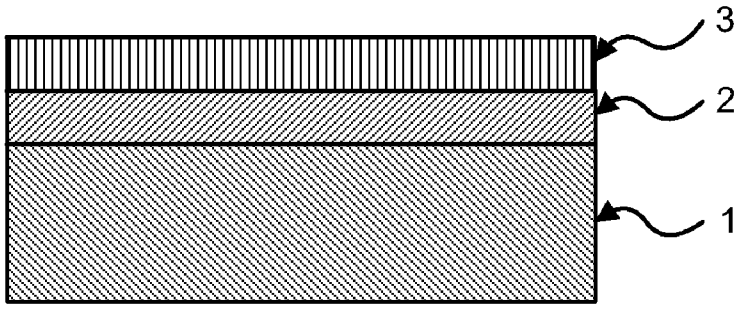


Figure 1

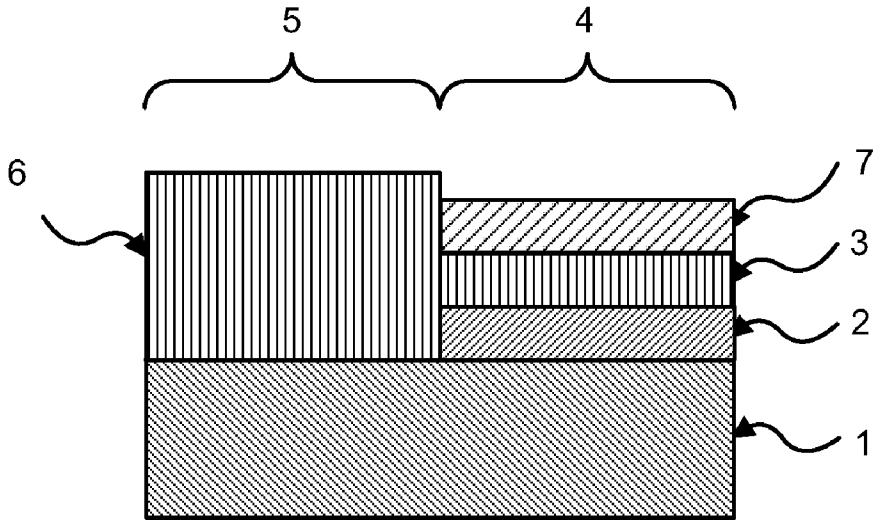


Figure 2

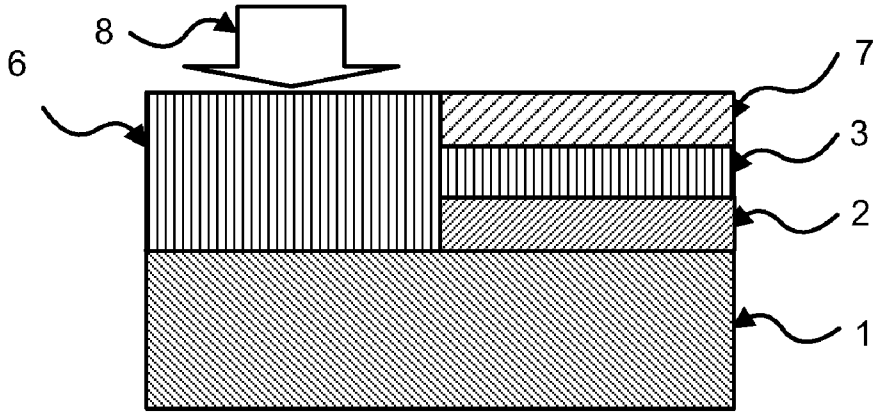


Figure 3

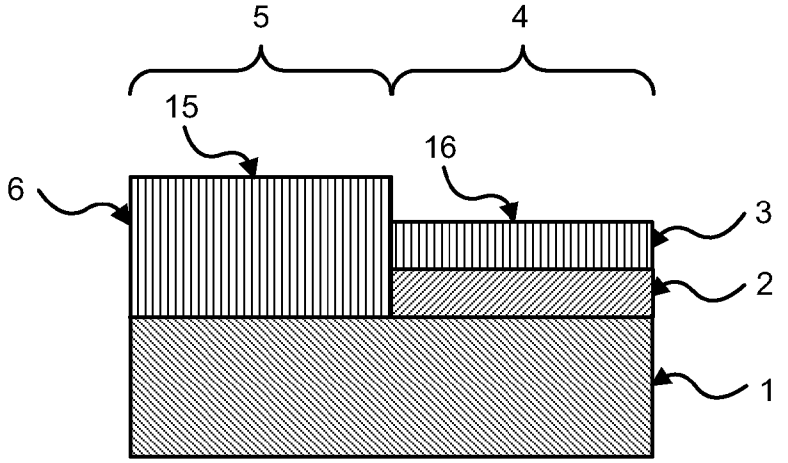


Figure 4

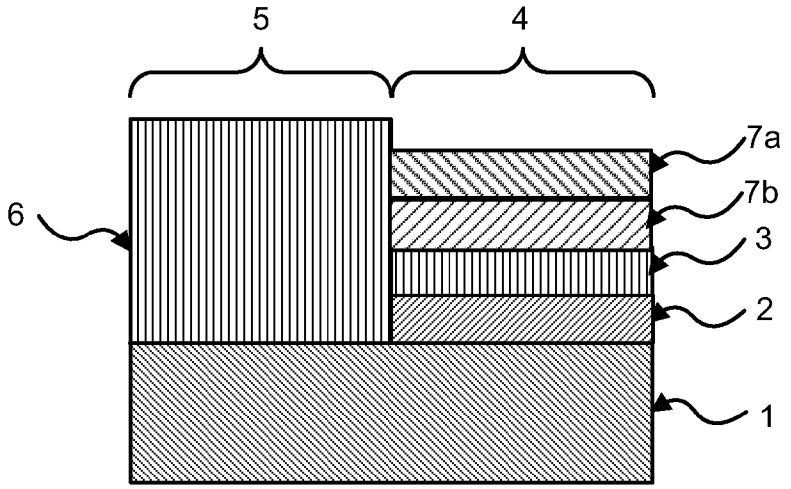


Figure 5

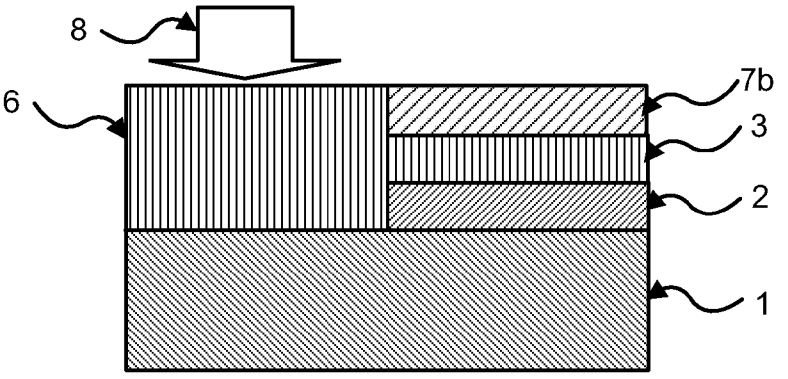


Figure 6

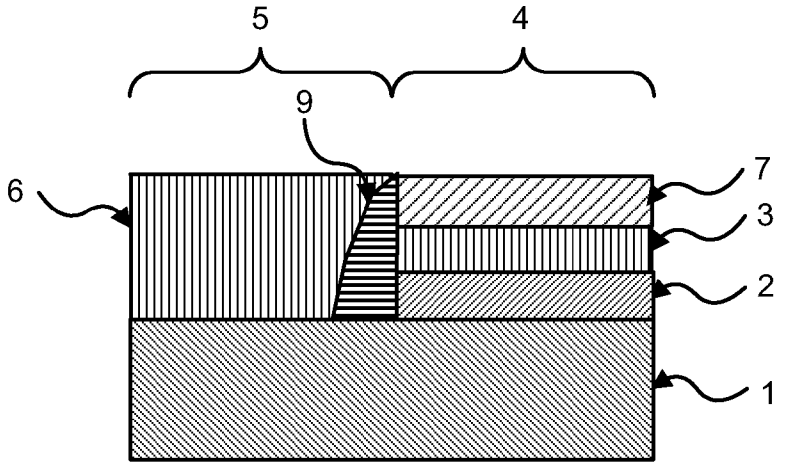


Figure 7

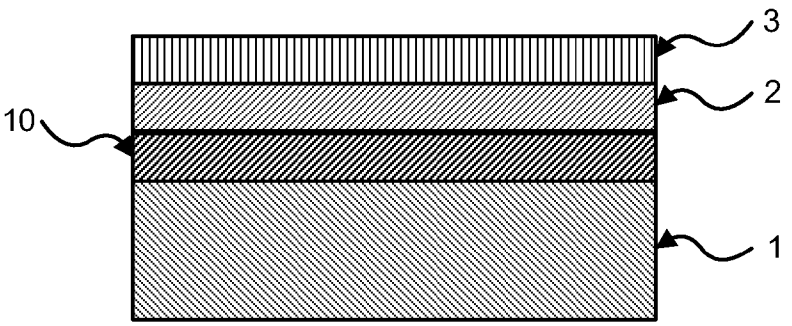


Figure 8

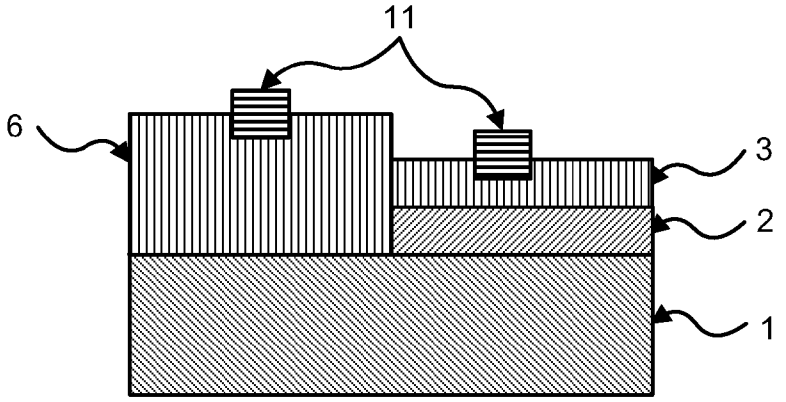


Figure 9

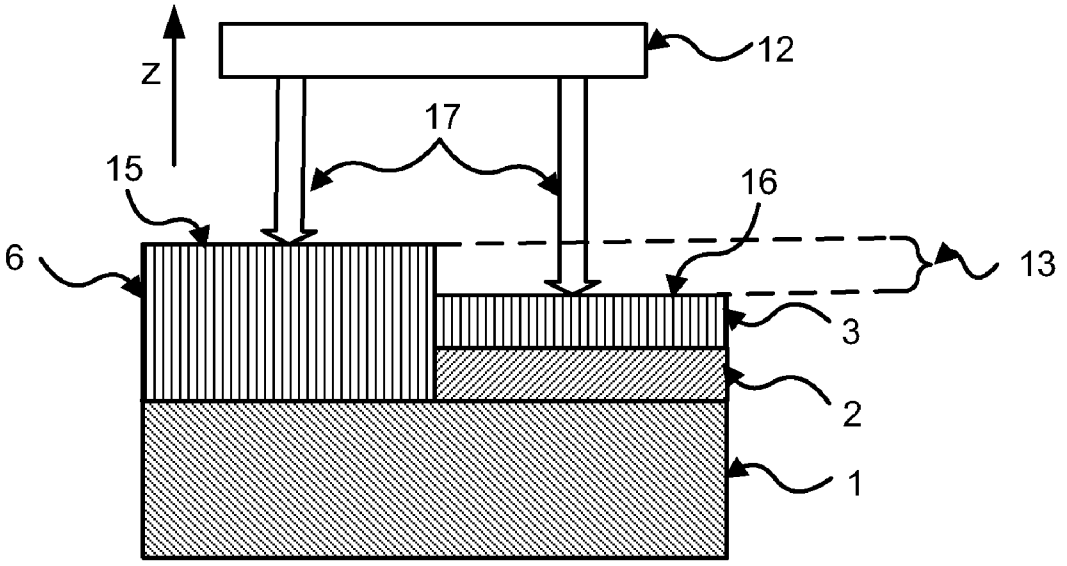


Figure 10

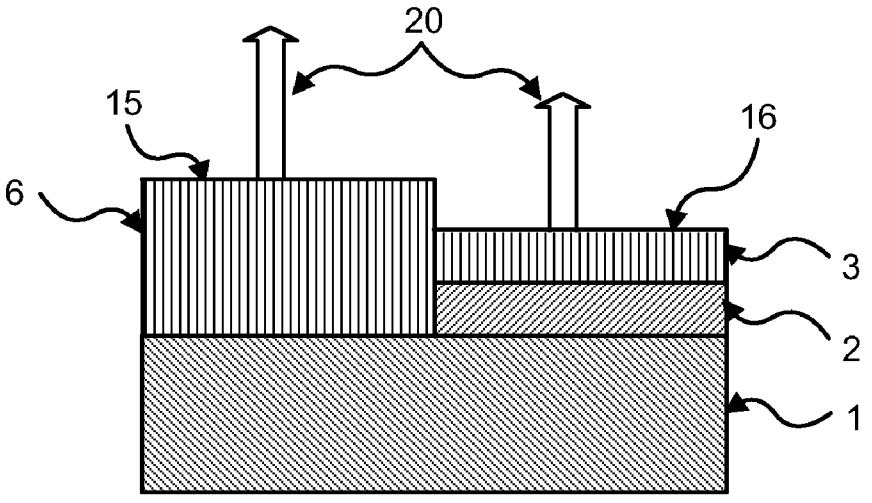


Figure 11

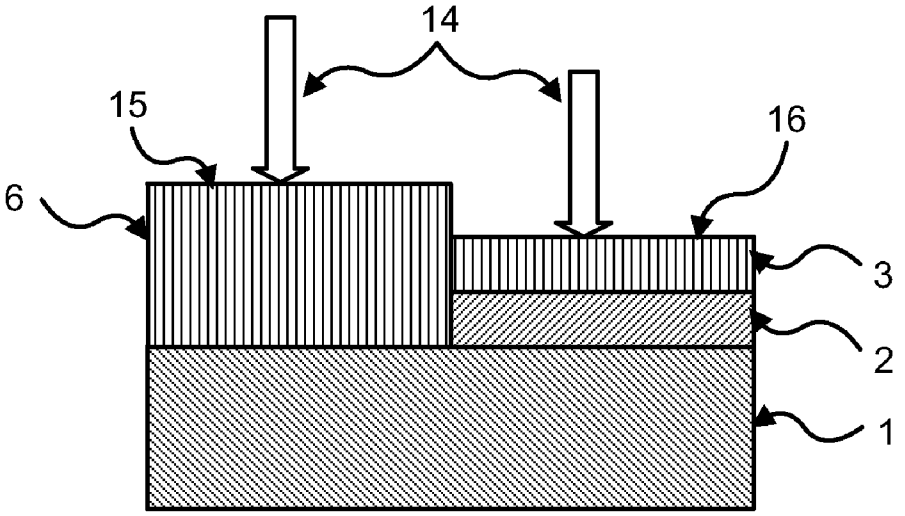


Figure 12

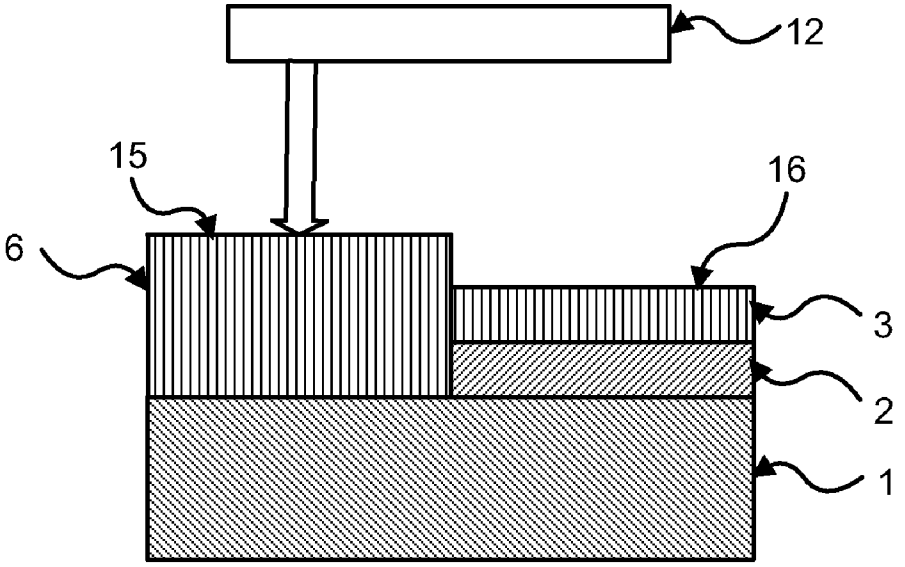


Figure 13

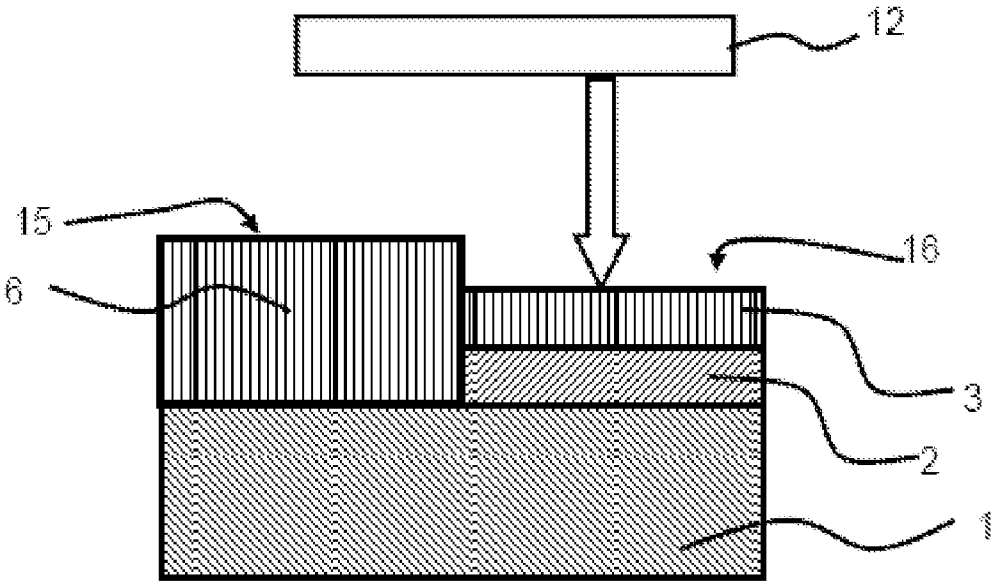


Figure 14

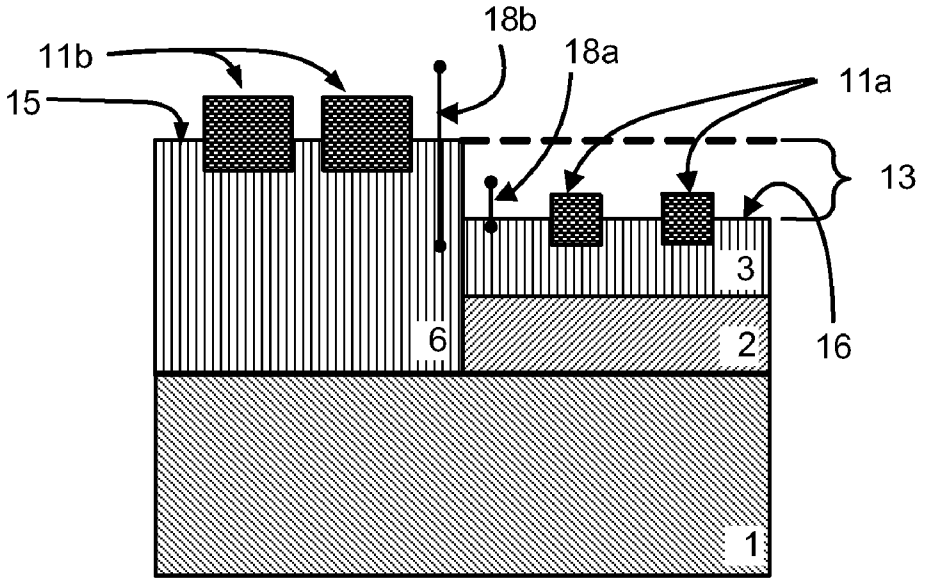


Figure 15

SUBSTRATE COMPRISING DIFFERENT TYPES OF SURFACES AND METHOD FOR OBTAINING SUCH SUBSTRATES

FIELD OF THE INVENTION

[0001] The present invention relates to substrates for semiconductor fabrication, and in particular to patterned substrates of satisfactory crystalline quality and comprising bulk areas and SOI (Silicon on Insulator) areas.

BACKGROUND OF THE INVENTION

[0002] Microelectronic devices are typically manufactured on either bulk semi-conductor substrates or on SOI substrates (Silicon on Insulator). It has also been proposed to use composite substrates comprising bulk areas and SOI areas. See, e.g., U.S. Pat. No. 6,955,971. The fabrication of such patterned substrates is generally difficult because it requires formation of local areas of a buried oxide next to bulk areas. In the case of wafer bonding methods, such local oxide areas can be formed either on the top wafer or the base wafer, and can give rise to so-called "dishing" problems. In the case of a SIMOX type methods (Separation by Implanted Oxygen), such local oxide areas are commonly formed in the original wafer, but the differential thermal expansion of silicon oxides versus silicon gives rise to stress, etc.

SUMMARY OF THE INVENTION

[0003] The present invention provides fabrication methods for patterned substrates of satisfactory crystalline quality and comprising bulk areas and SOI areas. The invention also provides substrates fabricated by the provided methods.

[0004] Substrates of the invention comprise an insulating layer disposed on a first region of a front face of a support, a superficial layer disposed on the insulating layer and an additional layer disposed at least on a second region of the front face of the support, the additional layer having an exposed surface over the second region.

[0005] In preferred embodiments, the invention provides a substrate comprising a support having crystalline defects of a size greater than 10 nm at a density greater than $10^3/cm^3$ or greater than $10^5/cm^3$, an insulating layer disposed on a first region of a front face of the support, a superficial layer disposed on the insulating layer, and an additional layer disposed at least on a second region of the front face of the support, the additional layer having an exposed surface over the second region, and has a thickness sufficient to bury crystalline defects of the support. Preferably, the substrate comprises an epitaxial layer arranged over the first region of the front face of the support, between the support and the insulation layer.

[0006] In preferred embodiments, the invention provides methods of manufacturing a semiconductor structure which includes providing a substrate comprising a support, a continuous insulating layer disposed on a front face of the support and a superficial layer disposed on the insulating layer, then forming a masking layer on a first region of the superficial layer, then removing the superficial layer and the insulating layer in a second region uncovered by the masking layer, and then forming an additional, preferably planarized, layer in the second region.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] Other features and advantages of the invention will become apparent from the following description and the appended drawings:

[0008] FIG. **1** illustrates embodiments of the methods and substrates of the invention;

[0009] FIG. **2** illustrates further embodiments of the methods and substrates of the invention;

[0010] FIG. **3** illustrates further embodiments of the methods and substrates of the invention;

[0011] FIG. **4** illustrates further embodiments of the methods and substrates of the invention;

[0012] FIG. **5** illustrates further embodiments of the methods and substrates of the invention;

[0013] FIG. **6** illustrates further embodiments of the methods and substrates of the invention;

[0014] FIG. **7** illustrates further embodiments of the methods and substrates of the invention;

[0015] FIG. **8** illustrates further embodiments of the methods and substrates of the invention;

[0016] FIG. **9** illustrates further embodiments of the methods and substrates of the invention;

[0017] FIG. **10** illustrates embodiments of the invention that include the formation electronic devices;

[0018] FIG. **11** illustrates further embodiments of the invention that include the formation electronic devices;

[0019] FIG. **12** illustrates further embodiments of the invention that include the formation electronic devices;

[0020] FIG. **13** illustrates further embodiments of the invention that include the formation electronic devices;

[0021] FIG. **14** illustrates further embodiments of the invention that include the formation electronic devices;

[0022] FIG. **15** illustrates another embodiment of the invention that includes forming electronic devices.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0023] The preferred embodiments and particular examples described herein should be seen as examples of the scope of the invention, but not as limiting the present invention. The scope of the present invention should be determined with reference to the claims.

[0024] FIGS. **1** to **3** illustrate preferred embodiments of the substrates and methods of the invention. In particular, FIG. **1** illustrates a substrate comprising support **1**, continuous insulating layer **2** disposed on front face of support **1**, and superficial layer **3** disposed on insulating layer **2**, so as to form, e.g., an SOI substrate (silicon on insulator). FIG. **2** illustrates that masking layer **7** is formed on first region **4** of superficial layer **3**. After removing superficial layer **3** and insulating layer **2** in second region **5** not covered by masking layer **7**, additional layer **6** can then be formed in second region **5**, preferably by epitaxy. FIG. **3** illustrates that additional layer **6** is then planarized, e.g., down to the top level of masking layer **7**, as shown by arrow **8**. The planarization can be carried out by polishing, e.g. by chemical mechanical polishing (CMP).

[0025] FIG. **4** illustrates embodiments of substrates that result from the above methods after final removal of masking layer **7**. The resulting substrates comprise support **1**, insulating layer **2** disposed on first region **4** of front face of support **1**, and superficial layer **3** disposed on insulating layer **2**. Additional layer **6** is disposed at least on second region **5** of the front face of support **1** and has exposed surface **15** over second region **5**. Since exposed surface **15** of additional layer **6** was planarized down to the top level of masking layer **7**, this exposed surface will not necessarily be coplanar with exposed surface **16** after removing masking layer **7**.

[0026] Support **1** and superficial layer **3** can comprise different semi-conducting materials or the same semi-conducting material but with different crystalline orientations, or both. Electronic devices can then be formed in the different materials. Support **1** and superficial layer **3** preferably comprise silicon, germanium, silicon-germanium, or III-V-type semi-conducting materials such as InP, GaN, or GaAs, optionally in a strained state. For instance, germanium could be chosen for PMOS transistors, and III-V-type semi-conducting materials for NMOS transistors, whereas silicon can be used for input-output-circuits and analog circuits.

[0027] Insulating layer **2** preferably can have a thickness less than 140 nm, and more preferably between 2 nm and 25 nm or less than 25 nm. Superficial layer **3** preferably has a thickness less than 100 nm and more preferably between 5 nm and 50 nm. In particular, layer **3** preferably has a thickness between 12 nm and 20 nm for planar full depletion SOI transistors, or between 20 nm and 50 nm for vertical multiple gate transistors.

[0028] Additional layer **6** preferably has a thickness sufficient to bury some or all of the crystalline defects present in support **1**. For example, additional layer **6** can have a thickness of 0.1 micron or more. It is understood that the term "burying" is used herein to describe a layer of sufficient thickness to substantially limit defects that are present at the lower surface of a burying layer from propagating to, and appearing on, the upper surface of the burying layer. Exposed surface **15** of additional layer **6** can then have a suitable crystalline quality and a suitable density of defects even if the front face of the substrate has a density of crystalline defects of a size greater than 10 nm of greater than $10^3/cm^3$ or even greater than $10^5/cm^3$. Since the front surface of support **1** can have a greater density of defects, it can consequently be less expensive.

[0029] Also, the thickness of additional layer **6** before planarizing is preferably greater than the combined thicknesses of superficial layer **3**, insulating layer **2** and masking layer **7**. The planarizing of additional layer **6** can then be stopped at the top level of masking layer **7**. Additional layer **6** can comprise materials with a crystalline orientation different than the crystalline orientation of superficial layer **3**, and can comprise materials different than those of superficial layer **3**.

[0030] Masking layer **7** preferably has a thickness between 20 nm and 100 nm, and more preferably has a thickness of 50 nm or less, and comprises an oxide material.

[0031] FIGS. **5** and **6** illustrate further preferred embodiments of the substrates and methods of the invention. Here, masking layer **7** in FIG. **5** comprises upper layer **7***a* and lower layer **7***b*. FIG. **6** illustrates that upper layer **7***a* is preferably removed before planarizing additional layer **6**, which can then be stopped at the top level of remaining lower layer **7***b*.

[0032] Upper layer **7***a* of masking layer **7** can comprise, for instance, a nitride material with a thickness between 10 nm and 100 nm, and lower layer **7***b* can comprise, for instance, an oxide material with a thickness between 5 nm and 20 nm. If layer **7** comprises only a single layer oxide mask, it should be thicker, for example between 20 nm and 120 nm.

[0033] FIG. **7** illustrates further preferred embodiments of the substrates and methods of the invention. Here, the substrates of the invention comprise insulator spacer **9** that is formed in order to seal laterally superficial layer **3** and insulating layer **2**. After spacer **9** has been formed, additional layer **6** can be grown.

[0034] FIG. **8** illustrates further preferred embodiments of the substrates and methods of the invention. Here, the substrates of the invention comprise initial epitaxial layer **10** preferably having a thickness greater than 0.1 micron and preferably arranged on the front face of the support, between support **1** and continuous insulation layer **2**, or at least arranged on the first region of support, and. Epitaxial layer **10** preferably has a density of crystalline defects with a size greater than 10 nm of less than $10^3/cm^3$. Then support **1** that can have a density of crystalline defects of a size greater than 10 nm of more than $10^3/cm^3$ or more than $10^5/cm^3$.

[0035] Since the epitaxial layer buries, at least partially, defects present at the surface of the front side of support **1**, the thickness of additional layer **6** that is also used for burying defects can be less than in the case where no epitaxial layer **10** is formed.

[0036] FIG. **9** illustrates further preferred embodiments of the substrates and methods of the invention. Here, the substrates further comprise electronic devices **11** in or on additional layer **6** and in or on superficial layer **3**.

[0037] FIGS. **10** to **14** illustrate embodiments of methods of the invention for fabricating the substrates of FIG. **9**. In general, these methods include steps of lithography, etching, and implantation.

[0038] More specifically, FIGS. **10-12** illustrate embodiments of these methods that form devices in or on additional layer **6** and in or on superficial layer **3** during the course of a single device forming process (a single sequence of steps). In other words, the devices can be considered as being formed "at the same time" or "simultaneously" because their formation shares common steps. FIG. **10** illustrates a first lithography step comprising projecting or forming lithographic images on selected portions of exposed surface **15** of additional layer **6** and at the same time on selected portions of exposed surface **16** of superficial layer **3**. Such projecting or forming can be performed by irradiating (arrows **17**) by means of image forming apparatus **12**. This lithography (arrows **17** in FIG. **10**) can be carried out simultaneously for both exposed surfaces **15** and **16**, when offset height **13** is less than the depth of focus of the image forming apparatus required for a predetermined image resolution. The smallest pattern and greatest resolution is usually determined by the gate length.

[0039] Here, exposed surfaces **15** and **16** are illustrated as being offset by offset height **13** which is preferably less than the depth of focus of a lithography exposure (along a Z-axis perpendicular to the surface of substrate) made by image forming apparatus **12** that corresponds to a predetermined resolution. The depth of focus depends on the image forming apparatus used and on the resolution required by the process applied.

[0040] In other words, images of the predetermined resolution can be formed simultaneously on both exposed surfaces **15** and **16** if the depth of focus of the selected lithography tool corresponding to the predetermined image resolution is greater than offset height **13**. In cases of lower image resolution, offset height **13** of less than 100 nm can be sufficient for the offset height **13** to be less than the depth of focus corresponding to the lower resolution. In cases of higher image resolution (needed for smaller structures), the depth of focus is preferably small and the offset height **13** is preferably even smaller, e.g., 50 nm or less. Generally, offset height **13** is preferably less than 100 nm, and more preferably less than 50 nm.

[0041] FIG. **11** illustrates a next step of etching (arrows **20**) that can be performed at the same time from both exposed surfaces **15** and **16**.

[0042] FIG. **12** illustrates a further next step of implantation (arrows **14**) that can be performed at the same time into exposed surfaces **15** and **16**.

[0043] FIGS. **13** and **14** illustrate embodiments of further methods of the invention for fabricating the substrates of FIG. **9**. Here, devices are formed in or on additional layer **6** and in or on superficial layer **3** by performing distinct lithography steps for each exposed surface. This embodiment is advantageous when the exposed surfaces are offset by a height greater than the depth of focus (along an axis Z perpendicular to the substrate) of the image forming apparatus corresponding to a lithography exposure of the predetermined resolution.

[0044] FIG. **13** illustrates a distinct lithography step for exposed surface **15**.

[0045] FIG. **14** illustrates a separate distinct lithography step for exposed surface **16**.

[0046] In these embodiments, etching and implantation steps can still be carried out simultaneously for both exposed surfaces **15** and **16**. Alternatively, distinct etching steps and/or distinct implantation steps can be performed.

[0047] FIG. **15** illustrates further embodiments of the methods of the invention in which a single lithography step is preformed for exposed surface **15** of additional layer **6** and for exposed surface **16** of superficial layer **3** even though offset height **13** is greater than the depth of focus of the image forming apparatus corresponding to certain required precisions. In this embodiment, different types of electronic devices having different required resolutions are formed in additional layer **6** and in superficial layer **3** (and optionally in the additional superficial layer described below).

[0048] For example, small electronic devices **11***a*, e.g., memory devices, can be formed in superficial layer **3** (and optionally in the additional superficial layer) and large electronic devices **11***b*, e.g., logic devices, can be formed in additional layer **6**, or conversely. The centre of focus of lithography is preferably adjusted to the level where the smallest devices with the highest required image resolution are formed, e.g. to superficial layer **3**. Even if the other level, e.g. exposed surface **15** of additional layer **6**, is beyond depth of focus **18***a* corresponding to the highest resolution, one single simultaneous lithography step can be used because the image resolution on the level beyond the depth of focus corresponding to the highest resolution can be sufficient for the larger devices formed therein which need only a lower resolution.

[0049] In other words, first depth of focus **18***a* can be associated to the first level with a higher required image resolution, e.g. superficial layer **3**, and second depth of focus **18***b* can be associated to the second level with a lower required resolution, e.g. exposed surface **15** of additional layer **6**. Depth of focus **18***b*, suitable for a lower image resolution, is typically larger than, and overlaps, depth of focus **18***a*, suitable for a higher resolution. Thus when considering two distinct depths of focus **18***a* and **18***b*, the lithography on exposed surface **15** of additional layer **6** is in fact within larger depth of focus **18***b*, while at the same time the lithography on exposed surface **16** of superficial layer **3** is in fact within smaller depth of focus **18***a*.

[0050] This approach is not limited to the particular stacks of layers **1**, **2**, **3** but can also be implemented with other substrates having several different levels in which electronic devices should be formed. This is for instance the case with a bulk substrate having two or more different surface levels.

[0051] For example, a substrate (not shown in the figures) useful for the practice of the invention can comprise an additional insulating layer disposed on an additional selected region of superficial layer **3** and an additional semi-conducting superficial layer disposed on the additional insulating layer. A substrate with an additional insulating layer and additional semi-conducting superficial layer can be manufactured by Smart Cut™. Then the four following layers are removed in second region **5** of the substrate: the additional insulating layer, the additional semi-conducting superficial layer, superficial layer **3** and insulating layer **2**. In the remaining regions only the additional insulating layer and the additional semi-conducting superficial layer are removed except in an additional selected region where the electronic devices are formed in the additional superficial layer.

[0052] Electronic devices can then be formed simultaneously in (or on) three levels of such a substrate by the methods of the invention. When the difference in height of the three levels is less than the depth of focus of the process used, lithography, etching and implantation steps are preferably carried out simultaneously. Even when the depth of focus is smaller than the difference in height, these steps can be carried out simultaneously in certain cases, for example when the resolution required in an upper level (or in a lower level) is not as high as in the other levels.

What is claimed is:

1. A semiconductor structure useful for the fabrication of semiconductor devices comprising:

a support having a front face and crystalline defects with a size greater than 10 nm at a density greater than $10^3/cm^3$;

an insulating layer disposed on a first region of the front face of the support;

a superficial layer disposed on the insulating layer and having an exposed surface; and

an additional layer disposed at least on a second region of the front face of the support, the additional layer having an exposed surface and a thickness sufficient to bury the crystalline defects of the support.

2. The structure of claim **1** wherein the additional layer has a thickness greater than 0.1 micron.

3. The structure of claim **1** further comprising an epitaxial layer arranged on at least the first region of the front face of the support and between the support and the insulating layer.

4. The structure of claim **3** wherein the epitaxial layer has a thickness greater than 0.1 micron.

5. The structure of claim **1** wherein the exposed surface of the additional layer is not coplanar with the exposed surface of the superficial layer.

6. The structure of claim **1** wherein the exposed surface of the additional layer and the exposed surface of the superficial layer are offset by less than 100 nm.

7. The structure of claim **1** wherein the additional layer has one crystalline orientation, and wherein the superficial layer has a different crystalline orientation.

8. The structure of claim **1** wherein the additional layer and the superficial layer comprise different materials.

9. A method of manufacturing a semiconductor structure useful for the fabrication of semiconductor devices comprising:

providing a substrate comprising a support, a continuous insulating layer disposed on a front face of the support, and a superficial layer disposed on the insulating layer;

forming a masking layer on a first region of the superficial layer;

removing the superficial layer and the insulating layer in a second region not covered by the masking layer;

forming an additional layer in the second region; and

planarizing the additional layer.

10. The method of claim **9** wherein the thickness of the additional layer is greater than a combined thickness of the superficial layer, the insulating layer, and the masking layer.

11. The method of claim **9** wherein planarizing of the additional layer is terminated at the masking layer.

12. The method of claim **9** wherein the masking layer comprises an oxide material with a thickness between 10 nm and 50 nm.

13. The method of claim **9** further comprising, before planarizing, removing an upper layer of the masking layer so as to leave a remaining lower layer of the masking layer, and wherein the planarizing of the additional layer is terminated at the remaining lower layer.

14. The method of claim **13** wherein the upper layer comprises a nitride material and the lower layer comprises an oxide material.

15. The method of claim **9** further comprising, before forming the additional layer, forming an insulator spacer for sealing laterally the superficial layer and the insulating layer.

16. The method of claim **9** wherein the support comprises crystalline defects, and wherein the additional layer has a sufficient thickness to bury the crystalline defects present in the support.

17. The method of claim **9** further comprising forming at the same time electronic devices in the additional layer and in the superficial layer.

18. The method of claim **17** further comprising:

performing a single lithographic exposure on the exposed surface of the second region and on the exposed surface of the superficial layer by use of an image forming apparatus, wherein both exposed surfaces are within a first depth of focus of the image forming apparatus corresponding to a first predetermined image resolution so that the exposures on both surfaces are within the first predetermined image resolution;

performing a single etching step of both exposed surfaces; and

performing a single implantation step into both exposed surfaces.

19. The method of claim **18** wherein a selected one of the exposed surface is within a second depth of focus corresponding to a second higher predetermined image resolution, and wherein the first depth of focus overlaps the second depth of focus so that the selected surface is within the second depth of focus while the other surface is within the first depth of focus.

20. The method according of claim **17** further comprising:

performing a first distinct lithographic exposure on an exposed surface of the second region;

performing a second distinct lithographic exposure on an exposed surface of the superficial layer;

performing a single etching step of both exposed surfaces; and

performing a single implantation step into both exposed surfaces.

* * * * *