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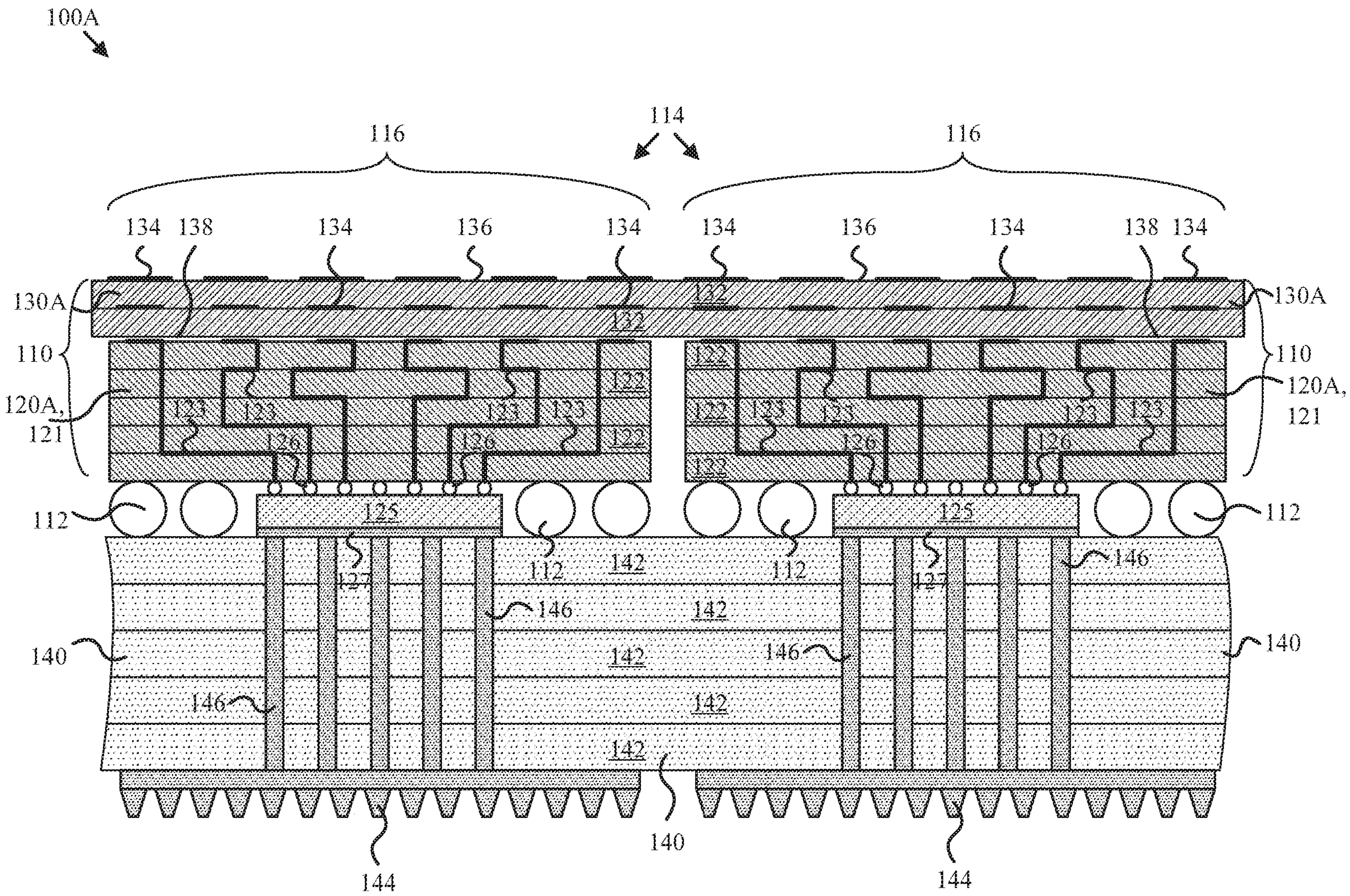

Fig. 1A

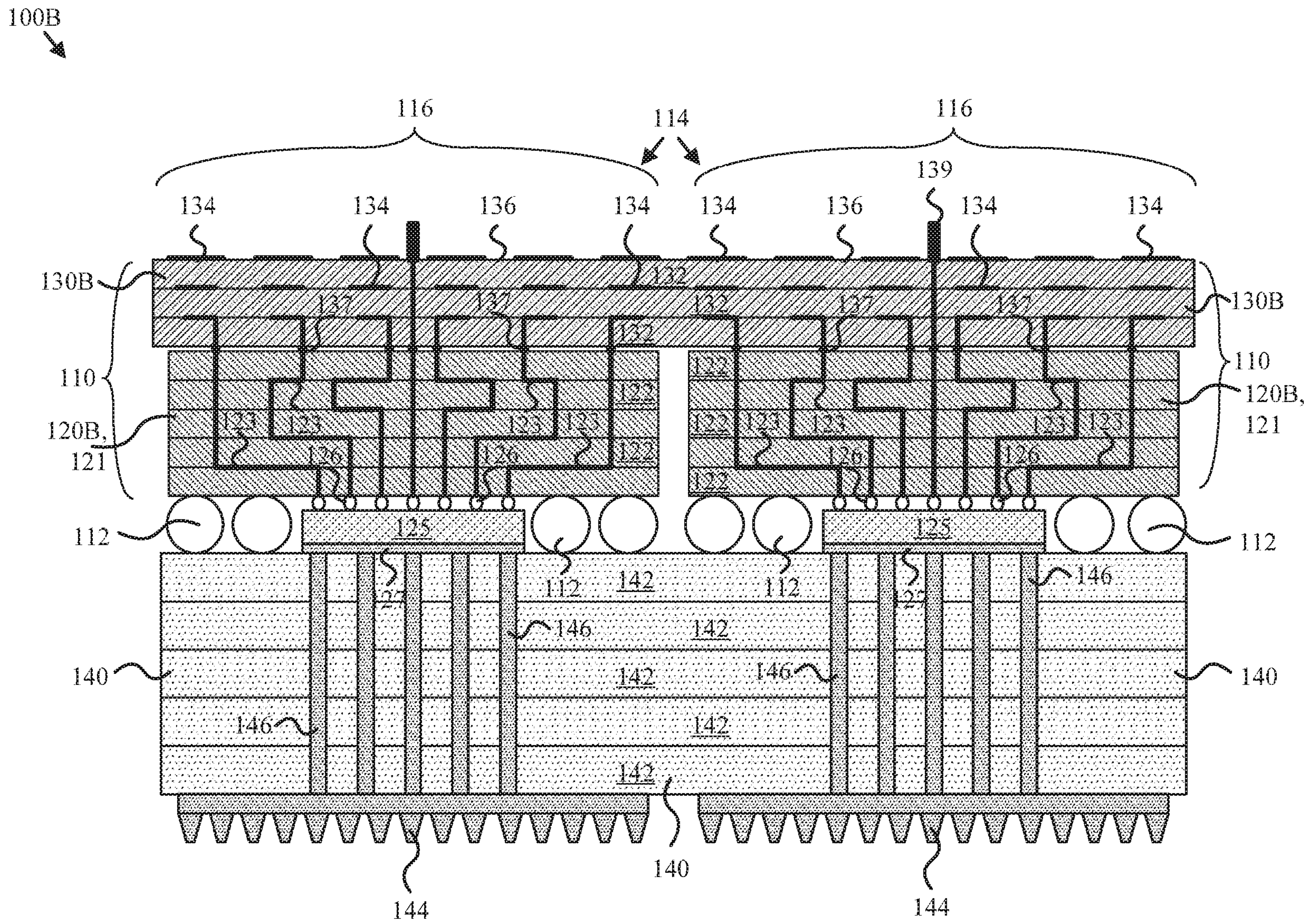

Fig. 1B

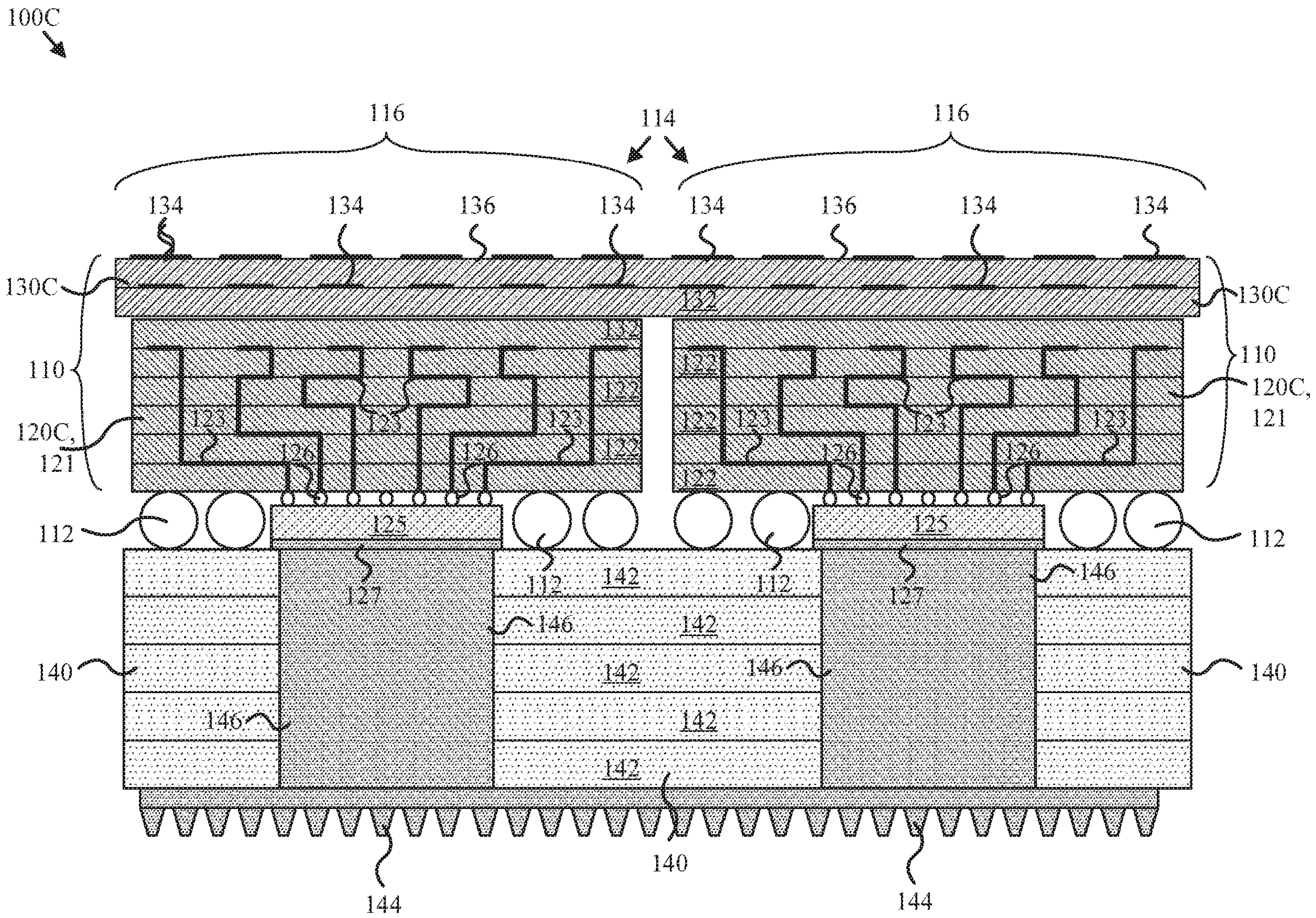

Fig. 1C

Cover with 2x2 array of 6x6 sub-arrays

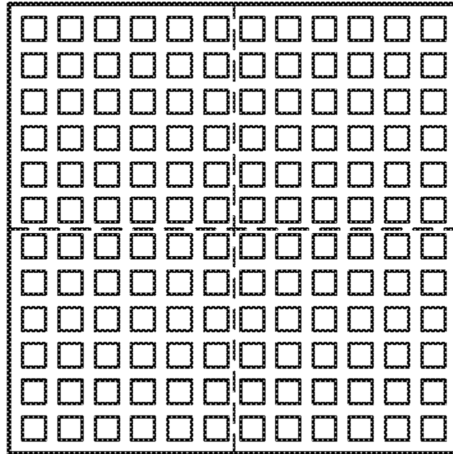

Fig. 2A

Cover with 1x5 array of 6x6 sub-arrays

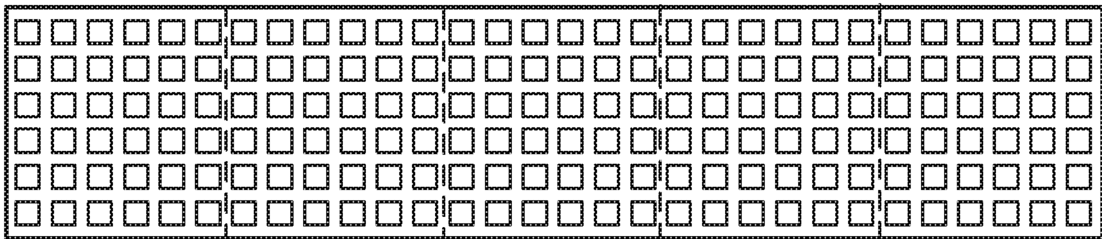

Fig. 2B

Cover with 2x3 array of 6x6 sub-arrays

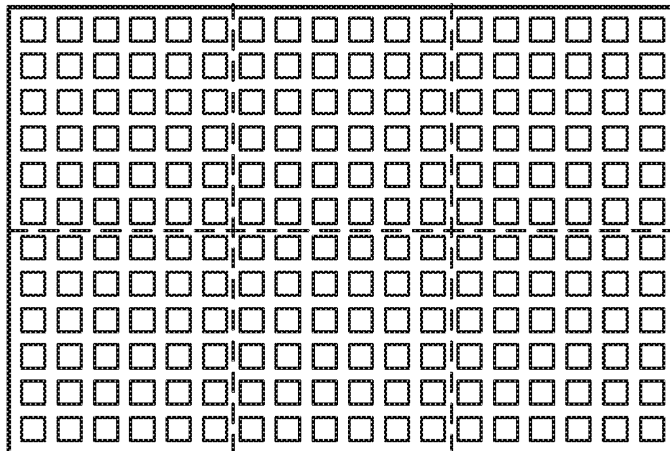

Fig. 2C

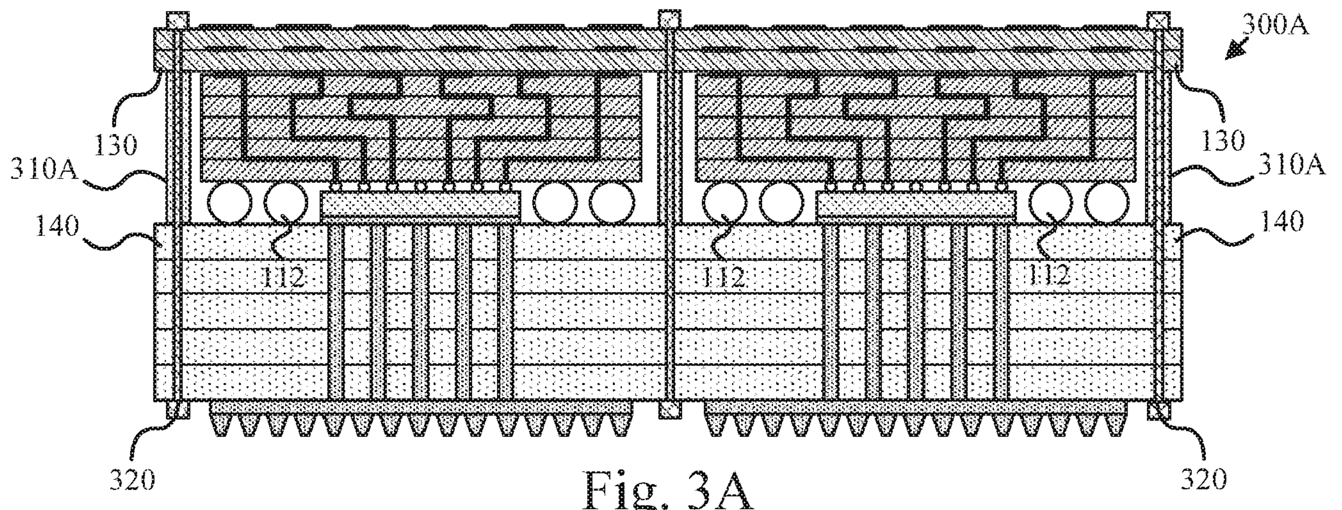

Fig. 3A

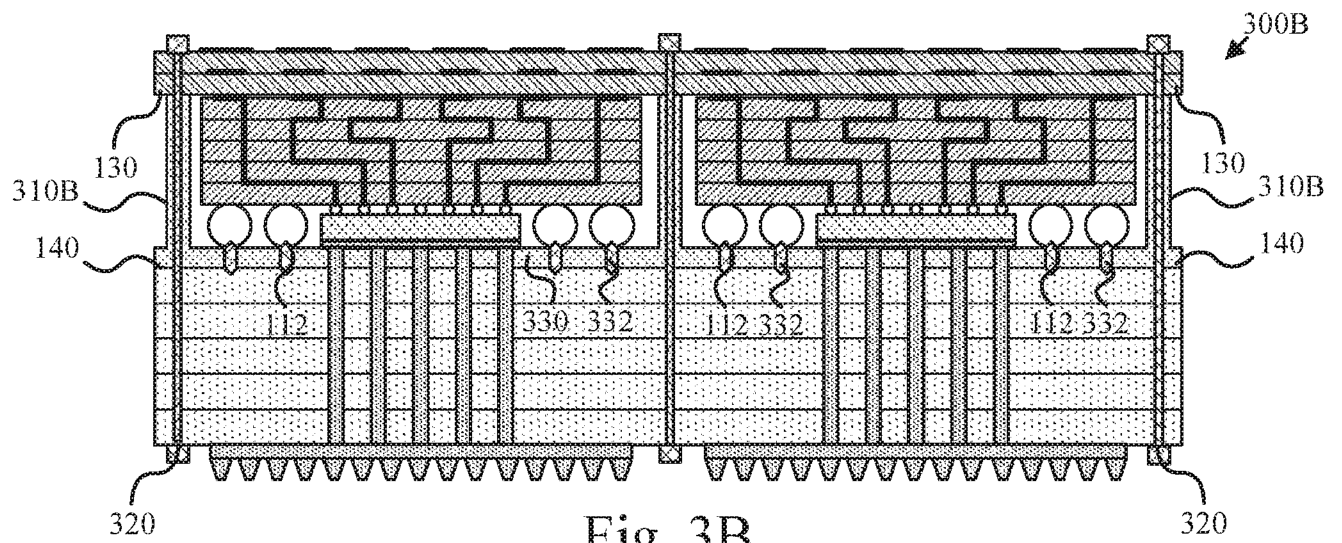

Fig. 3B

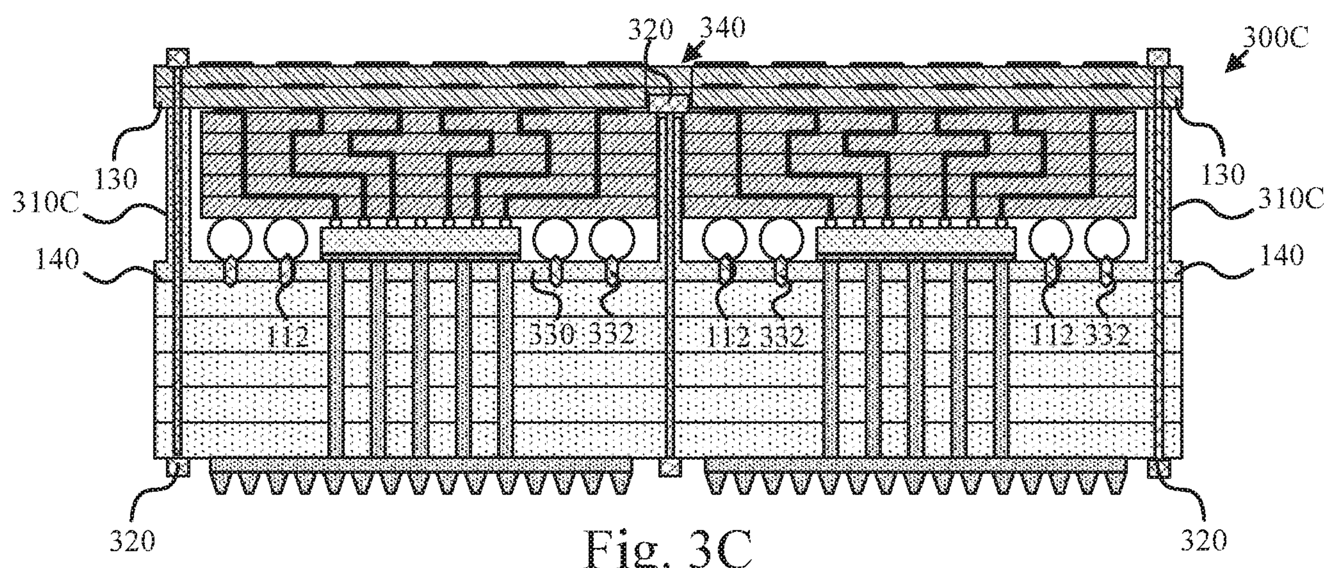

Fig. 3C

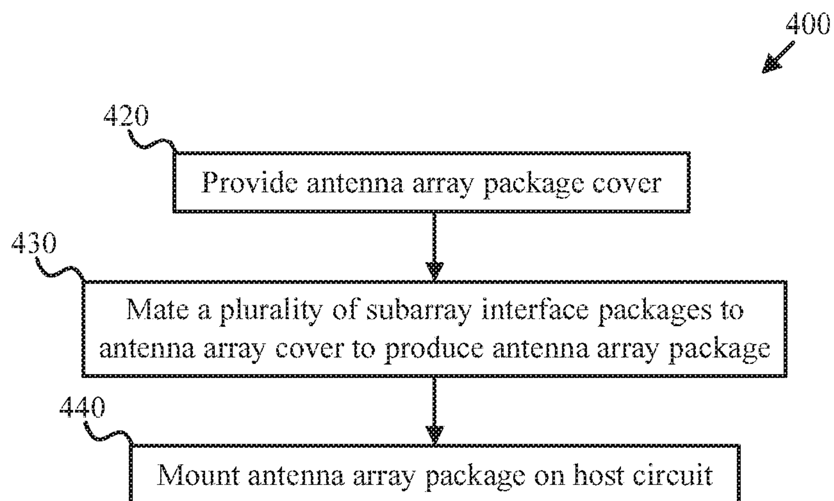

Fig. 4A

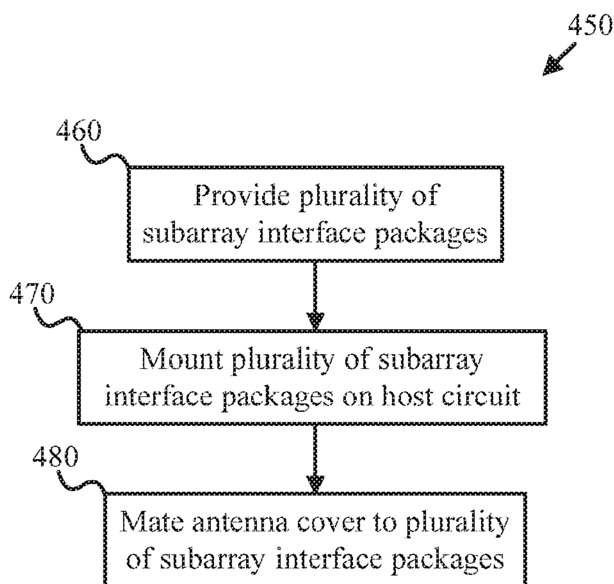

Fig. 4B

INTEGRATED ANTENNA ARRAY PACKAGING STRUCTURES AND METHODS

BACKGROUND

[0001] The invention relates generally to wireless device package structures and, in particular, to techniques for packaging antenna array structures with semiconductor chips such as mm Wave RF integrated circuits to form compact integrated wireless communication systems.

[0002] When constructing wireless communications package structures with integrated antenna arrays, it is important to implement package designs that provide proper antenna characteristics (e.g., high efficiency, wide bandwidth, good radiation characteristics, etc.) and array configurability (e.g., antenna elements in rows and columns), while providing low-cost and reliable package solutions.

[0003] Typical approaches to packaging wireless communication systems include creating a single package or modular packaging. Using a single package requires creating a complete custom package for each possible antenna configuration that may be needed. Such an approach increases upfront design costs, manufacturing rework costs and inventory costs. Modular packaging reduces the aforementioned costs but degrades the uniformity and/or placement precision of the antenna elements of large antenna arrays relative to each other and thereby reduces antenna performance.

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SUMMARY OF THE INVENTION

[0004] In one embodiment of the invention, there is provided an apparatus comprising: an antenna array package cover comprising a radiating surface, a mating surface disposed opposite the radiating surface, and an array of antenna array sub-patterns disposed on the radiating surface, each antenna array sub-pattern comprising at least one antenna element; and an array of sub-pattern interface packages each mated to the mating surface and each corresponding to a different one of the antenna array sub-patterns, each sub-pattern interface package comprising a package carrier, a sub-pattern integrated circuit electrically and mechanically coupled to the package carrier, and a set of interface lines corresponding to the or each antenna element of the corresponding antenna array sub-pattern; wherein the antenna array package cover further comprises a test interface element electrically connected to at least one of the sub-pattern integrated circuits..

[0005] Reserved.

[0006] In another embodiment of the invention, there is provided a method comprising: providing an antenna array package cover comprising a radiating surface, a mating surface disposed opposite the radiating surface, and an array of antenna array sub-patterns disposed on the radiating surface, each antenna array sub-pattern

comprising at least one antenna element; providing an array of sub-pattern interface packages each mated to the mating surface and each corresponding to a different one of the antenna array sub-patterns, each sub-pattern interface package comprising a package carrier, a sub-pattern integrated circuit electrically and mechanically coupled to the package carrier, and a set of interface lines corresponding to the or each antenna element of the corresponding antenna array sub-pattern; and, providing in the antenna array package cover a test interface element electrically connected to at least one of the sub-pattern integrated circuits.

[0007] The above described apparatus and methods enable providing wireless communication systems with reduced upfront design costs, manufacturing rework costs and inventory costs without degrading the uniformity and placement precision of the antenna elements used by those systems.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] In order that the advantages of the embodiments of the invention will be readily understood, a more particular description of the embodiments briefly described above will be rendered by reference to specific embodiments that are illustrated in the appended drawings. Understanding that these drawings depict only some embodiments of the invention and are not therefore to be considered to be limiting of scope, the embodiments of the invention will be described and explained with additional specificity and detail through the use of the accompanying drawings, in which:

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[0009] Figures 1A, 1B, and 1C are cross-sectional view illustrations of antenna array packages in accordance with embodiments of the invention;

[0010] Figures 2A, 2B, and 2C are plan view illustrations of antenna array covers in accordance with embodiments of the invention;

[0011] Figures 3A, 3B and 3C are cross-sectional view illustrations of antenna array packages with spacer frames in accordance with embodiments of the invention; and

[0012] Figures 4A and 4B are flowcharts of examples of an antenna system fabrication method in accordance with embodiments of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0013] Reference throughout this specification to “one embodiment,” “an embodiment,” or similar language means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment. Thus, appearances of the phrases “in one embodiment,” “in an embodiment,” and similar language throughout this specification may, but do not necessarily, all refer to the same embodiment, but mean “one or more but not all embodiments” unless expressly specified otherwise. The terms “including,” “comprising,” “having,” and variations thereof mean “including but not limited to” unless expressly specified otherwise. An enumerated listing of items does not imply that any or all of the items are mutually exclusive and/or mutually inclusive, unless expressly specified otherwise. The terms “a,” “an,” and “the” also refer to “one or more” unless expressly specified otherwise.

[0014] Figures 1A, 1B, and 1C are cross-sectional view illustrations of several examples of an antenna array system 100 in accordance with one or more embodiments of the invention. As depicted, the antenna array system 100 includes an antenna array package 110 comprising multiple sub-pattern interface packages 120 mated with an antenna array package cover 130. The antenna array package 110 may be mounted on a host circuit 140. The antenna array system 100 enables compact cost-effective integration of large antenna array structures with wireless circuits that interface to the antenna array structures.

[0015] The antenna array package 110 may include a set of host circuit connectors 112 that provide electrical and/or mechanical connections to the host circuit 140. In the depicted embodiment, the host circuit connectors 112 comprise an array of solder balls (BGA) with controlled diameter and height.

[0016] The antenna array package 110 includes one or more antenna arrays 114 formed on the antenna array package cover 130 that may be used to transmit and/or receive electromagnetic signals such as mmWave signals. In the depicted embodiment, the antenna array package 110 includes a single antenna array 114 comprising antenna elements 134 formed by one or more conductive structures placed on one or more package layers 132 of the antenna array package cover 130. For example, the antenna elements 134 could correspond to different types of antennas such as microstrip antennas; (e.g., patch and inverted-F antennas) stacked patch antennas; loop antennas; dipole antennas; bow-tie antennas; fractal antennas; slot antennas; traveling wave antennas, such as helical, spiral, and yagi-uda antennas; reflector antennas; and the like.

[0017] The sub-pattern interface packages 120 may provide signals to, and/or receive signals from, the antenna arrays 114 via a set of antenna feeds 123. In the depicted embodiments, each sub-pattern interface package 120 includes antenna feeds 123 that correspond to a subset of the antenna elements 134, referred to herein as an antenna array sub-pattern 116. In some embodiments of the invention, each sub-pattern interface package 120 is disposed below a corresponding antenna array sub-pattern 116. Disposing each interface package 120 below the

corresponding antenna array sub-pattern 116 shortens the signal path between package 120 and the corresponding antenna elements 134 and may improve performance. Furthermore, placing the antenna array sub-patterns 116 on the antenna array package cover 130 and above the corresponding sub-pattern interface packages 120, enables adjacent placement of multiple antenna array sub-patterns 116 and thereby reduces the surface area of the antenna array system 100. In some embodiments of the invention, each antenna array sub-pattern 116 is a sub-array of the antenna array 114.

[0018] Each sub-pattern interface package 120 includes a package carrier 121 comprising multiple package layers 122 that may be used to route the antenna feeds 123 connected to one or more sub-pattern integrated circuits 125 via one or more chip connectors 126. The chip connectors 126 may comprise C4 solder balls that are smaller in scale than the solder balls of the host circuit connectors 112. The integrated circuits 125 may interface with the antenna elements 134 via the antenna feeds 123 and provide other functions such as frequency conversion functions and amplitude and/or phase control functions for each antenna element 134.

[0019] In some embodiments of the invention, the package carrier 121 and/or the antenna array package cover 130 comprises a multilayer organic carrier that can be constructed using known carrier fabrication technologies, such as SLC (surface laminar circuit), HDI (high density interconnect), or other carrier fabrication techniques that enable the formation of organic-based multilayered circuit boards with high integration density. With these carrier fabrication techniques, a carrier substrate can be formed from a stack of laminated layers comprising alternating layers of metallization and dielectric/insulator materials, wherein the metallization layers are separated from overlying and/or underlying metallization layers by a respective layer of dielectric/insulating material. The metallization layers can be formed of copper and the dielectric/insulating layers can be formed of organic buildup and core materials. Other types of materials can be used for the metallization and insulating layers of the package carrier 121 and/or the antenna array package cover 130 such as LCP (liquid crystal polymer), glass, or LTCC (low-temperature co-fired ceramic). Moreover, these technologies enable the formation of small conductive vias (e.g., partial or buried vias between adjacent metallization layers) using laser ablation, photo imaging, or etching, for example, to enable the formation of high density wiring and interconnect structures within the carrier substrate.

[0020] The sub-pattern integrated circuits 125 may comprise a metallization pattern (not specifically shown) formed on the chip connector side (top side as shown) of each chip. The metallization pattern may include bonding/contact pads upon which the chip connectors 126 are formed. The bonding/contact pads may include, for example, ground pads, DC power supply pads, input/output pads, control signal pads, associated wiring, etc., that are formed as part of a BEOL (back end of line) wiring structure of the sub-pattern integrated circuits 125.

[0021] Each sub-pattern integrated circuit 125 may be electrically and mechanically connected to a particular sub-pattern interface package 120 and thereby the antenna array package 110 via flip-chip bonding (during which the orientation of the sub-pattern interface package 120 may be flipped from what is shown). Depending on the

application, the sub-pattern integrated circuits 125, either individually or collectively, may include RF circuitry and electronic components formed thereon including, for example, a receiver, a transmitter or a transceiver circuit, and other active or passive circuit elements that are commonly used to implement wireless RF chips.

[0022] The antenna array package cover 130 may include a radiating surface 136 from which electromagnetic radiation is preferably emitted and a mating surface 138 used for mating the antenna array package cover 130 to the sub-pattern interface packages 120. In some embodiments, the antenna array package cover 130 is mated to the sub-pattern interface package 120 generally, and the package carrier 121 specifically, using an epoxy adhesive or some other adhesive material. Alternately, the antenna array package cover 130 may be mated to the sub-pattern interface packages 120 via fasteners (see, for example, Figures 3A-3C) or via solder balls (not shown) and a solder reflow process.

[0023] The host circuit 140 may include multiple circuit layers 142 that can be used to route signals traces between the host circuit connectors 112 and components that are mounted on portions of the host circuit 140 that are not shown in the depicted examples. In some embodiments, a thermal connection layer 127 is disposed between the host circuit 140 and each sub-pattern integrated circuit 125. The thermal connection layer 127 may thermally couple the non-active surface (bottom surface as shown) of sub-pattern integrated circuit 125 to a region of the host circuit 140 that is aligned to a heat sink 144 and one or more thermal conduits 146 (e.g., metal filled vias or a pedestal). The thermal connection layer 127 serves to transfer heat from the sub-pattern integrated circuit 125 to the thermal conduits 146 which transfer the heat to the heat sink 144 for thermal dissipation (e.g., via conduction, convection, and radiation).

[0024] The antenna elements 134 may be coupled to the antenna feeds 123 via a variety of antenna feed structures including structures known by those of skill in the art such as aperture coupled structures and microstrip feed coupled structures. The antenna feed structures may be disposed within or on the surface the antenna array package cover 130 and/or the sub-pattern interface packages 120. For example, Figures 1A and 1C depict arrangements where the antenna feed structures are located entirely within the sub-pattern interface packages 120. In contrast, Figure 1B depicts an arrangement where at least a portion of the antenna feed structures are located in the antenna array package cover 130. In the depicted arrangement, the antenna feeds 123 cross from the sub-pattern interface packages 120 into the antenna array package cover 130 via connection elements 137.

[0025] Examples of possible connection elements 137 include package-on-package interconnects such as pillars. Some of the connection elements 137 may be connected to test pins 139 to enable testing of the sub-pattern integrated circuits 125. In another arrangement, not shown, the connection elements 137 may be connected to microstrip feedline structures that make direct connection to the antenna elements 134. In another arrangement, not shown, all connection elements 137 are connected to external test pins 139, forming an alternate version of the package cover that supports connectorized measurements for test purposes. Such testing may facilitate rework of

assembled antenna array packages 110 and reduce manufacturing losses.

[0026] Figures 2A, 2B and 2C are plan view illustrations of several examples of antenna array covers 130 in accordance with embodiments of the invention. As depicted, the antenna array covers 130 include a 2x2 (i.e., 2 rows and 2 columns) configuration 200A, a 1x5 (i.e., 1 row and 5 columns) configuration 200B, and a 2x3 (i.e., 2 rows and 3 columns) configuration 200C. In the depicted examples, the row and column boundaries are indicated with dashed lines for clarity. Each configuration is mated with a set of sub-pattern interface packages 120 where the number of packages in the set is equal to the product of the number of rows and the number of columns of the particular configuration.

[0027] One of skill in the art will appreciate that providing the antenna array package 110 by mating multiple sub-pattern interface packages 120 with an antenna array package cover 130 that corresponds to the desired antenna array size reduces the complexity of providing antenna arrays of various sizes (such as those depicted in Figures 2A-2C). Furthermore, signal routing on or within the antenna array package cover 130 may be simplified in that the signal routing pattern of antenna array package covers 130 of various sizes may use a common unit cell that is used (i.e., repeated) for each array sub-pattern 116 within the antenna array 114. Furthermore, size and spacing uniformity of the antenna elements 134 can be achieved with the common antenna array cover 130.

[0028] Figures 3A, 3B, and 3C are cross-sectional view illustrations of several examples of antenna array packages 300 in accordance with embodiments of the invention. Each depicted example includes a single spacer frame 310 with fasteners 320 that secure the spacer frame between the antenna array package cover 130 and the host circuit 140. The fasteners 320 may comprise a variety of fastening means such as pins, rivets, screws, bolts, nuts, or the like.

[0029] Figure 3A depicts an antenna array package 300A with a spacer frame 310A and BGA circuit connectors 112 that connect directly to the host circuit 140 as shown in previous figures. Figure 3B depicts an antenna array package 300B with a spacer frame 310B and an LGA interposer 330 disposed between the circuit connectors 112 and the host circuit 140. A set of pins 332 ensures an electrical connection between the circuit connectors 112 and the host circuit 140. In the depicted arrangement, the LGA interposer 330 is integral to the spacer frame 310B. Figure 3C depicts an antenna array package 300C with a multi-level spacer frame 310C and length fasteners 320 of multiple lengths and an LGA interposer 330 integral to the spacer frame 310C. The multi-level spacer frame 310C enables direct securement of the package carriers 121 via an aperture 340 in the antenna array cover 130 and a fastener 320 disposed therein.

[0030] Figures 4A and 4B are flowcharts of two examples of an antenna system fabrication method 400 in accordance with embodiments of the invention. A first example 400A, shown in Figure 4A, includes providing 410 the antenna array package cover, mating 420 a plurality of sub-pattern interface packages to the mating surface of the antenna array package cover to produce an antenna array package and mounting 430 the antenna array

package onto a host circuit. The depicted arrangement essentially uses the cover as a substrate for building an antenna package that is mounted to the host PCB.

[0031] A second example 400B of the antenna system fabrication method 400 includes providing 460 the sub-pattern interface packages and mounting 470 the plurality of sub-pattern interface packages onto a host circuit. The second example also includes mating 480 the plurality of sub-pattern interface packages to the mating surface of the antenna array package cover subsequent to mounting the plurality of sub-pattern interface packages onto the host circuit. The depicted arrangement essentially mounts multiple sub-pattern interface packages (carrier + RFIC) to a host PCB and covers the sub-pattern interface packages with a common antenna cover.

[0032] One of skill in the art will appreciate that the embodiments of the invention disclosed herein provide a modular approach to packaging wireless communication systems that reduces upfront design costs, manufacturing rework costs and inventory costs without degrading the uniformity and placement precision of the antenna elements of large antenna arrays relative to each other and without reducing antenna performance.

[0033] The features, advantages, and characteristics of the embodiments of the invention described herein may be combined in any suitable manner. One skilled in the relevant art will recognize that the embodiments of the invention may be practiced without one or more of the specific features or advantages of a particular embodiment of the invention. In other instances, additional features and advantages may be recognized in certain embodiments of the invention that may not be present in all embodiments of the invention.

[0034] Reference throughout this specification to “one embodiment,” “an embodiment,” or similar language means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment. Thus, appearances of the phrases “in one embodiment,” “in an embodiment,” and similar language throughout this specification may, but do not necessarily, all refer to the same embodiment, but mean “one or more but not all embodiments” unless expressly specified otherwise. The terms “including,” “comprising,” “having,” and variations thereof mean “including but not limited to” unless expressly specified otherwise. An enumerated listing of items does not imply that any or all of the items are mutually exclusive and/or mutually inclusive, unless expressly specified otherwise. The terms “a,” “an,” and “the” also refer to “one or more” unless expressly specified otherwise.

[0035] The schematic flowchart diagrams and/or schematic block diagrams in the Figures illustrate the architecture, functionality, and operation of possible implementations. It should also be noted that, in some alternative implementations, the functions noted in the block may occur out of the order noted in the Figures. For example, two blocks shown in succession may, in fact, be executed substantially concurrently, or the blocks may sometimes be executed in the reverse order, depending upon the functionality involved. Although various arrow types and line types may be employed in the flowchart and/or block diagrams, they are understood not to limit the

scope of the corresponding embodiments of the invention. Indeed, some arrows or other connectors may be used to indicate only an exemplary logical flow of the depicted embodiment of the invention.

[0036] The description of elements in each figure may refer to elements of proceeding figures. Like numbers refer to like elements in all figures, including alternate embodiments of like elements. The embodiments of the invention may be practiced in other specific forms. The described embodiments of the invention are to be considered in all respects only as illustrative and not restrictive. The scope of the invention is, therefore, indicated by the appended claims rather than by the foregoing description. All changes which come within the meaning and range of equivalency of the claims are to be embraced within their scope.

CLAIMS

1. An apparatus comprising:

an antenna array package cover comprising a radiating surface, a mating surface disposed opposite the radiating surface, and an array of antenna array sub-patterns disposed on the radiating surface, each antenna array sub-pattern comprising at least one antenna element; and

an array of sub-pattern interface packages each mated to the mating surface and each corresponding to a different one of the antenna array sub-patterns, each sub-pattern interface package comprising a package carrier, a sub-pattern integrated circuit electrically and mechanically coupled to the package carrier, and a set of interface lines corresponding to the or each antenna element of the corresponding antenna array sub-pattern;

wherein the antenna array package cover further comprises a test interface element electrically connected to at least one of the sub-pattern integrated circuits.

2. The apparatus of claim 1, wherein each sub-pattern interface package of the array of sub-pattern interface packages is disposed below a corresponding antenna array sub-pattern of the array of antenna array sub-patterns.

3. The apparatus of claim 1, wherein the sub-pattern integrated circuit is flip-chip bonded to the package carrier.

4. The apparatus of claim 1, wherein the antenna array package cover and the array of sub-pattern interface packages form an antenna array package.

5. The apparatus of claim 4, wherein the antenna array package is mounted on a host circuit.

6. The apparatus of claim 5, wherein the antenna array package is mounted on the host circuit via a ball grid array (BGA) or a land grid array (LGA) socket.

7. The apparatus of claim 5, wherein the host circuit comprises one or more heat sinks that are thermally connected to the plurality of sub-pattern integrated circuits via a plurality of thermal conduits.

8. The apparatus of claim 7, wherein a thermal conduit of the one or more thermal conduits comprises a pedestal.

9. The apparatus of claim 5, further comprising a spacer frame disposed between the antenna array package cover and the host circuit.

10. The apparatus of claim 1, wherein the antenna array package cover comprises a set of antenna feeds for

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each antenna array sub-pattern of the array of antenna array sub-patterns.

11. The apparatus of claim 1, wherein the array of sub-pattern interface packages are secured to the mating surface of the antenna array package cover via one or more of supporting balls, an adhesive, and at least one fastener.

12. The apparatus of claim 1, wherein the antenna array package cover or the package carrier comprises multiple layers.

13. The apparatus of claim 1, wherein the package carrier comprises bonding pads for a solder ball grid array.

14. The apparatus of claim 1, wherein each antenna element comprises a patch of conductive material disposed on the radiating surface.

15. The apparatus of claim 1, wherein the antenna elements are disposed on multiple layers of the antenna array package cover.

16. A method comprising:

providing an antenna array package cover comprising a radiating surface, a mating surface disposed opposite the radiating surface, and an array of antenna array sub-patterns disposed on the radiating surface, each antenna array sub-pattern comprising at least one antenna element;

providing an array of sub-pattern interface packages each mated to the mating surface and each corresponding to a different one of the antenna array sub-patterns, each sub-pattern interface package comprising a package carrier, a sub-pattern integrated circuit electrically and mechanically coupled to the package carrier, and a set of interface lines corresponding to the or each antenna element of the corresponding antenna array sub-pattern; and,

providing in the antenna array package cover a test interface element electrically connected to at least one of the sub-pattern integrated circuits.

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