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(54) ANTENNA PACKAGE FOR A MILLIMETRE WAVE INTEGRATED CIRCUIT

ANTENNENPAKET FÜR EINE INTEGRIERTE MILLIMETERWELLENSCHALTUNG

BOÎTIER D'ANTENNE POUR CIRCUIT INTÉGRÉ À ONDES MILLIMÉTRIQUES

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Description

TECHNICAL FIELD

[0001] The present invention relates to an antenna package and to a manufacturing method thereof. The antenna package is particularly designed for a millimetre wave integrated circuit, like a radio frequency (RF) transceiver.

BACKGROUND

[0002] Characterization and packaging of millimetre wave integrated circuits is challenging, since at higher frequencies (e.g. at f>90GHz in the W, D ... bands), a wavelength becomes comparable to, or at least a fraction of, the size of the packaging structure. A particularly critical issue for a millimetre wave transceiver design is a coupling of the chip to an antenna port (typically a rectangular waveguide).

[0003] In a conventional package 800 shown in Fig. 8, a classical technique, here wire bonding, is used for providing the coupling to an antenna port 802. In particular, a (transceiver) chip 803 is connected via a bonding wire 804 to a microstrip line 805, which is further connected to the antenna port 802 of an antenna 801. Classical techniques like wire bonding can, however, not guarantee an acceptable matching between the chip 803 and the antenna port 802 at high frequencies. Further, at such frequencies the bonding wire 804 will even work as a radiator itself.

[0004] The main problem at high frequencies is thus to provide a low-complex, robust, but low-cost packaging solution, in which classical techniques for RF coupling between a (transceiver) chip and an antenna port are avoided.

[0005] Conventionally, this problem is addressed by preventing, for instance, any wire bonding connections between the chip 803 and the package microstrip line 805 connected to the antenna port 802. Thereby, unwanted effects of a series RF bond inductance, which hamper operation at high frequencies, are avoided. Several conventional approaches for removing wire bonding connections exist.

[0006] In a first conventional approach, single antenna elements or multiple antenna elements (antenna arrays) are integrated into a chip, resulting in a highest level of integration. However, the disadvantage of this approach is that a high antenna gain, embedded in a semiconductor chip, is not a cost effective solution (because too much semiconductor area is needed).

[0007] In a second conventional approach, flip-chip bumps are used for the coupling. That is, in a wafer level chip scale packaging (WLCSP), a chip is packaged in a ball grid array with the surface of the chip facing down to a PCB, on which it is mounted (package). The flip-chip bump approach shows acceptable performance at high frequencies, but requires a very accurate assembling process, and moreover, a total packaging insertion loss is not optimized.

[0008] US 2007/216493 A1 suggests a coupling from a planar substrate/chip circuit microwave transmission line to an external waveguide on the back of the substrate/chip. However, the disadvantage of this approach is that the effective transition to the waveguide is external to the chip, and thus a back short (GND plane) is required. Moreover, in order to work properly, the interconnection needs two additional substrates provided below the chip.

[0009] US 2016/0079675 A1 discloses an integrated chip, and a radar assembly including the integrated chip in a module and a horn-like structure mounted onto the module.

[0010] 'Xiao-Jun Tang et al., "A 60-GHz Wideband Slot Antenna Based on Substrate Integrated Waveguide Cavity", International Journal of Infrared and Millimeter Waves (2007), pages 275-281' discloses a wideband W-band substrate integrated waveguide cavity-backed slot antenna.

SUMMARY

[0011] In view of the above-mentioned problems and disadvantages, the present invention aims at improving the conventional approaches for packaging millimetre wave integrated circuits. The present invention has the object to provide a low-complex, a robust, and a low-cost packaging solution, which is suitable for high frequencies and avoids classical techniques for signal coupling, like wire bonding. Further, the packaging solution should not be related to an antenna gain requirement. The packaging solution should also allow for a high performance, and should particularly be optimized with respect to insertion loss and return loss. Also a back short should be avoided in the packaging solution.

[0012] The object of the present invention is achieved by the solution provided in the enclosed independent claims. Advantageous implementations of the present invention are further defined in the dependent claims. In particular the present invention proposes an on-chip interconnection for high frequency signals.

[0013] A first aspect of the present invention provides an antenna package comprising an antenna with an embedded antenna port, the antenna including an antenna port side and an antenna radiation side, and a semiconductor chip provided on the antenna port side, wherein the chip comprises coupling elements for coupling RF signals from a top side of the chip to the antenna port, the coupling elements comprising: a matching network including a high-impedance microstrip line and a ground window on the top side of the chip, a resonant dielectric cavity within the chip, and a metal coupling slot facing the antenna port on a bottom side of the chip, wherein side walls of the resonant dielectric cavity are defined by ground vias connecting a top and a bottom ground layer of the chip, and wherein the coupling slot is dimensioned and arranged such that, when the package is viewed

from the antenna port side, the antenna port completely includes the coupling slot.

[0014] An embedded antenna port means that the antenna port is completely included within the structure of the antenna. A microstrip line is a high-impedance microstrip line, if its impedance is larger than 50Ω. In particular, the impedance of the microstrip line of the antenna package of the first aspect is even in the range of 70-80Q.

[0015] In the antenna package of the first aspect, the chip assembled on the antenna port side of the antenna is directly coupled to antenna port in the antenna. Therefore, a low-complex, robust, but also low-cost packaging solution is achieved by the antenna package. A particular advantage of the antenna package is that insertion loss can be optimized. Further, the antenna package requires no back short waveguide or the like. Also, no intermediate PCB is required between the chip and the antenna port. Finally, the antenna advantageously acts as grounded mechanical carrier for the chip in the antenna package.

[0016] The ground vias provide a simple implementation of the resonant dielectric cavity created inside of the chip.

[0017] By means of the dimensions and arrangements of the coupling slot, a low sensitivity to alignment tolerances, i.e. to smaller misalignment, between chip and antenna port is achieved.

[0018] In a first implementation form of the antenna package according to the first aspect as such or according to the first implementation form of the first aspect, a λ/4 waveguide is arranged between the chip and the antenna port.

[0019] The λ/4 waveguide significantly improves the performance of the antenna package, due to an improved matching between the chip and the antenna port.

[0020] In a second implementation form of the antenna package according to the third implementation form of the first aspect, the λ/4 waveguide is dimensioned and arranged such that it completely includes the coupling slot on the bottom side of the chip.

[0021] Thereby, a low sensitivity to alignment tolerances, i.e. small misalignments, between chip and antenna port is achieved.

[0022] In a third implementation form of the antenna package according to the third or fourth implementation form of the first aspect, a ratio between a surface size of the λ/4 waveguide and a surface size of the coupling slot is in a range of 6-8, and is in particular 7.

[0023] These ratios have been found to be the optimum design trade-off between a best wide-band transmission performance and a lower sensitivity of said transmission performance to alignment tolerances between the chip and the antenna port.

[0024] In a fourth implementation form of the antenna package according to the first aspect as such or according to any implementation form of the first aspect, the RF signals are of a frequency above 90 GHz, and in particular in a frequency range of 140-160 GHz.

[0025] At high frequencies above 90 GHz the antenna package is particularly feasible and effective.

[0026] In a fifth implementation form of the antenna package according to the first aspect as such or according to any implementation form of the first aspect, the antenna port is dimensioned smaller than the chip.

[0027] Thus, the antenna package provides an on-chip interconnection that is also feasible from a cost point of view.

[0028] In a sixth implementation form of the antenna package according to the first aspect as such or according to any implementation form of the first aspect, the coupling slot is included completely in the resonant dielectric cavity.

[0029] Thereby, the overall performance of the antenna package can be improved.

[0030] In a seventh implementation form of the antenna package according to the first aspect as such or according to any implementation form of the first aspect, the chip comprises a plurality of metal coupling slots on its bottom side for coupling the RF signals into a plurality of antenna ports.

[0031] Accordingly, a chip with, for instance, a double transition / interconnection can be used in the antenna package.

[0032] In an eighth implementation form of the antenna package according to the first aspect as such or according to any implementation form of the first aspect, the chip is manufactured in the GaAs material system.

[0033] The antenna package is designed and optimized for this GaAs material system.

[0034] A second aspect of the present invention provides a method of manufacturing an antenna package, the method comprising the steps of providing an antenna with an embedded antenna port, the antenna including an antenna port side and an antenna radiation side, providing a semiconductor chip on the antenna port side, configuring the chip with coupling elements for coupling RF signals from a top side of the chip to the antenna port by: providing a matching network including a high-impedance microstrip line and a ground window on the top side of the chip, creating a resonant dielectric cavity within the chip, and providing a metal coupling slot facing the antenna port on a bottom side of the chip, wherein side walls of the resonant dielectric cavity are defined by ground vias connecting a top and a bottom ground layer of the chip, and wherein the coupling slot is dimensioned and arranged such that, when the package is viewed from the antenna port side, the antenna port completely includes the coupling slot.

[0035] In a seventh implementation form of the method according to the second aspect as such or according to any implementation form of the second aspect, the chip is provided with a plurality of metal coupling slots on its bottom side for coupling the RF signals into a plurality of antenna ports.

[0036] In an eighth implementation form of the method according to the second aspect as such or according to any implementation form of the second aspect, the chip

is manufactured in the GaAs material system.

[0037] With the method of the second aspect as such and its implementation forms, the same advantages as described for the antenna package of the first aspect as such and its respective implementation forms can be achieved.

[0038] It has to be noted that all devices, elements, units and means described in the present application could be implemented in the software or hardware elements or any kind of combination thereof. All steps which are performed by the various entities described in the present application as well as the functionalities described to be performed by the various entities are intended to mean that the respective entity is adapted to or configured to perform the respective steps and functionalities. Even if, in the following description of specific embodiments, a specific functionality or step to be full formed by external entities is not reflected in the description of a specific detailed element of that entity which performs that specific step or functionality, it should be clear for a skilled person that these methods and functionalities can be implemented in respective software or hardware elements, or any kind of combination thereof.

BRIEF DESCRIPTION OF THE DRAWINGS

BRIEF DESCRIPTION OF THE DRAWINGS

[0039] The above described aspects and implementation forms of the present invention will be explained in the following description of specific embodiments in relation to the enclosed drawings, in which:

Fig. 1 shows a top view and a side view of an antenna package according to an embodiment of the present invention.

Fig. 2 shows an antenna package according to an embodiment of the present invention.

Fig. 3 shows a top view and a bottom view of a semiconductor chip of an antenna package according to an embodiment of the present invention.

Fig. 4 shows a bottom view and a side view of an antenna package according to an embodiment of the present invention.

Fig. 5 shows a simulation of insertion loss and return loss of an antenna package according to an embodiment of the present invention.

Fig. 6 shows a measurement of insertion loss and return loss of an antenna package according to an embodiment of the present invention.

Fig. 7 shows in a flow diagram a method according to an embodiment of the present invention.

Fig. 8 shows a conventional antenna package.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0040] Fig. 1 shows an antenna package 100 according to an embodiment of the present invention. The antenna package 100 is shown in a top view and in a side view, respectively. The antenna package 100 generally includes an antenna 101 with an antenna port side and an antenna radiator elements side (antenna radiation side), and a chip 103.

[0041] The antenna port side may be defined as the side of the antenna including a waveguide portion for connecting the antenna to the chip. The waveguide portion may be a portion of the antenna port as described below with reference to figure 1. Alternatively, the waveguide portion may be a portion of an additional waveguide embedded in the antenna and arranged between the antenna port and the chip.

[0042] The antenna radiation side is the side of the antenna including the radiation elements and opposite the antenna port side.

[0043] The chip 103 is provided on the antenna 101, specifically on the antenna port side of the antenna 101. The chip 103 is advantageously a millimeter wave integrated circuit, for instance, a high frequency transceiver. High frequencies in the context of the present invention are considered frequencies of at or above 90GHz. The chip 103 of the antenna package 100 may operate with RF signals having a frequency above 90 GHz, for example, in a frequency range of 140-160 GHz.

[0044] The chip 103 of the antenna package 100 is configured to couple RF signals from a top side of the chip 103 (the side not facing the antenna 101) into the antenna 101, more specifically to an antenna port 102, which is embedded within the antenna 101. The antenna port 102 is, for example, a rectangular waveguide within the antenna 101. However, the antenna port 102 can also be another interface port, e.g. a port of an antenna filter. The antenna port 102 may be dimensioned smaller than the chip 103.

[0045] The chip 103 is configured for the coupling of the RF signals by comprising dedicated coupling elements. The RF interconnection between the chip 103 and the antenna port 102 is particularly enabled by a proper design of these coupling elements. That is, the coupling elements are carefully designed to match the operating frequency, specifically in view of minimizing insertion loss and return loss at the operating frequency. The coupling elements comprise a matching network on the top side of the chip 103, a resonant dielectric cavity 106 within the chip 103, and a metal coupling slot 107 facing the antenna port 102 on a bottom side of the chip 103 (the side facing the antenna 101).

[0046] The top view of the antenna package 100 in Fig. 1 shows the chip 103 on the antenna port side of the antenna 101, and particularly shows the matching network provided on the top side of the chip 103. The match-

ing network includes a high-impedance microstrip line 104, and a ground window 105. A high impedance microstrip line 104 is in general any microstrip line having an impedance larger than 50Ω. In particular, the microstrip line 104 may have an impedance of 70-80Ω. The size of the microstrip line 104 and of the ground window 105, respectively, is optimized in dependence of the frequency of the RF signals. The microstrip line 104 may be grounded with one of its ends.

[0047] Further, the top view of the chip 103 shows outlines of the resonant cavity 106 created inside the chip 103. The side walls of the resonant cavity 106 may be defined by ground via holes, as explained in more detail below. The resonant cavity 106 is designed to create a resonance in the frequency band of the used RF signals, and supports injection of the RF signals via the coupling slot 107 into the antenna port 102.

[0048] Finally, the side view of the antenna package 100 in Fig. 1 shows the coupling metal slot 107 provided on the bottom side of the chip 103. As indicated by the arrow, the RF signals are in the end coupled from this coupling slot 107 into the antenna port 102. The coupling slot 107 may be made by patterning a back side metal of the chip 103. The coupling slot 107 may be arranged centrally in the resonant cavity 106 (in a top or bottom view of the chip 103), and has a width as narrow as possible. In particular, the coupling slot 107 included completely within the resonant cavity 106. The coupling slot 107 may also be dimensioned and arranged such that, when the antenna package 100 is viewed from below i.e. from the antenna port side, the antenna port 102 completely includes the coupling slot 107.

[0049] The main advantage of the antenna package 100 is that the chip 103 is coupled directly to the antenna port 102. Further, the coupling elements presented above are particularly suitable for the highest millimeter wave applications, and are not related to the antenna gain requirement. The interconnection for the RF signals is mainly on-chip, and is designed to couple the signals from the top side of chip 103 directly into the antenna port 102 under the chip 103. The antenna package 100 is specifically feasible at f>90GHz, due to the small size of the antenna port 102 compared to the size of the chip 103 at these high frequencies. Furthermore, the antenna port 102 mechanic is, at the same time, the mechanic carrier (ground), on which the chip 103 is assembled. Therefore, no dedicated ground is necessary, thereby reducing the size of the antenna package.

[0050] Fig. 2 shows another antenna package 100 according to an embodiment of the present invention. The antenna package 100 of Fig. 2 expands the antenna package 100 of Fig. 1, and identical elements are provided with the same reference signs.

[0051] The antenna package 100 of Fig. 2 also includes the chip 103 and the antenna 101. The chip 103 also has coupling elements comprising the microstrip line 104, the ground window 105 (not shown in Fig. 2), the resonant cavity 106, and the coupling slot 107. The antenna 101 also has the embedded antenna port 102, to which the RF signals are coupled from the top side of the chip 103.

[0052] Additionally, the antenna package 100 of Fig. 2 is shown with a ground via 203. A plurality of such ground vias 203 may define the side walls of the resonant cavity 106. The ground vias 203 thereby connect a top and a bottom ground layer of the chip 103, and may reach from the top side of the chip 103 to its bottom side.

[0053] Furthermore, the antenna package 100 of Fig. 2 may have a λ/4 waveguide 201 arranged between the chip 103 and the antenna port 102. The ground vias 203 and the λ/4 waveguide 201 can be provided together or independently from another. That means, only the ground vias 203 or only the λ/4 waveguide 201 may be present.

[0054] The λ/4 waveguide 201 is provided adjacent to the bottom side of the chip 103, which is configured with the metal coupling slot 107. That is, the open coupling slot 107, which could be provided in the bottom ground layer of the chip 103, faces down to the λ/4 waveguide line 201. The size of the λ/4 waveguide 201 may be designed greater than the metal coupling slot 107, in order to make the performance of the interconnection insensitive to alignment tolerances between the chip 103 and the mechanics of the antenna port 102.

[0055] The λ/4 waveguide 201 has the function to improve the matching between the chip 103 and the antenna port 102. The dimensions of the λ/4 waveguide 201 may be such that the coupling slot 107 of the chip 103 is completely included therein. In other words, the λ/4 waveguide 201 may be dimensioned and arranged such that it completely covers or includes the coupling slot 107 on the bottom side of the chip 103. This design constraint allows making the performance of the interconnection less sensitive to the alignment tolerances between the chip 103 and the mechanics of the antenna port 102.

[0056] A ratio between the sizes of the of the intermediate λ/4 waveguide 201 surface and the coupling slot 107 surface on the bottom side of the chip 103 is a design trade-off between the best wide band transition (RF interconnection) performance result and a lower sensitivity of the same transition performance to the alignment tolerances between the chip 103 and the mechanics of the antenna port 102. For example, this ratio is advantageously about 7 for a transition (RF interconnection) designed on a GaAs semiconductor substrate and working in the D-band. Generally, a ratio of a surface size of the λ/4 waveguide 201 and a surface size of the coupling slot 107 may be in a range of 6-8, and in particular it is around 7 for the antenna package 100.

[0057] Fig. 3 shows a top view and a bottom view of the chip 103 included in the antenna package 100 of Fig. 2. The chip 103 includes the resonant cavity 106 defined by a plurality of ground vias 203, the matching network made of microstrip line 104 and ground window 105, and the coupling slot 107. It can be seen that the coupling slot 107 may be included completely in the resonant di-

electric cavity 106. In particular, it is arranged centrally within the borders of the cavity 106.

[0058] Fig. 4 shows another antenna package 100, which expands the antenna packages 100 shown in the Figs. 1 and 2, respectively. The antenna package 100 is shown in a bottom view and a side view. In the bottom view, it can be seen that a plurality of ground vias 203 arranged for example in a regular pattern may define each side wall of the resonant cavity 106. Furthermore, it can be seen that the λ/4 waveguide 201 may be dimensioned and arranged such that it completely covers the coupling slot 107 on the bottom side of the chip 103.

[0059] In the side view, it can be seen that the antenna port 102 may be dimensioned smaller than the chip 103, which is feasible at high operating frequencies. Further, also the λ/4 waveguide 201 may be dimensioned smaller than the chip 103, but such that it still covers the coupling slot 107 completely. Further, the λ/4 waveguide 201 may be dimensioned larger than the antenna port 102, at least in one of its dimension.

[0060] In addition, the side view of the antenna package 100 shows that one or more PCBs 401 may be provided adjacent to the chip 103 on the antenna port side of the antenna 101. For instance, a two layer PCB 401 may be bonded to the antenna port side of the antenna 101. The PCB 401 can comprise biasing and/or signaling pads for connecting the chip 103.

[0061] In this way, for example, it is possible to design an antenna package 100 of small size, for instance for operating frequencies in the D-band, and specifically with dimensions of about 4x4cm. Such an antenna package 100 can be further assembled as a standard SMD device on a PCB or the like.

[0062] Fig. 5 shows exemplarily an implementation of an antenna package 100 (left side) designed for the D-band, i.e. 140-160 GHz. The transmission of RF signals from the chip 103 via the coupling slot 107 to the antenna port 102 is implemented as explained above. The exemplary antenna package 100 comprises a chip 103 made from GaAs, the chip 103 having a thickness of 50μm. The chip 103 is provided on the antenna 101 to directly face the antenna port 102. The antenna port 102 has dimensions of 1.65x0.825mm, and is thus suitable for frequencies between 120-170GHz.

[0063] Fig. 5 shows (right side) simulation results for insertion loss and return loss (in dB, provided on the vertical axis) in dependence of the operating frequency (in GHz, provided on the horizontal axis). The simulations were performed with an EM HFSS 3D simulator (Ansys).

[0064] Fig. 6 shows exemplarily a test jig implementation in order to check the chip to antenna port interconnection performances, of which simulation results are shown in Fig. 5. A single chip 103 includes a double transition into two ports.

[0065] Fig. 6 shows (bottom) measurement results for insertion loss and return loss (in dB, provided on the vertical axis) in dependence of the operating frequency (in GHz, provided on the horizontal axis). For the measurements, the chip 103 was assembled on a test jig with two standard rectangular waveguide output ports as antenna ports 102. As shown in Fig. 6, these output ports both connected (via a bend) to a waveguide. A network analyzer was used to measure the total losses in the assembly. Then, the single transition loss was obtained by de-embedding the test jig losses from the total measured losses.

[0066] The microstrip line loss numbered to 0.72dB. The interface loss between the output ports and the waveguide (labelled (waveguide+2bend) loss) in Fig. 6) numbered to 0.4dB. The single transition loss numbered to 1.04dB.

[0067] Fig. 7 shows a method 700 of manufacturing an antenna package 100, in particular a package for a millimeter wave integrated circuit. In a first step 701 of the method 700, an antenna 101 with an embedded antenna port 102 is provided, the antenna 101 including an antenna port side and an antenna radiation side. In a second step 702, a semiconductor chip 103 is provided on the antenna 101 port side. In a third step 703, the chip 103 is configured with coupling elements for coupling RF signals from a top side of the chip 103 to the antenna port 102.

[0068] The third step 703 includes to this end a first sub-step 7031, in which a matching network including a high-impedance microstrip line 104 and a ground window 105 is provided on the top side of the chip 103, a second sub-step 7032, in which a resonant dielectric cavity 106 is created within the chip 103, and a third sub-step 7033, in which a metal coupling slot 107 facing the antenna port 102 on a bottom side of the chip 103 is provided.

[0069] The present invention has been described in conjunction with various embodiments as examples as well as implementations. However, other variations can be understood and effected by those persons skilled in the art and practicing the claimed invention, from the studies of the drawings, this disclosure and the independent claims.

Claims

1. Antenna package (100) comprising:

an antenna (101) with an embedded antenna port (102), the antenna (101) including an antenna port side and an antenna radiation side, and

a semiconductor chip (103) provided on the antenna port side,

wherein the chip (103) comprises coupling elements for coupling radio frequency signals from a top side of the chip (103) to the antenna port (102), the coupling elements comprising:

a matching network including a high-impedance microstrip line (104) having an imped-

ance larger than 50Ω and a ground window (105) on the top side of the chip (103),
a resonant dielectric cavity (106) within the chip (103), and
a metal coupling slot (107) facing the antenna port (102) on a bottom side of the chip (103)

wherein side walls of the resonant dielectric cavity (106) are defined by ground vias (203) connecting a top and a bottom ground layer of the chip (103), and
wherein the coupling slot (107) is dimensioned and arranged such that, when the antenna package (100) is viewed from the antenna port side, the antenna port (102) completely includes the coupling slot (107).

2. Antenna package (100) according to claim 1, comprising:
a λ/4 waveguide (201) arranged between the chip (103) and the antenna port (102).

3. Antenna package (100) according to claim 2, wherein
the λ/4 waveguide (201) is dimensioned and arranged such that it completely includes the coupling slot (107) on the bottom side of the chip (103).

4. Antenna package (100) according to claim 2 or 3, wherein
a ratio between a surface size of the λ/4 waveguide (201) and a surface size of the coupling slot (107) is in a range of 6-8, and is preferably 7.

5. Antenna package (100) according to one of claims 1 to 4, wherein
the radio frequency signals are of a frequency above 90 GHz, and in particular in a frequency range of 140-160 GHz.

6. Antenna package (100) according to one of claims 1 to 5, wherein
the antenna port (102) is dimensioned smaller than the chip (103).

7. Antenna package (100) according to one of claims 1 to 6, wherein
the coupling slot (107) is included completely in the resonant dielectric cavity (106).

8. Antenna package (100) according to one of claims 1 to 7, wherein
the chip (103) comprises a plurality of metal coupling slots (107) on its bottom side for coupling the radio frequency signals into a plurality of antenna ports (102).

9. Antenna package (100) according to one of claims 1 to 8, wherein
the chip (103) is manufactured in the GaAs material system.

10. Method (700) of manufacturing an antenna package (100), the method comprising the steps of:

providing (701) an antenna (101) with an embedded antenna port (102), the antenna (101) including an antenna port side and an antenna radiation side,
providing (702) a semiconductor chip (103) on the antenna port side,
configuring (703) the chip (103) with coupling elements for coupling radio frequency signals from a top side of the chip (103) to the antenna port (102) by:

providing (7031) a matching network including a high-impedance microstrip line (104) having an impedance larger than 50Ω and a ground window (105) on the top side of the chip (103),
creating (7032) a resonant dielectric cavity (106) within the chip (103), and
providing (7033) a metal coupling slot (107) facing the antenna port (102) on a bottom side of the chip (103),

wherein side walls of the resonant dielectric cavity (106) are defined by ground vias (203) connecting a top and a bottom ground layer of the chip (103), and
wherein the coupling slot (107) is dimensioned and arranged such that, when the antenna package (100) is viewed from the antenna port side, the antenna port (102) completely includes the coupling slot (107).

Patentansprüche

1. Antennenpaket (100), umfassend:

eine Antenne (101) mit einem eingebetteten Antennenanschluss (102), wobei die Antenne (101) eine Antennenanschlussseite und eine Antennenstrahlungsseite beinhaltet; und
einen Halbleiterchip (103), der an der Antennenanschlussseite bereitgestellt ist,
wobei der Chip (103) Kopplungselemente zum Koppeln von Funkfrequenzsignalen von einer Oberseite des Chips (103) mit dem Antennenanschluss (102) umfasst, wobei die Kopplungselemente Folgendes umfassen:

eine Anpassungsnetzwerk, das eine hoch-

ohmige Mikrostreifenleitung (104), die eine Impedanz von mehr als 50 Ω aufweist, und ein Massefenster (105) an der Oberseite des Chips (103) beinhaltet,
einen dielektrischen Resonanzhohlraum (106) innerhalb des Chips (103) und
einen dem Antennenanschluss (102) zugewandten Metallkopplungsschlitz (107) an einer Unterseite des Chips (103),

wobei Seitenwände des dielektrischen Resonanzhohlraums (106) durch Masse-Vias (203) definiert sind, die eine obere und eine untere Masseschicht des Chips (103) verbinden, und
wobei der Kopplungsschlitz (107) so bemessen und angeordnet ist, dass der Antennenanschluss (102) den Kopplungsschlitz (107) vollständig beinhaltet, wenn das Antennenpaket (100) von der Antennenanschlussseite aus betrachtet wird.

2. Antennenpaket (100) nach Anspruch 1, umfassend: einen λ/4-Wellenleiter (201), der zwischen dem Chip (103) und dem Antennenanschluss (102) angeordnet ist.

3. Antennenpaket (100) nach Anspruch 2, wobei der λ/4-Wellenleiter (201) so bemessen und angeordnet ist, dass er den Kopplungsschlitz (107) an der Unterseite des Chips (103) vollständig beinhaltet.

4. Antennenpaket (100) nach Anspruch 2 oder 3, wobei ein Verhältnis zwischen einer Flächengröße des λ/4-Wellenleiters (201) und einer Flächengröße des Kopplungsschlitzes (107) in einem Bereich von 6-8 und vorzugsweise bei 7 liegt.

5. Antennenpaket (100) nach einem der Ansprüche 1 bis 4, wobei
die Funkfrequenzsignale eine Frequenz über 90 GHz aufweisen und insbesondere in einem Frequenzbereich von 140-160 GHz liegen.

6. Antennenpaket (100) nach einem der Ansprüche 1 bis 5, wobei
der Antennenanschluss (102) kleinere Abmessungen aufweist als der Chip (103).

7. Antennenpaket (100) nach einem der Ansprüche 1 bis 6, wobei
der Kopplungsschlitz (107) vollständig in dem dielektrischen Resonanzhohlraum (106) beinhaltet ist.

8. Antennenpaket (100) nach einem der Ansprüche 1 bis 7, wobei
der Chip (103) eine Vielzahl von Metallkopplungsschlitzen an seiner Unterseite (107) zum Koppeln der Funkfrequenzsignale in eine Vielzahl von Antennenanschlüssen (102) umfasst.

9. Antennenpaket (100) nach einem der Ansprüche 1 bis 8, wobei der Chip (103) in dem GaAs-Materialsystem hergestellt wird.

10. Verfahren (700) zum Herstellen eines Antennenpakets (100), wobei das Verfahren die folgenden Schritte umfasst:

Bereitstellen (701) einer Antenne (101) mit einem eingebetteten Antennenanschluss (102), wobei die Antenne (101) eine Antennenanschlussseite und eine Antennenstrahlungsseite beinhaltet,
Bereitstellen (702) eines Halbleiterchips (103) an der Antennenanschlussseite,
Konfigurieren (703) des Chips (103) mit Kopplungselementen zum Koppeln von Funkfrequenzsignalen von einer Oberseite des Chips (103) mit dem Antennenanschluss (102) durch:

Bereitstellen (7031) eines Anpassungsnetzwerks, das eine hochohmige Mikrostreifenleitung (104), die eine Impedanz von mehr als 50 Ω aufweist, und ein Massefenster (105) an der Oberseite des Chips (103) beinhaltet,
Erzeugen (7032) eines dielektrischen Resonanzhohlraums (106) innerhalb des Chips (103) und
Bereitstellen (7033) eines dem Antennenanschuss (102) zugewandten Metallkopplungsschlitzes (107) an einer Unterseite des Chips (103),

wobei Seitenwände des dielektrischen Resonanzhohlraums (106) durch Masse-Vias (203) definiert sind, die eine obere und eine untere Masseschicht des Chips (103) verbinden, und
wobei der Kopplungsschlitz (107) so bemessen und angeordnet ist, dass der Antennenanschluss (102) den Kopplungsschlitz (107) vollständig beinhaltet, wenn das Antennenpaket (100) von der Antennenanschlussseite aus betrachtet wird.

Revendications

1. Boîtier d'antenne (100) comprenant :

une antenne (101) avec un port d'antenne (102) incorporé, l'antenne (101) incluant un côté port d'antenne et un côté rayonnement d'antenne, et une puce semi-conductrice (103) disposée sur le côté port d'antenne,
dans lequel la puce (103) comprend des élé-

ments de couplage pour coupler des signaux radiofréquences d'un côté supérieur de la puce (103) au port d'antenne (102), les éléments de couplage comprenant :

un réseau d'adaptation incluant une ligne microruban à haute impédance (104) ayant une impédance supérieure à 50 Ω et une fenêtre de masse (105) sur le côté supérieur de la puce (103),
une cavité diélectrique résonante (106) à l'intérieur de la puce (103), et
un plot de couplage métallique (107) faisant face au port d'antenne (102) sur un côté inférieur de la puce (103)

dans lequel des parois latérales de la cavité diélectrique résonante (106) sont définies par des trous d'interconnexion de masse (203) connectant une couche de masse supérieure et une couche de masse inférieure de la puce (103), et dans lequel le plot de couplage (107) est dimensionné et agencé de sorte que, lorsque le boîtier d'antenne (100) est vu du côté port d'antenne, le port d'antenne (102) inclut complètement le plot de couplage (107).

2. Boîtier d'antenne (100) selon la revendication 1, comprenant :
un guide d'onde λ/4 (201) agencé entre la puce (103) et le port d'antenne (102).

3. Boîtier d'antenne (100) selon la revendication 2, dans lequel
guide d'onde λ/4 (201) est dimensionné et agencé de sorte qu'il inclut complètement le plot de couplage (107) sur le côté inférieur de la puce (103).

4. Boîtier d'antenne (100) selon la revendication 2 ou 3, dans lequel
un rapport entre une taille de la surface du guide d'onde λ/4 (201) et une taille de la surface du plot de couplage (107) est dans une plage de 6 à 8, et est de préférence 7.

5. Boîtier d'antenne (100) selon l'une quelconque des revendications 1 à 4, dans lequel les signaux radiofréquences ont une fréquence au-delà de 90 GHz, et sont, en particulier, dans une plage de fréquences de 140 à 160 GHz.

6. Boîtier d'antenne (100) selon l'une quelconque des revendications 1 à 5, dans lequel le port d'antenne (102) est dimensionné plus petit que la puce (103).

7. Boîtier d'antenne (100) selon l'une quelconque des revendications 1 à 6, dans lequel le plot de couplage (107) est inclus complètement dans la cavité diélectrique résonante (106).

8. Boîtier d'antenne (100) selon l'une quelconque des revendications 1 à 7, dans lequel la puce (103) comprend une pluralité de plots de couplage métalliques (107) sur son côté inférieur pour le couplage des signaux radiofréquences à une pluralité de ports d'antenne (102).

9. Boîtier d'antenne (100) selon l'une quelconque des revendications 1 à 8, dans lequel la puce (103) est fabriquée dans le système de matériaux GaAs.

10. Procédé (700) de fabrication d'un boîtier d'antenne (100), le procédé comprenant les étapes consistant à :

fournir (701) une antenne (101) avec un port d'antenne (102) incorporé, l'antenne (101) incluant un côté port d'antenne et un côté rayonnement d'antenne,
fournir (702) une puce semi-conductrice (103) sur le côté port d'antenne,
configurer (703) la puce (103) avec des éléments de couplage pour coupler des signaux radiofréquences d'un côté supérieur de la puce (103) au port d'antenne (102) par :

la fourniture (7031) d'un réseau d'adaptation incluant une ligne microruban à haute impédance (104) ayant une impédance supérieure à 50 Ω et une fenêtre de masse (105) sur le côté supérieur de la puce (103),
la création (7032) d'une cavité diélectrique résonante (106) à l'intérieur de la puce (103), et
la fourniture (7033) d'un plot de couplage métallique (107) faisant face au port d'antenne (102) sur un côté inférieur de la puce (103),

dans lequel des parois latérales de la cavité diélectrique résonante (106) sont définies par des trous d'interconnexion de masse (203) connectant une couche de masse supérieure et une couche de masse inférieure de la puce (103), et dans lequel le plot de couplage (107) est dimensionné et agencé de sorte que, lorsque le boîtier d'antenne (100) est vu du côté port d'antenne, le port d'antenne (102) inclut complètement le plot de couplage (107).

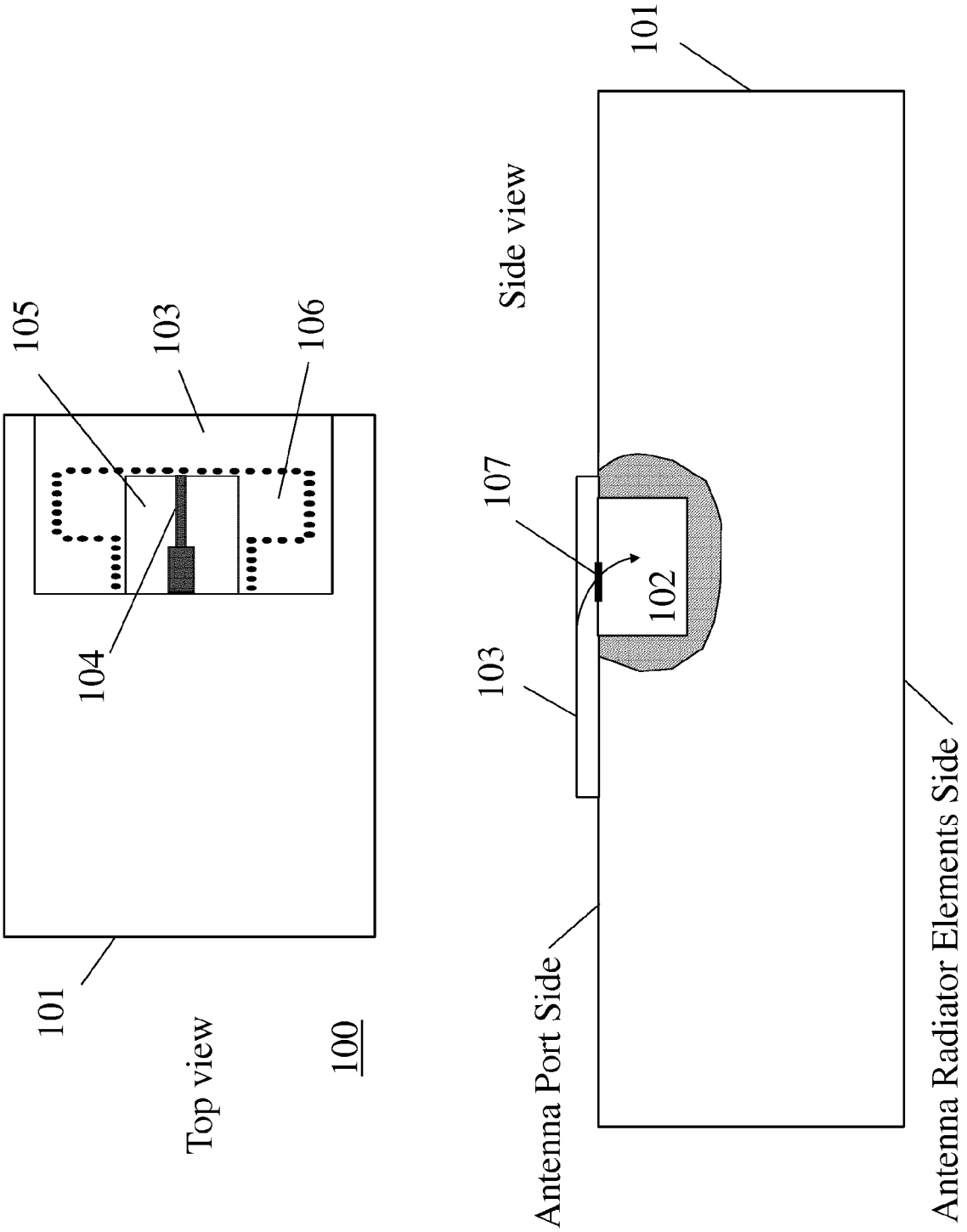
105
103
106
104
101
Top view
100
Side view
101
107
102
103
Antenna Port Side
Antenna Radiator Elements Side

Fig. 1

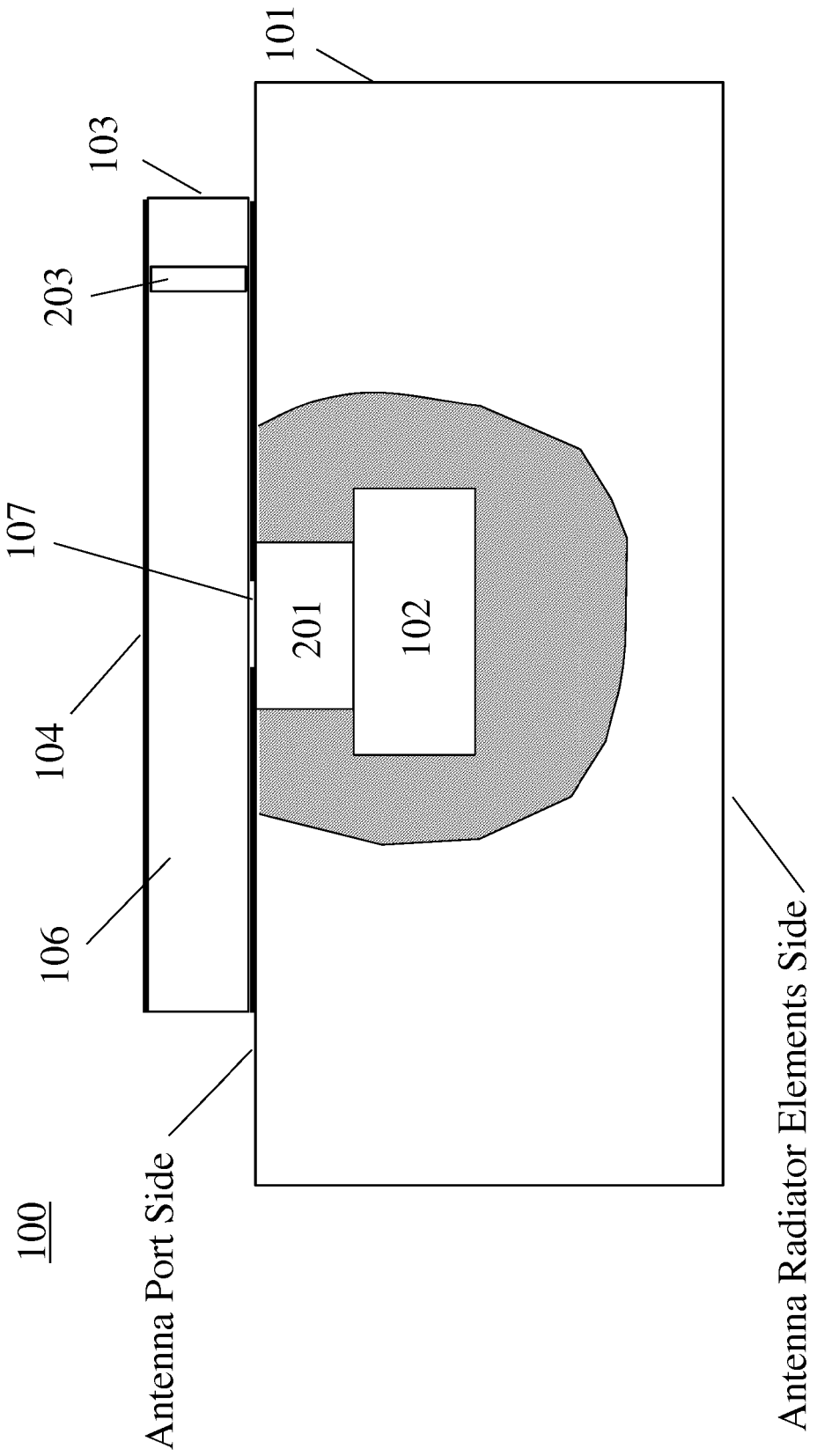
100
101
103
203
107
104
106
201
102
Antenna Port Side
Antenna Radiator Elements Side

Fig. 2

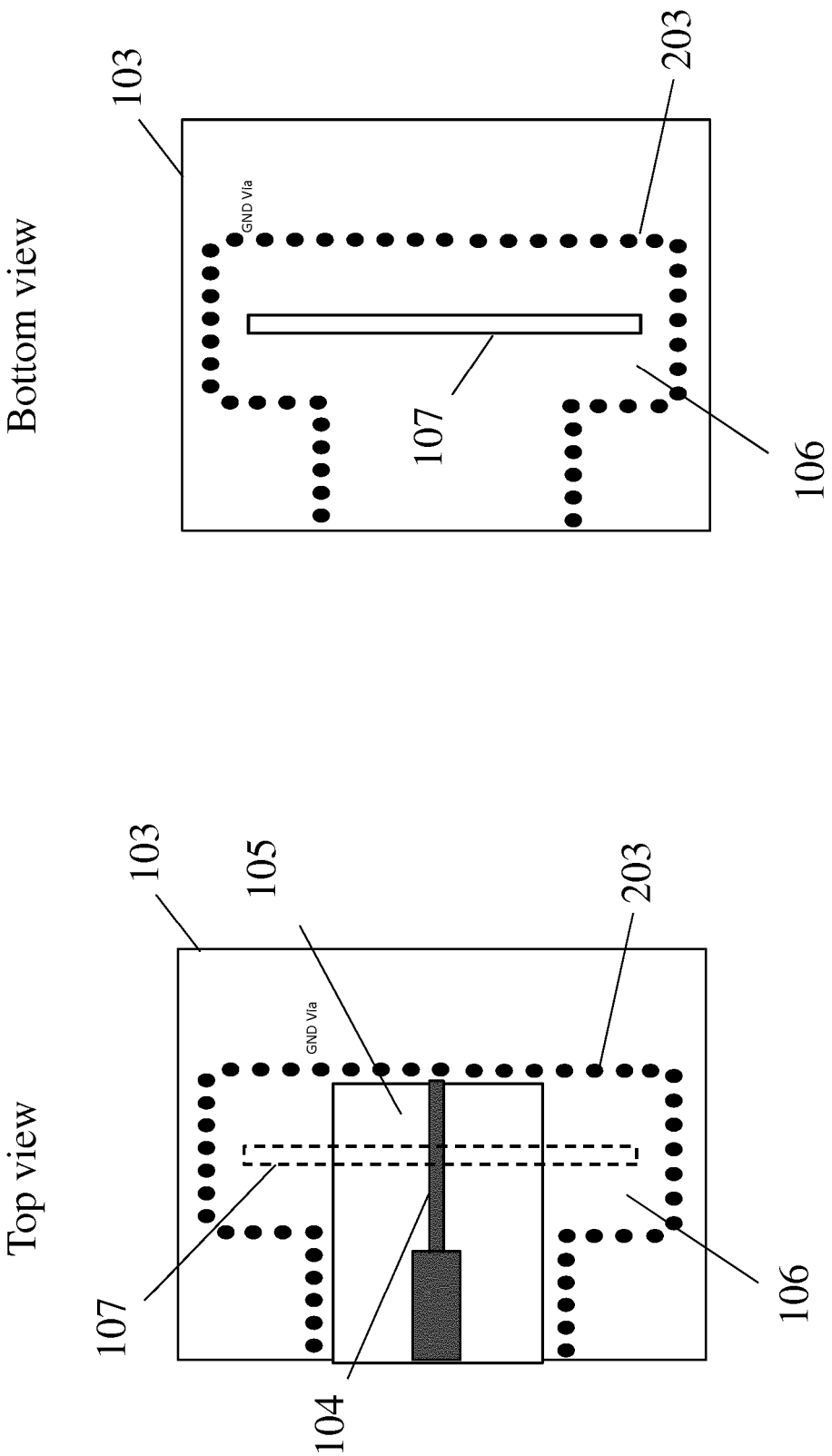
Bottom view
103
203
GND Via
107
106
Top view
103
105
203
GND Via
107
104
106

Fig. 3

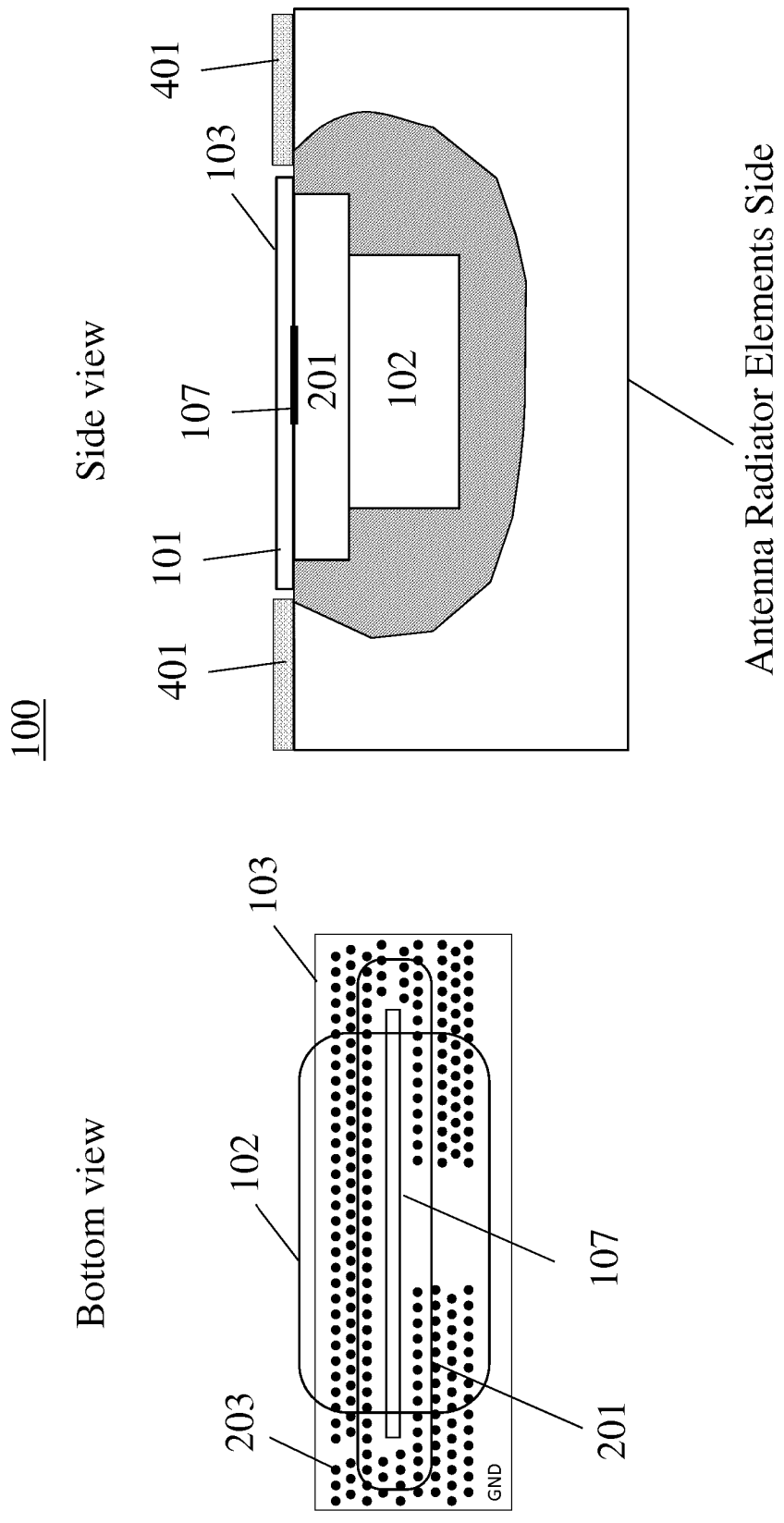
100
Side view
401
103
107
201
102
101
401
Antenna Radiator Elements Side
Bottom view
103
102
107
203
201
GND

Fig. 4

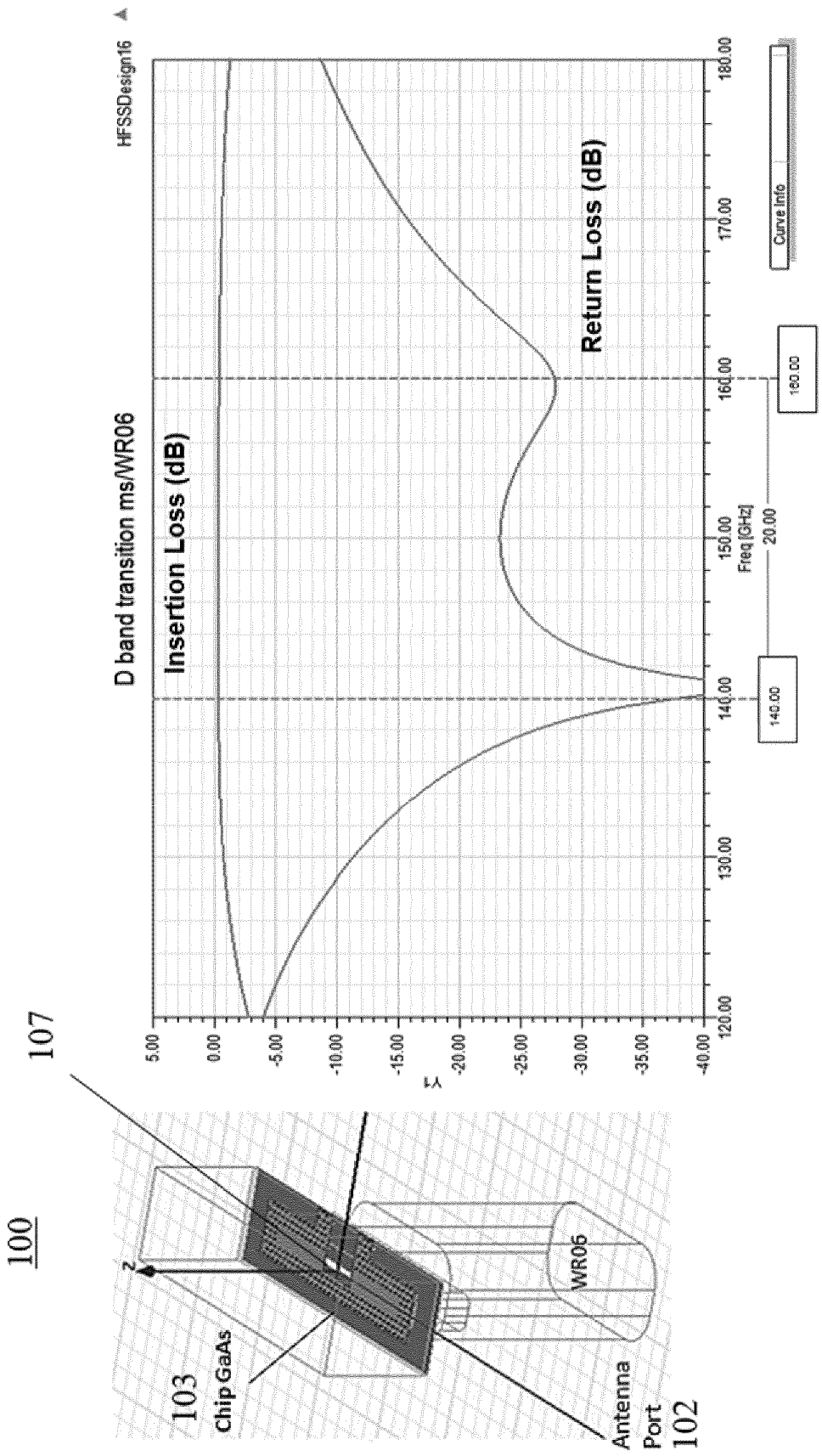
100
107
103
Chip GaAs
Z
WR06
Antenna
Port
102
HFSSDesign16
D band transition ms/WR06
Insertion Loss (dB)
Return Loss (dB)
Y1
5.00
0.00
-5.00
-10.00
-15.00
-20.00
-25.00
-30.00
-35.00
-40.00
120.00
130.00
140.00
150.00
160.00
170.00
180.00
Freq [GHz]
20.00
140.00
160.00
Curve Info

Fig. 5

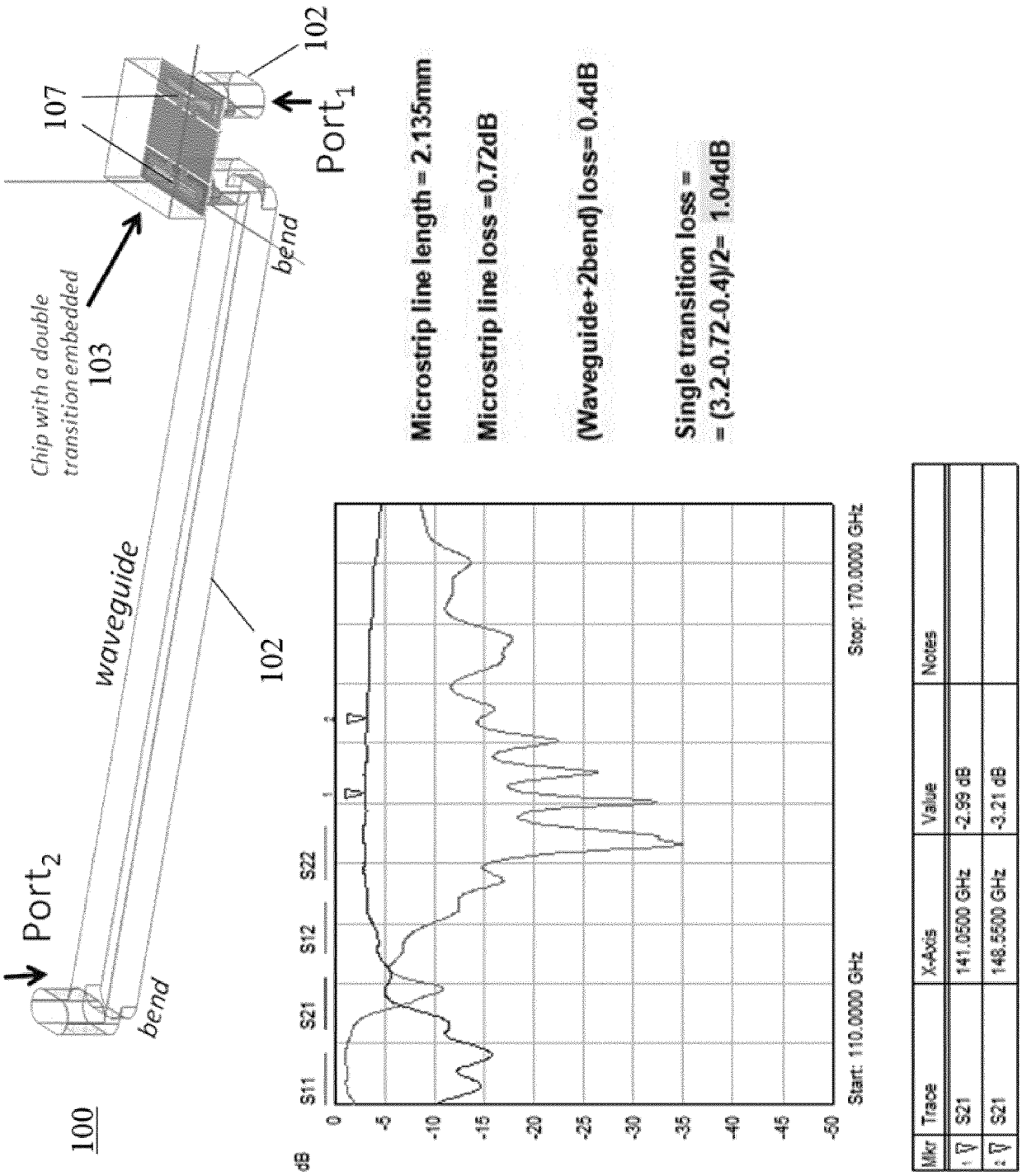
100
Port2
bend
waveguide
102
Chip with a double transition embedded
103
107
bend
Port1
102
Microstrip line length = 2.135mm
Microstrip line loss =0.72dB
(Waveguide+2bend) loss= 0.4dB
Single transition loss =
= (3.2-0.72-0.4)/2= 1.04dB
S11
S21
S12
S22
dB
0
-5
-10
-15
-20
-25
-30
-35
-40
-45
-50
Start: 110.0000 GHz
Stop: 170.0000 GHz
Mkr | Trace | X-Axis | Value | Notes
1 | S21 | 141.0500 GHz | -2.99 dB
2 | S21 | 148.5500 GHz | -3.21 dB

Fig. 6

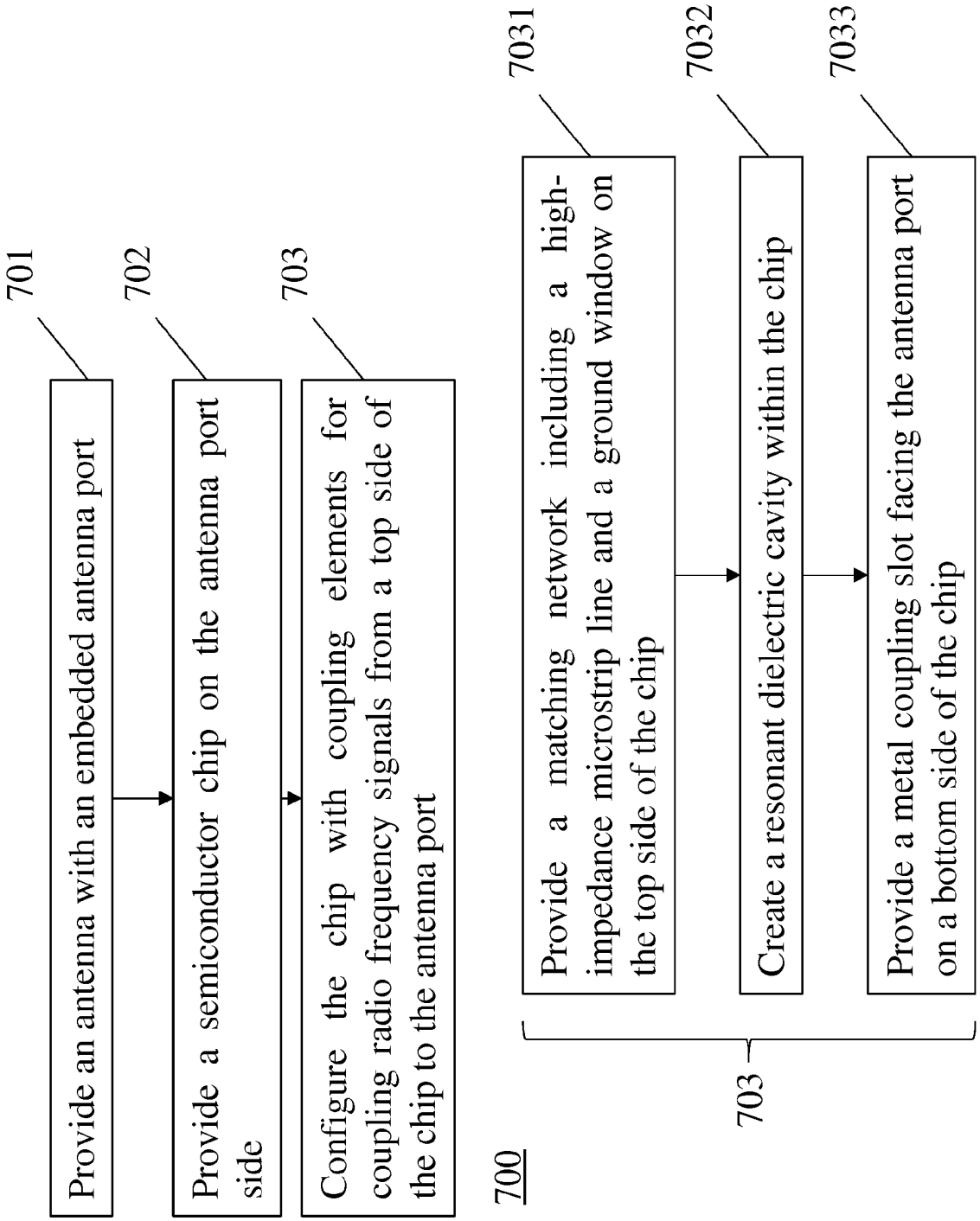
701
Provide an antenna with an embedded antenna port
702
Provide a semiconductor chip on the antenna port side
703
Configure the chip with coupling elements for coupling radio frequency signals from a top side of the chip to the antenna port
700
703
7031
Provide a matching network including a high-impedance microstrip line and a ground window on the top side of the chip
7032
Create a resonant dielectric cavity within the chip
7033
Provide a metal coupling slot facing the antenna port on a bottom side of the chip

Fig. 7

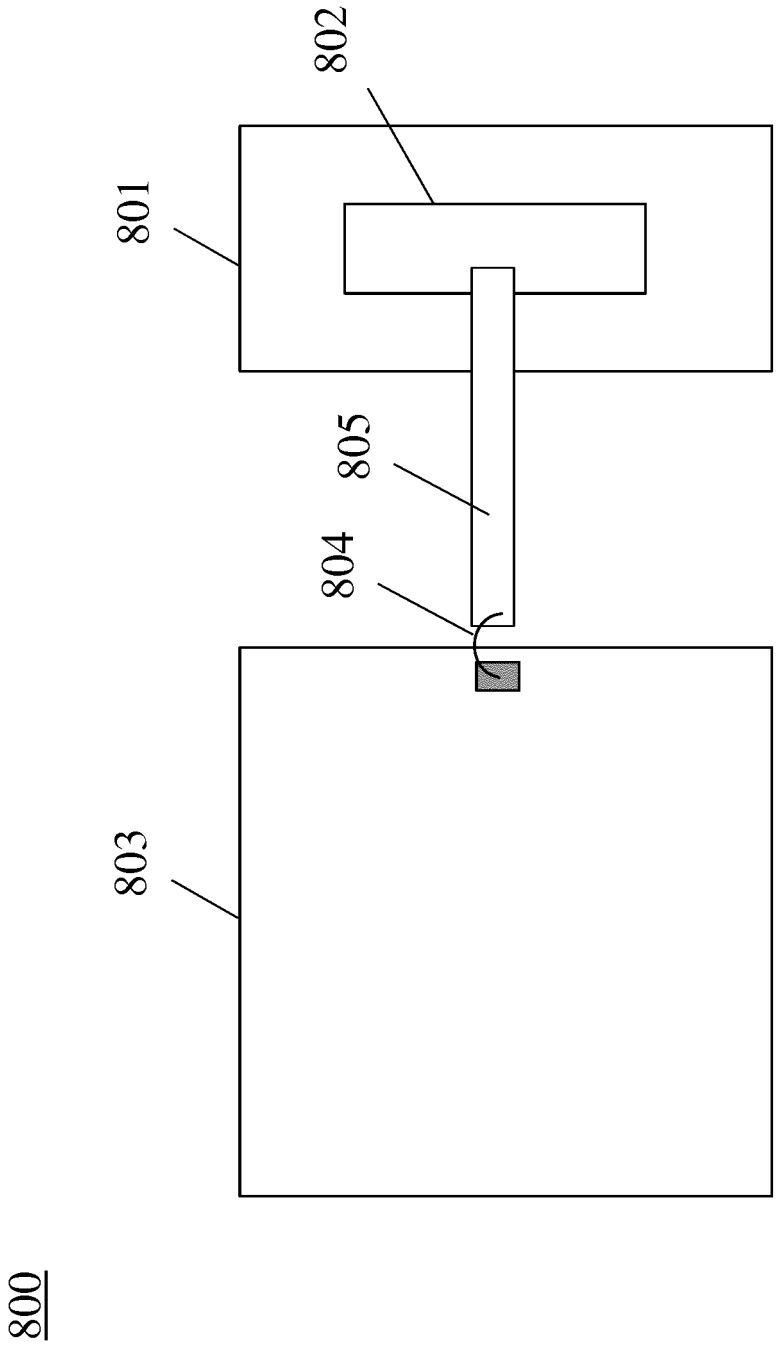

Fig. 8

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 2007216493 A1 **[0008]**
- US 20160079675 A1 **[0009]**

Non-patent literature cited in the description

- **XIAO-JUN TANG et al.** A 60-GHz Wideband Slot Antenna Based on Substrate Integrated Waveguide Cavity. *International Journal of Infrared and Millimeter Waves,* 2007, 275-281 **[0010]**