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(54) STACKED SEMICONDUCTOR PACKAGE HAVING ADHESIVE/SPACER STRUCTURE AND INSULATION

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(60) Provisional application No. 60/573,956, filed on May 24, 2004. Provisional application No. 60/573,903, filed on May 24, 2004.

Publication Classification

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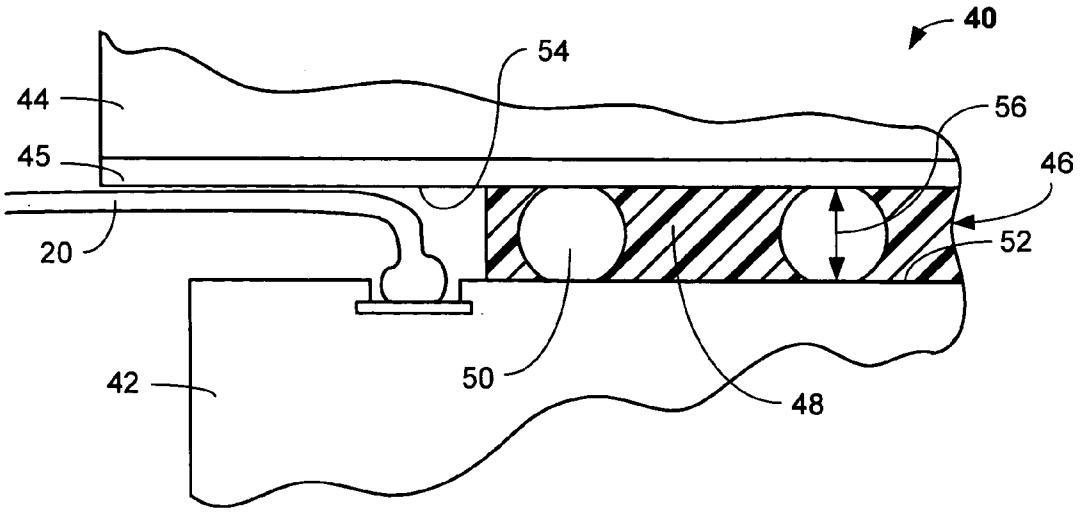
(57) **ABSTRACT**

Stacked semiconductor assemblies in which a device such as a die, or a package, or a heat spreader is stacked over a first wire-bonded die. An adhesive/spacer structure is situated between the first wire-bonded die and the device stacked over it, and the device has an electrically non-conductive surface facing the first wire-bonded die. That is, the first die is mounted active side upward on a first substrate and is electrically interconnected to the substrate by wire bonding; an adhesive/spacer structure is formed upon the active side of the first die; and a device such as a die or a package or a heat spreader, having an electrically nonconductive side, is mounted upon the adhesive/spacer structure with the electrically nonconductive side facing the first wire bonded die. The side of the device facing the first wire bonded die may be made electrically nonconductive by having an electrically insulating layer, such as a dielectric film adhesive. Also, methods for making the assemblies are disclosed.



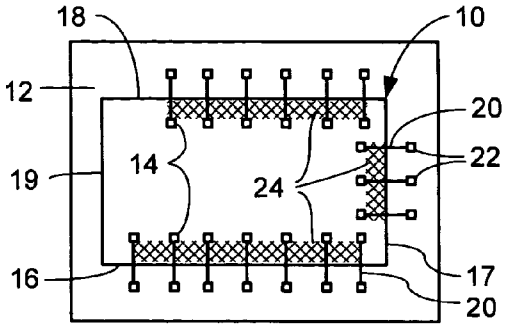


Fig. 1
PRIOR ART

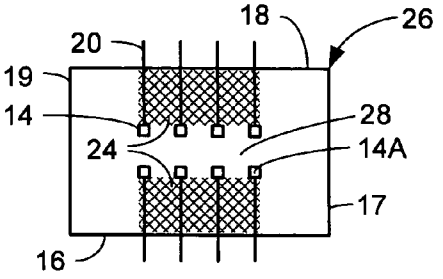


Fig. 2
PRIOR ART

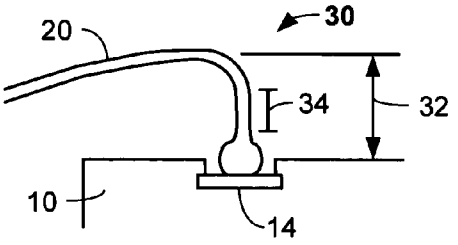


Fig. 3
PRIOR ART

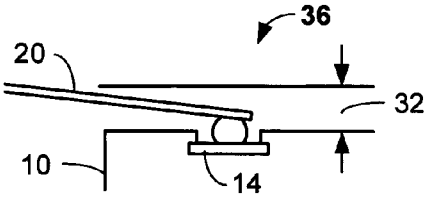


Fig. 4
PRIOR ART

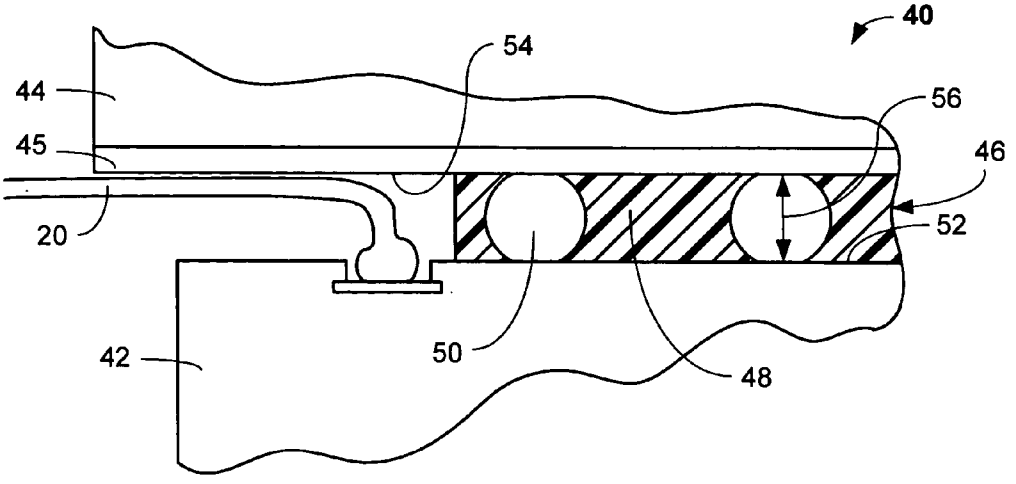


Fig. 5

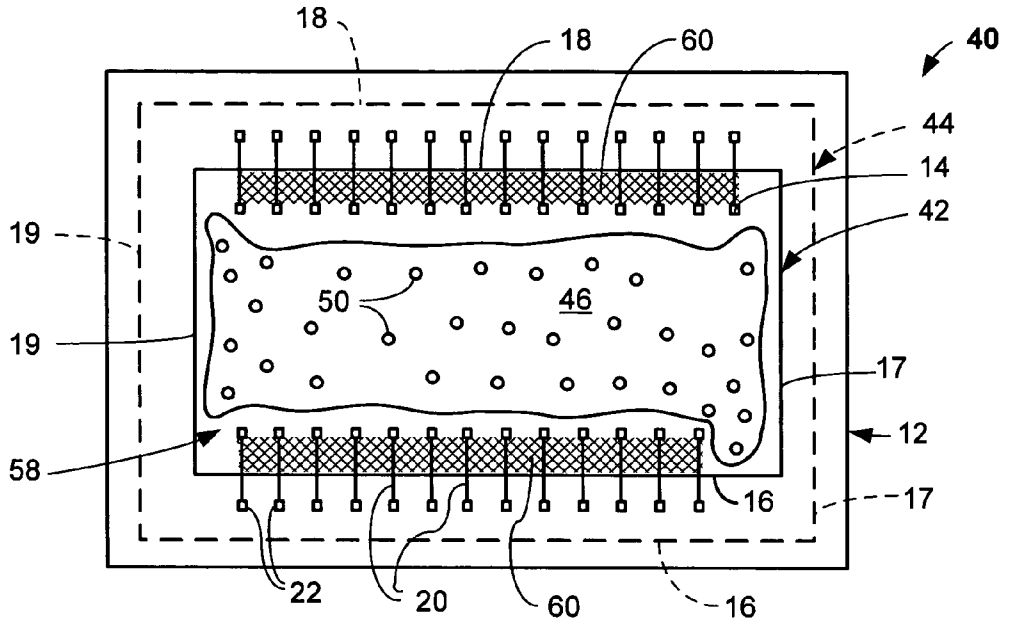

18
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Fig. 6

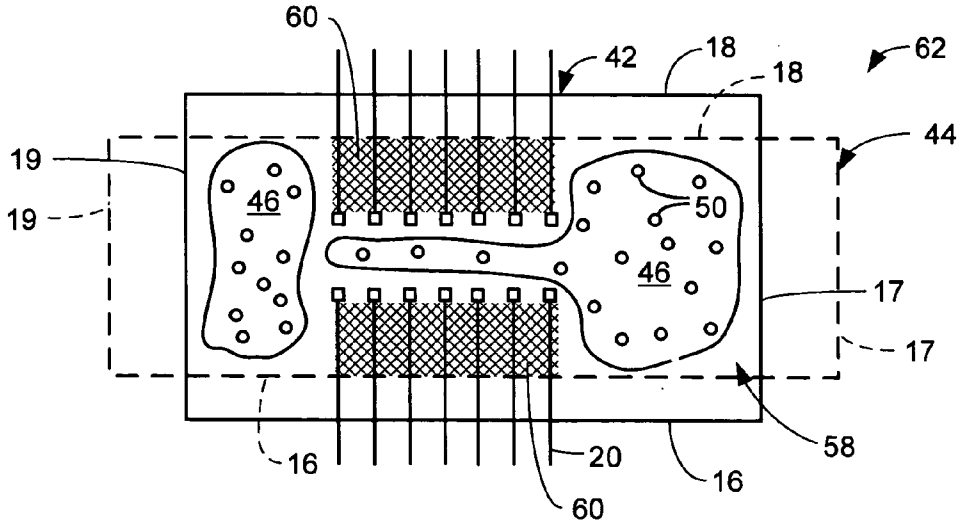
60
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Fig. 7

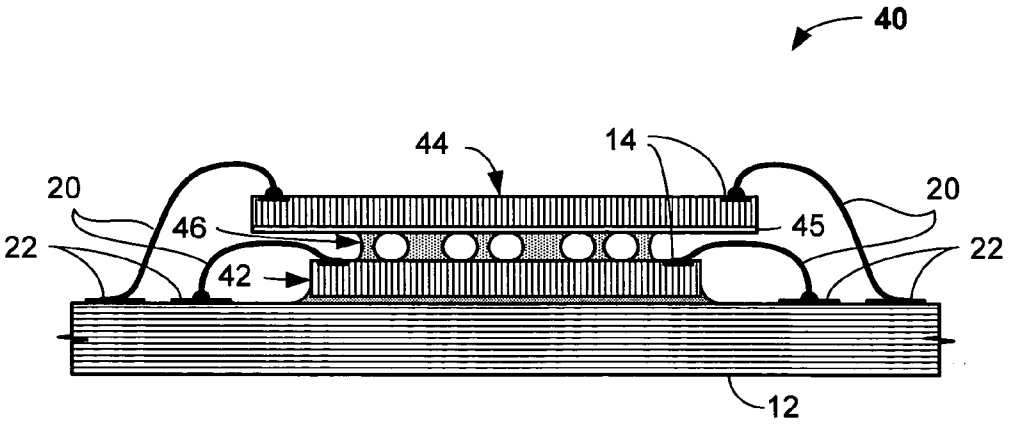

Fig. 8

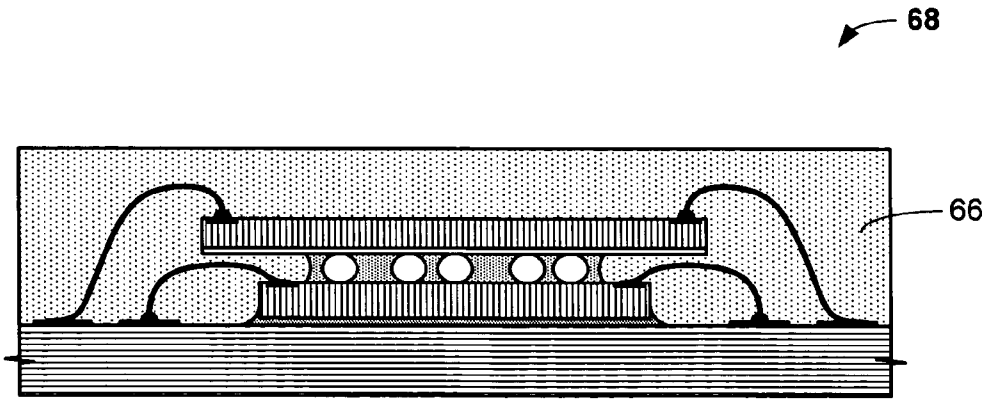

Fig. 9

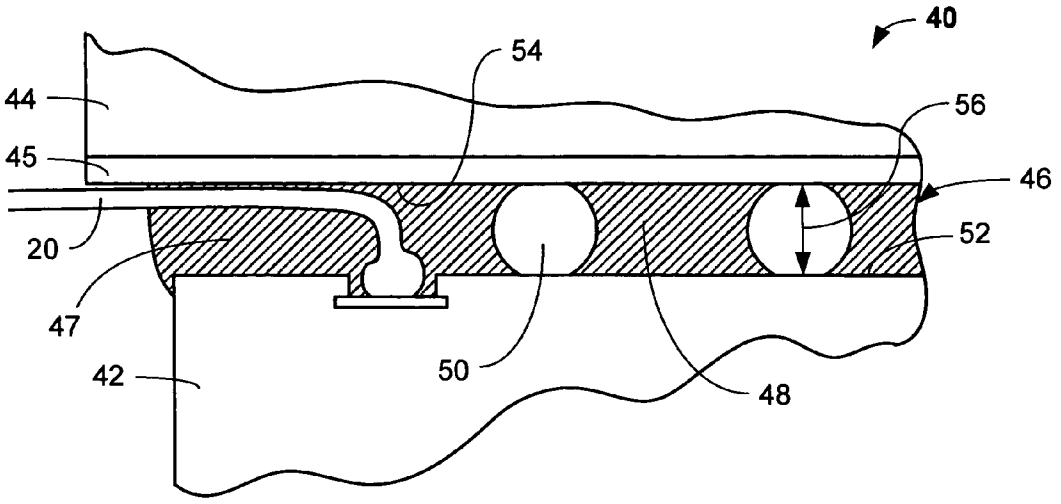

Fig. 10

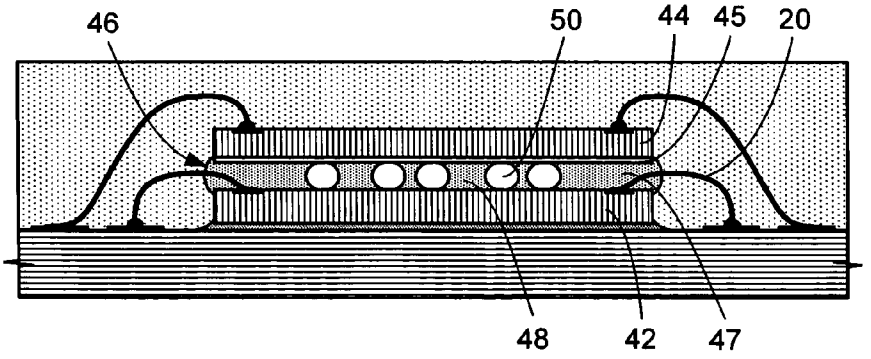

Fig. 11

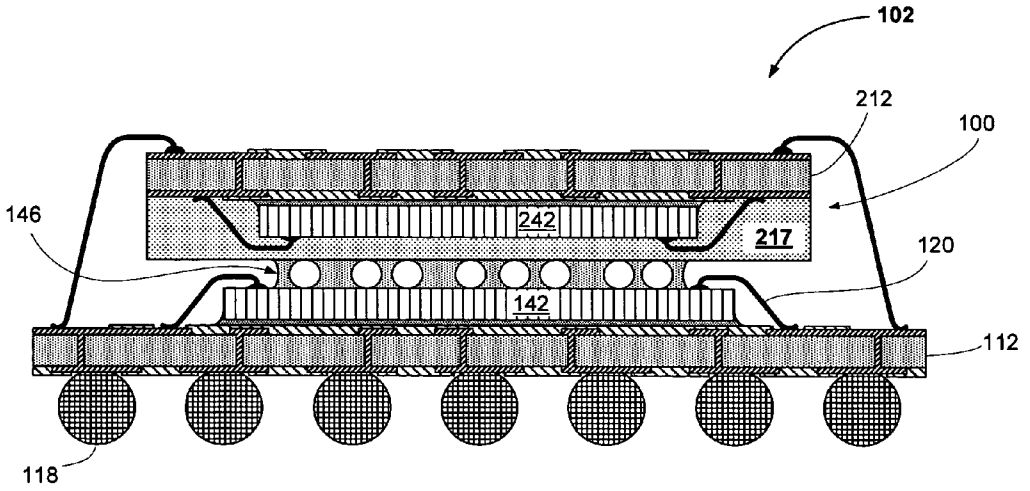
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Fig. 12

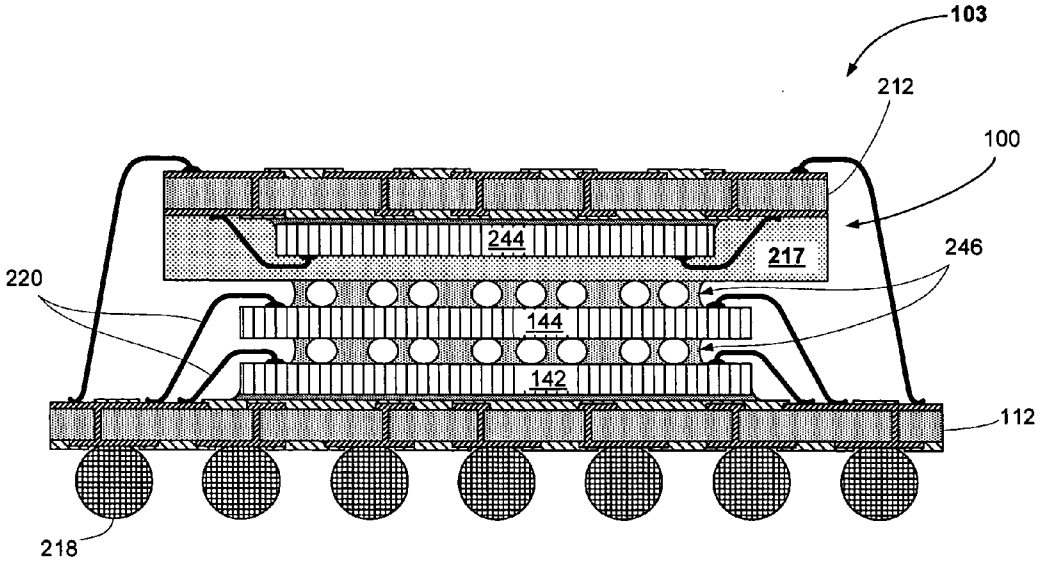
103
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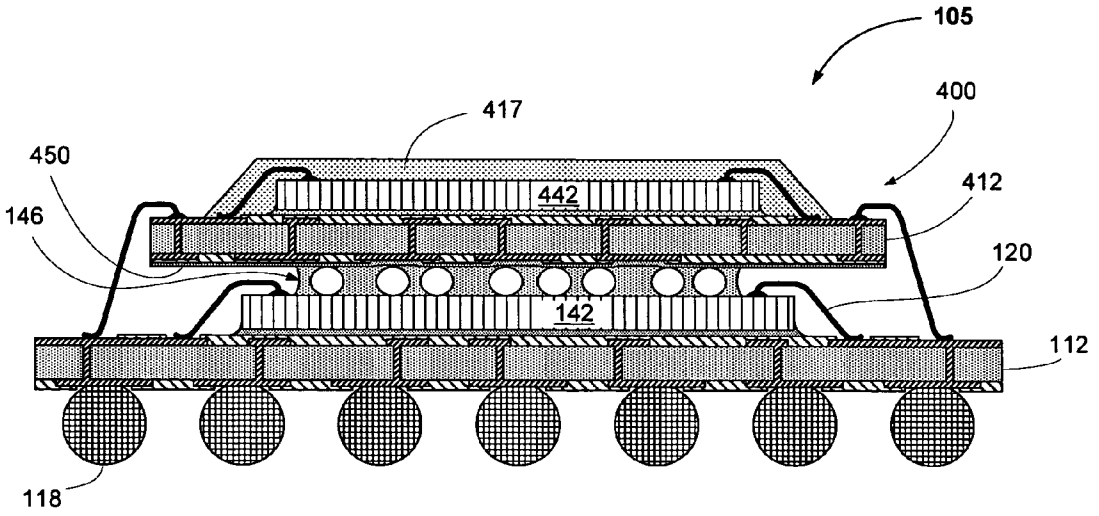
Fig. 13


105
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412
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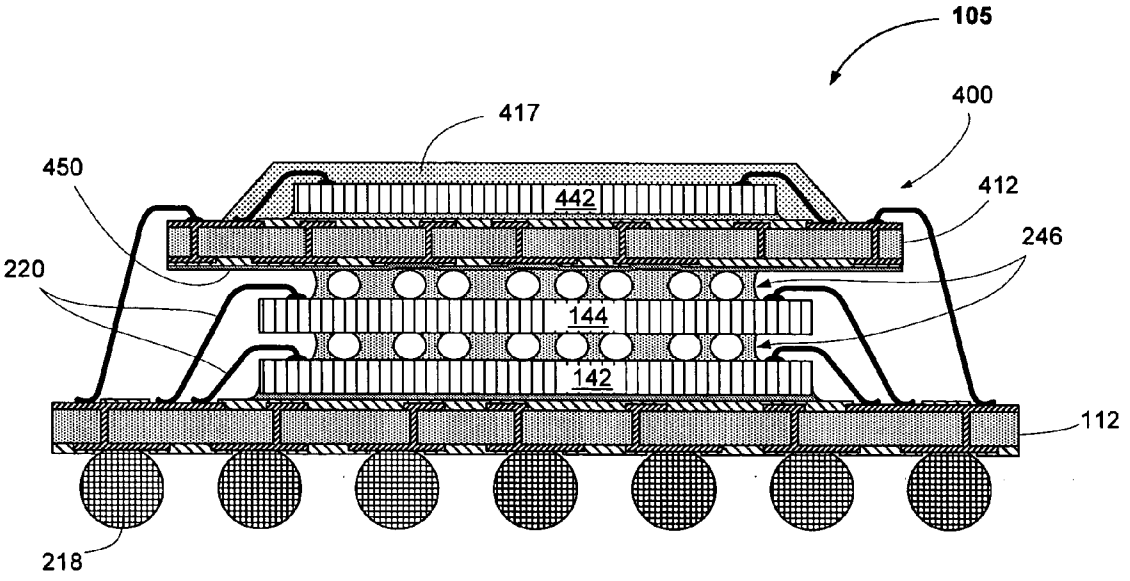
Fig. 14


105
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417
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Fig. 15

STACKED SEMICONDUCTOR PACKAGE HAVING ADHESIVE/SPACER STRUCTURE AND INSULATION

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a Continuation-in-Part of U.S. application Ser. No. 10/969,303, filed Oct. 20, 2004, titled "Multiple die package with adhesive/spacer structure and insulated die surface". The said U.S. application Ser. No. 10/969,303 claims priority from U.S. Provisional Application No. 60/573,956, filed May 24, 2004, titled "Multiple die package with adhesive/spacer structure and insulated die surface"; and also claims priority from related U.S. Provisional Application No. 60/573,903, filed May 24, 2004, titled "Adhesive/spacer island structure for multiple die package". This application is related to U.S. application Ser. No. 10/_____, Attorney Docket CPAC 1074-3, filed on the same day as this application.

BACKGROUND

[0002] To obtain the maximum function and efficiency from a package having minimum dimensions, various types of increased density packages have been developed. Among these various types of packages is the multiple-die semiconductor chip package, commonly referred to as a multi-chip module, multi-chip package or stacked chip package. A multi-chip module includes one or more integrated circuit semiconductor chips, often referred to as circuit die, stacked one onto another to provide the advantages of light weight, high density, and enhanced electrical performance. To stack the semiconductor chips, each chip can be lifted by a chip-bonding tool, which is usually mounted at the end of a pick-and-place device, and mounted onto the substrate or onto a semiconductor chip mounted previously.

[0003] In some circumstances, such as when the upper die is smaller than the lower die and the lower die is a peripheral bonded die (that is die with bond pads positioned near the periphery of the die as opposed to a center bonded die in which the bond pads are positioned at a central region of the die), the upper die can be attached directly to the lower die without the use of spacers. However, when spacers are needed between the upper and lower die, spacer die, that is die without circuitry, can be used between the upper and lower die. In addition, adhesives containing spacer elements, typically micro spheres, are often used to properly separate the upper and lower die. See U.S. Pat. Nos. 5,323,060; 6,333,562; 6,340,846; 6,388,313; 6,472,758; 6,569,709; 6,593,662;.6,441,496; and U.S. patent Publication No. US 2003/0178710.

[0004] After the chip mounting process, bonding pads of the chips are connected to bonding pads of the substrate with Au or Al wires during a wire bonding process to create an array of semiconductor chip devices. Finally, the semiconductor chips and their associated wires connected to the substrate are encapsulated, typically using an epoxy-molding compound, to create an array of encapsulated semiconductor devices. The molding compound protects the semiconductor devices from the external environment, such as physical shock and humidity. After encapsulation, the encapsulated devices are separated, typically by sawing, into individual semiconductor chip packages.

SUMMARY

[0005] In general, the invention features stacked semiconductor assemblies in which a device such as a die, or a package, or a heat spreader is stacked over a first wire-bonded die. An adhesive/spacer structure is situated between the first wire-bonded die and the device stacked over it, and the device has an electrically non-conductive surface facing the first wire-bonded die. That is, the first die is mounted active side upward on a first substrate and is electrically interconnected to the substrate by wire bonding; an adhesive/spacer structure is formed upon the active side of the first die; and a device such as a die or a package or a heat spreader, having an electrically nonconductive side, is mounted upon the adhesive/spacer structure with the electrically nonconductive side facing the first wire bonded die. The side of the device facing the first wire bonded die may be made electrically nonconductive by having an electrically insulating layer, such as a dielectric film adhesive.

[0006] In one aspect the invention features a multiple-die semiconductor chip assembly. A first die has a first surface bounded by a periphery and bond pads at the first surface. Wires are bonded to and extend from the bond pads outwardly past the periphery. A second die has an electrically non-conductive second surface positioned opposite the first surface. The first and second die define a first region therebetween. An adhesive/spacer structure, comprising spacer elements within an adhesive, is within the first region. The adhesive/spacer structure contacts the first and second surfaces and adheres the first and second die to one another at a chosen separation. The assembly may comprise a set of generally parallel wires which define a wire span portion of the first region. The adhesive/spacer structure is preferably located at other than the wire span portion of the first region.

[0007] In another aspect the invention features a method for adhering first and second die to one another at a chosen separation in a multiple-die semiconductor chip assembly. An adhesive/spacer material, having spacer elements within an adhesive, is selected. The adhesive/spacer material is deposited onto a first surface of a first die. The first surface is bounded by a periphery and has bond pads. A set of generally parallel wires is bonded to and extends from the bond pads outwardly past the periphery. The set of generally parallel wires define a wire span portion of the first surface. A second die, having an electrically non-conductive second surface, is selected. The second surface of the second die is located opposite the first surface of the first die and in contact with the adhesive/spacer material therebetween thereby securing the first and second die to one another at a chosen separation, the wire span portion of the first surface defining a wire span region between the first and second surfaces. The adhesive/spacer material is deposited in a manner to prevent any spacer elements from entering the wire span region.

[0008] In another aspect the invention features stacked semiconductor assemblies including an upper package stacked over a first wire-bonded die. The first die has a first surface bounded by a periphery and bond pads at the first surface. Wires are bonded to and extend from the bond pads outwardly past the periphery. An upper package has an electrically non-conductive second surface positioned opposite the first surface of the first die. The first die and the upper package define a first region therebetween. An adhesive/

spacer structure, comprising spacer elements within an adhesive, is within the first region. The adhesive/spacer structure contacts the first and second surfaces and adheres the first die and the upper package to one another at a chosen separation. The assembly may comprise a set of generally parallel wires which define a wire span portion of the first region. The adhesive/spacer structure is preferably located at other than the wire span portion of the first region.

[0009] The upper package in the stacked semiconductor assembly includes at least one upper package die affixed to a die attach side of an upper package substrate. In some embodiments the upper package is oriented so that the die attach side of the upper package substrate faces the first die; that is, the upper package is inverted. In other embodiments the upper package is oriented so that the side of the upper package substrate opposite the die attach side faces the first die. The upper package may be any of a variety of package types can be suitable as the upper package.

[0010] In another aspect the invention features a method for adhering a die and a package to one another at a chosen separation in a stacked semiconductor package. An adhesive/spacer material, having spacer elements within an adhesive, is selected. The adhesive/spacer material is deposited onto a first surface of a first die. The first surface is bounded by a periphery and has bond pads. A set of generally parallel wires is bonded to and extends from the bond pads outwardly past the periphery. The set of generally parallel wires define a wire span portion of the first surface. A package, having an electrically non-conductive second surface, is selected. The second surface of the package is located opposite the first surface of the die and in contact with the adhesive/spacer material therebetween thereby securing the die and the package to one another at a chosen separation, the wire span portion of the first surface defining a wire span region between the first and second surfaces. The adhesive/spacer material is deposited in a manner to prevent any spacer elements from entering the wire span region.

[0011] Various features and advantages of the invention will appear from the following description in which the preferred embodiments have been set forth in detail in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] **FIG. 1** is a simplified plan view of a conventional peripheral bonded die;

[0013] **FIG. 2** is a simplified plan view of a conventional center bonded die;

[0014] **FIGS. 3 and 4** illustrate conventional forward loop and reverse wire bonds;

[0015] **FIG. 5** is a partial cross sectional view of a multi-die semiconductor assembly made according to the invention;

[0016] **FIG. 6** is a top plan view of the assembly of **FIG. 5** with the periphery of the upper die shown in dashed lines;

[0017] **FIG. 7** illustrates an alternative embodiment to the assembly of **FIG. 6**;

[0018] **FIG. 8** is a side cross sectional view of the assembly of **FIGS. 5 and 6**;

[0019] **FIG. 9** shows the assembly of **FIG. 8** After encapsulation with a molding compound to create a multiple die semiconductor chip package; and

[0020] **FIG. 10** illustrates an alternative embodiment similar to that of **FIG. 5** in which adhesive fills the wire span portion of the adhesive region; and

[0021] **FIG. 11** illustrates an alternative embodiment in a view similar to that of **FIG. 9** but in which the upper die does not overhang the edge of the lower die, and in which adhesive fills the wire span portion of the adhesive region as in **FIG. 10**.

[0022] **FIGS. 12 through 15** illustrate embodiments of assemblies according to various aspects of the invention in which a package and a die are stacked.

DETAILED DESCRIPTION

[0023] The invention will now be described in further detail by reference to the drawings, which illustrate alternative embodiments of the invention. The drawings are diagrammatic, showing features of the invention and their relation to other features and structures, and are not made to scale. For improved clarity of presentation, in the FIGs. illustrating embodiments of the invention, elements corresponding to elements shown in other drawings are not all particularly renumbered, although they are all readily identifiable in all the FIGs. Terms of orientation, such as "upper" and "lower" and the like are employed for reference to the relative orientation of the various features as shown in the FIGs., it being understood that any of the various assemblies can be deployed in any orientation in use.

[0024] Several prior art structures and embodiments made according to the invention are discussed below. Like reference numerals refer to like elements.

[0025] **FIG. 1** illustrates a conventional peripheral bonded die **10** mounted to a substrate **12**. Die **10** has bond pads **14** along one, some or all of its peripheral edges **16-19**. Wires **20** connect bond pads **14** to corresponding bond pads **22** on substrate **12**. Wires **20** comprise sets of generally parallel wires along each peripheral edge **16-18** and define wire span areas **24**, indicated by crosshatching in **FIG. 1**, along such edges. Bond pads **14** on peripheral bonded die **10** are typically placed very close to the corresponding peripheral edge **16-19**, typically within 100 micrometers of the peripheral edge.

[0026] **FIG. 2** illustrates a conventional center bonded die **26**, such as a DRAM, having bond pads **14** at a central region **28** of die **26**. Wires **20** extending from bond pads **14** define, in this example, wire span areas **24** between the two sets of bond pads **14** and peripheral edges **16**, **18**. The distance between bond pads **14** and the corresponding peripheral edges for a center bonded die is preferably much more than 100 micrometers. More preferably, the distance between a bond pad **14** for a center bonded die **26** and the nearest peripheral edge is at least about 40% of the corresponding length or width of the die. For example, the distance between a bond pad **14A** and peripheral edge **16** is at least about 40% of the length of peripheral edge **17**. Assuming for example that peripheral edge **17** is 8 mm long, the distance between bond pad **14A** and peripheral edges **16** is at least about 3.2 mm.

[0027] **FIGS. 3 and 4** illustrate conventional forward loop wire bonding and conventional reverse wire bonding techniques. Forward loop wire bond **30** of **FIG. 3** has a wire loop height **32**, typically about 60-100 micrometers. Wire **20** has a recrystalization zone **34**. Recrystalization zone **34** is not as flexible as the remainder of wire **20** so that excessive flexion of wire **20** within zone **34** may cause wire **22** to break. Therefore, in it is important that wire **20**, especially within recrystalization zone **34**, not be deformed to any significant degree during manufacturing. This is especially important in the manufacture of multi-chip packages. To reduce the loop height **32** and eliminate recrystalization zone **34** above bond pads **14**, a reverse wire bond **36**, shown in **FIG. 4**, may be used. Reverse wire bonds **36** typically have a loop height **32** of about 40-70 micrometers. Forward loop wire bonding, shown in **FIG. 5**, is often preferred over reverse wire bonding because it has a much larger throughput and the therefore a lower cost.

[0028] **FIG. 5** illustrates a partial cross sectional view of a multi-die semiconductor assembly **40** made according to the invention. Assembly **40** includes a lower, peripheral bonded die **42** and an upper die **44**. Assembly **40** protects against shorting of wires **20** against upper die **44** in two basic ways. First, upper die **44** has electrically insulating layer **45**, typically a dielectric film adhesive, such as available from Lintec Corporation as Lintec LE5000 or an Hitachi DF series film adhesive. Second, lower die **42**, also shown in **FIG. 6**, is secured to upper die **44** with an adhesive/spacer structure **46**. Structure **46** includes adhesive **48** and spacer elements **50**. Structure **46** may be a conventional material such as Loctite® QMI536-3, 4, or 6, which use nominal 3, 4 or 6 mil (75, 100 and 150 micrometers) diameter organic polymer spherical particles as spacer elements **50**; or a spacer adhesive from the Ablestik 2025 Sx series. It is preferred that spacer elements **50** be of an organic polymer material and pliable and large enough to permit forward loop wire bonding. Spacer elements **50** are typically about 30-250 micrometers in diameter. Structure **46** also helps to provide bond line thickness control and die tilt control. Prevention of the incursion of the adhesive/spacer material, and in particular spacers **50**, into wire span portion **60** of first, adhesive region **58** (refer to **FIG. 6**) may be achieved by, for example, depositing the adhesive/spacer material at selected positions and carefully controlling the amount deposited at each position. Examples of suitable materials for spacer elements **50** include PTFE and other organic polymers.

[0029] Spacer elements **50**, prior to use, are typically spherical, ellipsoidal, cylindrical with hemispherical or ellipsoidal ends, or the like. After assembly, assuming spacer elements **50** are compressible, spacer elements **50** are compressed to some degree and have flattened areas where they contact upper surface **52** of lower die **42** and the electrically non-conductive lower surface **54** of upper die **44**; the shape of such spacers is collectively referred to as generally ellipsoidal. For example, an initially spherical spacer element **50** having an 8 mil (200 micrometer) diameter will typically compress to a height of about 7.5 mil (188 micrometers). The height **56** of spacers **50**, which is equal to the distance between surface **52** and **54**, is preferably at least equal to loop height **32**, is more preferably greater than loop height **32**, is even more preferably at least about 10% greater than loop height **32**. If desired, the selection of the spacer elements include selecting spacer elements so that height **56** is equal to the design loop height **32** plus an allowance for manufacturing tolerance build-up resulting from making the wire bonds, the variance in the size and compressibility the of spacer elements **50** and other appropriate variables.

[0030] **FIG. 6** illustrates assembly **40** with upper die **44** indicated by dashed lines. Lower and upper die **42**, **44** define a first, adhesive region **58** therebetween. In the embodiment of **FIGS. 5 and 6**, region **58** is defined by the periphery of lower die **42** because upper die **44** extends beyond the entire periphery of the lower die. Wire span areas **24**, indicated by crosshatching, define wire span portions **60** of first, adhesive region **58**. The adhesive/spacer material is deposited in a manner so that, as shown in **FIG. 6**, adhesive/spacer structure **46** is located at other than wire span portions **60** of first, adhesive region **58**. Doing so helps to ensure that spacer elements **50** do not interfere with wires **20** thus eliminating the possibility of a spacer element causing one or more wires **22** to deflect to contact and thus short, for example, an adjacent wire **22**.

[0031] **FIG. 7** illustrates a multi-die semiconductor assembly **62** in which lower die **42** is a center bonded die such as shown in **FIG. 2** and upper die **44**, shown in dashed lines, is longer but narrower than lower die **42**. Therefore, in this embodiment first, adhesive region **58** does not cover the entire lower die **42** but rather is bounded by peripheral edges **17** and **19** of lower die **42** and peripheral edges **16** and **18** of upper die **44**. Adhesive/spacer structure **46** is, in the embodiment of **FIG. 6**, located within first, adhesive region **58** at other than wire span portions **60**. Adhesive/spacer structure **46** may define a single adhesive/spacer structure region as shown in **FIG. 6** or two or more adhesive/spacer structure regions, such as shown in **FIG. 7**.

[0032] Adhesive/spacer material may be deposited using a conventional dispenser capillary. However, it is preferred that the adhesive/spacer material be deposited using a showerhead type of dispenser as shown in the above-mentioned US Provisional Patent Application entitled Adhesive/Spacer Island Structure For Multiple Die Package. Doing so can facilitate the positioning of the adhesive/spacer material at spaced apart locations to provide the desired coverage by adhesive/spacer structure **46**. This may be especially advantageous when working with center bonded die.

[0033] **FIG. 8** is a side cross sectional view of multi-die semiconductor assembly **40** of **FIGS. 5 and 6** showing wires **20** extending from bond pads **14** of upper and lower die **44**, **42** to bond pads **22** of substrate **12**. **FIG. 9** illustrates the structure of **FIG. 8** after a molding compound **66** has been applied to create a multiple die semiconductor chip package **68**.

[0034] Spacer elements **50** may also be prevented from incursion into wire span portion **60** by sizing the spacer elements so as not to fit between the generally parallel wires **20**. In this way wires **20** act as a sieve or strainer to permit a portion **47** of adhesive **48** to enter into wire span portion **60** but prevent spacer elements **50** from doing so. This is illustrated in **FIG. 10**, showing adhesive/spacer structure **46** including adhesive **48**, with spacer elements **50** situated in regions other than the wire span portion of the adhesive region, and showing a portion **47** of adhesive **48** having entered into the wire span portion of the adhesive region. In such embodiments, the spacer elements provide a suitable distance between the two die, the lower surface of the upper die being electrically insulated by dielectric layer **45**, as

described above with reference to **FIG. 5**. The full occupancy of adhesive region **58** by adhesive **48**, particularly the portion **47** of the adhesive in the wire span region, eliminates the open overhang of the upper die above wires **20** shown in **FIG. 5**. This provides some support for the upper die, and helps to reduce or eliminate die breakage, which is especially useful for large and thin semiconductor devices.

[0035] The adhesive/spacer structure according to the invention can be useful for multi-die assembly structures in which the upper die **44** does not extend over the edge of the lower die **42**, as illustrated in **FIG. 11**, which is a view similar to the view of **FIG. 9**. Here, as in **FIG. 10**, spacer structure **46** including spacer elements **50** and adhesive **48** is formed between the upper die **44** with insulating layer **45**, and the lower die **42**. The wires **20** prevent the spacer elements from entering into the wire span region, but permit a portion **47** of the adhesive **48** to fill the volume there and provide support for the part of the upper **44** die that overhangs the wire loops **20**.

[0036] In other embodiments, a stacked semiconductor assembly includes a package stacked with a die, separated by an adhesive/spacer material generally as described above for stacked die assemblies. **FIGS. 12 and 13** illustrate examples **102**, **103** of such assemblies, in which an inverted package is stacked over a die. Referring to **FIG. 12**, a lower, peripheral bonded die **142** is mounted upon a substrate **112**, and bond pads on the die are electrically interconnected with bond pads on the substrate by wire bonds **120**. An adhesive/spacer structure **146** is formed upon the die **142** including an adhesive and spacer elements as described above with reference to adhesive/spacer structure **46**. An upper package **100** is inverted and mounted upon the adhesive/spacer structure **146**, in substantially the same manner as the upper die **44** is mounted upon adhesive/spacer structure **46** in the stacked die assembly **40**, for example, of **FIG. 8**.

[0037] The upper package **100** in this example is a land grid array package, having a die **242** mounted onto a die attach side on upper package substrate **112**. Die **242** in this example is wire bonded to substrate **112**, and the die and wire bonds are enclosed in an encapsulation **217**. The package **100** is inverted so that the land side of the substrate **212** faces away from the first die **142** and substrate **212**, and so that an upper surface of the encapsulation **217** faces toward the first die **142** and substrate **212**. In the orientation of **FIG. 12**, the land side of the inverted upper package **212** is upward-facing, and the upper package is electrically interconnected with the bottom substrate **212** by wire bonds between bond pads on the land side of the upper package substrate **212** and bond pads on the upward-facing side of the lower substrate **112**. The assembly is then encapsulated (not shown in **FIG. 12**) to form a package, substantially as the stacked die assembly **40** of **FIG. 8** is encapsulated to form the package **68** of **FIG. 9**. Solder balls **118** are mounted onto pads on the downward-facing side of the substrate **112**, for interconnection of the package to, for example, a motherboard. Multiple chip modules having inverted package stacked over a die, in which the adhesive/spacer structures described herein may be particularly suitable, are described in U.S. patent application Ser. No. 11/014,257.

[0038] In other embodiments, two (or more) die may be stacked using an adhesive/spacer structure over one another on a lower substrate, and a package may be stacked over the uppermost one of the stacked die, using an adhesive/spacer structure, as shown by way of example in **FIG. 13**. Here, a die **142** is mounted onto a lower substrate **112**, and a die **144** is stacked over the die **142**, and separated from it by an adhesive/spacer structure **246** as described above for stacked die assemblies. Die **142** and **144** are electrically interconnectedd with substrate **112** by wire bonds **220**. An inverted pachage **100** is mounted over the stacked die **142**, **144**, separated by the die **144** by and adhesive/spacer structure **246**, as described above with reference to **FIG. 12**. As will be appreciated, either or both of the spacers, between the die, and between the die and the inverted package, may be an adhesive/spacer structre as described above with referenbce to stacked die assemblies.

[0039] Any of a variety of packages may be stacked over the die in assemblies according to these embodiments of the invention. Stacked multi-package modules having inverted upper packages are described in U.S. patent application Ser. No. 10/681,572; and examples of suitable upper inverted package types are described therein. These include, for example, besides land grid array packages as illustrated in **FIGS. 12 and 13**, bump chip carrier packages; and the upper package may include more than one die. Where the upper package encapsulant has a generally planar surface that contacts the adhesive/spacer structure, that surface (termed the "second" surface) is itself electrically nonconductive, and application of an additional insulating layer (as layer **45** in **FIGS. 5, 8, 10** and **11**) may be optional in such embodiments. Where, however, the second surface of the upper package is an electrically conductive material (such as a metal heat spreader, for example) or includes exposed electrically conductive areas or elements, an insulating layer **45** should be applied, as described above with reference for example to **FIG. 5**.

[0040] In still other embodiments, in which a stacked semiconductor assembly includes a package stacked with a die, separated by an adhesive/spacer material generally as described above for stacked die assemblies, the upper package is not inverted. **FIGS. 14 and 15** illustrate examples **104**, **104** of such assemblies. Referring to **FIG. 14**, a lower, peripheral bonded die **142** is mounted upon a substrate **112**, and bond pads on the die are electrically interconnected with bond pads on the substrate by wire bonds **120**. An adhesive/spacer structure **146** is formed upon the die **142** including an adhesive and spacer elements as described above with reference to adhesive/spacer structure **46**. An upper package **400** is inverted and mounted upon the adhesive/spacer structure **146**, in substantially the same manner as the upper die **44** is mounted upon adhesive/spacer structure **46** in the stacked die assembly **40**, for example, of **FIG. 8**.

[0041] The upper package **400** in this example is a land grid array package, having a die **442** mounted onto a die attach side on upper package substrate **412**. Die **442** in this example is wire bonded to substrate **412**, and the die and wire bonds are enclosed in a mold cap **417**. Here the package **400** is oriented so that the land side of the substrate **412** faces toward the first die **142** and substrate **212**, and so that the land side of the upper package substrate **412** faces toward the first die **142** and substrate **212**. In the orientation of **FIG. 14**, the land side of the inverted upper package **412** is downward-facing, and the upper package is electrically interconnected with the bottom substrate **112** by wire bonds between bond pads on the upward-facing (die attach) side of

the upper package substrate **412** and bond pads on the upward-facing side of the lower substrate **112**. The assembly is then encapsulated (not shown in **FIG. 14**) to form a package, substantially as the stacked die assembly **40** of **FIG. 8** is encapsulated to form the package **68** of **FIG. 9**. Solder balls **118** are mounted onto pads on the downward-facing side of the substrate **112**, for interconnection of the package to, for example, a motherboard.

[**0042**] In other embodiments, two (or more) die may be stacked using an adhesive/spacer structure over one another on a lower substrate, and a package may be stacked over the uppermost one of the stacked die, using an adhesive/spacer structure, as shown by way of example in **FIG. 15**. Here, as in **FIG. 13**, a die **142** is mounted onto a lower substrate **112**, and a die **144** is stacked over the die **142**, and separated from it by an adhesive/spacer structure **246** as described above for stacked die assemblies. Die **142** and **144** are electrically interconnectedd with substrate **112** by wire bonds **220**. An inverted pachage **100** is mounted over the stacked die **142**, **144**, separated by the die **144** by and adhesive/spacer structure **246**, as described above with reference to **FIG. 14**. As will be appreciated, either or both of the spacers, between the die, and between the die and the inverted package, may be an adhesive/spacer structre as described above with referenbce to stacked die assemblies.

[**0043**] Any of a variety of packages may be stacked over the die in assemblies according to these embodiments of the invention. Stacked multi-package modules suitable upper packages are described in U.S. patent applications Ser. Nos. 10/632,549; 10/632,568; 10/632,551; 10/632,552; 10/632,553; and 10/632,550; and examples of suitable upper package types are described therein. These include, for example, besides land grid array packages as illustrated in **FIGS. 14 and 15**, bump chip carrier packages, and flip chip packages; and the upper package may include more than one die. Where the downward-facing surface of the upper package ("second" surface) had electrically conductive elements or areas, application of an additional insulating layer (as layer **45** in **FIGS. 5, 8, 10** and **11**) may be required and may be applied as described above with reference for example to **FIG. 5**, and as shown for example at **450** in **FIGS. 14 and 15**. This additional insulating layer may be applied as a film to the land side of the upper package substrate, and voids between the film and the substrate surface removed by heating at low pressure, according to techniques known in the art.

[**0044**] Other devices may be stacked over the first die, and separated therefrom by an adhesive/spacer structure as described above, and provided with an insulating layer as appropriate. For example, a metal heat spreader may be stacked upon an adhesive/spacer structure over the first die in place of the upper die or upper package in the descriptions above.

[**0045**] The assemblies and packages according to the invention can be useful in any of a variety of products, such as for example computers, mobile telecommunications devices, personal digital assistance devices, media storage devices, particularly portable cameras and audio and video equipment.

[**0046**] Any and all patents, patent applications and printed publications referred to above are incorporated by reference.

[**0047**] Other modification and variation can be made to the disclosed embodiments without departing from the subject of the invention as defined in following claims.

What is claimed is:

1. A multiple-die semiconductor chip package comprising:

a first die having a first surface bounded by a periphery and having bond pads at the first surface;

wires bonded to and extending from the bond pads outwardly past the periphery, the wires extending to a maximum height h above the first die;

a second die with an electrically non-conductive second surface positioned opposite the first surface;

the first and second die defining a first region therebetween;

an adhesive/spacer structure within the first region, the adhesive/spacer structure contacting the first and second surfaces and adhering the first and second die to one another at a chosen separation, the adhesive/spacer structure comprising spacer elements within an adhesive.

2. The package according to claim 1 wherein the wires comprise a plurality of sets of generally parallel wires, said plurality of sets of generally parallel wires defining a plurality of wire span portions of the first region.

3. The package according to claim 1 wherein the wires comprise a set of generally parallel wires, said set of generally parallel wires defining a wire span portion of the first region.

4. The package according to claim 3 wherein the adhesive/spacer structure is located at other than the wire span portion of the first region.

5. The package according to claim 4 wherein said adhesive is located at the wire span portion of the first region.

6. The package according to claim 5 wherein the spacer elements are sized so as not to fit between the generally parallel wires.

7. The package according to claim 3 wherein the spacer elements are located at other than the wire span portion of the first region.

8. The package according to claim 1 wherein the adhesive/spacer structure defines first and second spaced-apart adhesive/spacer structure regions.

9. The package according to claim 1 wherein the first die has a length and a width and a central region.

10. The package according to claim 9 wherein the first die comprises a center-bonded die with at least some of said die pads positioned at the central region.

11. The package according to claim 10 wherein at least one of the spacer elements is positioned within the central region.

12. The package according to claim 1 wherein the spacer elements have a height H with H being at least about equal to h.

13. The package according to claim 12 wherein H is greater than h.

14. The package according to claim 12 wherein H is at least about 10% greater than h.

15. The package according to claim 1 wherein the spacer elements are generally ellipsoidal.

16. The package according to claim 15 wherein the spacer elements are flattened spheres.

17. The package according to claim 15 wherein the spacer elements are about 30 μm-250 μm in diameter.

18. The package according to claim 1 wherein the spacer elements are all substantially the same size.

19. The package according to claim 1 wherein the spacer elements comprise an organic and pliable solid material.

20. The package according to claim 1 wherein the spacer elements comprise at least PTFE.

21. A method for adhering first and second die to one another at a chosen separation in a multiple-die semiconductor chip package, the method comprising:

selecting an adhesive/spacer material having spacer elements within an adhesive;

depositing the adhesive/spacer material onto a first surface of a first die, the first die having a first surface bounded by a periphery, bond pads at the first surface, and wires bonded to and extending from the bond pads outwardly past the periphery, the wires extending to a maximum height h above the first die, the wires comprising a set of generally parallel wires, the set of generally parallel wires defining a wire span portion of the first surface;

selecting a second die having an electrically non-conductive second surface;

locating the second surface of the second die opposite the first surface of the first die and in contact with the adhesive/spacer material therebetween thereby securing the first and second die to one another at a chosen separation, the wire span portion of the first surface defining a wire span region between the first and second surfaces; and

preventing any spacer elements from entering the wire span region.

22. The method according to claim 21 further comprising preventing any adhesive/spacer material from entering the wire span region.

23. The method according to claim 21 wherein the preventing step comprises using spacer elements sized so as not to fit between the generally parallel wires.

24. The method according to claim 21 wherein the depositing step is carried out a manner to prevent any adhesive/spacer material from entering the wire span region.

25. The method according to claim 21 wherein the selecting step is carried out to select spacer elements having the same size and shape.

26. The method according to claim 21 wherein the depositing step is carried out with the first die having a length and a width and a central region.

27. The method according to claim 26 wherein the depositing step is carried out with the first die comprising a center-bonded die with at least some of said die pads positioned at the central region.

28. The method according to claim 27 wherein depositing step comprises positioning at least some of the adhesive/spacer material within the central region so that at least one spacer element is positioned within the central region.

29. The method according to claim 21 wherein the adhesive/spacer material selecting step comprises selecting spacer elements having a height H with H being at least about equal to h.

30. The method according to claim 29 wherein the spacer elements selecting step comprises selecting spacer elements in which H is greater than h.

31. The method according to claim 29 wherein the spacer elements selecting step comprises determining an allowance for manufacturing tolerance buildup and selecting spacer elements so that H is equal to h plus the allowance for the manufacturing tolerance buildup.

32. The method according to claim 29 wherein the spacer elements selecting step comprises determining an allowance for manufacturing tolerance buildup and selecting spacer elements so that H is greater than h plus the allowance for the manufacturing tolerance buildup.

33. The method according to claim 29 wherein the spacer elements selecting step comprises selecting spacer elements so that H is at least about 10% greater than h.

34. A stacked semiconductor assembly comprising:

a first die having a first surface bounded by a periphery and having bond pads at the first surface;

wires bonded to and extending from the bond pads outwardly past the periphery, the wires extending to a maximum height h above the first die;

a package, comprising a package die mounted to and electrically interconnected with a package substrate, the package having an electrically non-conductive second surface positioned opposite the first surface;

the first die and the package defining a first region therebetween;

an adhesive/spacer structure within the first region, the adhesive/spacer structure contacting the first and second surfaces and adhering the first die and the package to one another at a chosen separation, the adhesive/spacer structure comprising spacer elements within an adhesive.

35. The stacked semiconductor assembly of claim 34 wherein the upper package is oriented so that the die attach side of the upper package substrate faces the first die.

36. The stacked semiconductor assembly of claim 34 wherein the upper package is oriented so that side of the upper package substrate opposite the die attach side faces the first die.

37. Stacked semiconductor packages comprising the assembly of claim 34.

38. A method for adhering a die and a package to one another at a chosen separation in a stacked semiconductor package, the method comprising:

Selecting an adhesive/spacer material having spacer elements within an adhesive;

depositing the adhesive/spacer material onto a first surface of a first die, the first die having a first surface bounded by a periphery, bond pads at the first surface, and wires bonded to and extending from the bond pads

outwardly past the periphery, the wires extending to a maximum height h above the first die, the wires comprising a set of generally parallel wires, the set of generally parallel wires defining a wire span portion of the first surface;

Selecting a package having an electrically non-conductive second surface;

locating the second surface of the package opposite the first surface of the first die and in contact with the adhesive/spacer material there between thereby securing the package and the first die to one another at a chosen separation, the wire span portion of the first surface defining a wire span region between the first and second surfaces; and

Preventing any spacer elements from entering the wire span region.

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