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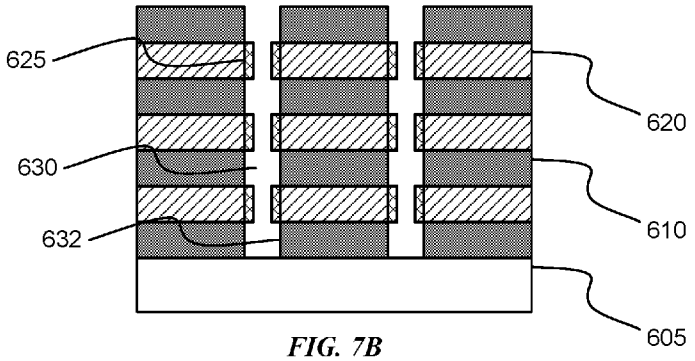

FIG. 7B

(57) Abstract: Processing methods may be performed to form semiconductor structures that may include three-dimensional memory structures. The methods may include forming a plasma of a fluorine-containing precursor in a remote plasma region of a processing chamber. The methods may include contacting a semiconductor substrate with effluents of the plasma. The semiconductor substrate may be housed in a processing region of the processing chamber. The methods may include selectively etching a metal material laterally between exposed regions of a dielectric material on the semiconductor substrate. The methods may also include subsequently depositing a cap material over the metal material. The cap material may be selectively deposited on the metal material relative to exposed regions of the dielectric material.

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STRUCTURE WITH SELECTIVE BARRIER LAYER

RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application No. 62/487,728, filed April 20, 2017, the disclosure of which is hereby incorporated by reference in its entirety for all purposes.

TECHNICAL FIELD

[0002] The present technology relates to semiconductor systems, processes, and equipment. More specifically, the present technology relates to systems and methods for selectively etching and selectively depositing material layers on a semiconductor device.

BACKGROUND

[0003] Integrated circuits are made possible by processes which produce intricately patterned material layers on substrate surfaces. Producing patterned material on a substrate requires controlled methods for removal of exposed material. Chemical etching is used for a variety of purposes including transferring a pattern in photoresist into underlying layers, thinning layers, or thinning lateral dimensions of features already present on the surface. Often it is desirable to have an etch process that etches one material faster than another facilitating, for example, a pattern transfer process or individual material removal. Such an etch process is said to be selective to the first material. As a result of the diversity of materials, circuits, and processes, etch processes have been developed with a selectivity towards a variety of materials. Deposition processes, however, continue to be performed across substrates generally utilizing a blanket coat or a conformal fill.

[0004] As device sizes continue to shrink in next-generation devices, selectivity may play a larger role when only a few nanometers of material are formed in a particular layer, especially when the material is critical in the transistor formation. Many different etch process selectivities have been developed between various materials, although standard selectivities may no longer be suitable at current and future device scale. Additionally, queue times for processes continue to

rise based on the number of masking, formation, and removal operations needed to form and protect the various critical dimensions of features across a device while patterning and formation are performed elsewhere on a substrate.

[0005] Thus, there is a need for improved systems and methods that can be used to produce high quality devices and structures. These and other needs are addressed by the present technology.

SUMMARY

[0006] Processing methods may be performed to form semiconductor structures that may include three-dimensional memory structures. The methods may include forming a plasma of a fluorine-containing precursor in a remote plasma region of a processing chamber. The methods may include contacting a semiconductor substrate with effluents of the plasma. The semiconductor substrate may be housed in a processing region of the processing chamber. The methods may include selectively etching a metal material laterally between exposed regions of a dielectric material on the semiconductor substrate. The methods may also include subsequently depositing a cap material over the metal material. The cap material may be selectively deposited on the metal material relative to exposed regions of the dielectric material.

[0007] In some embodiments, the etching may be performed in a first processing chamber, and the depositing may be performed in a second processing chamber. The methods may also include transferring the semiconductor substrate from the first processing chamber to the second processing chamber, and the transferring may be performed without breaking vacuum. The metal material may include tungsten or cobalt. The dielectric material may include silicon oxide. The cap material may include a metal nitride or a metal oxide. The metal material may be laterally etched less than 10 nm from the sidewalls of the trench. The etching may be performed with a selectivity towards the metal material relative to the dielectric material greater than or about 10:1. The deposition may be performed with a selectivity towards the metal material relative to the dielectric material greater than or about 2:1. Additionally, in some embodiments selectively depositing the cap material may include inhibiting growth of the cap material on the dielectric material.

[0008] The present technology also encompasses methods of forming a semiconductor structure. The methods may include forming a plasma of a fluorine-containing precursor in a

remote plasma region of a processing chamber. The methods may include contacting a semiconductor substrate with effluents of the plasma. The semiconductor substrate may be housed in a processing region of the processing chamber. The methods may include selectively etching layers of a metal material laterally between exposed layers of a dielectric material on the semiconductor substrate. The methods may also include subsequently depositing a cap material over the metal material. The cap material may be selectively deposited on the metal material relative to exposed regions of the dielectric material.

[0009] In some embodiments, the layers of silicon nitride may be laterally etched less than 10 nm from the sidewalls of the trench. The dielectric material may be or include silicon oxide. The cap material may be or include a metal nitride or a metal oxide. The metal nitride may be or include titanium nitride. The etching may be performed in a first processing chamber, and the depositing may be performed in a second processing chamber. The methods may also include transferring the semiconductor substrate from the first processing chamber to the second processing chamber, and the transferring may be performed without breaking vacuum. The semiconductor substrate may define multiple trenches, and the metal material may be etched on multiple surfaces. The etching may be performed with a selectivity towards the metal material relative to the dielectric material greater than or about 10:1. The deposition may be performed with a selectivity towards the metal material relative to the dielectric material greater than or about 2:1.

[0010] Such technology may provide numerous benefits over conventional systems and techniques. For example, the processes may enable smaller devices due to improved structures. Additionally, by performing selective operations, fewer masking and removal operations may be performed, which may reduce fabrication queue times dramatically, and allow otherwise difficult structures to be formed. These and other embodiments, along with many of their advantages and features, are described in more detail in conjunction with the below description and attached figures.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] A further understanding of the nature and advantages of the disclosed technology may be realized by reference to the remaining portions of the specification and the drawings.

[0012] FIG. 1 shows a top plan view of an exemplary processing system according to embodiments of the present technology.

[0013] FIG. 2A shows a schematic cross-sectional view of an exemplary processing chamber according to embodiments of the present technology.

[0014] FIG. 2B shows a detailed view of an exemplary showerhead according to embodiments of the present technology.

[0015] FIG. 3 shows a bottom plan view of an exemplary showerhead according to embodiments of the present technology.

[0016] FIG. 4 shows a schematic cross-sectional view of an exemplary processing chamber according to embodiments of the present technology.

[0017] FIG. 5 shows selected operations in a method of forming a semiconductor structure according to embodiments of the present technology.

[0018] FIGS. 6A-6C show schematic cross-sectional views of exemplary substrates according to embodiments of the present technology.

[0019] FIGS. 7A-7B show schematic cross-sectional views of exemplary substrates according to embodiments of the present technology.

[0020] Several of the figures are included as schematics. It is to be understood that the figures are for illustrative purposes, and are not to be considered of scale unless specifically stated to be of scale. Additionally, as schematics, the figures are provided to aid comprehension and may not include all aspects or information compared to realistic representations, and may include exaggerated material for illustrative purposes.

[0021] In the appended figures, similar components and/or features may have the same reference label. Further, various components of the same type may be distinguished by following the reference label by a letter that distinguishes among the similar components. If only the first reference label is used in the specification, the description is applicable to any one of the similar components having the same first reference label irrespective of the letter.

DETAILED DESCRIPTION

[0022] The present technology includes systems and components for semiconductor processing of small pitch features. In transitioning from 2D NAND to 3D NAND, many process operations are modified from vertical to horizontal operations, so as to laterally etch and form material layers. Additionally, as 3D NAND structures grow in the number of cells being formed, the aspect ratios of memory holes and other structures increase, sometimes dramatically. In conventional 3D NAND processing, stacks of placeholder layers and dielectric materials may form the inter-electrode dielectric or IPD layers. These placeholder layers may have a variety of operations performed to place structures before fully removing the placeholder material and replacing it with metal. As devices continue to shrink in size, the placeholder layers may increase in aspect ratios as far as a width versus a depth. Accordingly, when the material is removed and replaced with metal, a complete fill may be more difficult. Moreover, seams may be formed within the metal layers, which may affect device performance or may damage the device.

[0023] Many conventional technologies utilize a wet etch to access each of the cell placeholder materials to perform a lateral etch of placeholders before incorporating metal. Dry etches may not be feasible in conventional technology because of the high aspect ratios of the memory holes, which may not allow symmetrical etching to be performed. However, wet etching may be more robust than other etching techniques, and the wet etching may etch materials in addition to the placeholder materials causing damage within the structure, which may weaken the structures causing deformation. The subsequent metallization may be incomplete or produce seams or voids within the layers of the structure. The resultant memory cell may have reduced capacity or may fail. Additionally, conventional technologies have been incapable of converting to an initial metal structure due to issues with core oxide fill operations, and adhesion issues with other materials.

[0024] The present technology overcomes these issues by forming a structure obviating the conventional placeholder removal operations. Where conventional cells utilizing oxide and nitride materials, known as ONON, the present technology may not include replacement materials, and may form the metallization directly. These new structures, which may be considered oxide and metal structures, or OMOM, may overcome the need for extracting

placeholder materials and depositing metal. By forming an initial structure including the metallization, the issues described may be avoided. The present technologies allow these structures to be formed by utilizing a selectively deposited barrier layer to separate nodes, and increase adhesion capabilities of subsequently deposited materials, such as oxides and other core materials. By selectively depositing the barrier layer, complete node separation can be performed without etch back processes that may extend further within the metal layers.

[0025] Although the remaining disclosure will routinely identify specific etching and deposition processes utilizing the disclosed technology, it will be readily understood that the systems and methods are equally applicable to a variety of other etching, deposition, and cleaning processes as may occur in the described chambers. Accordingly, the technology should not be considered to be so limited as for use with the described etching and deposition processes alone. The disclosure will discuss one possible system and chambers that can be used with the present technology to perform certain of the removal and deposition operations before describing operations of an exemplary process sequence according to the present technology.

[0026] **FIG. 1** shows a top plan view of one embodiment of a processing system 100 of deposition, etching, baking, and curing chambers according to embodiments. In the figure, a pair of front opening unified pods (FOUPs) 102 supply substrates of a variety of sizes that are received by robotic arms 104 and placed into a low pressure holding area 106 before being placed into one of the substrate processing chambers 108a-f, positioned in tandem sections 109a-c. A second robotic arm 110 may be used to transport the substrate wafers from the holding area 106 to the substrate processing chambers 108a-f and back. Each substrate processing chamber 108a-f, can be outfitted to perform a number of substrate processing operations including the dry etch processes and selective deposition described herein in addition to cyclical layer deposition (CLD), atomic layer deposition (ALD), chemical vapor deposition (CVD), physical vapor deposition (PVD), wet etch, pre-clean, degas, orientation, and other substrate processes.

[0027] The substrate processing chambers 108a-f may include one or more system components for depositing, annealing, curing and/or etching a dielectric film on the substrate wafer. In one configuration, two pairs of the processing chambers, e.g., 108c-d and 108e-f, may be used to deposit dielectric material or metal-containing material on the substrate, and the third pair of processing chambers, e.g., 108a-b, may be used to etch the deposited dielectric. In another

configuration, all three pairs of chambers, e.g., 108a-f, may be configured to etch a dielectric film on the substrate. Any one or more of the processes described may be carried out in chamber(s) separated from the fabrication system shown in different embodiments.

[0028] In some embodiments the chambers specifically include at least one etching chamber as described below as well as at least one deposition chamber as described below. By including these chambers in combination on the processing side of the factory interface, all etching and deposition processes discussed below may be performed in a controlled environment. For example, a vacuum environment may be maintained on the processing side of holding area 106, so that all chambers and transfers are maintained under vacuum in embodiments. This may also limit water vapor and other air components from contacting the substrates being processed. It will be appreciated that additional configurations of deposition, etching, annealing, and curing chambers for dielectric films are contemplated by system 100.

[0029] **FIG. 2A** shows a cross-sectional view of an exemplary process chamber system 200 with partitioned plasma generation regions within the processing chamber. During film etching, e.g., titanium nitride, tantalum nitride, tungsten, cobalt, aluminum oxide, tungsten oxide, silicon, polysilicon, silicon oxide, silicon nitride, silicon oxynitride, silicon oxycarbide, etc., a process gas may be flowed into the first plasma region 215 through a gas inlet assembly 205. A remote plasma system (RPS) 201 may optionally be included in the system, and may process a first gas which then travels through gas inlet assembly 205. The inlet assembly 205 may include two or more distinct gas supply channels where the second channel (not shown) may bypass the RPS 201, if included.

[0030] A cooling plate 203, faceplate 217, ion suppressor 223, showerhead 225, and a substrate support 265, having a substrate 255 disposed thereon, are shown and may each be included according to embodiments. The pedestal 265 may have a heat exchange channel through which a heat exchange fluid flows to control the temperature of the substrate, which may be operated to heat and/or cool the substrate or wafer during processing operations. The wafer support platter of the pedestal 265, which may comprise aluminum, ceramic, or a combination thereof, may also be resistively heated in order to achieve relatively high temperatures, such as from up to or about 100°C to above or about 1100°C, using an embedded resistive heater element.

[0031] The faceplate 217 may be pyramidal, conical, or of another similar structure with a narrow top portion expanding to a wide bottom portion. The faceplate 217 may additionally be flat as shown and include a plurality of through-channels used to distribute process gases. Plasma generating gases and/or plasma excited species, depending on use of the RPS 201, may pass through a plurality of holes, shown in FIG. 2B, in faceplate 217 for a more uniform delivery into the first plasma region 215.

[0032] Exemplary configurations may include having the gas inlet assembly 205 open into a gas supply region 258 partitioned from the first plasma region 215 by faceplate 217 so that the gases/species flow through the holes in the faceplate 217 into the first plasma region 215. Structural and operational features may be selected to prevent significant backflow of plasma from the first plasma region 215 back into the supply region 258, gas inlet assembly 205, and fluid supply system 210. The faceplate 217, or a conductive top portion of the chamber, and showerhead 225 are shown with an insulating ring 220 located between the features, which allows an AC potential to be applied to the faceplate 217 relative to showerhead 225 and/or ion suppressor 223. The insulating ring 220 may be positioned between the faceplate 217 and the showerhead 225 and/or ion suppressor 223 enabling a capacitively coupled plasma (CCP) to be formed in the first plasma region. A baffle (not shown) may additionally be located in the first plasma region 215, or otherwise coupled with gas inlet assembly 205, to affect the flow of fluid into the region through gas inlet assembly 205.

[0033] The ion suppressor 223 may comprise a plate or other geometry that defines a plurality of apertures throughout the structure that are configured to suppress the migration of ionically-charged species out of the first plasma region 215 while allowing uncharged neutral or radical species to pass through the ion suppressor 223 into an activated gas delivery region between the suppressor and the showerhead. In embodiments, the ion suppressor 223 may comprise a perforated plate with a variety of aperture configurations. These uncharged species may include highly reactive species that are transported with less reactive carrier gas through the apertures. As noted above, the migration of ionic species through the holes may be reduced, and in some instances completely suppressed. Controlling the amount of ionic species passing through the ion suppressor 223 may advantageously provide increased control over the gas mixture brought into contact with the underlying wafer substrate, which in turn may increase control of the

deposition and/or etch characteristics of the gas mixture. For example, adjustments in the ion concentration of the gas mixture can significantly alter its etch selectivity, e.g., SiNx:SiOx etch ratios, Si:SiOx etch ratios, etc. In alternative embodiments in which deposition is performed, it can also shift the balance of conformal-to-flowable style depositions for dielectric materials.

[0034] The plurality of apertures in the ion suppressor 223 may be configured to control the passage of the activated gas, i.e., the ionic, radical, and/or neutral species, through the ion suppressor 223. For example, the aspect ratio of the holes, or the hole diameter to length, and/or the geometry of the holes may be controlled so that the flow of ionically-charged species in the activated gas passing through the ion suppressor 223 is reduced. The holes in the ion suppressor 223 may include a tapered portion that faces the plasma excitation region 215, and a cylindrical portion that faces the showerhead 225. The cylindrical portion may be shaped and dimensioned to control the flow of ionic species passing to the showerhead 225. An adjustable electrical bias may also be applied to the ion suppressor 223 as an additional means to control the flow of ionic species through the suppressor.

[0035] The ion suppressor 223 may function to reduce or eliminate the amount of ionically charged species traveling from the plasma generation region to the substrate. Uncharged neutral and radical species may still pass through the openings in the ion suppressor to react with the substrate. It should be noted that the complete elimination of ionically charged species in the reaction region surrounding the substrate may not be performed in embodiments. In certain instances, ionic species are intended to reach the substrate in order to perform the etch and/or deposition process. In these instances, the ion suppressor may help to control the concentration of ionic species in the reaction region at a level that assists the process.

[0036] Showerhead 225 in combination with ion suppressor 223 may allow a plasma present in first plasma region 215 to avoid directly exciting gases in substrate processing region 233, while still allowing excited species to travel from chamber plasma region 215 into substrate processing region 233. In this way, the chamber may be configured to prevent the plasma from contacting a substrate 255 being etched. This may advantageously protect a variety of intricate structures and films patterned on the substrate, which may be damaged, dislocated, or otherwise warped if directly contacted by a generated plasma. Additionally, when plasma is allowed to contact the substrate or approach the substrate level, the rate at which oxide species etch may increase.

Accordingly, if an exposed region of material is oxide, this material may be further protected by maintaining the plasma remotely from the substrate.

[0037] The processing system may further include a power supply 240 electrically coupled with the processing chamber to provide electric power to the faceplate 217, ion suppressor 223, showerhead 225, and/or pedestal 265 to generate a plasma in the first plasma region 215 or processing region 233. The power supply may be configured to deliver an adjustable amount of power to the chamber depending on the process performed. Such a configuration may allow for a tunable plasma to be used in the processes being performed. Unlike a remote plasma unit, which is often presented with on or off functionality, a tunable plasma may be configured to deliver a specific amount of power to the plasma region 215. This in turn may allow development of particular plasma characteristics such that precursors may be dissociated in specific ways to enhance the etching profiles produced by these precursors.

[0038] A plasma may be ignited either in chamber plasma region 215 above showerhead 225 or substrate processing region 233 below showerhead 225. In embodiments, the plasma formed in substrate processing region 233 may be a DC biased plasma formed with the pedestal acting as an electrode. Plasma may be present in chamber plasma region 215 to produce the radical precursors from an inflow of, for example, a fluorine-containing precursor or other precursor. An AC voltage typically in the radio frequency (RF) range may be applied between the conductive top portion of the processing chamber, such as faceplate 217, and showerhead 225 and/or ion suppressor 223 to ignite a plasma in chamber plasma region 215 during deposition. An RF power supply may generate a high RF frequency of 13.56 MHz but may also generate other frequencies alone or in combination with the 13.56 MHz frequency.

[0039] **FIG. 2B** shows a detailed view 253 of the features affecting the processing gas distribution through faceplate 217. As shown in FIGS. 2A and 2B, faceplate 217, cooling plate 203, and gas inlet assembly 205 intersect to define a gas supply region 258 into which process gases may be delivered from gas inlet 205. The gases may fill the gas supply region 258 and flow to first plasma region 215 through apertures 259 in faceplate 217. The apertures 259 may be configured to direct flow in a substantially unidirectional manner such that process gases may flow into processing region 233, but may be partially or fully prevented from backflow into the gas supply region 258 after traversing the faceplate 217.

[0040] The gas distribution assemblies such as showerhead 225 for use in the processing chamber section 200 may be referred to as dual channel showerheads (DCSH) and are additionally detailed in the embodiments described in FIG. 3. The dual channel showerhead may provide for etching processes that allow for separation of etchants outside of the processing region 233 to provide limited interaction with chamber components and each other prior to being delivered into the processing region.

[0041] The showerhead 225 may comprise an upper plate 214 and a lower plate 216. The plates may be coupled with one another to define a volume 218 between the plates. The coupling of the plates may be so as to provide first fluid channels 219 through the upper and lower plates, and second fluid channels 221 through the lower plate 216. The formed channels may be configured to provide fluid access from the volume 218 through the lower plate 216 via second fluid channels 221 alone, and the first fluid channels 219 may be fluidly isolated from the volume 218 between the plates and the second fluid channels 221. The volume 218 may be fluidly accessible through a side of the gas distribution assembly 225.

[0042] **FIG. 3** is a bottom view of a showerhead 325 for use with a processing chamber according to embodiments. Showerhead 325 may correspond with the showerhead 225 shown in FIG. 2A. Through-holes 365, which show a view of first fluid channels 219, may have a plurality of shapes and configurations in order to control and affect the flow of precursors through the showerhead 225. Small holes 375, which show a view of second fluid channels 221, may be distributed substantially evenly over the surface of the showerhead, even amongst the through-holes 365, and may help to provide more even mixing of the precursors as they exit the showerhead than other configurations.

[0043] Turning to **FIG. 4** is shown a schematic cross-sectional view of an atomic layer deposition system 400 or reactor in accordance with one or more embodiments of the present technology. The system 400 may include a load lock chamber 10 and a processing chamber 20. The processing chamber 20 may be generally a sealable enclosure, which may be operated under vacuum, or at least low pressure. The processing chamber 20 may be isolated from the load lock chamber 10 by an isolation valve 15. The isolation valve 15 may seal the processing chamber 20 from the load lock chamber 10 in a closed position and may allow a substrate 60 to be transferred

from the load lock chamber 10 through the valve to the processing chamber 20 and vice versa in an open position.

[0044] The system 400 may include a gas distribution plate 30 capable of distributing one or more gases across a substrate 60. The gas distribution plate 30 may be any suitable distribution plate known to those skilled in the art, and specific gas distribution plates described should not be taken as limiting the scope of the technology. The output face of the gas distribution plate 30 may face the first surface 61 of the substrate 60.

[0045] The gas distribution plate 30 may include a plurality of gas ports configured to transmit one or more gas streams to the substrate 60 and a plurality of vacuum ports disposed between each gas port and configured to transmit the gas streams out of the processing chamber 20. As illustrated in FIG. 4, the gas distribution plate 30 may include a first precursor injector 420, a second precursor injector 430 and a purge gas injector 440. The injectors 420, 430, 440 may be controlled by a system computer (not shown), such as a mainframe, or by a chamber-specific controller, such as a programmable logic controller. The precursor injector 420 may be configured to inject a continuous or pulse stream of a reactive precursor of compound A into the processing chamber 20 through a plurality of gas ports 425. The precursor injector 430 may be configured to inject a continuous or pulse stream of a reactive precursor of compound B into the processing chamber 20 through a plurality of gas ports 435. The purge gas injector 440 may be configured to inject a continuous or pulse stream of a non-reactive or purge gas into the processing chamber 20 through a plurality of gas ports 445. The purge gas may be configured to remove reactive material and reactive by-products from the processing chamber 20. The purge gas may typically be an inert gas, such as nitrogen, argon or helium. Gas ports 445 may be disposed in between gas ports 425 and gas ports 435 so as to separate the precursor of compound A from the precursor of compound B, thereby avoiding cross-contamination between the precursors.

[0046] In another aspect, a remote plasma source (not shown) may be connected to the precursor injector 420 and the precursor injector 430 prior to injecting the precursors into the processing chamber 20. The plasma of reactive species may be generated by applying an electric field to a compound within the remote plasma source. Any power source that is capable of activating the intended compounds may be used. For example, power sources using DC, radio

frequency, and microwave based discharge techniques may be used. If an RF power source is used, it can be either capacitively or inductively coupled. The activation may also be generated by a thermally based technique, a gas breakdown technique, a high intensity light source, such as ultraviolet light, or exposure to an x-ray source.

[0047] The system 400 may further include a pumping system 450 connected to the processing chamber 20. The pumping system 450 may be generally configured to evacuate the gas streams out of the processing chamber 20 through one or more vacuum ports 455. The vacuum ports 455 may be disposed between each gas port so as to evacuate the gas streams out of the processing chamber 20 after the gas streams react with the substrate surface and to further limit cross-contamination between the precursors.

[0048] The system 400 may include a plurality of partitions 460 disposed on the processing chamber 20 between each port. A lower portion of each partition may extend close to the first surface 61 of substrate 60, such as, for example, about 0.5 mm or greater from the first surface 61. In this manner, the lower portions of the partitions 460 may be separated from the substrate surface by a distance sufficient to allow the gas streams to flow around the lower portions toward the vacuum ports 455 after the gas streams react with the substrate surface. Arrows 498 indicate the direction of the gas streams. Since the partitions 460 may operate as a physical barrier to the gas streams, they may also limit cross contamination between the precursors. The arrangement shown is merely illustrative and should not be taken as limiting the scope of the technology. It will be understood by those skilled in the art that the gas distribution system shown is merely one possible distribution system and that other types of showerheads may be employed.

[0049] In operation, a substrate 60 may be delivered, such as by a robot, to the load lock chamber 10 and may be placed on a shuttle 65. After the isolation valve 15 is opened, the shuttle 65 may be moved along the track 70. Once the shuttle 65 enters in the processing chamber 20, the isolation valve 15 may close, sealing the processing chamber 20. The shuttle 65 may then be moved through the processing chamber 20 for processing. In one embodiment, the shuttle 65 may be moved in a linear path through the chamber.

[0050] As the substrate 60 moves through the processing chamber 20, the first surface 61 of substrate 60 may be repeatedly exposed to the precursor of compound A coming from gas ports 425 and the precursor of compound B coming from gas ports 435, with the purge gas coming

from gas ports 445 in between. Injection of the purge gas may be designed to remove unreacted material from the previous precursor prior to exposing the substrate surface 61 to the next precursor. After each exposure to the various gas streams, the gas streams may be evacuated through the vacuum ports 455 by the pumping system 450. Since a vacuum port may be disposed on both sides of each gas port, the gas streams may be evacuated through the vacuum ports 455 on both sides. Thus, the gas streams may flow from the respective gas ports vertically downward toward the first surface 61 of the substrate 60, across the first surface 410 and around the lower portions of the partitions 460, and finally upward toward the vacuum ports 455. In this manner, each gas may be uniformly distributed across the substrate surface 61. Substrate 60 may also be rotated while being exposed to the various gas streams. Rotation of the substrate may be useful in preventing the formation of strips in the formed layers. Rotation of the substrate may be continuous or in discreet steps.

[0051] The extent to which the substrate surface 61 is exposed to each gas may be determined by, for example, the flow rates of each gas coming out of the gas port and the rate of movement of the substrate 60. In one embodiment, the flow rates of each gas may be configured so as not to remove adsorbed precursors from the substrate surface 61. The width between each partition, the number of gas ports disposed on the processing chamber 20, and the number of times the substrate may be passed back and forth may also determine the extent to which the substrate surface 61 is exposed to the various gases. Consequently, the quantity and quality of a deposited film may be optimized by varying the above-referenced factors.

[0052] In another embodiment, the system 400 may include a precursor injector 420 and a precursor injector 430, without a purge gas injector 440. Consequently, as the substrate 60 moves through the processing chamber 20, the substrate surface 61 may be alternately exposed to the precursor of compound A and the precursor of compound B, without being exposed to purge gas in between.

[0053] The embodiment shown in FIG. 4 has the gas distribution plate 30 above the substrate. While the embodiments have been described and shown with respect to this upright orientation, it will be understood that the inverted orientation is also possible. In that situation, the first surface 61 of the substrate 60 may face downward, while the gas flows toward the substrate may

be directed upward. In one or more embodiments, at least one radiant heat source 90 may be positioned to heat the second side of the substrate.

[0054] In some embodiments, the shuttle 65 may be susceptor 66 for carrying the substrate 60. Generally, the susceptor 66 may be a carrier which helps to form a uniform temperature across the substrate. The susceptor 66 may be movable in both directions left-to-right and right-to-left, relative to the arrangement of FIG. 4, between the load lock chamber 10 and the processing chamber 20. The susceptor 66 may have a top surface 67 for carrying the substrate 60. The susceptor 66 may be a heated susceptor so that the substrate 60 may be heated for processing. As an example, the susceptor 66 may be heated by radiant heat source 90, a heating plate, resistive coils, or other heating devices, disposed underneath the susceptor 66. Although illustrated as a lateral transition, embodiments of system 400 may also be utilized in a rotationally based system in which a wheel may rotate clockwise or counter-clockwise to successively treat one or more substrates positioned under the gas distribution system illustrated. Additional modifications are similarly understood to be encompassed by the present technology.

[0055] **FIG. 5** illustrates a method 500 of forming a semiconductor structure, many operations of which may be performed, for example, in the chamber 200 and 400 as previously described. Method 500 may include one or more operations prior to the initiation of the method, including front end processing, deposition, etching, polishing, cleaning, or any other operations that may be performed prior to the described operations. The method may include a number of optional operations as denoted in the figure, which may or may not be specifically associated with the method according to the present technology. For example, many of the operations are described in order to provide a broader scope of the structural formation, but are not critical to the technology, or may be performed by alternative methodology as will be discussed further below. Method 500 describes the operations shown schematically in **FIGS. 6A-6C**, the illustrations of which will be described in conjunction with the operations of method 500. It is to be understood that FIG. 6 illustrates only partial schematic views, and a substrate may contain any number of transistor sections having aspects as illustrated in the figures.

[0056] Method 500 may involve operations performed on a substrate having multiple exposed regions, such as on a substrate including regions to be further developed in producing a 3D NAND structure. As illustrated in FIG. 6A, a portion of a processed structure 600 is shown

including a substrate 605, which may have a plurality of stacked layers overlying the substrate, which may be silicon, silicon germanium, or other substrate materials. The layers may include layers for producing memory nodes including dielectric material 610, which may be an oxide, such as silicon oxide, in alternating layers with a metal material 620, which may be tungsten, cobalt, or other low resistivity metals. Although illustrated with only 7 layers of material, exemplary structures may include any number of layers, such as up to or greater than about 10, greater than or about 15, greater than or about 20, greater than or about 25, greater than or about 30, greater than or about 35, greater than or about 40, greater than or about 45, greater than or about 50, greater than or about 55 , greater than or about 60, greater than or about 65, greater than or about 70, greater than or about 80, greater than or about 90, greater than or about a hundred, or more layers of materials.

[0057] Trenches 630, which may be memory holes, may be defined through the stacked structure to the level of substrate 605. Trenches 630 may be defined by sidewalls 632 that may be composed of the alternating layers of dielectric material 610 and metal material 620. Although the remaining disclosure will discuss tungsten and silicon oxide, any other known materials having similar operational characteristics may be substituted for one or more of the layers. Some or all of these operations may be performed in chambers or system tools as previously described, or may be performed in different chambers on the same system tool, which may include the chamber in which the operations of method 400 are performed.

[0058] Method 500 may initially include recessing metal material 620 as illustrated in FIG. 6B. The metal material 620 may be recessed in an etching chamber similar to chamber 200 previously described. In some embodiments wet etching or other dry etching may be performed. However, the following describes one possible treatment to remove the tungsten or metal material laterally from within the memory hole. Once positioned within a processing region of the semiconductor processing chamber, the method may include forming a plasma of a fluorine-containing precursor in a remote plasma region of the processing chamber at operation 505. The remote plasma region may be fluidly coupled with the processing region, although it may be physically partitioned to limit plasma at the substrate level, which may damage exposed structures or materials.

[0059] Effluents of the plasma may be flowed into the processing region, where they may contact the semiconductor substrate at operation 510. At operation 515, the metal material may be selectively etched laterally with respect to the exposed regions of dielectric material 610. The lateral etching may be performed through the trench, such as a memory hole, and may occur from sidewalls within the trench along an exposed portion of each layer of metal material 620, such as tungsten. In some embodiments, the lateral etching may be selectively performed on the metal material layers, and may substantially maintain the intervening layers of silicon oxide or other dielectric material. Additionally, as illustrated, the etching may be performed on multiple surfaces of metal material 620, such as on opposite sides accessed from multiple trenches or memory holes. Method 500 may laterally etch the metal material less than 50 nm from the sidewalls of the trench, and between exposed layers of dielectric material 610 in exemplary operations before the lateral etching operation ends. In some embodiments, method 500 may laterally etch the metal material less than or about 45 nm, less than or about 40 nm, less than or about 35 nm, less than or about 30 nm, less than or about 25 nm, less than or about 20 nm, less than or about 15 nm, less than or about 10 nm, less than or about 9 nm, less than or about 8 nm, less than or about 7 nm, less than or about 6 nm, less than or about 5 nm, less than or about 4 nm, less than or about 3 nm, less than or about 2 nm, less than or about 1 nm, or less.

[0060] Method 500 may involve reducing the etch rate to allow more complete diffusion to occur, to help provide more even etching from top to bottom. Without the techniques described below, regions of metal material at or near the top of the trench may begin to etch before regions at the bottom. This may then produce a profile within the trench, such as a V-profile of metal material layers from the top to the bottom of the trench. This may occur, for example, when the amount of fluorine is increased in the mixture, or the temperature is increased.

[0061] The V-profile may be unavoidable with conventional dry technologies because of the high aspect ratios of trenches or memory holes in which the lateral etching may be performed. The diameter or width of exemplary trenches may be a few tens of nanometers or less, while the height of the trenches may be on the order of a few microns or more. This may produce aspect ratios or height to width ratios of greater than 20:1, greater than 50:1, greater than 75:1, greater than 100:1, or even greater. Accordingly, in embodiments over 25 layers, over 50 layers, over

75 layers, or over one hundred layers of alternating metal material and dielectric material may be formed and processed within each trench.

[0062] Because of the greater lengths a dry or gaseous etchant may travel, the top regions of the trench may be exposed to significant amounts of etchant before the etchant has even reached the bottom of the trench. In this way, the metal material located at upper regions of the trench may be etched more than portions at the bottom of the trench. Although a wet etch technique may more uniformly etch the layers of metal material, it may be incapable of etching less than, up to, or about 10 or more nanometers because of the properties and residence time of the etchant. Accordingly, conventional technologies may be incapable of finely etching an amount of material from each metal material layer, such as only a few nanometers, as well as produce a flat or substantially similar profile of etched metal material throughout the trench, unlike the present technology. The present technology, however, may compensate for the greater diffusion pathway by limiting the etchant in any of the ways discussed to allow a more uniform etching process to occur.

[0063] Process conditions may also impact the operations performed in method 500 as well as other etching methods according to the present technology. Each of the operations of method 500 may be performed during a constant temperature in embodiments, while in some embodiments the temperature may be adjusted during different operations. For example, the substrate, pedestal, or chamber temperature during the lateral etching operation 515 may be maintained between about -100° C and about 100° C in embodiments. The temperature may also be maintained below or about 80° C, below or about 60° C, below or about 40° C, below or about 20° C, below or about 0° C, below or about -20° C, below or about -40° C, or lower. Temperature may affect the etching process itself, and higher temperature may produce higher etch rates, increased etching, or other effects. Similarly, lower temperatures may slow the etching operation and allow improved diffusion. Thus, in some embodiments, maintaining a temperature below or about 50° C, or below or about 0° C, may provide more uniform etching amounts of metal material at the top of the trench and at the bottom of the trench. As temperature increases, the etching operations may additionally begin to affect the dielectric regions, and may cause slight rounding of exposed corners or regions of the dielectric material, such as silicon oxide.

[0064] The pressure within the chamber may also affect the operations performed, and in embodiments the chamber pressure may be maintained below about 10 Torr, below about 5 Torr, or below about 1 Torr. In embodiments a pressure below or about 1 Torr may allow the precursors or plasma effluents to more easily flow into the trenches or memory holes. However, when the pressure is reduced below about 0.5 Torr, a remote plasma may be affected, and may have reduced stability or may become unstable. As mentioned previously, the remote plasma may include an RPS unit, and may also be a region or portion of the chamber physically partitioned from the processing region of the chamber to limit or eliminate plasma at the substrate level. In some embodiments in which an RPS unit is utilized, a choke may be utilized to maintain a higher pressure within the RPS unit for plasma stability with a lower pressure within a chamber for improved in-trench flow of precursors or plasma effluents. Accordingly, a turbomolecular pump may be utilized in the chamber allowing a chamber pressure down to a few milliTorr, while the RPS is maintained above or about 0.6 Torr.

[0065] The chamber conditions, flow-rate ratio, and other operational characteristics may be adjusted to perform a controlled etch of the metal material. For example, each region of the metal material from the trench sidewalls may be etched laterally to a distance or depth less than or about 10 nm, or any of the previously described thicknesses depending on the thickness of materials to be deposited. In embodiments each layer of the metal material may be etched to a depth or distance from a trench sidewall of between about 1 nm and about 7 nm, or between about 2 nm and about 6 nm.

[0066] By performing the operations according to the present technology, the etching power may be reduced relative to the diffusion power of the etchant materials, which may allow a more uniform, substantially uniform, or essentially uniform etch to be performed at each metal material region exposed within the trench or memory hole. In embodiments, a metal material region at or near the top of the trench or memory hole, such as within 2 layers from the top, within 4 layers, within 6 layers, within 8 layers, within 10 layers, or more, may have an amount of material etched measured from the sidewall that is similar to a metal material layer or region at or near the bottom of the trench of memory hole, such as within 2 layers from the bottom, within 4 layers, within 6 layers, within 8 layers, within 10 layers, or more.

[0067] The two layers being compared may be separated by at least 1 layer, at least 5 layers, at least 11 layers, at least 21 layers, at least 51 layers or more depending on the overall number of stacked layers within the structure through which the trench or memory hole has been etched. The lateral etch of the two layers being compared may differ by less than or about 30%, in terms of the upper layer being etched no more than 30% more than the lower layer. Additionally, the present technology may perform a lateral etch of the two layers so a difference between the amount of metal material etched between the two layers is less than or about 25%, less than or about 20%, less than or about 15%, less than or about 10%, less than or about 5%, less than or about 1%, or zero difference in which case both regions of metal material are etched to an equal depth or distance from a sidewall of the trench. Substrate 605 may show minimal etching at the bottom of trenches 630, and may be reduced by an amount less than or about 5 nm, and may be reduced by an amount less than or about 3 nm, less than or about 2 nm, less than or about 1 nm, or may be substantially maintained during the lateral etching operations of metal material.

[0068] At optional operation 520, the substrate may be transferred from the etching chamber to a deposition chamber. The transfer may occur under vacuum, and the two chambers may both reside on the same cluster tool to allow the transfer to occur in a controlled environment. For example, vacuum conditions may be maintained during the transfer, and the transfer can occur without breaking vacuum. Once in the deposition chamber, such as chamber 400 described above, a cap material may be formed or deposited over the recessed metal material 620 at operation 525. As illustrated in FIG. 6C, cap material 625, which may be a barrier material, may be formed directly on or contacting recessed metal material 620. The deposition operation may be a selective deposition in which the cap material is formed preferentially on the metal material 620 relative to exposed dielectric material 610. As opposed to conventional technologies that may include additional masking operations, operation 525 may be performed directly subsequent etching operation 515.

[0069] Although transfer of the substrate may occur, no other substrate processing may be performed between the selective etching and the selective deposition. As will be explained in further detail below, the selective deposition may include multiple operations, but the entire deposition process may be performed directly after the etching set of operations, although substrate transfer in between the operations may be performed in embodiments. By performing a

selective etch and a selective deposition according to the method 500, queue times may be substantially reduced over conventional technology that may require additional masking and removal techniques due to blanket deposition or formation of the cap material 625.

[0070] A variety of materials may be utilized in the processing, and the etching and deposition may be selective to multiple components. Accordingly, the present technology may not be limited to a single set of materials. For example, as previously noted, metal material 620 may be several conductive species utilized in semiconductor processing. Metal material 620 may be or include tungsten, cobalt, or any other conductive metal that may perform as a metal layer in a memory structure. Dielectric material 610 may also include an insulative material, and may also include a silicon-containing material, an oxygen-containing material, a carbon-containing material, or some combination of these materials, such as silicon oxide or silicon oxycarbide. Cap material 625 may include one or more dielectric materials, insulative materials, ceramic materials, or barrier materials.

[0071] Cap material 625 may be utilized over tungsten for multiple purposes. In some embodiments titanium nitride may be used as cap material 625, although it is to be understood that similar materials may also be used including other metal nitrides, oxides, or dielectric materials. Titanium nitride may serve as a barrier over the tungsten. However, in many conventional depositions, the cap material may also form over the dielectric material 610, which may then allow connections between the separate nodes or layers. Thus, an etch back process may be performed. When recessing the material from the dielectric, the process may similarly reduce the cap material from the tungsten or metal material due to the minimal coverage or incorporation, and may expose the tungsten.

[0072] Subsequent operations in forming the memory structure may include depositing additional core materials, which may include a blocking layer, such as aluminum oxide. While aluminum oxide may deposit on the dielectric material, tungsten and other metals may have low adhesion capabilities, and the aluminum oxide may not readily deposit over this material, which may cause voids in the blocking layer. The formation of the aluminum oxide on exposed tungsten may also oxidize the metal, which may increase the resistivity. Titanium nitride and other barrier layer materials may adhere to tungsten to operate as a barrier layer, and may allow formation of aluminum oxide along the sidewall. Accordingly, by utilizing a cap material 625,

such as a titanium nitride barrier layer, the oxide-metal NAND structure may be more readily produced.

[0073] The etching operations may involve additional precursors along with particular fluorine-containing precursors. Nitrogen trifluoride may be utilized to generate plasma effluents in some embodiments. Additional or alternative fluorine-containing precursors may also be utilized. For example, a fluorine-containing precursor may be flowed into the remote plasma region and the fluorine-containing precursor may include at least one precursor selected from the group consisting of atomic fluorine, diatomic fluorine, bromine trifluoride, chlorine trifluoride, nitrogen trifluoride, hydrogen fluoride, sulfur hexafluoride, and xenon difluoride. The remote plasma region may be within a distinct module from the processing chamber or a compartment within the processing chamber. As illustrated in FIG. 2, both RPS unit 201 and first plasma region 215 may be utilized as the remote plasma region. An RPS may allow dissociation of plasma effluents without damage to other chamber components, while first plasma region 215 may provide a shorter path length to the substrate during which recombination may occur.

[0074] An additional precursor may also be delivered to the remote plasma region to augment the fluorine-containing precursor. For example, a carbon-and-hydrogen-containing precursor or a hydrogen precursor may be delivered with the fluorine-containing precursor. The additional precursor may also be a fluorine-containing precursor, such as methyl fluoride, for example. The hydrogen-containing or carbon-and-hydrogen-containing precursor may be included to maintain a particular H:F atomic ratio for the plasma effluents. In embodiments the etching may be performed with an H:F ratio greater than 1, which may provide increased selectivity towards tungsten or other metals relative to dielectric materials discussed above. The H:F atomic flow ratio may be maintained greater than 2:1 or greater than 3:1 in embodiments, which may be controlled by adjusting relative flow rates of the fluorine-containing precursor and the hydrogen-containing precursor.

[0075] The etch selectivity of tungsten relative to other components exposed on the surface of the substrate when the present methods are performed may be greater than or about 10:1, greater than or about 20:1, greater than or about 50:1, or greater than or about 100:1, or more, for a variety of materials formed on the substrate, and which may be exposed to plasma effluents. The etch selectivity of tungsten relative to (poly)silicon may be greater than or about 100:1, greater

than or about 150:1, greater than or about 200:1 or greater than or about 250:1 in disclosed embodiments. The etch selectivity of tungsten relative to silicon oxide may be greater than or about 15:1, greater than or about 25:1, greater than or about 30:1 or greater than or about 40:1 in embodiments. The etch selectivity of tungsten relative to silicon oxycarbide may be greater than or about 10:1, greater than or about 20:1, greater than or about 30:1, or greater than or about 40:1 in embodiments. The etch selectivity of tungsten relative to tungsten oxide may be greater than or about 10:1, greater than or about 20:1, greater than or about 50:1, or greater than or about 100:1 in embodiments.

[0076] Accordingly, depending on the feature sizes, tungsten may be removed from the surface of the substrate while the other exposed materials may be reduced by less than 1 nm. The depth of the recess for the metal material 620 may be less than or about 50 nm, and may be less than or about 40 nm, less than or about 30 nm, less than or about 20 nm, less than or about 10 nm, or less in embodiments. Because of this depth of etching, a minimal amount of dielectric material may be removed, which may be less than or about 3 nm, less than or about 1 nm, less than or about 0.5 nm, or the materials may be substantially or essentially maintained. Accordingly, the tungsten etch relative to the dielectric material and substrate may be characterized by any of the selectivities discussed above for the materials that may be utilized for each structure.

[0077] The selective deposition may be performed in a chamber capable of deposition, and which may be capable of atomic layer deposition, including chamber 400 as described above. The deposition may be premised on selectively depositing an insulative material on a metal material relative to another insulative material. For example, the cap material 625 may be formed substantially on metal material 620, while being minimally formed or limited from dielectric material 610. The selective deposition may be performed by multiple operations, which may include formation of a self-assembled monolayer to facilitate selective deposition, or may include actively inhibiting formation of dielectric on other dielectric materials.

[0078] Self-assembled monolayers may be formed on regions of the structure to tune deposition. For example, a first self-assembled monolayer may be formed over the structure, and then exposed to remove the monolayer from metal material 620. The monolayer may be maintained over dielectric material 610. The monolayer may have termination moieties that may repel or fail to interact with later delivered precursors. For example, the termination moieties

may be hydrophobic in embodiments, and may terminate with hydrogen-containing moieties, such as methyl groups, which may not interact with additional precursors. A second self-assembled monolayer may be formed over the metal material 620, which may be hydrophilic or reactive with one or more precursors utilized to produce cap material 625. The second self-assembled monolayer may be formed selectively over the metal material 620, as the material may be repelled from the first self-assembled monolayer, or may be drawn selectively to the metal. The second self-assembled monolayer may terminate with hydroxyl or other hydrophilic moieties, or with moieties that interact specifically with additional precursors used to form cap material 625.

[0079] An atomic layer deposition may then be performed utilizing two or more precursors to develop cap material 625. The precursors of the deposition may include a metal-containing precursor and a precursor configured to interact with the moieties terminating the second self-assembled monolayer, but not the first self-assembled monolayer. For example, when hydrophilic and hydrophobic terminating monolayers are utilized, one of the atomic layer deposition precursors may include water, or some other precursor to develop the cap material that may be hydrophilic. In this way, the deposition may not form over the first self-assembled monolayer, which may be hydrophobic. If the cap material includes a metal oxide, such as titanium oxide or titanium nitride, the precursors used in the atomic layer deposition may include a titanium-containing precursor, as well as water or a nitrogen-containing precursor. The water may then fail to interact with the first self-assembled monolayer formed over the dielectric material 610 during the half reaction with water or the other precursor, and thus the deposition will not form over the first self-assembled monolayer. In this way, the cap material 625 may be selectively formed over the metal material 620 without a mask layer being formed that may be chemically etched.

[0080] After cap material 625 has been formed to a suitable height, the first self-assembled monolayer may be exposed, such as to UV light in one example, and removed from the substrate. Accordingly, the first self-assembled monolayer may be formed directly subsequent the selective etch of the metal material, or after transfer to an additional chamber but before additional process operations, and an additional masking layer that requires chemical removal or etching may not be utilized on the structure. Similarly an etch of cap material 625 may not be necessary

subsequent the selective deposition to ensure the cap material 625 is formed selectively over the metal material. In this way, multiple operations utilized in conventional formation may be obviated, which may reduce queue times significantly, such as by hours.

[0081] Additional selective deposition techniques may also be utilized that may include alternative mechanisms for selectively depositing a dielectric material such as a nitrogen-containing material. For example, a nitrogen-containing material may be utilized as one of the self-assembled monolayers on a material for which deposition is to occur, such as in one of the termination moieties of the monolayers, which may allow attraction of particular precursors used in the formation of one or more of the materials previously described. Still other techniques may utilize temperature differentials to enhance deposition on metal relative to silicon oxide. For example, an atomic layer deposition utilizing a titanium-containing precursor and a nitrogen-containing precursor may be performed at temperatures above or about 500° C, and may be performed at temperatures above or about 750° C, above or about 900° C, above or about 1000° C, or up to, above, or about 1100° C.

[0082] As temperature is increased within this range, the deposition may occur on tungsten at a higher rate than on silicon oxide. A selective etch of nitrogen may then be performed to remove the first dielectric material from the silicon oxide surface. Although the first dielectric material may also be reduced on the metal material surface, because the thickness may be many times greater than that on the silicon oxide, full removal from the silicon oxide may be performed while maintaining a thickness on the metal material.

[0083] Embodiments may also utilize an inhibitor to form cap material 625 selectively over metal material 620, while not forming cap material 625 over dielectric material 610. For example, an inhibitor may be applied across the dielectric material. The inhibitor may be any number of materials that may be characterized by a siloxane backbone, such as silicone, or a tetrafluoroethylene backbone, such as PTFE, along with other oil or surfactant materials. The material may be applied to cover exposed portions of dielectric material 610. The inhibitor material may prevent adhesion or adsorption of the material, which may form or deposit normally on metal material 620. Subsequent formation of cap material 625, a removal agent may be applied to the substrate to remove the inhibitor material. The removal agent may be a wet etchant, reactant, or surfactant cleanser that may remove residual inhibitor material exposing

the underlying dielectric material 610. Accordingly, the inhibitor may be applied directly subsequent the selective etch, or subsequent transfer of the substrate, but prior to other process operations affecting the substrate. Utilizing an inhibitor may allow formation of the cap material in a defined region that need not be defined via subsequent patterning and/or etching of a blanket film. By removing prior and subsequent patterning operations, the processes may further reduce queue times over conventional processes.

[0084] The inhibitor may also be a poisoning agent or a product of a plasma application that may neutralize or render inert a surface of the substrate. For example, a modifying plasma may be formed from one or more precursors, which may include inert precursors. The plasma may be applied to a surface of the substrate, which may alter surfaces of dielectric material 610, but which may not affect the metal material 620. In one possible example, a nitrogen-containing precursor, which may be nitrogen, may be delivered to a plasma processing region of a processing chamber, where a plasma is generated. The plasma effluents, which may include nitrogen-containing plasma effluents, may be delivered to a substrate, and may form a nitrogenized surface along dielectric material 610.

[0085] The plasma effluents may not affect the metal material 620, which may maintain a neat or unreacted surface. Cap material 625 may then be formed with one or more deposition techniques, which may include atomic layer deposition or other vapor or physical deposition. For example, an atomic layer deposition technique may be utilized subsequent processing with the plasma effluents. After each cycle of the deposition, a nitrogen-containing plasma may be reapplied to the substrate, such as over dielectric material 610. In this way, the surface of dielectric material 610 may be passivated to prevent or limit formation of cap material 625 over those regions. Other plasma or non-plasma materials may also be used to modify or poison dielectric material 610, which may also be treated to repel one or more of the precursors which may be used in the formation of cap material 625. Utilizing these plasma effluents on non-recessed portions of the substrate may allow formation of the cap material in a defined region that need not be defined via subsequent patterning and/or etching of a blanket film. By removing prior and subsequent patterning operations, the processes may further reduce queue times over conventional processes.

[0086] Any of these techniques may selectively deposit or form dielectric or insulative materials over a metal-containing region relative to one or more non-metal, dielectric, or insulative regions. The selectivity may be complete in that the cap material forms only over metal material 620, or an intervening layer, and cap material may not form at all over dielectric material 610. In other embodiments the selectivity may not be complete, and may be in a ratio of deposition on metal-containing materials relative to dielectric or insulative materials greater than about 2:1. The selectivity may also be greater than or about 5:1, greater than or about 10:1, greater than or about 15:1, greater than or about 20:1, greater than or about 25:1, greater than or about 30:1, greater than or about 35:1, greater than or about 40:1, greater than or about 45:1, greater than or about 50:1, greater than or about 75:1, greater than or about 100:1, greater than or about 200:1, or more.

[0087] The cap material may be formed to a thickness described previously, which may be less than or about 50 nm, and may be less than or about 40 nm, less than or about 30 nm, less than or about 20 nm, less than or about 10 nm, less than or about 5 nm, or less. Accordingly, selectivities below 50:1 may be acceptable to fully deposit cap material 625 while forming a limited amount or essentially not forming material over the dielectric material 610. A slight etch back operation may be performed in chamber 200 subsequent the deposition to ensure cap material 625 is fully removed from dielectric material 610, to ensure that the nodes are separated completely. Because the coverage may be complete within the recessed regions of metal material 620, the etch back may not affect the material deposited, or may clean the edges or sidewalls to produce a smooth surface. As the deposition may be greater on the metal material 620, any amount that may deposit on dielectric material 610, may be compensated on metal material 620 by a slightly longer deposition time, which may then be recessed to the thickness of the recess, and which may clean the sidewalls of the dielectric material 610.

[0088] The deposition operations may be performed at any of the temperature or pressures previously described, and may be performed at temperatures greater than or about 50° C, and may be performed greater than or about 100° C, greater than or about 150° C, greater than or about 200° C, greater than or about 250° C, greater than or about 300° C, greater than or about 350° C, greater than or about 400° C, greater than or about 450° C, greater than or about 500° C, greater than or about 600° C, greater than or about 700° C, greater than or about 800° C, or

higher. For example, temperatures greater than or about 400° C may be utilized during atomic layer deposition operations in order to activate precursors to interact with one another as layers of material are being formed. By utilizing the present technology, fabrication may be performed with more selective formation and removal over conventional techniques, which may reduce queue times by hours over conventional processes. By performing the recessing operations in addition to the barrier formation, node separation may be more clearly defined, and subsequent processes or formation within the memory hole may be more easily performed. The processes may also enable new structures available by forming selective layers to ensure that the metal material is protected, while the nodes are maintained separated in the memory structure.

[0089] In an additional method encompassed by the present technology, the recessing of the metal material may not be performed. Turning to **FIG. 7** is shown schematic cross-sectional views of exemplary substrates 700 according to embodiments of the present technology. Substrates 700 may be similar to substrates 600 previously described and illustrated in FIG. 7A, and may include similar material, or other materials as previously described, and may be characterized by any of the dimensions or other characteristics as described previously. For example, structure 700 may include a substrate 605, as well as alternating layers of dielectric material 610, and metal material 620. Memory holes or trenches 630 may be formed within the structure, and may be characterized by sidewalls 632.

[0090] Unlike method 500, which included recessing metal material 620, an additional structure may be formed by the present technology as illustrated in FIG. 7B. As illustrated, recessing metal material 620 may not be performed. The method illustrated may directly deposit cap material 625 on metal material 620 subsequent formation of the memory holes, or trenches 630. Similar methods or operations of selectively depositing the cap material as described previously may be performed, and the cap material, which may be a barrier material, may be any of the previously described materials, including titanium nitride, for example.

[0091] Cap material may be formed to extend outward from metal material 620, and extend within trench 630. Similarly to the previously described structures, cap material 625 may not be formed on dielectric material 610, or may not be continuous across dielectric material 610, in order to produce a separation between each cell. Subsequent the formation of the cap material 625, additional operations may be performed, including cleaning any residual formation on

dielectric material 610, as well as formation of a blocking layer, such as aluminum oxide, and additional core formation. By performing the methods without a recessing process, queue times may be reduced, and surface roughening and other etching side effects may limited.

[0092] In the preceding description, for the purposes of explanation, numerous details have been set forth in order to provide an understanding of various embodiments of the present technology. It will be apparent to one skilled in the art, however, that certain embodiments may be practiced without some of these details, or with additional details.

[0093] Having disclosed several embodiments, it will be recognized by those of skill in the art that various modifications, alternative constructions, and equivalents may be used without departing from the spirit of the embodiments. Additionally, a number of well-known processes and elements have not been described in order to avoid unnecessarily obscuring the present technology. Accordingly, the above description should not be taken as limiting the scope of the technology.

[0094] Where a range of values is provided, it is understood that each intervening value, to the smallest fraction of the unit of the lower limit, unless the context clearly dictates otherwise, between the upper and lower limits of that range is also specifically disclosed. Any narrower range between any stated values or unstated intervening values in a stated range and any other stated or intervening value in that stated range is encompassed. The upper and lower limits of those smaller ranges may independently be included or excluded in the range, and each range where either, neither, or both limits are included in the smaller ranges is also encompassed within the technology, subject to any specifically excluded limit in the stated range. Where the stated range includes one or both of the limits, ranges excluding either or both of those included limits are also included.

[0095] As used herein and in the appended claims, the singular forms “a”, “an”, and “the” include plural references unless the context clearly dictates otherwise. Thus, for example, reference to “a layer” includes a plurality of such layers, and reference to “the precursor” includes reference to one or more precursors and equivalents thereof known to those skilled in the art, and so forth.

[0096] Also, the words “comprise(s)”, “comprising”, “contain(s)”, “containing”, “include(s)”, and “including”, when used in this specification and in the following claims, are intended to specify the presence of stated features, integers, components, or operations, but they do not preclude the presence or addition of one or more other features, integers, components, operations, acts, or groups.

CLAIMS:

1. A method of forming a semiconductor structure, the method comprising:

forming a plasma of a fluorine-containing precursor in a remote plasma region of a processing chamber;

contacting a semiconductor substrate with effluents of the plasma, wherein the semiconductor substrate is housed in a processing region of the processing chamber;

selectively etching a metal material laterally between exposed regions of a dielectric material on the semiconductor substrate; and

subsequently depositing a cap material over the metal material, wherein the cap material is selectively deposited on the metal material relative to exposed regions of the dielectric material.

2. The method of forming a semiconductor structure of claim 1, wherein the etching is performed in a first processing chamber, and the depositing is performed in a second processing chamber, the method further comprising transferring the semiconductor substrate from the first processing chamber to the second processing chamber, and wherein the transferring is performed without breaking vacuum.

3. The method of forming a semiconductor structure of claim 1, wherein the metal material comprises tungsten or cobalt, and wherein the dielectric material comprises silicon oxide.

4. The method of forming a semiconductor structure of claim 1, wherein the cap material comprises a metal nitride or a metal oxide.

5. The method of forming a semiconductor structure of claim 1, wherein the metal material is laterally etched less than 10 nm from exposed sidewalls.

6. The method of forming a semiconductor structure of claim 1, wherein the etching is performed with a selectivity towards the metal material relative to the dielectric material greater than or about 10:1, and wherein the deposition is performed with a selectivity towards the metal material relative to the dielectric material greater than or about 2:1.

7. The method of forming a semiconductor structure of claim 1, wherein selectively depositing the cap material comprises inhibiting growth of the cap material on the dielectric material.

8. A method of forming a semiconductor structure, the method comprising:

forming a plasma of a fluorine-containing precursor in a remote plasma region of a processing chamber;

contacting a semiconductor substrate with effluents of the plasma, wherein the semiconductor substrate is housed in a processing region of the processing chamber;

selectively etching layers of silicon nitride laterally between exposed layers of a dielectric material on the semiconductor substrate; and

subsequently depositing a cap material over the metal material, wherein the cap material is selectively deposited on the metal material relative to exposed regions of the dielectric material.

9. The method of forming a semiconductor structure of claim 8, wherein the layers of silicon nitride are laterally etched less than 10 nm from exposed sidewalls.

10. The method of forming a semiconductor structure of claim 9, wherein the dielectric material comprises silicon oxide, wherein the cap material comprises a metal nitride or a metal oxide.

11. The method of forming a semiconductor structure of claim 10, wherein the metal nitride comprises titanium nitride.

12. The method of forming a semiconductor structure of claim 8, wherein the etching is performed in a first processing chamber, and the depositing is performed in a second processing chamber.

13. The method of forming a semiconductor structure of claim 12, further comprising transferring the semiconductor substrate from the first processing chamber to the second processing chamber, and wherein the transferring is performed without breaking vacuum.

14. The method of forming a semiconductor structure of claim 8, wherein the semiconductor substrate defines multiple trenches, and wherein the silicon nitride is etched on multiple surfaces.

15. The method of forming a semiconductor structure of claim 8, wherein the etching is performed with a selectivity towards the silicon nitride relative to the dielectric material greater than or about 10:1, and wherein the deposition is performed with a selectivity towards the silicon nitride relative to the dielectric material greater than or about 2:1.

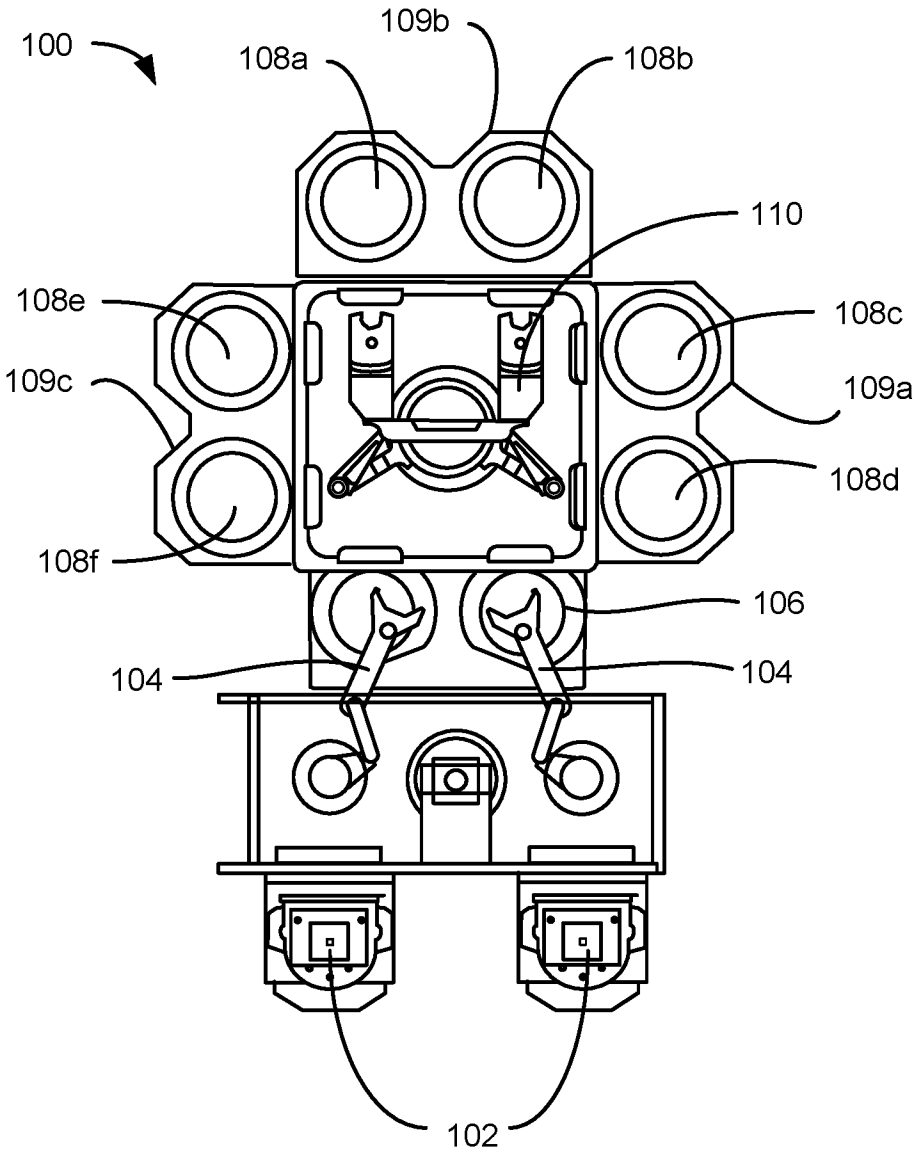

100
109b
108a
108b
110
108e
108c
109c
109a
108d
108f
106
104
104
102

FIG. 1

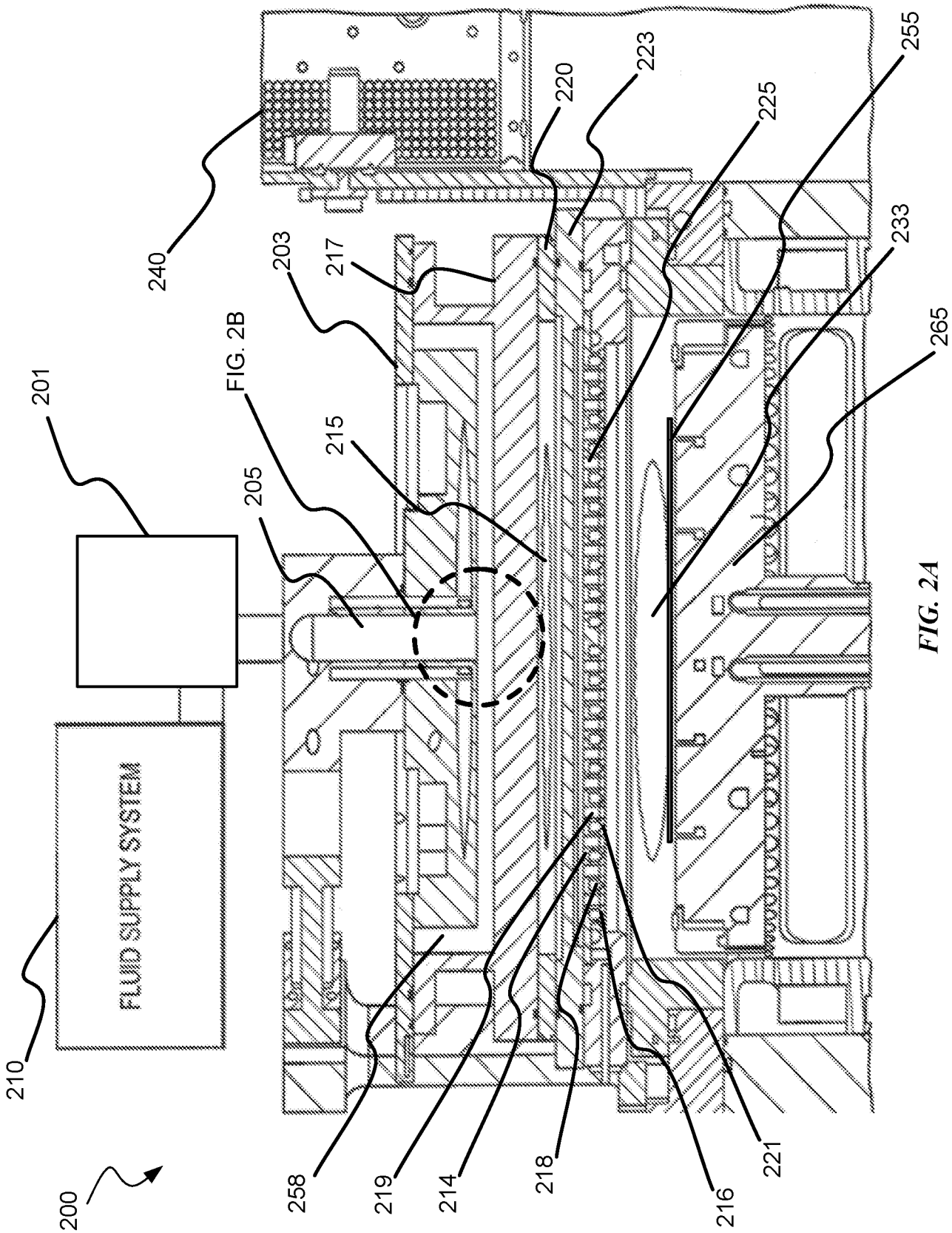

200
210
FLUID SUPPLY SYSTEM
201
205
FIG. 2B
215
203
217
240
220
223
225
255
233
265
258
219
214
218
216
221

FIG. 2A

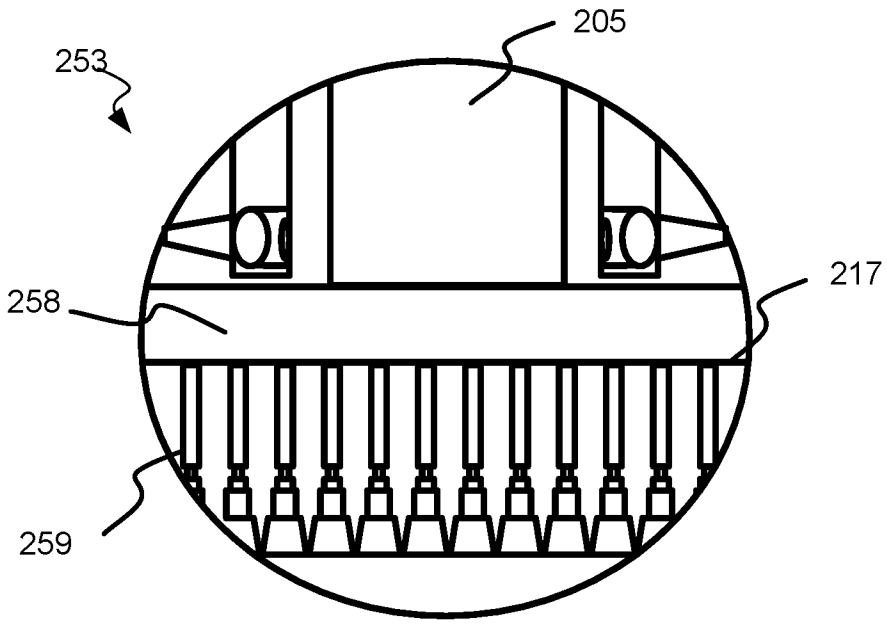


FIG. 2B

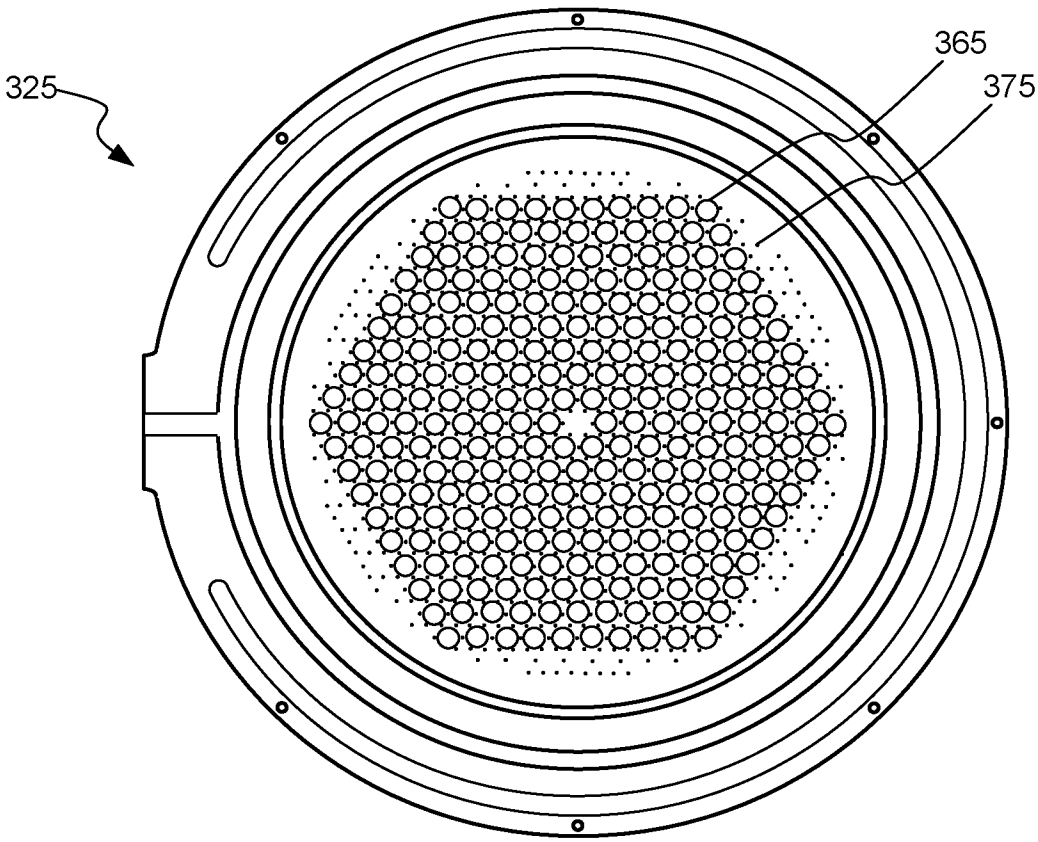
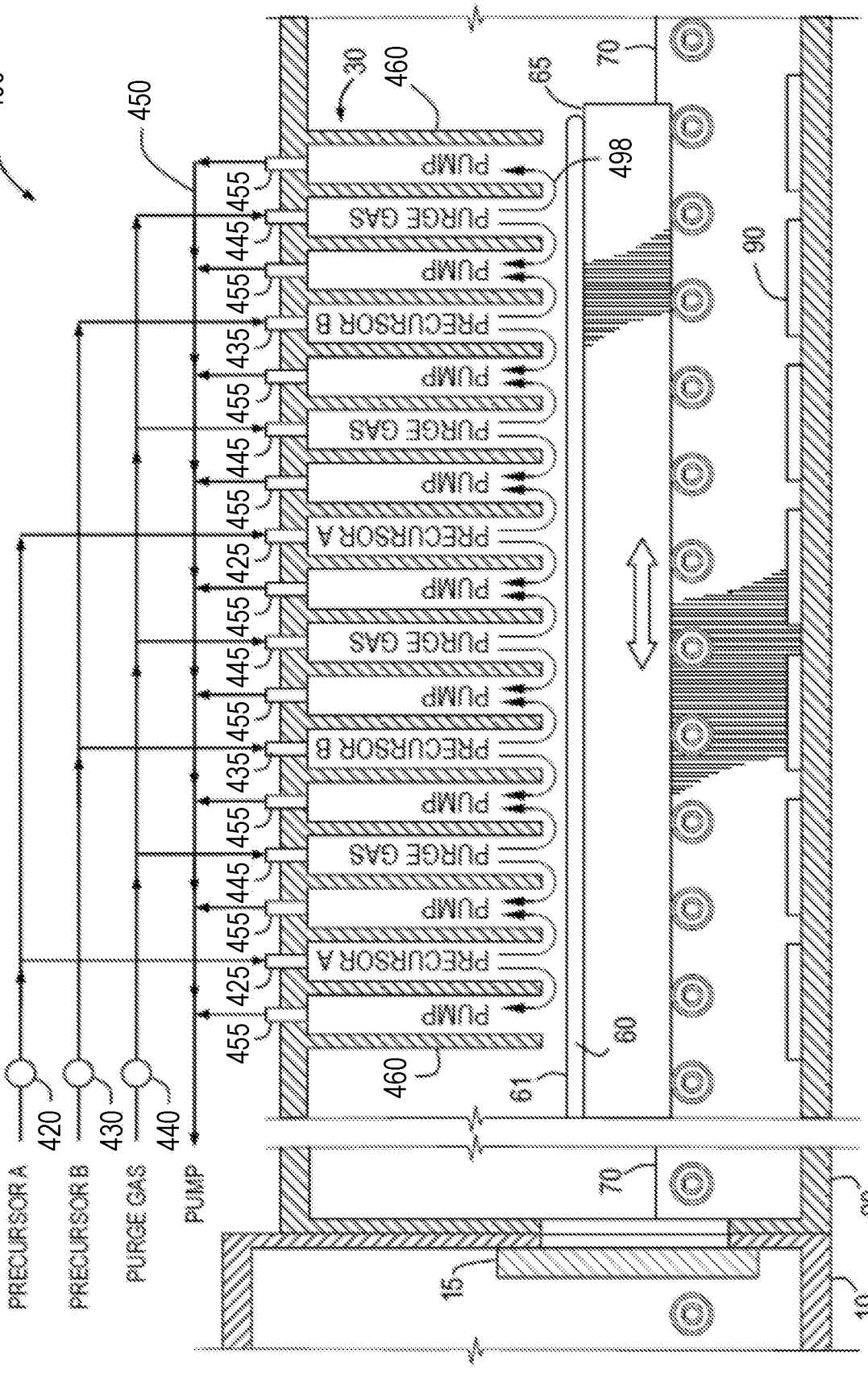


FIG. 3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450
30
460
65
70
498
90
PUMP
PURGE GAS
PRECURSOR B
PRECURSOR A
455
445
435
425
420
430
440
PRECURSOR A
PRECURSOR B
PURGE GAS
PUMP
60
61
15
20
10

FIG. 4

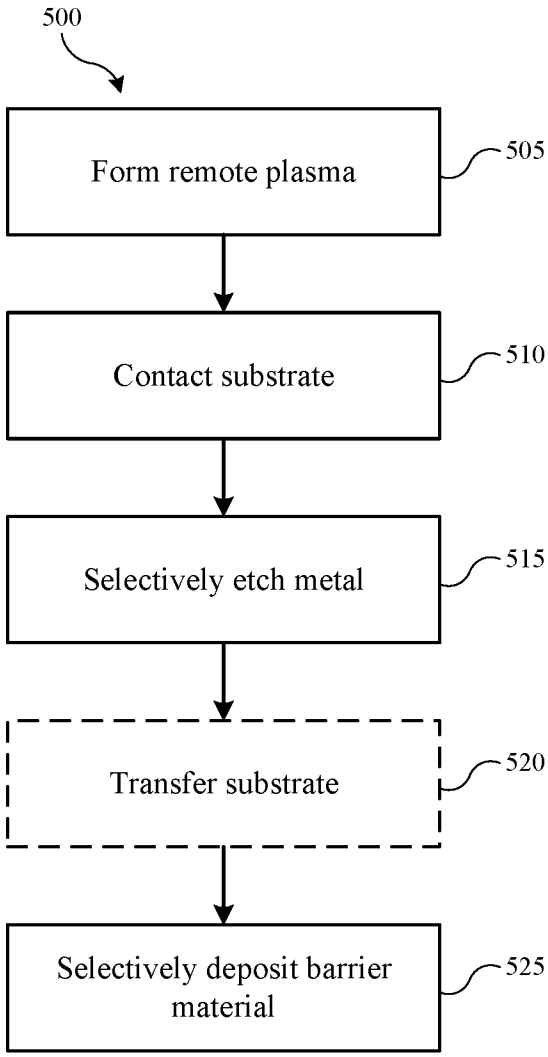
500
Form remote plasma
505
Contact substrate
510
Selectively etch metal
515
Transfer substrate
520
Selectively deposit barrier material
525

FIG. 5

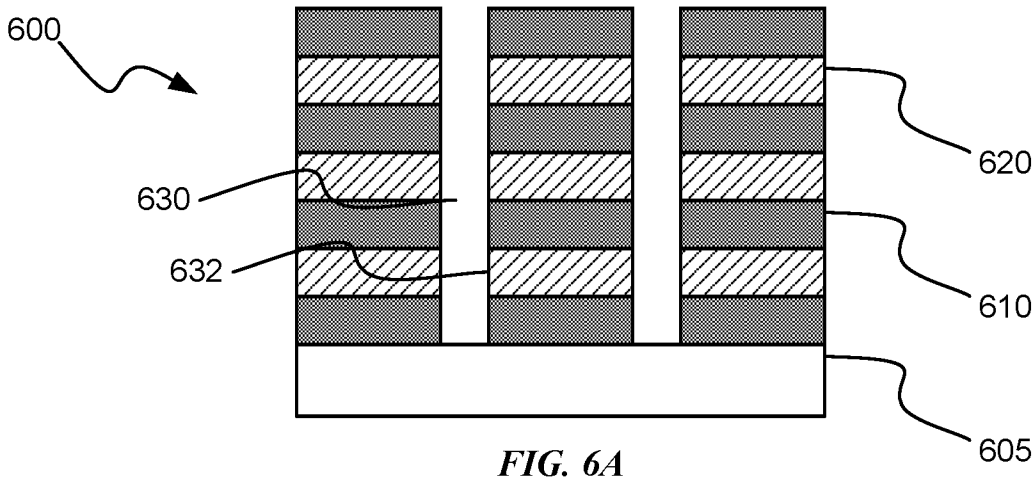

FIG. 6A

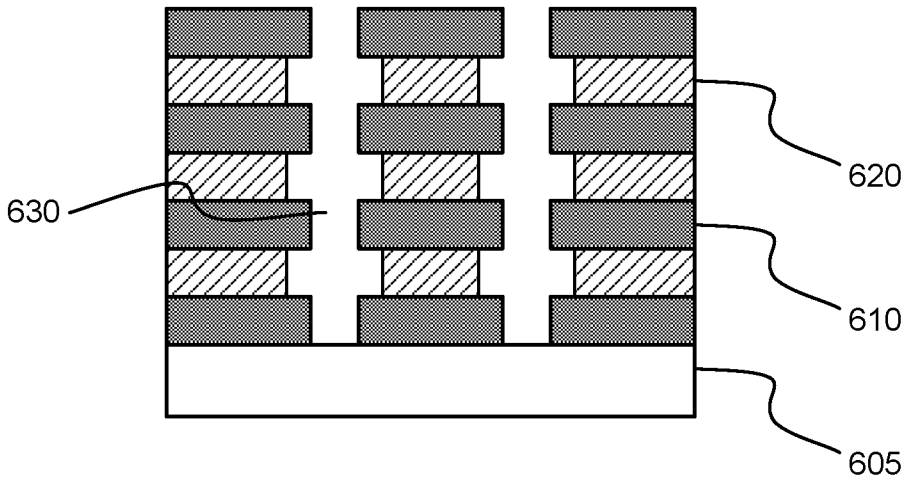

FIG. 6B

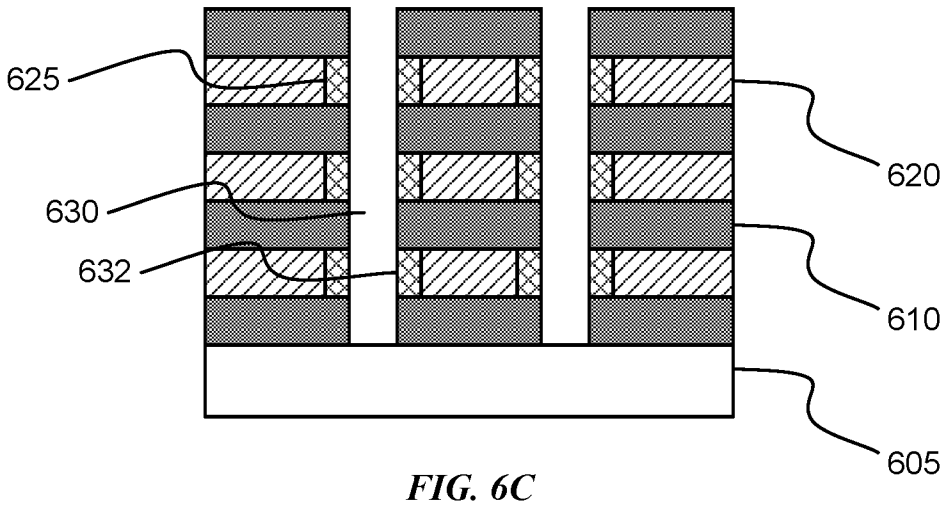

FIG. 6C

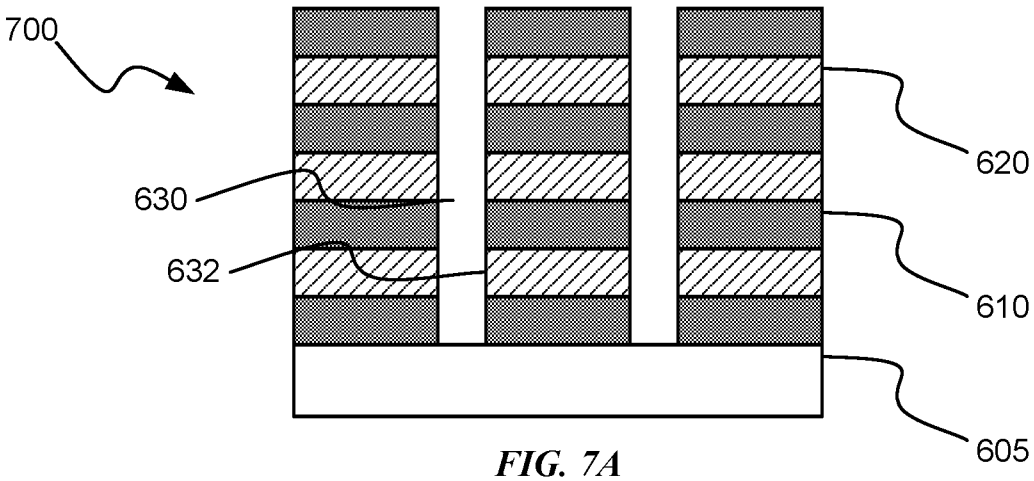

FIG. 7A

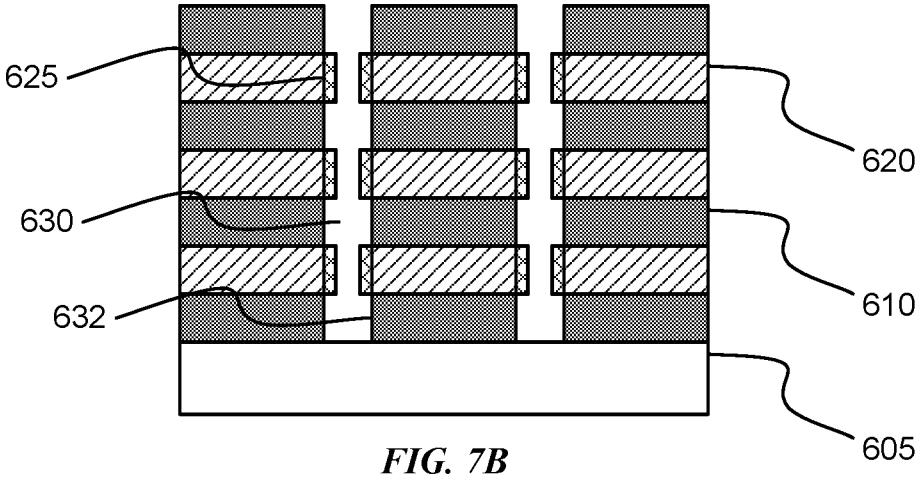

FIG. 7B

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2018/028568

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/768(2006.01)i, H01L 21/02(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/768; H01L 27/115; H01L 21/28; H01L 21/8247; C23C 16/00; H01L 21/02

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & keywords: fluorine-containing, etching, metal, silicon nitride, cap

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2007-0119373 A1 (KUMAR et al.) 31 May 2007 See paragraphs [0027]-[0029],[0088]-[0091] and figures 1-7.	1-15
Y	KR 10-2013-0124289 A (SANDISK TECHNOLOGIES INC.) 13 November 2013 See paragraphs [0034]-[0043], claim 1 and figures 5b-8a.	1-7
Y	US 2017-0084623 A1 (SANDISK TECHNOLOGIES INC.) 23 March 2017 See paragraphs [0095],[0156]-[0164], claim 10 and figures 15A-15F.	8-15
A	KR 10-0985881 B1 (HYNIX SEMICONDUCTOR INC.) 08 October 2010 See claims 1-12 and figures 1,2.	1-15
A	KR 10-0655277 B1 (SAMSUNG ELECTRONICS CO., LTD.) 08 December 2006 See pages 2-4 and figure 2d.	1-15

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
09 August 2018 (09.08.2018)	**09 August 2018 (09.08.2018)**

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Telephone No. +82-42-481-8291

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2018/028568

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

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		US 8461641 B2	11/06/2013
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