United States Patent [19]

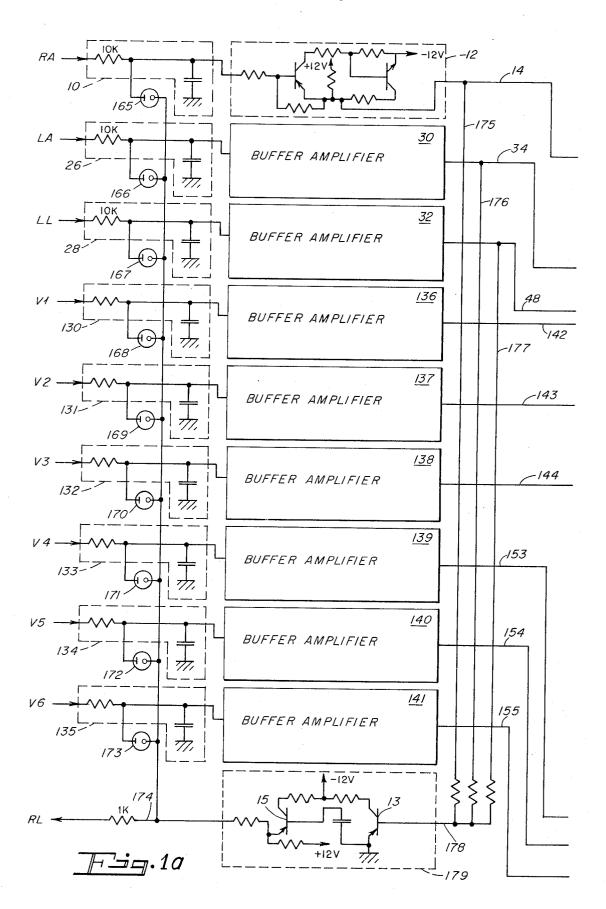
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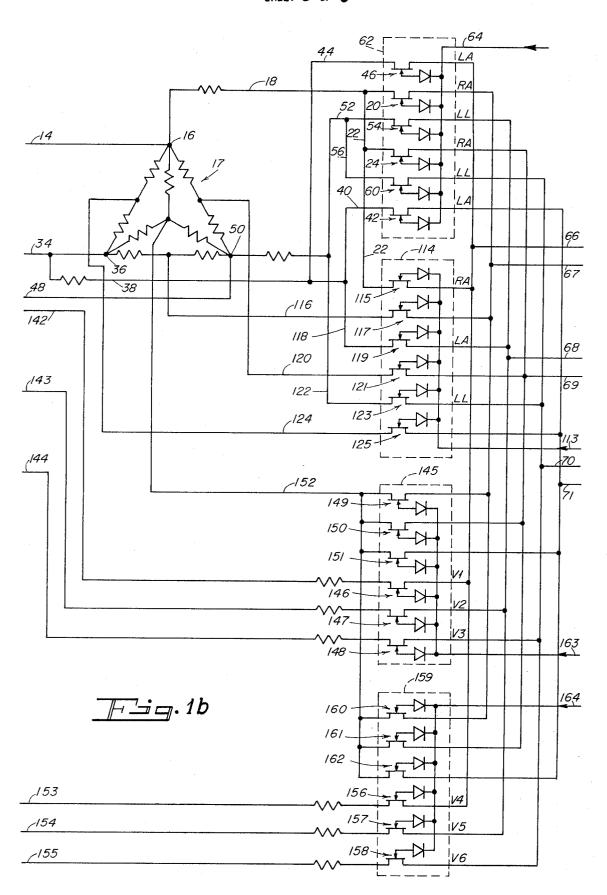
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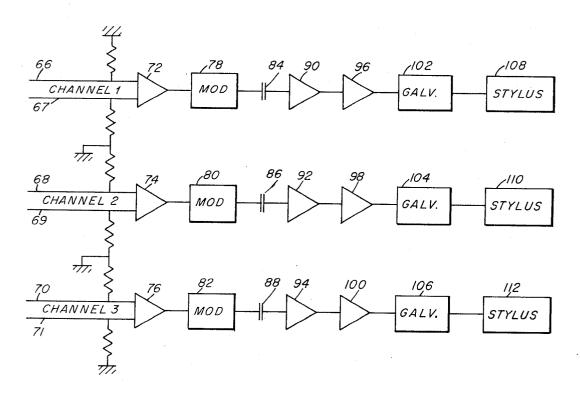
[45] Mar. 4, 1975

[54] [75]	ELECTR	LE CHANNEL OCARDIOGRAPH Ernest F. J. Graetz, Derry, N.H.	3,477,421 3,579,138 3,699,948 3,757,778	11/1969 5/1971 10/1972 9/1973	Partridge 128/2.06 B Harris et al. 128/2.06 B Ota et al. 128/2.06 G Graham 128/2.06 B	
[73]		Assignee: Parke, Davis & Company, Detroit,	FOR	FOREIGN PATENTS OR APPLICATIONS		
[]		Mich.	850,926	9/1952	Germany 128/2.06 B	
[22]	Filed:	Mar. 4, 1974	1,416,855 47,437	10/1968 4/1969	Germany	
[21]	Appl. No.	: 448,173	•		·	
[63]	Related U.S. Application Data Continuation of Ser. No. 281,074, Aug. 16, 1972, abandoned.		Attorney,	Primary Examiner—William E. Kamm Attorney, Agent, or Firm—James F. Powers, Jr.; Albert H. Graddis		
[52]	U.S. Cl	128/2.06 G, 330/29, 330/86	[57]		ABSTRACT	
[51]	[51] Int. Cl			The specific disclosure provides a multiple channel		
[58]	* * * * * * * * * * * * * * * * * * *			electrocardiograph wherein three body voltage measurements are simultaneously read-out on a moving chart. The electrocardiograph comprises means for automatically changing the body voltage measure-		
[56]	References Cited		ments tha	ments that are recorded on the chart, and means in-		
	UNITED STATES PATENTS			cluding a selectively operable circuit for automatically		
2,660 3,058		100 to 0 C D	attentuating cinity of t		oltage measurements taken in vi-	
3,343	,528 9/19	067 Kirkham 128/2.06 B		9 Claim	s, 12 Drawing Figures	

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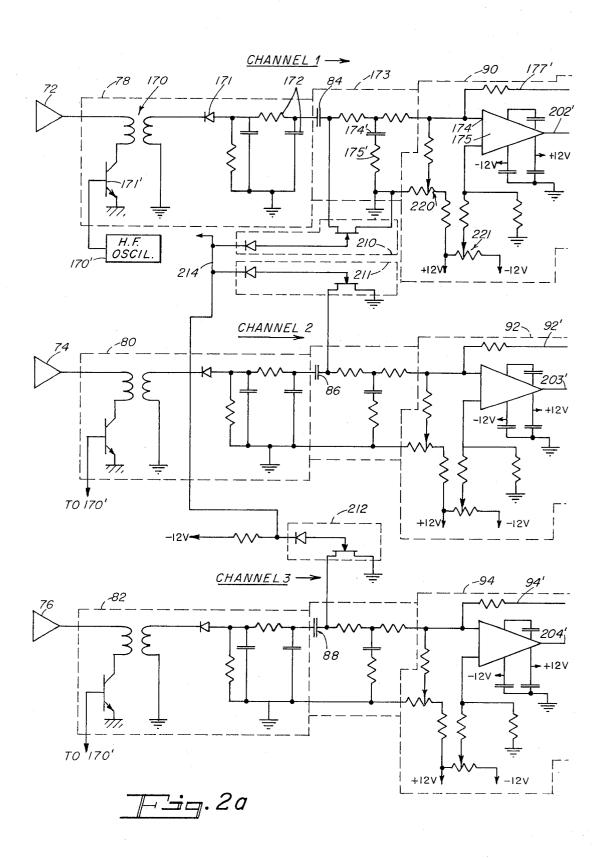


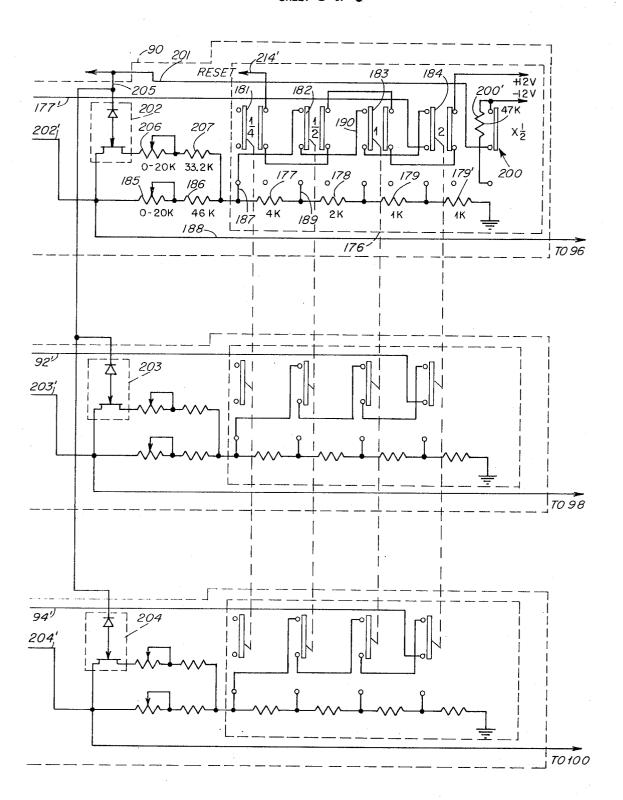




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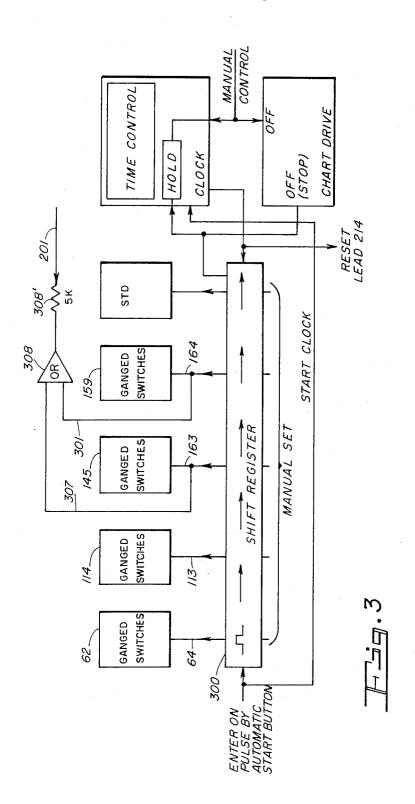
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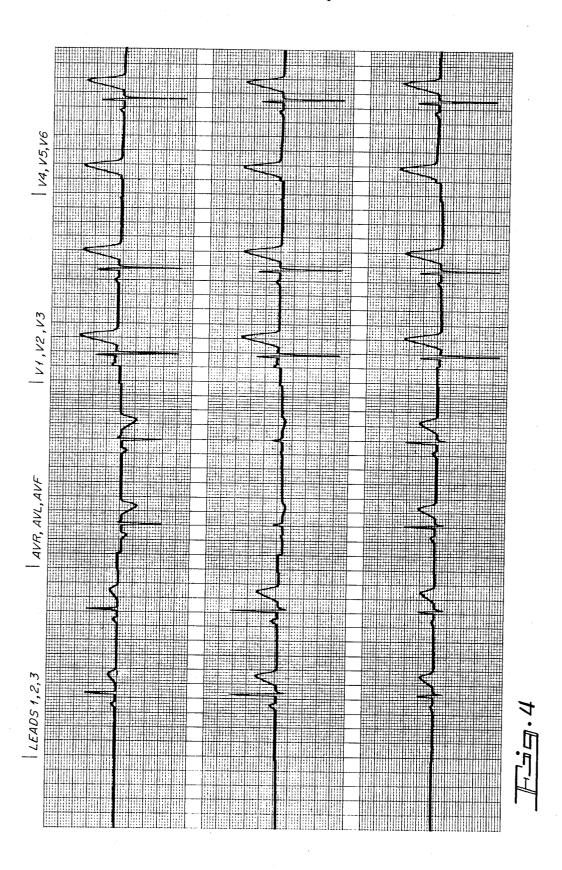


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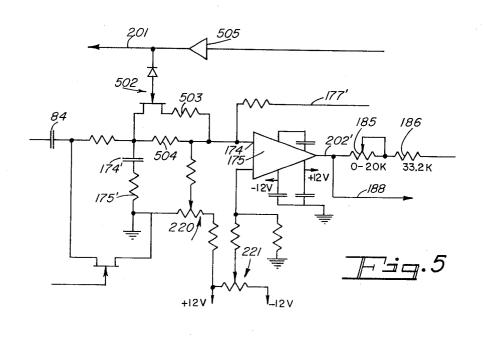
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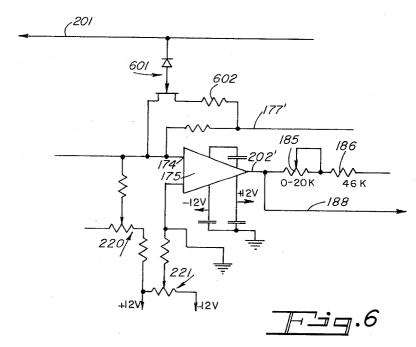


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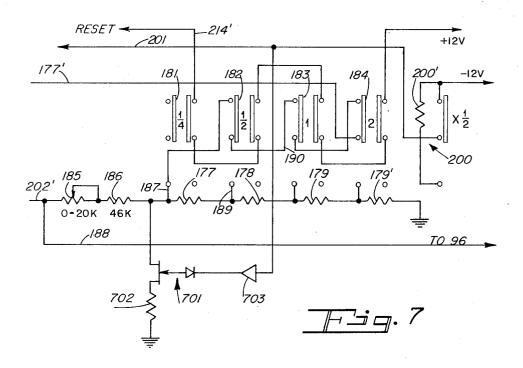


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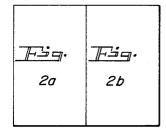




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MULTIPLE CHANNEL ELECTROCARDIOGRAPH

This is a continuation of application Ser. No. 281,074, filed Aug. 16, 1972, now abandoned.

BACKGROUND OF THE INVENTION

The present invention relates to a multi-channel electrocardiograph. More particularly, the present invention relates to automatically changing the body voltage measurements printed out by an electrocardiograph, 10 and to automatically reducing the amplitudes of the body voltage measurements taken in the vicinity of the heart.

An electrocardiograph is an instrument which records a heart cycle consisting of atrial contraction, ven- 15 tricular contraction and heart rest. The electrocardiograph typically prints out an electrocardiogram representative of electrical potentials measured between various points on the body surface during the heart cycle.

Multiple channel electrocardiographs are known in the art. For example, U.S. Pat. Nos. 2,627,267, 2,630,797 and 2,684,278 each disclose electrocardiographs wherein three different electrical potential body out on a moving chart. An advantage of simultaneously printing out a plurality of measurements is that a physician, cardiologist, or a disgnostician can obtain the information separately revealed by each of the plurality of measurements, and can also consider the plurality of 30 measurements in a correlated manner at any particular instant of time along a common time coordinate. This advantage not only minimizes the problem of correlating sequentially generated cardiograms, but also provides a plurality of cardiograms generated with assur- 35 as alternative embodiments of the invention; ance that the subject's heart condition is identical for each one of the plurality of cardiograms.

Typically, a cardiogram records (1) a plurality of inter-extremity potentials such as between the right arm and the left arm, (2) the potential differences between 40 extremities and averages of other extremities such as between the right arm and the average of the left arm and the left leg, and (3) the potential differences between each one of a plurality of chest positions in the vicinity of the heart and an average of the right arm, the left arm and the left leg potentials. Since the chest potentials are in the vicinity of the heart, the chest signals are significantly larger than the inter-extremity potentials. These high amplitude chest signals would tend to drive a recording stylus off a chart paper unless the electrocardiograph includes a compensating circuit. U.S. Pat. No. 2,684,278 discloses a manually operable means for reducing chest signals prior to their application to a recording stylus.

SUMMARY OF THE INVENTION

In accordance with the present invention, there is provided an improvement in an electrocardiograph comprising a plurality of parrallel signal processing 60 channels having means for amplifying signals, means for simultaneously applying a plurality of signals representative of different body electrical potentials including potentials in the vicinity of the heart to respective ones of the channels, and means connected to the outputs of the channels for simultaneously displaying a plurality of graphic representations of the body electrical potentials.

The improvement in accordance with the present invention comprises means for automatically changing the applying means to sequentially apply different pluralities of body electrical potential signals to the chan-5 nels. At least one of the different pluralities of the electrical potential signals are representative of potentials in the vicinity of the heart. The improvement further comprises means responsive to the changing means for automatically reducing the amplitudes of the signals representative of potentials in the vicinity of the heart.

In accordance with a specific aspect of the present invention, the changing means comprises selectively operable logic circuitry for initiating the reducing means when signals representative of electrical potentials in the vicinity of the heart are applied to each one of the plurality of electrocardiograph channels.

The invention thus provides an electrocardiograph wherein all non-chest signals can be processed and displayed with a predetermined gain, and wherein the 20 chest signals are automatically attentuated to preclude off-scale excursions of the displaying device.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1a, 1b and 1c when connected as shown in measurements are simultaneously processed and read- 25 FIG. 8 provide a diagrammatic representation of a multi-channel electrocardiograph circuit:

> FIGS. 2a and 2b when connected as shown in FIG. 9 provide a schematic representation of a portion of FIG. 1c showing multi-channel amplifier circuitry having amplitude reducing means;

FIG. 3 is a logic block diagram for actuating the components of FIGS. 1a, 1b, 1c, 2a and 2b;

FIG. 4 shows a multi-trace electrocardiogram;

FIGS. 5-7 show modifications of FIGS. 2a and 2b

FIG. 8 is a block diagram showing the orientation of FIGS. 1a, 1b and 1c; and

FIG. 9 is a block diagram showing the orientation of FIGS. 2a and 2b.

DESCRIPTION OF SPECIFIC EMBODIMENTS

With reference to FIGS. 1a to 1c, a right arm (RA) electrical potential signal is applied through an RF filter 10 to a buffer amplifier 12. The output of the buffer amplifier 12 is applied to a terminal 16 of a Wilson Network 17 by a lead 14, and to a solid state switch 20 by a lead 18. The output of the buffer amplifier 12 is also applied to another solid state switch 24 by a lead 22.

Similarly, a left arm (LA) potential signal and a left leg (LL) potential signal are applied through respective RF filters 26, 28 to buffer amplifiers 30, 32. The LA output signal from the buffer amplifier 30 is applied by a line 34 to another terminal 36 of the Wilson Network 17, and by leads 38, 40 to a solid state switch 42. The output of the buffer amplifier 30 is also passed by a lead 44 to another solid state switch 46.

In like manner, the LL output signal of the buffer amplifier 32 is applied by a lead 48 to a third terminal 50 of the Wilson Network 17, and by a lead 52 to another solid state switch 54.

Each one of the solid state switches 20, 24, 42, 46, 54, 60 thus far described are elements of a ganged network of switches 62 which are actuatable to a conductive state upon application of a signal to a lead 64. Upon actuation of the network 62 to a conductive state, LA and RA signals pass through solid state switches 46 and 20, respectively, to leads 66, 67, re-

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spectively, defining the input to Channel 1 of the electrocardiograph. Simultaneously, the LL and RA signals passed by the conductive solid state switches 54, 24 respectively, are applied to leads 68, 69, respectively, defining in input of Channel 2. Also, simultaneously, the 5 LL and LA signals applied to the solid state switches 60, 42, respectively, are applied to Channel 3 input leads 70, 71, respectively. The arm and leg signals in Channels, 1, 2 and 3 are simultaneously applied to differential amplifiers 72, 74, 76, respectively. The output 10 of the Channel 1 differential amplifier 72 is a difference signal between the LA and RA signals applied thereto which is commonly known as a lead 1 signal. The output of the Channel 2 differential amplifier 74 is known as a lead 2 signal and is indicative of the difference be- 15 tween the left leg and right arm signals applied thereto. Channel 3 differential amplifier 76 generates an output signal known as a lead 3 signal which is the difference between left leg and left arm signals applied thereto. The lead 1, 2 and 3 outputs from the differential ampli-20 fiers 72, 74, 76 are applied to modulators 78, 80, 82 which act to isolate the patient from a subsequent amplifier circuit and from the chassis of the electrocardiograph. The lead 1, 2 and 3 outputs from the modulators 78, 80, 82 are respectively applied through DC block- 25 ing capacitors 84, 86, 88 to adjustable gain amplifiers 90, 92, 94. The outputs from the adjustable gain amplifiers 90, 92, 94 are applied to power amplifiers 96, 98, 100 which in turn provide sufficient drive to respective galvanometers to move respective writing styluses 108, 110, 112. The styluses 108, 110, 112, in turn, simultaneously generates graphic displays of the lead 1, 2 and 3 signals on a moving strip chart such as shown in FIG.

At the end of a predetermined period of time, the ac- 35 tuating signal on line 64 is removed therefrom to cause the ganged switches 62 to open. Simultaneously, an actuating signal is applied to a lead 113 which acts to close another ganged network of switches 114. The lead 22 also applies a RA signal to a solid state switch 115 in the network 114. A lead 116 applies a signal representative of the average of the LA and LL signals from the Wilson Network 17 to a solid state switch 117 and the network 114. Similarly, a lead 118 applies a LA signal to a solid state switch 119, and a lead 120 applies a signal representative of the average of the RA and LL signals from the Wilson Network 17 to a solid state switch 121 in a network 114. In like manner, a lead 112 applies a LL signal to a solid state switch 123, and a lead 124 applies a signal representative of the average of the RA and LL signals from the Network 17 to a solid state switch 125 in the network 114.

When the network 114 is in a conductive state as a result of a signal being applied to the lead 113, the solid state switches 115 and 117 pass the RA signal, and the LA and LL average signal, respectively, along Channel 1 leads 66, 67 to the differential amplifier 72. The differential amplifier 72 generates at its output a signal (AVR) indicative of the difference between RA signal, and the LA and LL average signal applied thereto. Simultaneously, the solid state switches 119, 121 pass the LA signal, and the RA and LL average signal, respectively, to the Channel 2 leads 68, 69 for application to the differential amplifier 74. The differential amplifier 74 generates a signal (AVL) indicative of the difference between the LA signal, and the RA and LL average signal applied thereto. Solid state switches 123, 125

also simultaneously pass the LL signal, and the RA and LA average signal, respectively, to the Channel 3 leads 70, 71 for application to the differential amplifier 76. The differential amplifier 76 generates at its output a signal (AVF) representative of the difference between the LL signal, and the RA and LA average signal applied thereto. The AVR, AVL and AVF signals are further processed in the same manner as that described hereinabove with respect to the leads 1, 2 and 3 signals for simultaneous display on a strip chart such as shown in FIG. 4.

Chest signals V1 through V6 are generated at points extending from the fourth intercostal space at the right sternal margin in a standard pattern across chest to the left midaxillary line at a horizontal level with the fifth intercostal space at the left medclavicular line. The V1-V6 chest signals are applied through respective RF filters 130-135 to respective buffer amplifirs 136-141.

V1, V2 and V3 signals from the buffer amplifiers 136, 137, 138 are applied by leads 142, 143, 144 to solid state switches 146, 147, 148 in a ganged switch network 145. A signal representing the average of the RA, LA and LL signals is applied by a lead 152 from the Wilson Network 17 to each one of the remaining solid state switches 149, 150, 151 in the network 145.

In like manner, leads 153, 154, 155 apply the V4, V5 and V6 output signals from the buffer amplifiers 139, 140, 141 to respective ones of solid state switches 156, 157, 158 in a still another ganged switch network 159. The lead 152 also applies the signal representative of the average of the LL, RA and LA signals from the Wilson Network 17 to the remaining solid state switches 160, 161, 162 in the network 159.

After the ganged network 114 is opened by removing the signal from the lead 113, a signal is applied to a lead 163 for simultaneously changing each of the switches 146-151 in the network 145 to a conductive state. Closure of the switch network 145 applies the V1 signal and the average signal from switches 146, 149 respectively to leads 66, 67 of Channel 1 for application to the input side of the differential amplifier 72. Simultaneously, switches 147, 150 pass the V2 and average signals to leads 68, 69 of Channel 2 at the input side of the differential amplifier 74. Also simultaneously, the switchs 148, 151 apply the V3 and average signals to leads 70, 71 of Channel 3, and to the differential amplifier 76. The differential amplifiers 72, 74, 76 substract the average signals applied thereto from the respective V signals to generate at their respective outputs signals known as V1, V2 and V3. The V1, V2 and V3 signals are processed through the remainder of the circuit for simultaneous display such as shown as in FIG. 4.

After a predetermined period of time, the signal is removed from the lead 163 to cause the switches in the ganged network 145 to open, and a signal is applied to lead 164 to close the network 159. Closure of switches 156, 160 pass the V4 signal and the average signal to differential amplifier 72 in Channel 1. Simultaneously, the V5 signal and the average signal are passed by switches 157 and 161 to the input side of the differential amplifier 74 in Channel 2. Also, simultaneously, the input side of the differential amplifiers 76 in Channel 3 received the V6 signal and the average signal from switches 158, 162. The differential amplifiers 72, 74, 76 respectively generate at their output sides signals commonly known as V4, V5, and V6 signals. These sig-

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nals are processed through the remainder of the circuit for display such as shown in FIG. 4.

The circuit of FIGS. 1a to 1c also includes a defibrillation protection network. When defibrillation occurs, the input voltages applied to the RF filters 10, 26, 28, 5 130-135 tends to rise to approximately 3,000 volts. To protect the electrocardiograph in the event of defibrillation, neon lamps 165-173 are parallelly connected to the Rf filters as shown. A suitable neon lamp is one that will fire at 125 volts, ionized at approximately 80 volts. 10 During normal electrocardiograph recording, the neon lamps 165-173 are effectively open circuits. However, if the input voltages rise such as during patient defibrillation, the neon lamps 165-173 first fire, then ionize, to effectively short circuit the high potentials through 15 a lead 174 connected to the right leg of the patient and thereby protect the sensitive electrocardiograph circuits.

The circuit of FIGS. 1a to 1c also provides circuitry for reducing interference caused by common mode voltages. The RA, LA and LL output signals from the buffers 12, 30, 32 are applied to respective leads 175, 176, 177 for generating a summed signal on a lead 178. The lead 178 applies the summed signal to a RL driver circuit 179. The RL driver circuit includes a 180° phase inverting amplifier 13 and an emitter follower 15 used as a buffer driver which applies an amplified summed signal 180° out of phase with the patient common mode signals to the lead 174 connected to the patient's right leg. The out of phase signal applied to the patient's right leg tends to cancel out the common mode voltage effects on the input signals applied to the RF filters 10, 26, 28, 130–135.

FIGS. 2a and 2b shows a detailed schematic of the modulator circuits 78, 80, 82 and of the gain controlled amplifiers 90, 92, 94. As described above, the outputs of the differential amplifiers 72, 74, 76 are applied to respective modulator circuits 78, 80, 82. Since the components in each channel of FIGs. 2a and 2b contain substantially identical components and operate in a like manner, only Channel 1 will be described. However, it should be understood that Channel 2 and Channel 3 simultaneously processes signals in the same manner as described with reference to Channel 1.

The output from the differential amplifier 72 is applied to a transformer 170 in the modulator circuit 78. A high frequency (e.g. 100,000 Hertz) oscillator 170' drives the base of a transistor 171' to modulate the signal applied to the transformer 170. The output from the transformer 170 is demodulated by an amplitude detector diode 171. The output from the diode 171 is filtered by RC components 172 and the output from the RC components 172 is applied to the DC blocking capacitor 84 which forms part of a pulse shaping circuit 173. The pulse shaping circuit 173 provides an RC coupling to an input terminal 174 of a negative feedback amplifier 175. The RC coupling is modified by a capacitor 174' and a resistor 175' to flatten out the initial portion of the RC decay. The gain of the amplifier 175 is controlled by a resistor feedback network 176. The resistor feedback network 176 has selectively operable panel switches 181-184 which act to selectively apply signals developed between serially connected resistors 186, 177-179, 179' to a feedback lead 177'. The switches 181-184 are each ganged with corresponding switches in Channels 2 and 3, and are selectively operable to provide a quarter, a half, unity or double gain 6

control to the amplifier 175. Operation of the quarter switch 181 acts to remove a reset signal 12V from lead 214' which is connected to reset lead 214, and to permit passage of a signal developed between resistors 177 and 186 to a lead 187 and through the switches 182, 183, 184 in the positions shown to the feedback lead 177'. Since the amplifier 175 is a negative feedback amplifier the greater the feedback signal the less the output signal generated on a lead 202' connected to a lead 188 for application to the power amplifier 96. Operation of the switch 182 acts to maintain the other switches 181, 183 and 184 in the position shown and to pass a lower amplitude signal developed between resistors 177 and 178 to lead 189 through the switch 182, in the position not shown, a lead 190, and the switches 183 and 184 in the positions shown to the lead 177. Since the feedback signal is now less than the feedback signal when the switch 181 was depressed, the amplitude of the signal on the lead 188 will be larger. Operation of the switches 183 or 184 will further decrease the feedback signal on the lead 177 to thus further increase the amplitude of the signal applied to the power amplifier 96 by the lead 188.

In accordance with the present invention, the resistor feedback network 176 also includes a panel switch 200 which when actuated to the position not shown acts to attenuate the signal applied to the lead 188 by the amplifier 175 whenever the V1, V2 and V3 or V4, V5 and V6 signals are being processed. When the switch 200 is in the position shown, a negative signal is applied by a lead 201 and a lead 205 to ganged solid state switches 202, 203, 204 in the three channels. The negative signal applied to the solid state switches 202, 203, 204 insures that these switches are maintained in a nonconducting state. When the panel switch 200 is moved to the position not shown, a positive signal is applied by the lead 201 to the logic circuit of FIG. 3 which when either one of the V1-V3 or V4-V6 signals are being processed causes the solid state switches 202, 203 and 204 to be changed to a conductive state.

As noted above, each one of Channels 1, 2 and 3 function in the same manner. Accordingly, only the operation of Channel 1 will be described with the understanding that Channels 2 and 3 will both simultaneuosly function in the same manner. When switch 202 is actuated to a conductive state, resistors 206 and 207 are placed in parallel with the resistors 185, 186 in the feedback network to increase feedback signal applied by the lead 177 to the amplifier 175 irrespective of which one of the gain switches 181–184 are in an actuated state. Thus, the specific embodiment provides for selectively operable means for automatically reducing or attenuating the V1–V3 or V4–V6 signals to preclude off-scale excursions by the styluses 108, 110, 112.

In one embodiment, values of the resistors 206 and 207 are chosen to double the signals developed between resistors 186, 177, 178, 179 and 179', and thus halve the signals applied to the styluses 108, 110, 112. Suitable resistor values for the feedback circuit of this embodiment are shown in FIGS. 2a and 2b.

It will be noted that the output side of each one of the DC blocking capacitors 84, 86, 88 are connected to a solid state switch 210, 211, 212. Whenever a new set of body potential signals are applied to Channels 1, 2 and 3 a reset signal is applied to a lead 214 to change the solid state switches 210, 211, 212 to a conductive state. When the solid state switches 210, 211, 212 are

in a conductive state, the DC blocking capacitors 84, 86, 88 are discharged to ground. The discharge function is carried out for a relatively short period of time such as 0.5 seconds after which the reset signal is removed from the lead 214 to change the solid state 5 switches 210, 211, 212 to a non-conductive state.

It should also be noted that each one of the amplifier networks 90, 92, 94 has a reset balance resistor network 220 for insuring that the voltage at the input to the amplifier 175 is zero whenever a body potential sig- 10 nal is not applied thereto. Similarly, each one of the amplifiers has a gain balance resistor network 221 for insuring that the output of the amplifier 175 is zero whenever a body potential signal is not being processed by the amplifier.

FIG. 3 shows a logic block diagram wherein a shift register 300 is entered by a pulse generated by actuation of an automatic start button (not shown) on the panel of the electrocardiograph, and the shift register 300 applies an actuating pulse to the lead 64 (FIG. 1b) 20 The register 300 also has a MANUAL SET made for to actuate the ganged switch network 62 to a conductive state such that the signals applied thereto are fed to Channels 1, 2 and 3 to generate the leads 1, 2 and 3 signals for display such as shown in FIG. 4. After a predetermined period of time, the signal is removed 25 from the lead 64 and a signal is applied to the lead 113 (FIG. 1b) for actuation of the ganged switch network 114 to pass the signals applied thereto to the three channels for generation of the AVR, AVL and AVF signals for display such as shown in FIG. 4.

After another predetermined period of time, the shift register removes the signal from the lead 113 and applies a signal to the lead 163 (FIG. 1b) to change the ganged solid state switch network 145 to a conductive state. The ganged network 145 in a conductive state 35 passes the V1, V2, and V3 and average signals to Channels 1, 2 and 3 for display of V1, V2, V3 values such as shown in FIG. 4. Simultaneously with the application of a signal to the lead 163, a signal is also applied to a lead 307 and to one input of an OR gate 308. The output side of the OR gate 308 is connected to a small value short circuit protector resistor 308'. If the signal on the lead 201 is negative (e.g.,-12V), the ganged switches 202, 203, 204 (FIG. 2b) remain in a nonconductive state, and the V1-V3 signals are recorded 45 at the gain determined by whichever one of the panel switches 181-184 are actuated.

However, when the panel switch 200 is actuated the negative voltage (e.g.,-12V) is applied to a resistor 200' now connected to the lead 201. When the OR gate 308 has a signal thereto, it generates a positive output signal (e.g., ÷12V) and a positive signal is applied via the lead 205 to the solid state switches 202, 203, 204. The solid state switches 202, 203, 204 are thus placed in a conductive state to insert the resistors 206, 207 in each one of the channels into parallel arrangement with the resistors 185, 186 in the feedback network to thus reduce or attenuate the V1, V2 and V3 signals applied to the amplifiers 96, 98, 100.

After another predetermined period of time the shift register 300 removes the signal from the lead 163 and applies a signal to the lead 164 (FIG. 1b) to actuate the ganged switch network 159 to a conductive state, and thus apply the V4, V5, V6 and average signals to Channels 1, 2 and 3. As described in the preceeding two paragraphs, if the panel switch 200 is in the position shown, the V4-V6 signals are recorded at a gain deter-

mined by the panel switches 181-184. However, if the panel switch 200 is actuated to the position not shown, the V4-V6 recorded amplitudes are reduced by placing the resistors 206 and 207 into parallel arrangement with the resistors 185 and 186 in the feedback network.

After another predetermined period of time, the signal is removed from leads 164 and 301, and a signal is applied to a standardization mode circuit (STD) for self-calibration of the electrocardiograph.

FIG. 3 also depicts starting a clock by actuation of an automatic start button (not shown). The clock determines the predetermined time periods for applications of signals to the leads 64, 113, 163, 307, 164 and 301 and to STD. The clock also applies positive signals to the reset lead 214 (FIG. 2a) to discharge the capacitors 84, 86 and 88 prior to application of new signals to Channels 1, 2 and 3 as described hereinabove.

At the end of STD the register 300 applies a signal to HOLD of the clock and also to OFF of a chart drive. stopping the clock and maintaining a signal on anyone of the leads 64, 113, 163 and 164, or STD.

FIG. 5 shows an alternative circuit for reducing the gain of the signals representative of body potentials in the vicinity of the heart. In this circuit, a normally closed solid state switch 502 is substituted for the solid state switch 202 of FIG. 2b, and an inverting amplifier 505 is positioned in the lead 201. The resistors 206 and 207 of FIG. 2b are also removed from the circuit. In this embodiment, when the panel switch 200 is in the position shown in FIG. 2b, a negative signal (e.g., -12V.) is applied to the inverting amplifier 505 which inverts the signal to a positive signal for application to the solid state switch 502 to maintain it in a conducting state. When the solid state switch 502 is in a conducting state, a resistor 503 is placed in circuit with the resistor 504 to thus apply a relatively high signal to the input 174 of the negative feedback amplifier 175. However, when the panel switch 200 is moved to the position not shown in FIG. 2b, the resistor 200' is placed in the circuit containing the lead 201, and upon application of a pulse to the leads 307 and 301 of FIG. 3, a positive signal is applied to the inverting amplifier 505, which in turn generates at its output a negative signal to change the solid state switch 502 to a non-conductive state. When the switch 502 is changed to a non-conductive state, the resistor 503 is taken out of the circuit to thus decrease the amplitude of the signal applied to the input 174 of the negative feedback amplifier 175. In this mode, the signals representative of voltage potentials in the vicinity of the heart are decreased to preclude off-scale excursions of the styluses.

FIG. 6 shows yet another alternative embodiment. In this embodiment, a normally opened solid state switch 601 is connected to the lead 201 and to a resistor 602. The solid state switch 202 and the resistors 206 and 207 of FIG. 1b are removed from the circuit. When the switch 200 is in the position shown in FIG. 2b, the solid state switch 601 is in a non-conductive state to maintain the resistor 602 out of parallel with the resistor in the feedback line 177'. However, when the switch 200 is moved to the position not shown in FIG. 2b, the resistor 200' is placed in the circuit comprising the lead 201, and when the shift register 300 (FIG. 3) applies a signal to the leads 307 and 301, a positive signal is applied to the solid state switch 601 to change it to a conductive state. When the switch 601 is in a conductive state, the resistor 602 is placed in parallel with the resistor in the feedback line 177' to thus increase the signal fed back to the input 174 of the negative feedback amplifier 175. In this manner, the output signal applied to the lead 188 is decreased to preclude off-scale excursions of the signals representative of chest potentials.

FIG. 7 shows still another alternative embodiment wherein the solid state switch 202 and the resistors 207 and 206 of FIG. 2b are removed from the circuit, and a solid state switch 701 is interconnected between the resistors 186 and 177 and to a resistor 702 connected to ground. An inverting amplifier 703 is also connected to the diode of the solid state switch 701 and to the logic lead 201. When the switch 200 of FIG. 2b is in the position shown, the negative signal (e.g., -12V.) is applied to the inverting amplifier 703 which generates at its output a positive signal for maintaining the solid state switch 701 is a conductive state. When the switch 701 is in a conductive state, the resistor 702 is effectively placed in parallel with the resistors 177 - 179, 170, 179' to maintain the feedback signals generated on the lead 177' at a relatively low amplitude. However, when the switch 200 of FIG. 2b is moved to the position not shown, the resistor 200' is placed in the logic feedback line 201, and when the logic circuit of FIG. 3 applies a signal to either one of the leads 307 or 301, a positive signal is applied to the inverting amplifier 703 which in turn applies a negative signal to the 30 solid state switch 701. The resistor 702 is taken out of the circuit to cause the feedback signals applied to the feedback line 177' to increase and thereby decrease the amplitudes of the chest signals applied to the lead 188.

In each of the preceding embodiments, the gain controlled amplifiers 90, 92 and 94 are negative feedback inverting amplifiers. However, it is obvious to one skilled in the art that the inputs to the amplifiers 90, 92 and 94 can be reversed and the feedback line 177' 40 maintained at the 174 amplifier input such that the amplifiers operate in a negative feedback non-inverting mode. When the amplifiers 90, 92 and 94 are in a negative feedback non-inverting mode, the feedback resistor networks of FIGS. 3, 6 and 7 can be used in the manner described to control the outputs applied to the amplifiers 96, 98 and 100.

In yet another embodiment, the solid state switches 202 - 204 and the resistors 206, 207 are removed from the FIG. 2b circuit, and any one of many well known attenuating circuits can be placed at the output leads 188 to the amplifiers 96, 98 and 100. The attenuating circuits (not shown) can be readily actuatable in response to signals generated by the respective positions of the panel switch 200 and the logic of FIG. 3.

In each of the foregoing embodiments, the amplifiers 90, 92 and 94 can be a LM301A manufactured by National Semiconductor, Inc., Santa Clara, Calif.

In yet another alternative embodiment, the channel 1-3 signals can be applied to serially connected amplifiers which apply predetermined amplitude signals to the styluses 108-112. However, when signals representative of voltage potentials in the vicinity of the heart are being processed, one or more amplifiers in the serially connected amplifier circuit can be bypassed to thus reduce or attenuate the signals applied to the styluses.

Although shift registers suitable for carrying out the functions of the logic block diagram shown in FIG. 3 are wall known in the art, an improved shift register circuit suitable for carrying out the functions of FIG. 3 is 5 disclosed in U.S. patent application Ser. No. 281,075, now U.S. Pat. No. 3,753,124 for Manual Set System For Shift Register by Ernest F. J. Graetz. U.S. patent application Ser. No. 281,075 is being filed concurrently herewith (Aug. 16, 1972), and is incorporated herein 10 by reference.

It is obvious that the ECG signals processed by the foregoing embodiments can be recorded or applied to a telephone circuit for transmission and display at a remote site.

What is claimed is:

1. In an electrocardiograph comprising a plurality of parallel signal processing channels, each one of said channels including means for amplifying signals, means for simultaneously applying a plurality of signals representative of different body electrical potentials including electrical potentials in the vicinity of the heart to said channels, and means for simultaneously recording signals processed by said channels, the combination comprising:

means for automatically changing said applying means to sequentially apply different pluralities of body electrical potential signals to said channels, at least one of said different pluralities of body electrical potential signals being chest signals representative of electrical potentials in the vicinity of the heart, and

means in each one of said channels responsive to said changing means for reducing the amplitudes of the chest signals.

2. The electrocardiograph of claim 1 wherein said changing means comprises a plurality of switch networks corresponding in number to said different pluralities of body electrical potential signals, and a shift register for sequentially actuating said switch networks.

3. The electrocardiograph of claim 2 wherein said changing means further comprises a logic circuit connected to said shift register for applying a signal to said reducing means when one of the switch networks is actuated to pass chest signals to said channels.

4. The electrocardiograph of claim 1 wherein said changing means comprises a plurality of switch networks corresponding in number to said different pluralities of body electrical potential signals, means for sequentially actuating the switch networks, and means responsive to said actuating means for generating an initiation signal to said reducing means when said chest signals are applied to said channels.

5. The electrocardiograph of claim 4 wherein said reducing means comprises an amplifier circuit having an adjustable gain in each one of the channels, said amplifier circuits each including means responsive to said initiation signal for lowering the gain.

6. The electrocardiograph of claim 5 wherein each one of said amplifier circuits includes an amplifier feedback circuit comprising a plurality of serially connected resistors, and a plurality of manually operable switches for connecting points between successive ones of the resistors and a feedback amplifier input, whereby operation of one of the manually operable switches adjusts the gain to a predetermined level.

7. The electrocardiograph of claim 6 wherein said reducing means further comprises resistor means placed

in circuit in response to said initiation signal for adjusting the signal at the feedback input in a direction to reduce the amplitude of chest signals.

8. The electrocardiograph of claim 7 wherein said initiation signal places said resistor means in parallel 5 with at least the first resistor in said plurality of serially

connected resistors.

9. The electrocardiograph of claim 4 further comprising a manually operable switch for enabling said ini-