

[54] ARRANGEMENT FOR ALTERNATION OF TWO OUTPUTS IN DEPENDENCE ON A CHANGE IN THE DIRECTION OF A CURRENT APPEARING ON AN INPUT

[75] Inventor: **Sven-Eric Gote Persson**, Farsta, Sweden

[73] Assignee: **Telefonaktiebolaget L.M., Ericsson**, Stockholm, Sweden

[22] Filed: **Jan. 20, 1972**

[21] Appl. No.: **219,389**

[30] **Foreign Application Priority Data**

Jan. 29, 1971 Sweden..... 1056/71

[52] U.S. Cl..... 307/255, 307/240, 307/270, 307/311, 307/313, 307/317

[51] Int. Cl..... H03k 17/30, H03k 17/78

[58] Field of Search..... 307/241, 255, 270, 307/288, 289, 311, 313, 317; 250/211 J, 217 SS

[56] **References Cited**

UNITED STATES PATENTS

3,010,031	11/1961	Baker.....	307/288
3,413,480	11/1968	Biard et al.....	250/217 SS X
3,668,437	6/1972	Bankovic.....	307/255 X
3,278,923	10/1966	Archer.....	307/317 X

3,315,176	4/1967	Biard.....	250/217 SS X
3,042,810	7/1962	Rochelle.....	307/288 X
3,304,431	2/1967	Biard et al.....	307/311 X
3,417,249	12/1968	Akmenkalns et al.....	250/217 SS
3,492,488	1/1970	Goettelmann.....	307/311 X
3,524,986	8/1970	Harnden, Jr.....	307/311 X

OTHER PUBLICATIONS

Silicon Zener Diode and Rectifier Handbook, 2nd Edition, p. 98-100, Motorola, Inc.

Primary Examiner—John W. Huckert

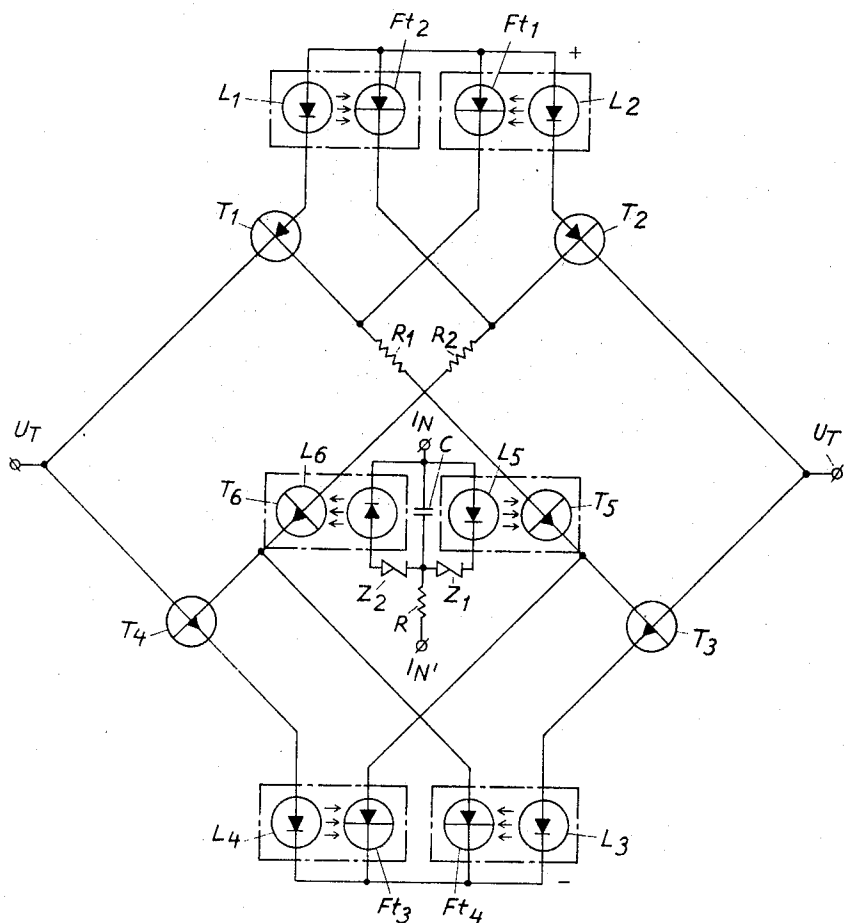
Assistant Examiner—L. N. Anagnos

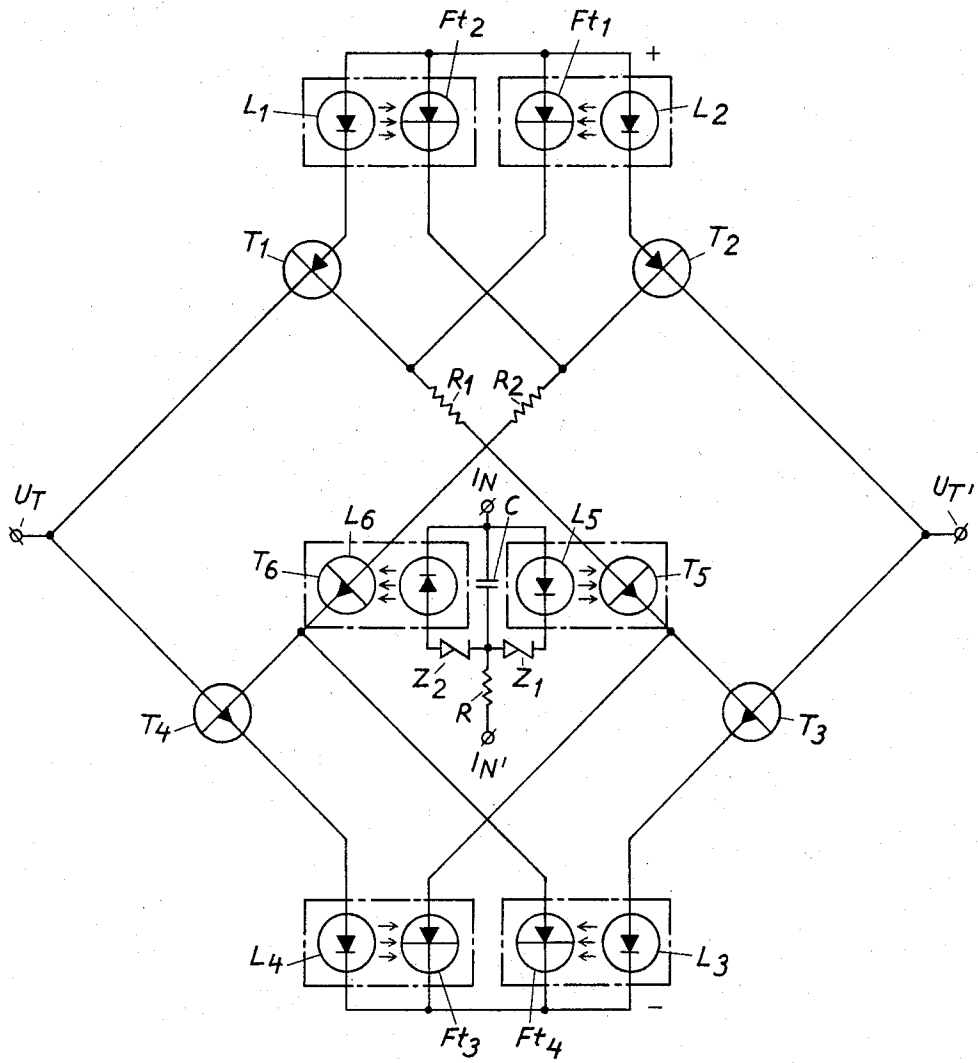
Attorney—Hane, Baxley & Spicens

[57] **ABSTRACT**

The arrangement in accordance with the present invention carries out an alternation of the polarities of two output terminals upon a change in the direction of an input current such that the polarities of the output terminals always represent the actual direction of the input current. For one direction of the current one transistor in each of two pairs of transistors is made conducting and for the other direction of said current, the other transistor in each of said pairs is made conducting, whereby in the first case a reference potential is connected to one of the output terminals and in the other case the reference potential is connected to the other of the output terminals.

5 Claims, 1 Drawing Figure





ARRANGEMENT FOR ALTERNATION OF TWO OUTPUTS IN DEPENDENCE ON A CHANGE IN THE DIRECTION OF A CURRENT APPEARING ON AN INPUT

The present invention relates to an arrangement for the alternation of two output terminals upon a change in the current direction of a signal appearing on an input terminal.

An object of the present invention is primarily to provide an alternative to polarity switching arrangements, for example, those being built up by conventional relays. In addition the arrangement according to the present invention has the advantages of a simple construction, freedom from maintenance and reliability of operation, and consequently is particularly economically competitive with arrangements known in the art.

What principally can be considered as characterizing an arrangement according to the present invention appears from the appended claims. A presently preferred embodiment which shows the significant characteristics of the invention will be described more in detail with reference to the accompanying drawing which schematically shows an arrangement according to the present invention.

In the FIGURE two switching elements in form of transistors T_1 and T_2 are shown each of which can conduct a main current in dependence of a control current. Transistor T_1 is connected between a first potential, which in the embodiment has been chosen as a positive potential and the first output terminal U_T of the two terminals U_T and $U_{T'}$ of the arrangement. Transistor T_2 is connected between said positive potential and another output terminal $U_{T'}$.

Transistors T_1 and T_2 consist of pnp-transistors. Correspondingly two further current conducting elements which can conduct a main current in dependence on a control current in the form of transistors T_3 and T_4 are connected between the outputs U_T and $U_{T'}$ respectively and a further potential, namely, the negative potential. Transistors T_3 and T_4 consist of npn-transistors.

The control circuits of transistors T_1 and T_3 are interconnected via a resistor R_1 and the same is the case with the control circuits of transistor T_2 and T_4 which are interconnected through a resistor R_2 . A third main current in dependence on a control current conducting element is included in the control circuits and comprises transistors T_5 and T_6 , transistor T_5 being associated with transistors T_1 and T_3 and transistor T_6 being associated with transistors T_2 and T_4 . The control circuits of transistors T_5 and T_6 are connected to the input of the arrangement through luminescent or light-emitting diodes L_5 and L_6 , which are connected in anti-parallel to a conductor (not shown), in which the arrangement is assumed to be inserted via the terminals I_N and $I_{N'}$. The luminescent diodes are thereby connected to the conductor through zener diodes Z_1 and Z_2 , the zener voltages of which are assumed to be below the inverse voltages of the luminescent diodes L_5 and L_6 . The incoming signal through the conductor to the arrangement is applied to the same through a timing circuit indicated by a capacitor C and a resistor R .

If it is assumed that an incoming signal appears on the connecting point I_N through the conductor, then the luminescent diode L_5 will be activated in case the value of the incoming signal exceeds the value of the zener voltage of the zener diode Z_1 . Transistor T_5 will conse-

quently be activated thus starting to conduct a collector-emitter-current. The result is that the pnp-transistor T_1 as well as the npn-transistor T_3 will saturate. The saturation of transistor T_1 results in that the one output U_T is connected to the positive potential, while the saturation of transistor T_3 results in that the second output $U_{T'}$ is connected to the negative potential.

Upon a reversed current direction when the incoming signal instead is connected through the terminal $I_{N'}$ the activation of transistor T_5 ceases, while instead transistor T_6 is activated. Thus transistor T_6 starts to conduct thus causing the transistors T_2 and T_4 to saturate. through transistor T_4 the negative potential will be connected to the first output U_T and through transistor T_2 the positive potential will be connected to the other output $U_{T'}$. As long as this incoming signal is present the arrangement will accordingly maintain both of its output terminals at these potentials which is not the case during the absence of said signal. By an appropriate choice of the zener voltages for the zener diodes Z_1 and Z_2 , as well as a suitable dimensioning of the timing circuit represented by the capacitor C and resistor R it is assured that the transistor pairs T_1, T_3 and T_2, T_4 are not conducting at the same time. Hence, a short circuit between the elements T_1, T_4 and T_2, T_3 respectively, is avoided.

In the Figure there is also shown how blocking circuits can be arranged for the nonconducting element pair T_1, T_3 and T_2, T_4 respectively, the blocking circuits of which are initiated by the conducting element pair. The blocking circuits include the luminescent diode, L_1-L_4 which operate together with the associated photo-transistors $F_{T_1}-F_{T_4}$. Each of the transistors T_1-T_4 is thereby connected in series with one of the luminescent diodes L_1-L_4 . When an element pair, T_1, T_3 for instance, is conducting, luminescent diodes L_1 and L_3 are ignited. These luminescent diodes activate associated photo transistors F_{T_2} and F_{T_4} . The activated photo transistors F_{T_2} and F_{T_4} are so connected in order to block the base current (the same as the collector-emitter-current of transistor T_6) of the other element pair which in the chosen case consist of transistors T_2, T_4 . Correspondingly the element pair T_2, T_4 blocks the current of the element pair T_1, T_3 .

The invention is not limited to the embodiments, which have been described above. For example, the construction of the input circuits can be varied widely without departing from the basic idea of the invention. The above-described circuits for blocking the nonconducting element pair can be omitted and, in case they are used, the luminescent diodes can be replaced with, for instance, lamps. The invention is not either limited to the chosen combination of pnp- and npn-transistors or to shown potentials. It is also possible to replace the transistors with other switching elements showing the necessary characteristics.

We claim:

1. An electronic switching arrangement having an input terminal and two output terminals for the alternation of the polarity of the output terminals upon a change in the direction of a current passing through said input terminal and maintaining said polarity of the output terminals only as long as said current flows comprising:

a first pair of switching elements, each of said switching elements having a control circuit for causing

3

4

said switching elements to conduct a first main current;

a second pair of switching elements, each of said switching elements having a control circuit for causing said switching elements to conduct a second main current;

a first source of potential;

means for connecting each of the switching elements of said first pair of switching elements between said first source of potential and one of said output terminals associated with the respective switching element;

a second source of potential;

means for connecting each of the switching elements of said second pair of switching elements between said second source of potential and one of said output terminals associated with the respective switching element;

a further pair of switching elements, each of said switching elements having a first main electrode, a second main electrode and light sensitive control means;

means for connecting said main electrodes of the respective switching elements of said further pair of switching elements to the control circuit of the first switching element of said first pair of switching elements and the second switching element of said second pair of switching elements and the second switching element of said first pair of switching elements and the first switching element of said second pair of switching elements, respectively,

light emitting unidirectional conducting means for generating and transmitting light signals to the light sensitive control means of said further pair of switching elements in dependence on the direction of the current flowing through said input terminal,

so that the respective pairs of switching elements are light activated in dependence on the direction of the current flowing through said input terminal, and

first and second blocking circuit means connected to said first and second source of potential, respectively, said blocking circuits allowing potential to pass to the control circuit of the first switching element of the first pair of switching elements when the second element of the same pair is conducting and to the control circuit of the second switching element of the second pair of switching elements when the first switching element of the second pair of switching elements is conducting, and vice versa.

2. An arrangement as claimed in claim 8, wherein the switching elements in each of said first and second pairs of switching elements consist of transistors.

3. An arrangement as claimed in claim 9, wherein said light emitting unidirectional conducting means consist of luminescent diodes and said further switching elements consist of photo transistors, said luminescent diodes being optically coupled to each of said photo transistors forming said further switching element pair.

4. An arrangement as claimed in claim 9, wherein said light emitting unidirectional conducting means coupled to said further switching element pair are connected in antiparallel to the input terminal.

5. An arrangement as claimed in claim 11, wherein said luminescent diodes are connected to the input terminal via zener diodes, the zener voltage of which being less than the reverse voltage of said luminescent diodes whereby a threshold value for the activation of the arrangement by the current received at said input terminal is obtained.

* * * * *

40

45

50

55

60

65