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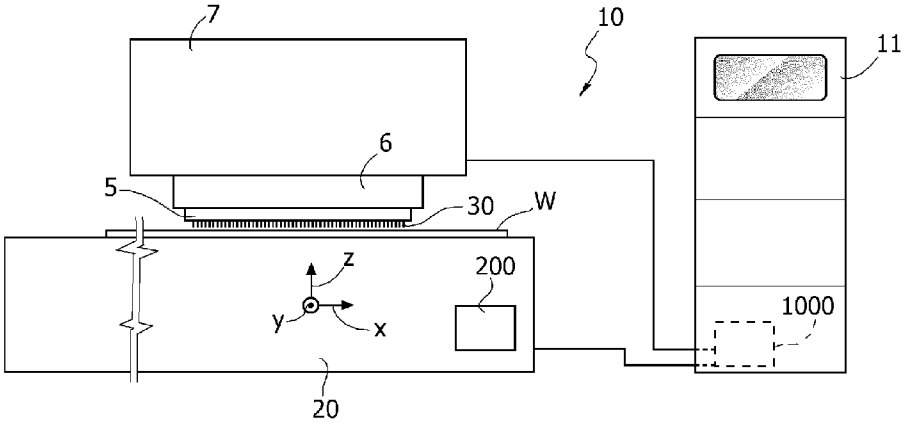
(54) **Title:** TESTING DEVICES UNDER TEST BY AN AUTOMATIC TEST APPARATUS HAVING A MULTISITE PROBE CARD



(57) **Abstract:** Automated tester apparatus (10) for testing devices (W) includes a probe card (5) to establish contact (30) with the devices under test (W) under the control of prober modules. The probe card (5) is a multisite probe card including a plurality of sites exposed to site malfunctioning. The apparatus includes: - a malfunction detection module for checking malfunctioning of the sites in the multisite probe card (5), - a control module (1000) configured, if at least one site in the multisite probe card (5) is found to be malfunctioning, for continuing testing by using sites of the probe card (5) that are correctly operating. Continuing testing typically includes: - i) re-testing a set of devices that were already tested by using the site in the probe card (5) found to be malfunctioning; and - ii) testing at least one new set of devices in a lot of devices under test (W) not previously tested.

WO 2007/090465 A1

TESTING DEVICES UNDER TEST BY AN AUTOMATIC TEST APPARATUS HAVING A MULTISITE PROBE CARD

Field of the invention

The invention relates to test techniques and arrangements. The invention was developed with specific attention paid to the possible application to semiconductor test apparatus, also referred to as Automated Test Equipment (ATE).

Description of the related art

Integrated Circuits (IC) need to be tested to ensure proper operation. During testing, an IC, as a device under test (DUT), is exposed to stimulus data signals of an Automatic Test Equipment (ATE). The IC transmits corresponding response data back to the ATE. The ATE measures, processes and usually compares this response data with expected responses. The ATE usually performs these tasks according to a device-specific test program. ATE's with decentralized resources based on a per-pin architecture are known, wherein during test, each pin of a plurality of pins of the DUT is connected to one ATE pin electronic. The per-pin architecture generally enables high performance and scalability.

Examples of ATE's with per-pin architecture are the Agilent 83000 (83K) and 93000 (93K) families of Semiconductor Test Systems by Agilent Technologies. Details of those families are disclosed e.g. in EP-A-0 859 318, EP-A-0 864 977, EP-A-0 886 214, EP-A-0 882 991, US-A-5 499 248, US-A-5 453 995 and US Patent Application Serial No.11/176,928.

Essentially, testing apparatus of the kind considered in the foregoing is made up by a series of tester channels, acting each as an independent tester machine. For instance, in an Agilent 93000 (93K) testing apparatus, the tester channels are grouped in boards, each board containing 16 channels, and in the standard 93K configuration, the Agilent tester machine in question includes up to 1024 tester channels.

Such testing apparatus (ATE) usually performs wafer tests by using a so-called probe card, that is by contacting the DUT pads with the needles of a probe card connected to the tester "pogo pins" and channels. Usually, a probe card is made up of several sites, with each site in the multi-site card having needles carrying electrical signals to one DUT.

Each site can test one DUT, and the tester apparatus is configured to run test programs in parallel, by testing several DUTs at the same time. This approach is called multisite testing. Specifically, an Agilent 93000 Tester is configured to perform a series of tests on a semiconductor DUT, and these tests are grouped into test programs. When a test program is running, the tester sends/receives electrical signals to/from each DUT.

Summary

Site dependency is a problem commonly encountered during multisite testing on ATE. Site dependency is found to occur when one or more sites on a probe card, also referred to as prober card, perform worse than the others.

When one or more sites on a probe card of an ATE start malfunctioning, one or more tests in the test program start failing (wrongly) on "good" DUTs that are tested on a malfunctioning site. If the problem is not promptly detected, the ATE continues testing by rejecting (i.e. "killing") good DUTs, which is currently referred to as an "overkill" problem.

Usually the problem is found out by operators or device engineers by checking the wafer maps produced by the tester or device datalogs. Once the site dependency problem is detected, the ATE is stopped and then the failing probe card is replaced with a good one, and the ATE machine is started again.

This situation is a source of major drawbacks and problems.

In the first place, detecting site dependency by analyzing wafer maps or datalogs is far from easy.

If one or more sites of the probe card are not operating properly, and this situation goes undetected, any good DUT tested on the sites involved in malfuctioning can be - wrongly - rejected, which may lead to a severe yield loss, and a throughput decrease thus increasing the so-called COT (Cost Of Test).

In fact, during the tester undetected malfunctioning, many good DUTs will go lost (i.e. be discarded with no reason), possibly due to only one or a few tests in the test program failing at the malfunctioning site.

Once the defective probe card site is detected, the tester is stopped before completing the lot test in progress, and the tester is put at standby – i.e. kept in a non-operative condition - while waiting for a new good probe card to be substituted for the malfunctioning one.

During this time frame, the tester machine is not operative, which in turn may result in production being stopped. Such a situation adversely affects

throughput and cost of testing, and goes on top of direct money losses due to keeping the test cell on hold.

To sum up, site dependency problems as discussed in the foregoing have a strong negative impact on:

- the production throughput/yield: if site dependency is not detected, many good DUTs are wrongly rejected ("overkill");

- the time/cost of testing: when site dependency is detected, the tester is stopped while waiting for the probe card to be replaced, and the wafer found to be allegedly defective has to be tested again;

- ATE test cell (tester + probe card + prober) re1iability e.g. in terms of MTBF (Mean Time Between Failure), which reliability is decreased by the site dependency problem.

The object of the invention is thus to provide an improved ATE arrangement which may be exempt from the problems/drawbacks outlined in the foregoing.

According to the present invention, that object is achieved by means of a system having the features set forth in the claims that follow. The invention also relates to a corresponding method as well as a related computer program product, loadable in the memory of at least one computer and including software code portions for performing the steps of the method of the invention when the product is run on a computer. As used herein, reference to such a computer program product is intended to be equivalent to reference to a computer-readable medium containing instructions for controlling a computer system to coordinate the performance of the method of the invention. Reference to "at least one computer" is evidently intended to highlight the possibility for the present invention to be implemented in a distributed/ modular fashion.

The claims are an integral part of the disclosure of the invention provided herein.

A preferred embodiment of the arrangement described herein is thus an improved ATE (Automated Test Equipment) including a multisite testing feature adapted to automatically detect and repair site dependency problems as typically occurring in multi-site testing of semiconductor wafers/devices.

Such a multi-site testing feature will reduce the cost of testing by improving i) yield gain, ii) reliability, iii) throughput, and iv) MTBF performance of the associated ATE.

Brief description of the drawings

The invention will now be described, by way of example only, with reference to the enclosed representations, wherein:

- figure 1 is a schematic view of test apparatus adapted to incorporate the arrangement described therein,
- figure 2 is a functional block diagram of apparatus as shown in figure 1,
- figure 3 is a flow chart representative of possible operation of semiconductor testing apparatus as described herein, and
- figures 4 to 6 are schematic representations of operation of semiconductor testing apparatus as described herein.

In the following description, numerous specific details are given to provide a thorough understanding of embodiments of the invention. One skilled in the relevant art will recognize, however, that the invention can be practised without one or more the specific details or with other methods, components, materials and so on.

In other instances, well-known structures, materials, or operations are not shown or described in detail to avoid obscuring aspects of the invention.

Reference throughout this specification to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Thus, the appearances of the phrases "in one embodiment" or "in an embodiment" in various places throughout this specification are not necessary or referring to the same embodiment. Furthermore, the particular features, structures, or characteristic may be combined in any suitable manner in one or more embodiments.

Figure 1 is a schematic view of apparatus 10 for use in testing Integrated Circuits (IC's) in order to ensure proper operation thereof. During testing, an IC, as a device under test (DUT), is exposed to stimulus data signals generated by the Automatic Test Equipment (ATE) 10. The IC transmits corresponding response data back to the ATE. The ATE measures, processes and usually compares this response data with expected responses. The ATE usually performs these tasks according to a device-specific test program.

In a typical exemplary arrangement the equipment (ATE) 10 includes a so-called prober 20 onto which the Devices Under Test (DUTs) are arranged.

Specifically, in the exemplary arrangement considered herein, the DUTs being tested are in the form of e.g. a semiconductor wafer W including a (large)

plurality of "naked" chips still to be separated from each other (e.g. so-called "dice").

The DUTs include contact points or pads typically arranged in arrays usually comprised of a matrix of contact points/pads. Each such array of contact points/pads is mirrored by a corresponding array of contact pins or needles 30 carried by a so-called multisite probe card 5.

When the probe card 5 is in facing relationship with the DUTs, the needles 30 of the probe card 5 establish electrical contact between the DUT points/pads and a so-called pogo tower 6 carried by a test head 7.

Usually, a probe card 5 is made up of several sites, with each site in the card having needles 30 adapted to carry electrical signals to/from one DUT.

Each site can test one DUT, and the tester apparatus 10 is configured to run test programs in parallel, by testing several DUTs at the same time. This approach is called multisite testing.

To that effect, the prober 20 has associated motor means 200 – of a known type – configured to move in three directions along three axes x, y, and z. The prober 20 (and, consequently the DUTs i.e. the wafer W carried therein) can thus be displaced to selectively bring the contact points/pads of a given DUT in contact with the needles 30 of a specific site of the probe card 5. Movement of the prober 20 is effected in steps under the control of prober programs (prober modules) hosted in a main tester unit 1000 located in the prober 20 and/or in a central shelf 11 where user interfaces (GUIs and the like) are arranged.

Essentially, the prober programs dictate the trajectories to be followed (in the horizontal xy plane) by the prober 20 in order to ensure that the DUTs to be tested are exposed in subsequent steps to the needles 30 of one of the sites of the probe card 5. Movement in the vertical direction (z axis) corresponds to:

- the prober 20 being lifted in order to bring the contact points/pads of a set of DUTs to be tested in contact with the needles 30 of the probe card 5; and

- the prober 20 being subsequently lowered in order to disengage the contact points/pads of the DUTs tested from the needles 30 of the probe card 5 in order to permit unimpeded displacement of the prober 20 in the xy plane.

As indicated, testers such as an Agilent 93000 Tester are configured to perform a series of tests on a semiconductor DUTs, and these tests are grouped into test programs. When a test program is running, the tester sends/receives electrical signals to/from each DUT.

During the test process, the connections established via the multi-site probe card 5, the pogo tower 6 and the test head 7 are used by the main tester unit 1000

to apply to the DUTs signals in the form of "stimuli" and to collect corresponding "reactions" or "responses" from the circuits. Absence of these reactions/responses, or the reactions/responses collected being different from those expected, is generally construed as evidence of fault or malfunctioning of the DUT tested.

All of the foregoing corresponds to principles of operation that are well known in the art, thus making it unnecessary to provide a more detailed description herein.

As discussed in the introductory portion of this description, the arrangement described herein aims at dispensing with the negative effects of site dependency problems.

Essentially, the arrangement described herein achieves that result by:

- automatically locating any malfunctioning site in the probe card 5;

- replacing the current prober program with a new program that no longer uses the malfunctioning site for re-testing those DUTs in a wafer that were found to be defective (most probably in an erroneous way, as test failure was presumably due to malfunctioning of the relative site in the probe card 5); and

- using a new prober program (typically different from the prober program used for re-testing), which again does not use the malfunctioning site for testing new coming wafers: in that way new coming wafers are tested by using the new function not affected by site dependency.

Replacement of prober programs can easily take place "on-the-fly", without discontinuing operation of the tester apparatus 10.

Of course, the tester apparatus 10 may be configured for issuing (e.g. via the main tester unit 1000) an automatic alert signal (alarm or mail) to advise the supervising personnel about the probe card problem encountered, so that the malfunctioning probe card may be replaced.

While waiting for the new probe card that should replace (usually only after the wafer lot currently under test has been completely tested) the malfunctioning card, operation of the ATE 10 will not have to be discontinued, while no good DUTs will be erroneously discarded.

Operation of the arrangement described herein will now be described by referring to operation within the context of operation of an Agilent 93000 (93K) testing apparatus as described e.g. in the related Agilent 93000 Manual.

Specifically, the block 100 in the flow chart of figure 3 corresponds to the condition where a WAFER TEST step has been completed in an Agilent 93000 (93K) testing apparatus in connection with a given DUT. As detailed in the Agilent

93000 Manual, this corresponds to a situation where a Wafer Datalog containing Test Data has been generated.

After each WAFER TEST step is completed, a diagnostic software using a PERL (Practical Extraction and Reporting Language) script is run in a step 102. The PERL script checks out the datalog generated at the end of the wafer test step 100.

The PERL script will find out ma1functioning sites in the probe card 5 by detecting any site dependency problem occurring therein. Such as script will be able to run on a server (e.g. in the main tester unit 1000) in a background mode, with no impact on test time.

In the exemplary embodiment considered herein, the MAIN program (PGM) of the PERL script executes the following functions:

&input_data1og(); this function takes a Wafer Datalog as input to the script

&parse_datalog(); this function parses the data in the datalog creating a matrix with :

X-AXIS → Failing Tests in the Test Program (Bins) Y-AXIS → PROBE CARD sites.

For example, if one refers to:

l) a Test program of N tests, each one tagged with a Bin (Binl, …, BinN)

2)an ATE Tester using a PROBE CARD with M sites,

the parse_datalog will extract from the ATE Tester Datalog a matrix of the type:

	Bin1	Bin2	Bin3	BinN
Site 1	40	3	16	7
Site 2	40	4	20	4
Site 3	38	6	21	3
….	…	…	…	…
Site M	56	2	22	4

&calc_datalog(); based on the results in the matrix, this function finds out if a specific bin (i.e. the test related to this bin) is “overfailing” on a specific site of the probe card 5 considered.

The “overfailing” site can be located e.g. as follows.

For each bin, the system calculates the average number of failing bins for the various sites. For example, for Bin1 in the table above, this will yield:

AVERAGE_NUMBER_OF_FAILING_BIN1 = (40 + 40 + 38 + ... +S6)/M

For each Bin (Bin_i) and each site (Site_j) the system compares the number of fails for that bin on that site with the AVERAGE_NUMBER_OF_FAILING_BIN_j.

If no overfailing is found (negative outcome of a step 104) the system reaches a waiting state (step 106) for a new wafer end test (step 100).

If, conversely, the step 104 yields a positive outcome, for example because Bin_i is found to be "overfailing", namely found to fail a given threshold amount (e.g. 30%) above the average on Site_j, in a step 108 the PERL script will issue a warning like the following.

!!!! WARNING - SITE DEPENDENCY !!!!
site $i fails more than 30% respect average for binj !!!!

This warning can be displayed (e.g on a screen associated with the main tester unit 1000) either immediately, or, possibly, once testing of the lot of wafers currently under test has been completed, to advise operators that the probe card 5 is malfunctioning and needs to be replaced.

Upon detecting the occurrence of site dependency, in a step 110, the system will replace (typically "on-the–fly") the prober program currently used with a new prober program chosen from a previously created set of prober programs in order to test again the wafer currently under test with probe card sites found to be fully operative.

At this stage, only those DUTs (e.g. chips in the wafer-map WM) that have been wrongly tested by the malfunctioning sites are re-tested.

After completing re-testing, in a step 112 any new coming wafers are tested with a new prober program (chosen from the previous set of prober programs). Again, this new prober program used in the step 112 for testing the new coming wafers (which is usually different from the new prober program used for re-testing purposes in the step 110) does not use any malfunctioning sites.

After performing the step 112, the system finally evolves towards the step 106.

The action of replacing a prober program currently used with a new prober program can be easily implemented "on-the–fly" e.g. by using the ATE 93K HP SmarTest module already equipping current Agilent 93000 (93K) testing apparatus. Specifically, the prober function can be controlled through the ATE 93k HP SmarTest module in order to perform the actions performed during the steps 110 and 112 - namely i) re-testing those wafers that were previously tested

wrongly (step 110) and ii) testing any new coming wafers (step 112)using only the operating sites of the probe card 5.

In order to perform the steps 110 and 112, a dedicated set of prober programs is prepared and stored in the ATE, namely in the prober unit 20. In that way a different prober program can be used any time a new wafer is subjected to testing.

These several prober programs would depend on the probe card type (i.e. probe card size and number of probe card sites). In this set of prober programs the ATE 10 will select the probers to perform (depending on what probe card sites are failing) re-testing of those wafers that were previously tested wrongly and testing any new coming wafers.

The basic concept underlying the approach just described can easily exemplified by referring, by way of example, to a simple probe card including four sites, e.g.

1	2
3	4

Those of skill in the art will appreciate that referring to a probe card 5 including four sites (designated 1, 2, 3, and 4) is dictated by the sole sake of simplicity and ease of understanding the invention. Probe cards 5 including e.g. 128 or 256 sites are in common use in the art, especially for testing semiconductor memories.

The four-site probe card 5 considered here by way of example can test in parallel four DUTs for each step of the prober 20.

For instance, figure 4 shows the possible application of such a four-site probe card 5 to testing a 148 chip wafer in 40 steps. In these 40 steps, the four-site probe card considered here would be able to test 40 x 4 = 160 chips/DUTs. However, the exemplary case is considered here where the chips/DUTs included in the wafer map WM to be tested are less than 160, namely only those 148 chips/DUTs indicated in cross-hatching in figure 4.

Suppose that, while the prober program performs such a wafer test in 40 steps (with all the sites 1,2,3,4 of the probe card 5 enabled), a malfunction occurs at site 1 of the probe card 5 so that, at the end of the wafer test, e.g. 37 chips are indicated to be defective, these 37 allegedly defective chips corresponding to the dark areas in figure 5.

As explained, these chips may not be defective at all, and the indication of defect is highly likely to be related only to wrong testing due to the malfunctioning of site 1.

Stated otherwise, the chips having no dark areas in figure 5 have been correctly tested, while the dark areas correspond to 37 wrongly tested chips that must be re-tested with a different prober program.

As described in the foregoing, at the end of wafer test (step 100 figure 3) the PERL script detects the malfunctioning site 1.

At that point, the wafer currently under test is re-tested using a prober program (chosen from the dedicated set) in which only one site of the probe card 5 is used. This may be e.g. site 2, which enabled for re-testing, that is:

X	2
X	X

where the symbol X denotes a disabled site in the probe card 5.

The prober program is thus switched on-the-fly from a 40 step program into a 37 step program wherein the 37 chips that previously were wrongly tested due to malfunctioning of site 1 in the probe card 5 will now be tested using e.g. site 2 only.

Any new incoming wafers will be tested using a prober program (from the dedicated set) adapted to operate with the probe card 5 having site 1 disabled.

By still referring to the four site probe card 5 considered as a simple example, the new prober program may be one adapted to operate with the probe card 5 having sites 1 and 2 disabled while sites 3 and 4 are enabled, namely

X	X
3	4

The resulting site configuration is shown in figure 6 with reference to the same wafer map M shown in figure 4. The steps included in the prober program using the probe card 5 with four sites operating includes 40 steps. One would thus expect that the new prober program used for testing new incoming wafers using the probe card 5 with only two sites (e.g. 3 and 4) should include 40 x 2 steps. Figure 6 shows that only 78 steps are in fact needed, since positioning of the prober 20 in the two other steps would correspond to placing the sites 3 and 4 out of the wafer map WM shown in cross-hatching.

Obviously both prober programs used during re-testing (step 110) and testing new wafers (step 112) could be optimized to use different numbers of activate probe card sites.

For instance, the prober program used for testing new wafers (step 112) could be optimized to use three sites instead of two: two sites being referred to is primarily intended to make this explanation simpler to understand.

Being able to use three sites instead of two may appear to represent a significant advantage in terms of reducing the number of steps in the (new) prober program. However, as indicated in the foregoing, probe cards 5 including e.g. 128 or 256 sites are in common use in the art, especially for testing semiconductor memories. In that case, the prober program used for testing new wafers using all the sites in the probe card 5 save those included in a row or column where a malfunctioning site was located (this one being notionally a sub-optimal arrangement) hardly penalizes tester operation in terms of steps, thus making site optimization hardly attractive.

It will be appreciated that the ATE arrangement described herein effectively overcomes at least three basic disadvantages encountered in prior art arrangements affected by site dependency problems and likely to adversely affecting the cost of testing and reliability of an ATE/test-cell, namely:

- undetected site dependency, which may lead to good DUTs being wrongly rejected ("overkill"), thus unduly reducing production yield;

- the tester equipment having to be stopped when site dependency is detected while the defective probe card is replaced, wafer testing (and possibly production) also having to be stopped ;

- the test cell equipment (tester + probe card + prober) MTBF being decreased by site dependency problems.

The arrangement described herein thus provides a truly self-detecting, self-repairing, notionally never-stopping automated equipment for testing semiconductor wafers/devices.

Essentially, the arrangement described herein is in a position to:

- automatically self-detect any site dependency problems, and

- provide a temporary remedy to any site dependency problem possibly detected without discontinuing the wafer lot test by: i) re-testing the wrongly "bad-binned" chips, and ii) testing any new wafers via on-the-fly modified prober programs that do not use the probe card sites found to be malfunctioning.

Consequently, without prejudice to the underlying principles of the invention, the details and the embodiments may vary, even appreciably, with reference to

what has been described by way of example only, without departing from the scope of the invention as defined by the annexed claims.

CLAIMS

1. A method of testing devices (W) by an automated tester apparatus (10) comprising at least one multisite probe card (5) to establish contact (30) with said devices under test (W) under the control of at least one prober module, said multisite probe card (5) including a plurality of sites (1, 2, 3, 4), comprising:

- checking (102) for malfunctioning said sites in said multisite probe card (5),

- if at least one of said sites (1) in said multisite probe card (5) is found to be malfunctioning, continuing (110, 112) said testing under the control of at least one new prober module different from said at least one prober module, wherein said at least one new prober module uses at least one site (2 ; 3, 4) in said multisite probe card (5) different from said at least one site found to be malfunctioning.

2. The method of claim 1, wherein continuing said testing includes re-testing (110), under the control of a new prober module different from said at least one prober module, a set of devices under test (W) that were already tested by using said at least one site (1) of said multisite probe card (5) found to be malfunctioning.

3. The method of claim 1 or 2, wherein continuing said testing includes testing (112), under the control of a respective new prober module different from said at least one prober module, at least one new set of devices in a lot of devices under test (W) not previously tested.

4. The method of claim 2 or 3, wherein said new prober module and said respective new prober module are different prober modules in a set of new prober modules that use sites of said multisite probe card (5) different from said at least one site found to be malfunctioning.

5. The method of claim 2 or 4, wherein said new prober module used for re-testing (110) a set of devices that were already tested uses a single site (2) in said multisite probe card (5) different from said at least one site found to be malfunctioning.

6. The method of claim 3 or 4, wherein said respective new prober module used for testing (112) at least one new set of devices not previously tested uses a plurality of sites (3, 4) in said multisite probe card (5) different from said at least one site found to be malfunctioning.

7. The method of claim 1 or any one of the above claims, wherein it includes on-the-fly switching control to said at least one new prober module without interrupting said testing.

8. The method of claim 1 or any one of the above claims, wherein it includes checking (102) said malfunctioning of any of said sites in said multisite probe card (5) via a Practical Extraction and Reporting Language (PERL) script.

9. The method of claim 1 or any one of the above claims, wherein it includes checking (102) said malfunctioning by:

- parsing the testing results from said sites (1, 2, 3, 4) in said multisite probe card (5) in the form of failing test results versus probe card sites, and
- locating said at least one site (1) found to be malfunctioning as an overfailing site in said testing results.

10. The method of claim 9, comprising:

- calculating the average number of failing test results for said plurality of sites (1, 2, 3, 4) in said multisite probe card (5),
- locating said at least one overfailing site (1) as a site overfailing of a given threshold amount above the average number of failing test results.

11. An Automated test apparatus (10) for testing devices (W), the apparatus (10) comprising at least one multisite probe card (5) to establish contact (30) with said devices under test (W) under the control of at least one prober module, said multisite probe card (5) including a plurality of sites (1, 2, 3, 4), comprising:

- a detection module (102) for checking for malfunctioning said sites in said multisite probe card (5), and
- a control module (1000) configured, if at least one of said sites (1) in said multisite probe card (5) is found to be malfunctioning, for continuing (110, 112) said testing under the control of at least one new prober module different from said at least one prober module, wherein said at least one new prober module uses at least one site (2 ; 3, 4) in said multisite probe card (5) different from said at least one site found to be malfunctioning.

12. The apparatus of claim 11, comprising a new prober module different from said at least one prober module to continue said testing by re-testing (110) a

set of devices under test (W) that were already tested by using said at least one site (1) of said multisite probe card (5) found to be malfunctioning.

13. The apparatus of claim 11 or 12, comprising a respective new prober module different from said at least one prober module to continue said testing by testing (112) at least one new set of devices in a lot of devices under test (W) not previously tested.

14. The apparatus of claim 12 or claim 13, wherein said new prober module and said respective new prober module are different prober modules selected from a set of new prober modules using sites in said multisite probe card (5) different from said at least one site found to be malfunctioning.

15. The apparatus of any one of claims 12 to 14, wherein said new prober module used for re-testing (110) a set of devices that were already tested uses a single site (2) in said multisite probe card (5) different from said at least one site found to be malfunctioning.

16. The apparatus of any one of claims 13 or 14, wherein said respective new prober module used for testing (112) at least one new set of devices not previously tested uses a plurality of sites (3, 4) in said multisite probe card (5) different from said at least one site found to be malfunctioning.

17. The apparatus of any one of claims 11 to 16, wherein said control module (1000) is configured for on-the-fly switching control to said at least one new prober module without interrupting said testing.

18. The apparatus of any one of claims 11 to 17, wherein said detection module (102) includes a Practical Extraction and Reporting Language (PERL) script.

19. The apparatus of any one of claims 11 to 18, wherein said detection module (102) is configured for checking (102) for said malfunctioning by:

- parsing the testing results from said sites (1, 2, 3, 4) in said multisite probe card (5) in the form of failing test results versus probe card sites, and
- locating said at least one site (1) found to be malfunctioning as an overfailing site in said testing results.

20. The apparatus of claim 19, wherein said detection module (102) is configured for checking said malfunctioning by:

- calculating the average number of failing test results for said plurality of sites (1, 2, 3, 4) in said multisite probe card (5),
- locating said at least one overfailing site (1) as a site overfailing of a given threshold amount above the average number of failing test results.

21. A computer program product, loadable into the memory of at least one computer and including software code portions for performing the method of any one of claims 1 to 10.

WO 2007/090465 PCT/EP2006/050745

FIG. 1

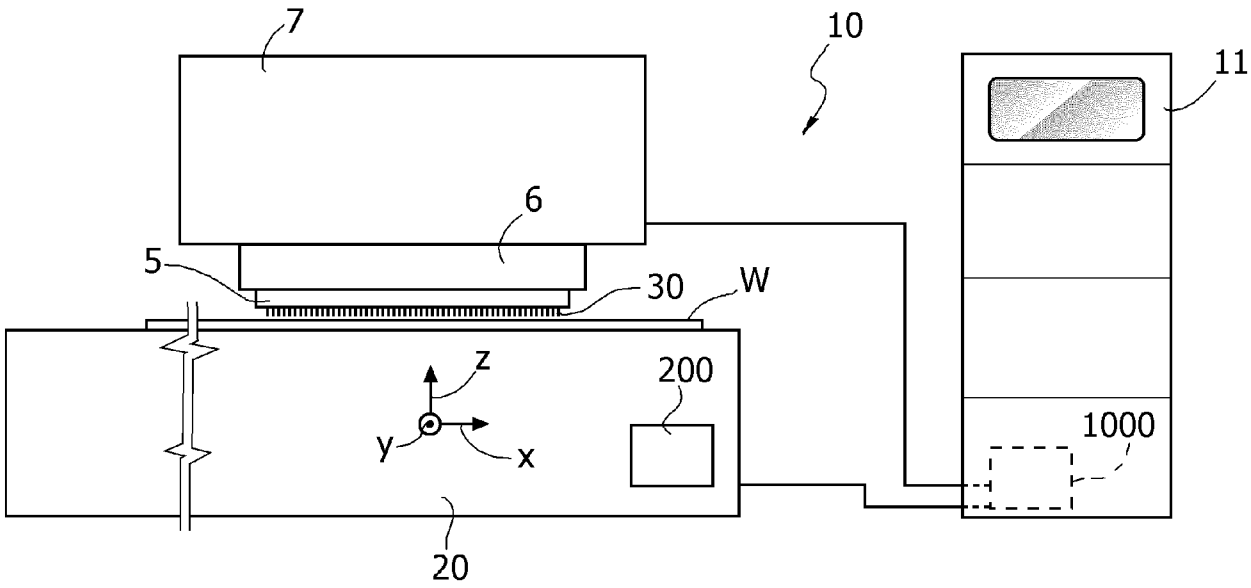


FIG. 2

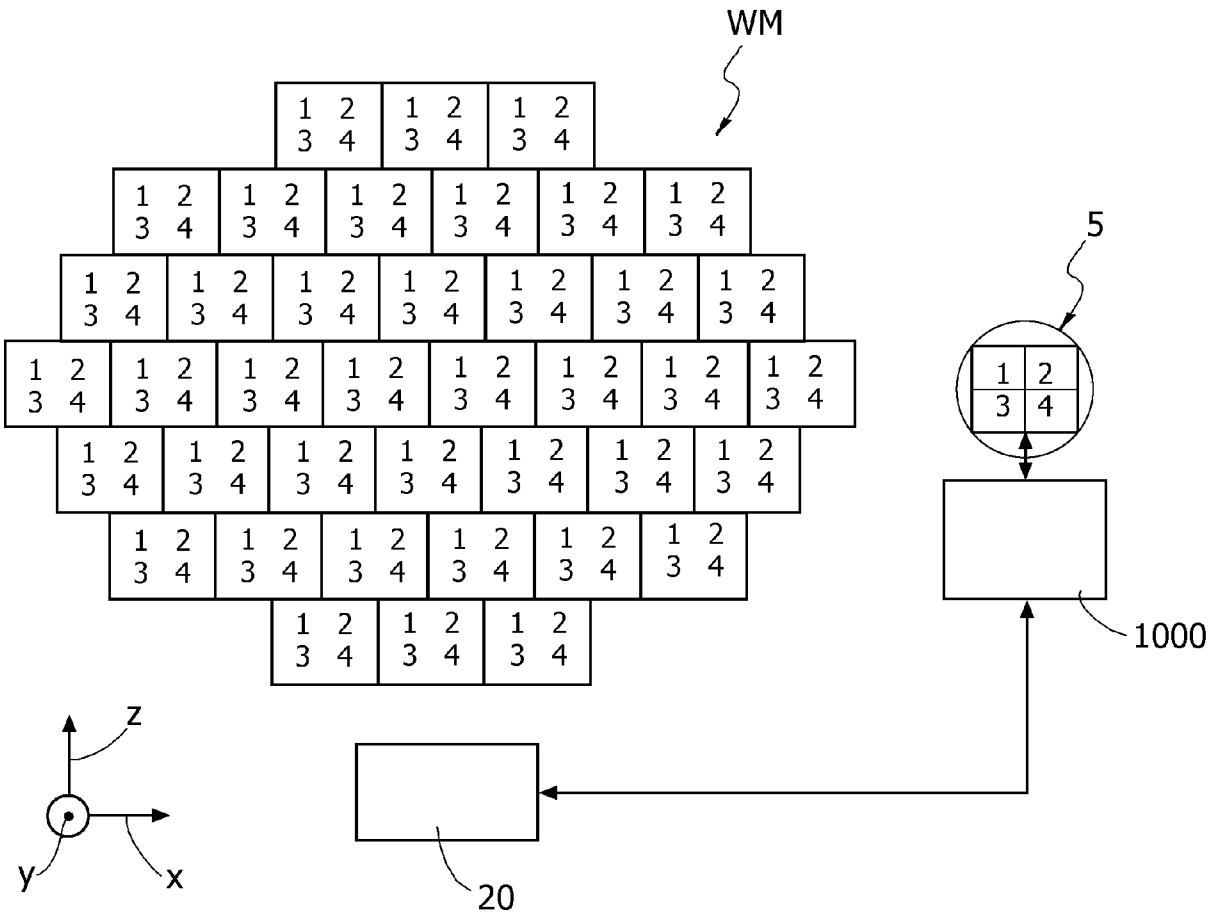


FIG. 3

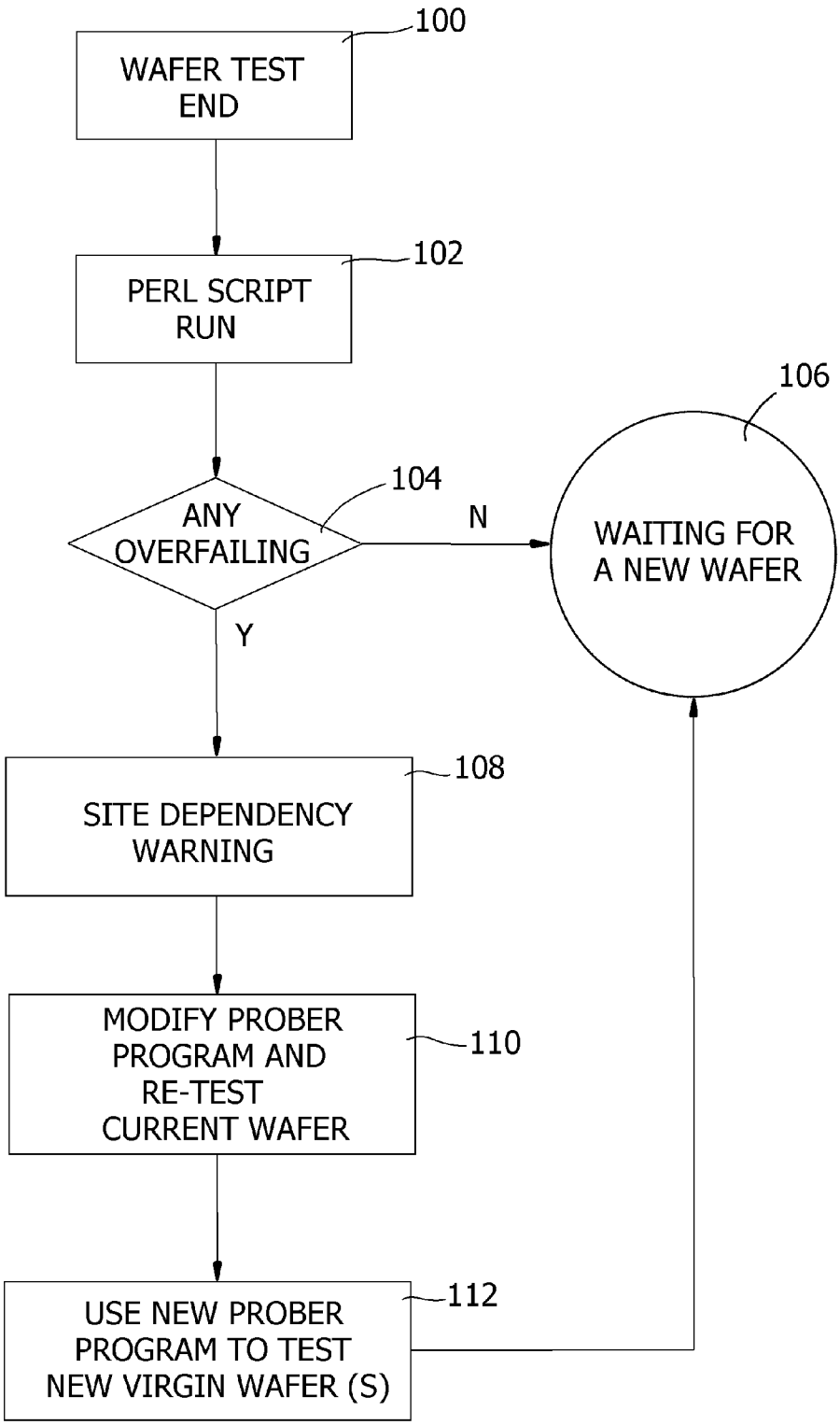

100
WAFER TEST END
102
PERL SCRIPT RUN
104
ANY OVERFAILING
N
106
WAITING FOR A NEW WAFER
Y
108
SITE DEPENDENCY WARNING
MODIFY PROBER PROGRAM AND RE-TEST CURRENT WAFER
110
USE NEW PROBER PROGRAM TO TEST NEW VIRGIN WAFER (S)
112

FIG. 4

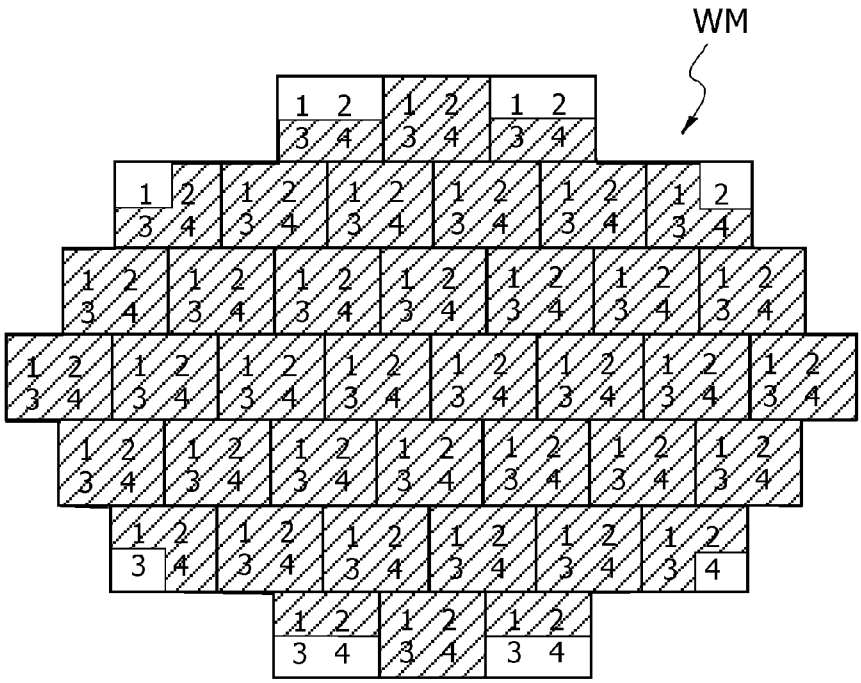


FIG. 5

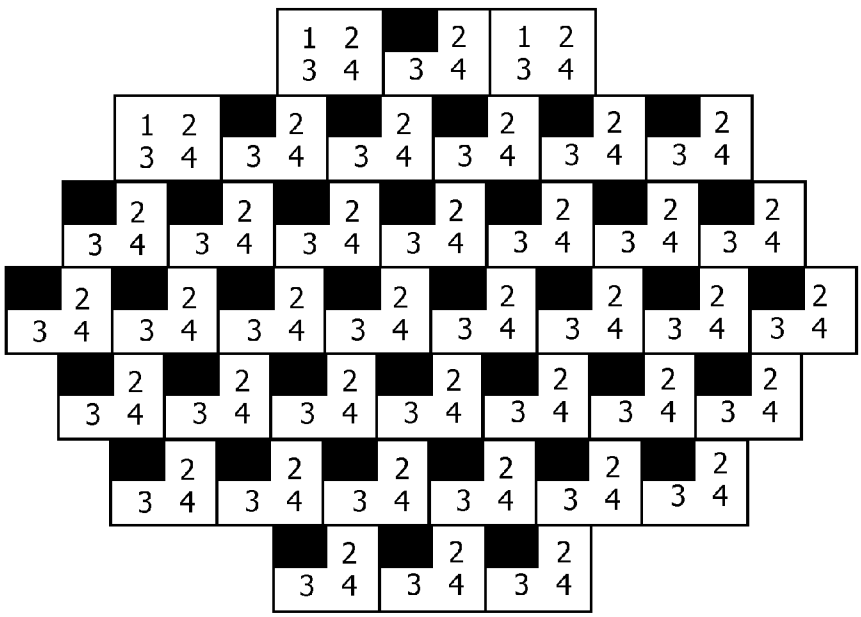
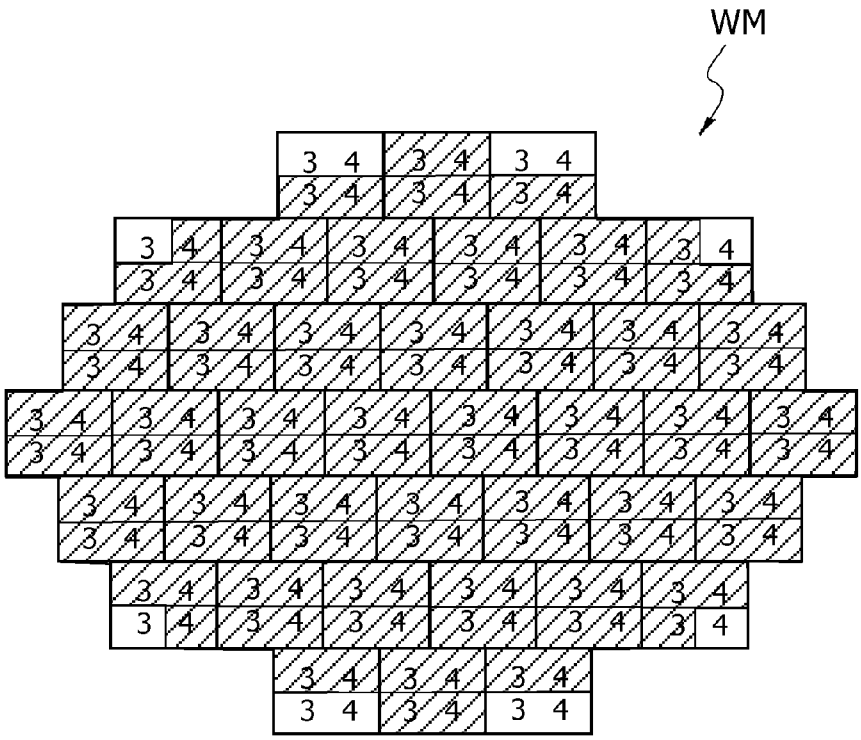


FIG. 6



INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2006/050745

A. CLASSIFICATION OF SUBJECT MATTER
INV. G01R31/28

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 639 777 A (HEWLETT PACKARD CO [US]) 22 February 1995 (1995-02-22) figures 16,22 column 1, line 1 - line 26 column 5, line 1 - line 29 column 6, line 30 - line 38 column 8, line 43 - column 9, line 2 column 19, line 31 - line 44 column 25, line 20 - column 26, line 3	1-21
A	US 5 726 920 A (CHEN SUSAN HSUCHING [US] ET AL) 10 March 1998 (1998-03-10) figures 1A-4,6 column 3, line 55 - column 4, line 35 column 6, line 12 - line 49 column 9, line 6 - column 10, line 8 column 12, line 66 - column 16, line 48 column 27, line 25 - line 61	1-21

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
10 October 2006	18/10/2006

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Höller, Helmut

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2006/050745

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	MILL-JER WANG ET AL: "Yield improvement by test error cancellation" TEST SYMPOSIUM, 1996., PROCEEDINGS OF THE FIFTH ASIAN HSINCHU, TAIWAN 20-22 NOV. 1996, LOS ALAMITOS, CA, USA,IEEE COMPUT. SOC, US, 20 November 1996 (1996-11-20), pages 258-262, XP010200240 ISBN: 0-8186-7478-4 the whole document	1-21
A	US 2005/237073 A1 (MILLER CHARLES A [US] ET AL) 27 October 2005 (2005-10-27) figures 1,6,7 paragraph [0048]	1-21
A	US 6 741 085 B1 (KHANDROS IGOR Y [US] ET AL) 25 May 2004 (2004-05-25) figures 5B,9A-9D column 5, line 49 - line 58 column 40, line 39 - line 50	1-21
A	US 6 113 646 A (HOLDEN BLANE [US]) 5 September 2000 (2000-09-05) figures 2,5A,5B column 1, line 24 - line 59 column 3, line 22 - line 25 column 6, line 5 - line 41	1,5,11, 15,21

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2006/050745

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0639777 A	22-02-1995	JP 7063788 A US 5491427 A	10-03-1995 13-02-1996
US 5726920 A	10-03-1998	NONE	
US 2005237073 A1	27-10-2005	WO 2005103740 A2	03-11-2005
US 6741085 B1	25-05-2004	NONE	
US 6113646 A	05-09-2000	NONE	