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**H04N 5/04**

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UK CL (Edition L ) **H4P PSEX PSX PT , H4R RLS RPNR**
INT CL$^5$ **H04N 5/04 7/13**
**ONLINE DATABASES : WPI.**

(54) **A combined digital video/audio synchroniser**

(57) A data synchroniser 1 used to synchronise an incoming video/audio signal SDI with a reference clock SPG is adapted for operation with a signal in which the numbers of audio samples in a sequence of fields differ to accommodate the fact that the number of audio samples per field is not an integer. During a resynchronisation operation in which a frame is dropped or repeated, the frame is selected in such a manner as to ensure that the number of audio samples in each outputted sequence of fields is constant, Figs. 3a, 3b, (not shown).

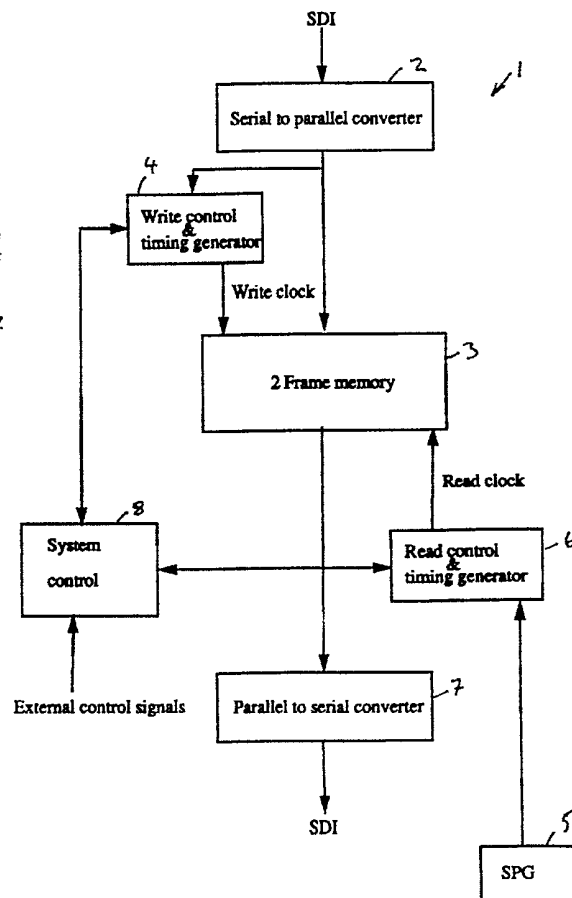The synchroniser operates with both 625 line 50Hz and 525 line 59.94Hz video systems.

FIG 1

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SDI

↓
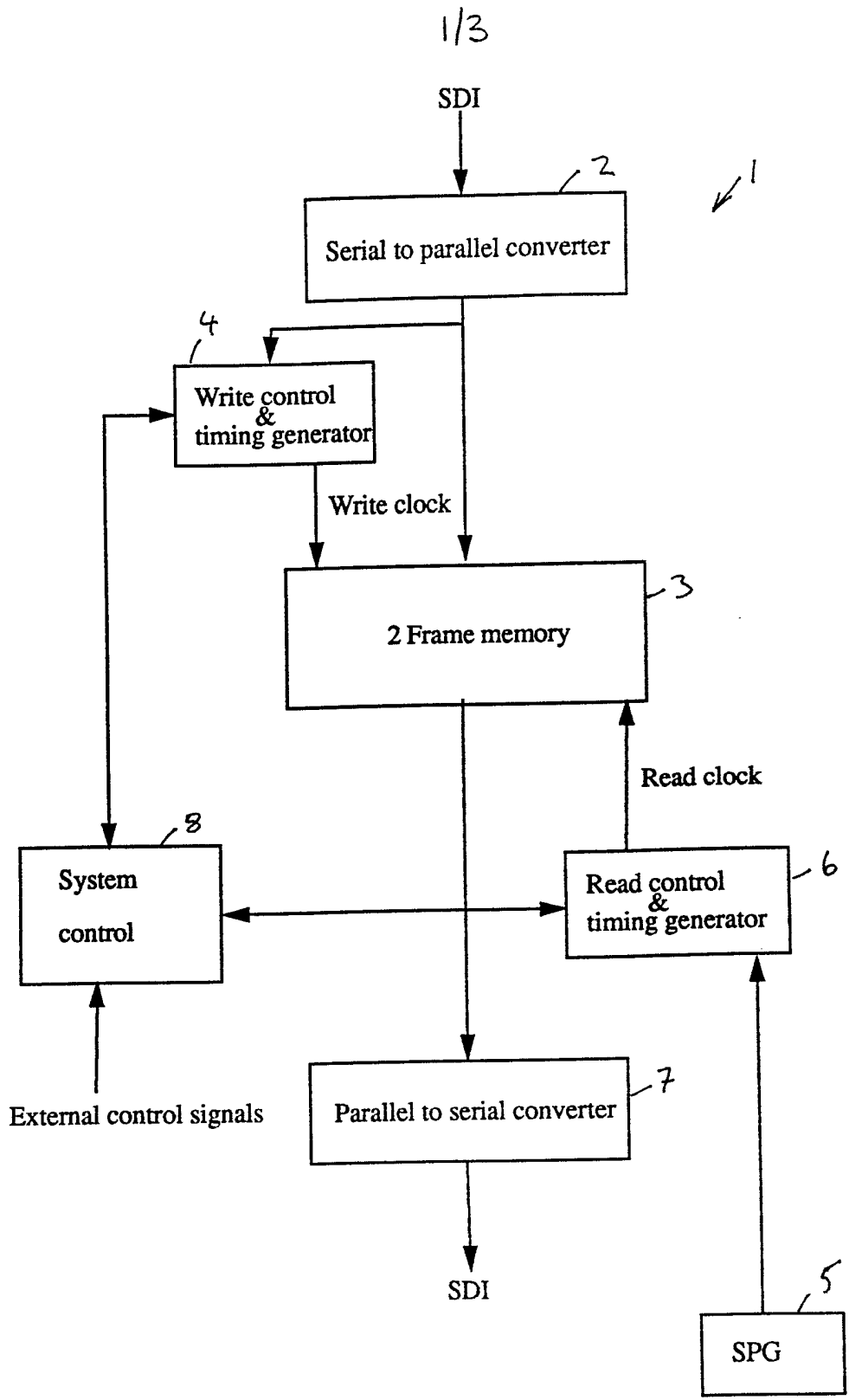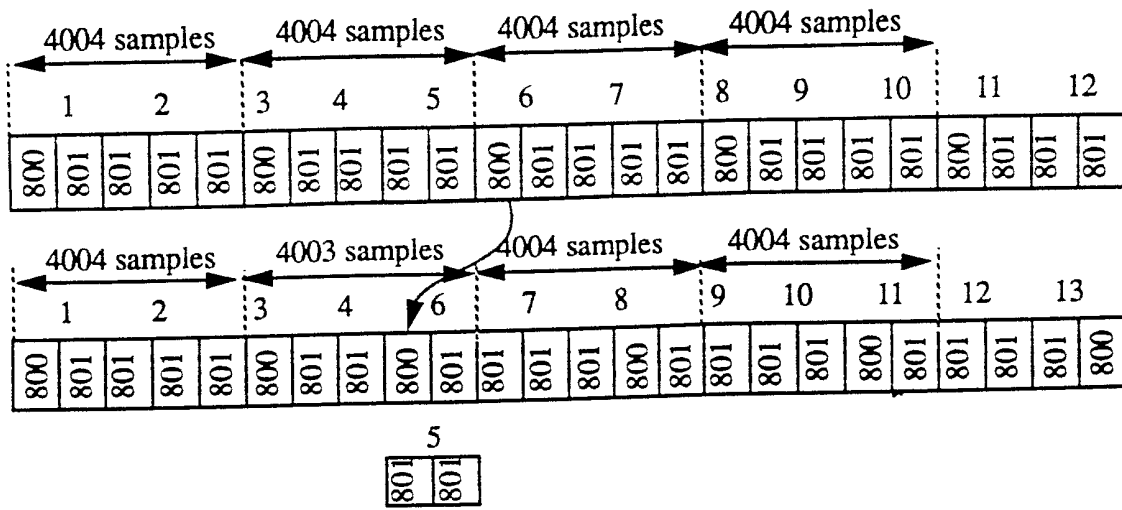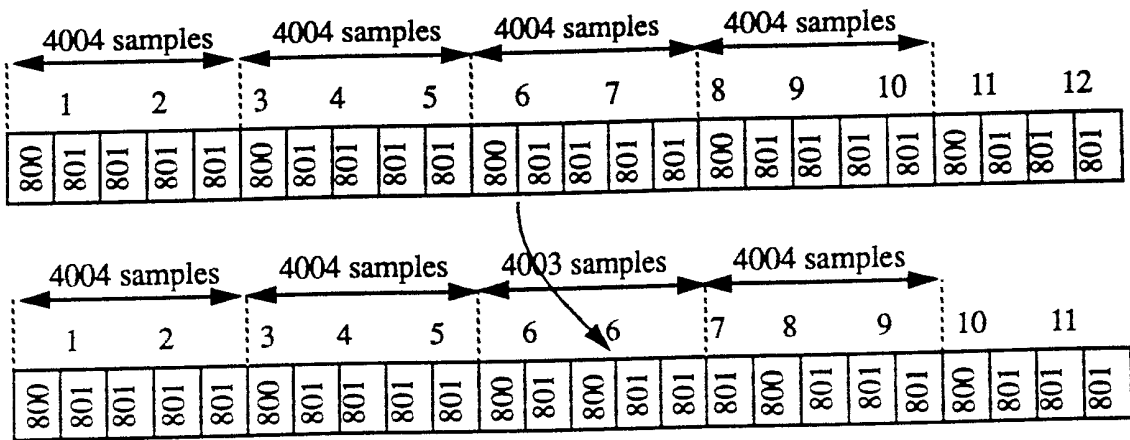
Serial to parallel converter  2

Write control
&
timing generator  4

Write clock

2 Frame memory  3

Read clock

System
control  8

Read control
&
timing generator  6

External control signals

Parallel to serial converter  7

SDI

SPG  5

FIG 1

4004 samples · 4004 samples · 4004 samples · 4004 samples

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |

800 801 801 801 801 800 801 801 801 801 800 801 801 801 801 800 801 801 801 801 800 801 801 801

4004 samples · 4003 samples · 4004 samples · 4004 samples

| 1 | 2 | 3 | 4 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |

800 801 801 801 801 800 801 801 800 801 801 801 801 800 801 801 801 801 800 801 801 801 801 800

5

801 801

FRAME 5 DROPPED

**FIG 2a**

4004 samples · 4004 samples · 4004 samples · 4004 samples

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |

800 801 801 801 801 800 801 801 801 801 800 801 801 801 801 800 801 801 801 801 800 801 801 801

4004 samples · 4004 samples · 4003 samples · 4004 samples

| 1 | 2 | 3 | 4 | 5 | 6 | 6 | 7 | 8 | 9 | 10 | 11 |

800 801 801 801 801 800 801 801 801 801 800 801 800 801 801 801 800 801 801 801 800 801 801 801

FRAME 6 REPEATED

**FIG 2b**

4004 samples   4004 samples   4004 samples   4004 samples

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |

| 800 | 801 | 801 | 801 | 801 | 800 | 801 | 801 | 801 | 801 | 800 | 801 | 801 | 801 | 801 | 800 | 801 | 801 | 801 | 801 | 800 | 801 | 801 | 801 |

4004 samples   4004 samples   4004 samples   4004 samples

| 1 | 2 | 3 | 4 | 5 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |

| 800 | 801 | 801 | 801 | 801 | 800 | 801 | 801 | 801 | 801 | 801 | 801 | 801 | 800 | 801 | 801 | 801 | 801 | 800 | 801 | 801 | 801 | 801 | 800 |

6

| 800 | 801 |

FRAME 6 DROPPED

FIG 3a

4004 samples   4004 samples   4004 samples   4004 samples

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |

| 800 | 801 | 801 | 801 | 801 | 800 | 801 | 801 | 801 | 801 | 800 | 801 | 801 | 801 | 801 | 800 | 801 | 801 | 801 | 801 | 800 | 801 | 801 | 801 |

4004 samples   4004 samples   4004 samples   4004 samples

| 1 | 2 | 3 | 4 | 5 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |

| 800 | 801 | 801 | 801 | 801 | 800 | 801 | 801 | 801 | 801 | 801 | 801 | 801 | 800 | 801 | 801 | 801 | 801 | 800 | 801 | 801 | 801 | 801 | 800 |

5

| 801 | 801 |

FRAME 5 REPEATED

FIG 3b

1

## A COMBINED DIGITAL VIDEO/AUDIO SYNCHRONISER

The present invention relates to a combined digital video/audio synchroniser and a method of
5    synchronization.

A synchroniser may be used to phase and frequency lock two independent video/audio programme sources having the audio data embedded in the horizontal/vertical timing intervals of the video signal. The independent sources,
10    although being of nominally the same frequency, have an arbitrary phase relationship which is subject to continual change. This results in the synchroniser memory being filled up faster than it can be emptied or vice versa until it becomes necessary for information to be dropped or
15    repeated so as to realign the sources, resynchronise the data from the synchronise memory, by adjusting the read address. This information may be dropped or repeated as whole frames each comprising two video fields.

In a combined digital video and digital audio
20    synchroniser having a Serial Digital Interface (SDI), the audio data may be embedded in the horizontal and vertical timing interval of the video signal. A device of this type may treat the audio and video information as a single entity thus providing a "DATA" synchroniser. The advantages of
25    this arrangement are that perfect "lip-sync" between the video and audio is maintained and no audio signal degradation occurs in the synchroniser during normal operation.

With 525-line 59.94Hz systems which use 48KHz
30    audio sampling, a problem arises from the fact that there is a non-integral number of audio samples per field of the video signal. This requires that when the audio and video samples are combined, the same number of audio samples cannot be interleaved with each field, and instead, over a
35    sequence of fields, (five with 525 line, 59.94Hz systems

with 48KHz sampling) that does correspond with a whole number of audio samples, different number of audio samples are interleaved with the video data to make up the total. This, however, presents a problem in operation of the
5   synchroniser, namely that the pattern of numbers of audio samples from the synchroniser output in a field sequence which is in progress when a resynchronisation operation occurs may not be correct.

        According to the present invention, there is
10   provided a synchroniser for a combined video and audio signal, which is in a format in which blocks of audio sample data are time-interleaved with the samples of successive fields of video sample data in a repeating sequence of numbers of audio samples per field of video samples, such
15   that the number of audio samples in at least one of the fields of the sequence differ from that in the remainder of the fields of the sequence and that, prior to passage through the synchroniser, the total number of audio samples in each sequence is constant, comprising:

20        a)   a memory buffer having a capacity for storing at least two frames' worth of video and audio samples;

        b)   write- and read-control circuits for writing incoming video/audio data sample to the memory buffer and reading the buffered data therefrom at rates which are
25   respectively synchronised in frequency and phase with the incoming data and with a reference clock signal;

        c)   resynchronising means for resynchronising the data read from the buffer by adjusting the sequence of read and/or write addresses used for reading and/or writing data
30   from and to the memory buffer to avoid overflow or underflow of the buffer contents, so selectively repeating or dropping frames of the stored data; wherein

        d)   the resynchronising means is operative, when resynchronisation is required, to select the timing of the
35   resynchronisation operation and adjustment of the read

address, and thereby the frame to be repeated or dropped, such that the total number of audio samples in the sequence of fields being read from the memory buffer when the resynchronisation is carried out is unchanged.

5       Preferably when a resynchronisation operation is carried out, the read address is adjusted by an amount corresponding to an integral number of frames' worth of data stored in the memory buffer.

        Preferably, where a frame is to be dropped, the
10   frame selected for dropping is one having a total number of samples which is equal to the total number of samples in the first two fields of the sequence and where a frame is repeated, the frame to be repeated is one having a total number of samples which is equal to the total number of
15   samples in the last two fields of the sequence.

        Preferably the sequence inputted to the synchroniser has a first field of a first predetermined number of audio samples, a second field of a second predetermined number of audio samples and a last field of
20   said second predetermined number of audio samples and when a resynchronisation operation is required, if a frame is to be dropped, the frame selected for dropping is one which comprises both a field of said first number of samples and a field of said second number of samples and, if a frame is to
25   be repeated, the frame selected for repeating comprises two fields of said second number of audio samples.

        Preferably the apparatus is adapted for use with a signal in which said sequence comprises a field of 800 samples and 4 fields of 801 samples, per channel of audio.
30   Typically, there may be up to four channels of audio in the signal.

        The invention will be more clearly understood from the following description given by way of example only with reference to the accompanying drawings in which:
35       Figure 1 illustrates a block diagram of a

synchroniser according to an embodiment of the present invention.

Figure 2(a) and (b) illustrate a frame sequence before and after a frame is respectively dropped or repeated

5   according to a previous arrangement.

Figures 3(a) and (b) illustrate a frame sequence before and after a frame is respectively dropped or repeated, according to the embodiment of Figure 1.

Figure 1 illustrates in block diagram form

10   synchronizer 1 to which, for instance, a signal from a video source may be input for synchronization with other signals which are to be broadcast from a main transmitter.

In this embodiment, the input signal, in the form of a serial video/audio data bit stream is inputted to the

15   serial to parallel converter 2 and resulting parallel video/audio data, eg. 10 bit video/audio data at 27M samples/sec, is transferred to a 2-frame memory 3 under the control of the write control circuit 4 which derives from the serial to parallel converter 2 a write clock signal

20   which clocks the writing of data to the 2-frame memory 3.

The 2-frame memory 3 acts as a circular buffer from which the stored data may be read out at a different rate from that at which it is written.

A reference signal synchronised with the

25   horizontal and vertical synchronizing signals of the signal with which the input signal is to be synchronised, is input from a signal pulse generator (SPG) 5 to a read control circuit 6.  The read control circuit 6 provides a read clock signal to the 2-frame memory 3 so as to control the rate at

30   which data is read from the 2-frame memory and this data can then pass to the parallel to serial converter 7 for reconversion to a 270 Mbit/second bit serial stream output from the synchroniser.

A system control circuit 8 is also provided which

35   accepts external control signals to control the synchroniser

and controls the operation of the other elements of the synchroniser.

As discussed above, at some point in the normal operation of the combined digital video/audio synchroniser,
5  it will become necessary to drop or repeat information to maintain synchronisation. This is due to the limited size of data storage inside the synchroniser and its inability to indefinitely buffer the continually changing phase relationship between input and output signals.
10  With 625 line 50Hz video systems, the audio sample rate of 48KHz when locked to a video reference, produces an integer number of audio samples per frame (1920 samples). When the synchroniser drops or repeats frames of information, an integer number of audio samples will be
15  effected by the frame disturbance.

However, because the field rate of the 525 line system is not exactly 60Hz, but 59.94Hz, there will not be an integer number of 48KHz audio samples in a frame period, but 1601.6 samples.
20  Assuming the audio sample rate is locked to the video reference, when audio sample data is time compressed to fit in the horizontal timing interval of the video signal for the SDI, a five field audio sample sequence is produced. Over five fields of 59.94Hz video there will be an integer
25  number of 48KHz audio samples (4004). These samples are preferably distributed within the SDI such that, for each audio channel, there is one field containing 800 samples followed by four fields of 801 samples each and this sequence is illustrated in Figures 2 and 3.
30  However, when the synchroniser drops or repeats information, if the synchroniser were not operated according to the present invention it would be possible to disturb this five field sequence so that a sequence of 4003 audio samples is produced.
35  For instance, referring to Figure 2(a), if frame 5

is dropped, frame 6 replaces it in its block thereby creating a block of only 4003 audio samples rather than the usual 4004. Similarly, referring to Figure 2(b), repetition of frame 6 will result in a block of 4003 samples. As discussed above, this can give rise to unacceptable disturbances in the audio signal. More particularly, when the audio data is separated from the SDI and time expanded as may be required prior to transmission or recording, a sequence of 4003 samples will result in single sample audio disturbance and the risk of propagating errors into downstream equipment.

In the preferred embodiment of the present invention as illustrated in Figure 1, the system control circuit 8 is arranged to control the read control circuit 6 so as to drop or repeat a frame in such a manner as to maintain the block of five fields at 4004 samples.

Referring to Figure 3(a), if frame 6 is dropped, it will be noted that the resulting block is still of 4004 samples. Thus, in the example of the 4004 sample sequence, when the synchroniser must drop a frame of information, if a frame boundary containing one field of 800 samples, plus one field of 801 samples is dropped, then the 4004 samples five field sequence is maintained.

Similarly from Figure 3(b) if frame 5 is repeated, the resulting block is of 4004 samples and thus when the synchroniser must repeat a frame of information, choosing a frame boundary that contains two fields of 801 samples each will similarly preserve the sample count.

In accordance with the invention, the system controller 8 selects which frame to drop or to repeat when performing a resynchronising operation, so as to maintain the number of output audio samples in each five field sequence of blocks constant at 4004. Repeating a frame effectively retards the incoming sequence by two fields whereas dropping a frame effectively advances the incoming

sequence by two fields. In order to maintain the value 4004, therefore, the frame to be repeated is selected by the system controller 8 to be one which has the same number of audio samples as the last two fields in a sequence, whereas

5     the frame which is selected for dropping has a total number of audio samples equal to that in the first two fields of the sequence.

In view of the above, by the particular choice of frame boundaries used during resynchronisation, the

10    synchronizer may drop or repeat a frame without disrupting the 4004 audio sample sequence.

It is therefore possible to ensure that the five field digital audio sample sequence can be maintained in a combined digital video/audio synchroniser, when operating

15    with 525 line 59.94Hz video signals.

This allows such a "DATA" synchroniser to operate with both 625 50Hz and 525 59.94Hz video systems having a Serial Digital Interface (SDI), in which both video and audio data are combined.

20    It should be noted that the invention is not limited to interlaced TV signals, but is also applicable to non-interlaced TV signals. As applied to non-interlaced TV signals, the term "field" as used herein is intended to be synonymous with "frame".

25

## CLAIMS

1.  A synchroniser for a combined video and audio signal, which is in a format in which blocks of audio sample data are time-interleaved with the samples of successive fields of video sample data in a repeating sequence of numbers of audio samples per field of video samples, such that the number of audio samples in at least one of the fields of the sequence differ from that in the remainder of the fields of the sequence and that, prior to passage through the synchroniser, the total number of audio samples in each sequence is constant, comprising:

  a) a memory buffer having a capacity for storing at least two frames' worth of video and audio samples;

  b) write- and read-control circuits for writing incoming video/audio data sample to the memory buffer and reading the buffered data therefrom at rates which are respectively synchronised in frequency and phase with the incoming data and with a reference clock signal;

  c) resynchronising means for resynchronising the data read from the buffer by adjusting the sequence of read and/or write addresses used for reading and/or writing data from and to the memory buffer to avoid overflow or underflow of the buffer contents, so selectively repeating or dropping frames of the stored data; wherein

  d) the resynchronising means is operative, when resynchronisation is required, to select the timing of the resynchronisation operation and adjustment of the read address, and thereby the frame to be repeated or dropped, such that the total number of audio samples in the sequence of fields being read from the memory buffer when the resynchronisation is carried out is unchanged.

2.  A synchroniser according to claim 1 in which, when a resynchronisation operation is carried out, the read

address is adjusted by an amount corresponding to an integral number of frames' worth of data stored in the memory buffer.

5    3.        A synchroniser according to claim 1 or 2, wherein when a frame is required to be dropped, the resynchronising means is operative to select for dropping a frame having a total number of samples which is equal to the total number of samples in the first two fields of a sequence and when a
10   frame is required to be repeated, the resynchronising means is operative to select for repeating a frame having a total number of samples which is equal to the total number of samples in the last two fields of a sequence.

15   4.        An synchroniser according to any one of claims 1 to 3, wherein a first field of the sequence has a first predetermined number of samples, a second field of the sequence has a second predetermined number of samples and a last field of said second predetermined number of samples
20   and wherein, the resynchronising means is operative such that when a frame is required to be dropped, the frame selected for dropping is one which comprises both a field of said first number of samples and a field of said second number of samples and, when a frame is required to be
25   repeated, the frame selected for repetition is one which comprises two fields of said second number of audio samples.

5.        A synchroniser according to any one of the preceding claims, wherein the number of fields in a sequence
30   is five, four fields of the sequence having 801 audio samples and one having 800 samples.

6.        A synchroniser constructed and arranged to operate substantially as hereinbefore described with reference to
35   and as illustrated in the accompanying drawings.

| | |
|---|---|
| | Application number |
| | GB 9304587.0 |

**Relevant Technical fields**

(i) UK Cl (Edition   L  )    H4P (PSEX, PSX, PT);
                      H4R (RLS, RPNR)

(ii) Int Cl (Edition   5  )    H04N 5/04, 7/13

**Search Examiner**

K WILLIAMS

**Databases** (see over)

(i) UK Patent Office

(ii)    ONLINE DATABASE: WPI

**Date of Search**

4 JUNE 1993

Documents considered relevant following a search in respect of claims     1 TO 5

| Category (see over) | Identity of document and relevant passages | Relevant to claim(s) |
|---|---|---|
| | NONE | |

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