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(54) **Title:** ERROR CORRECTION IN A STACKED MEMORY

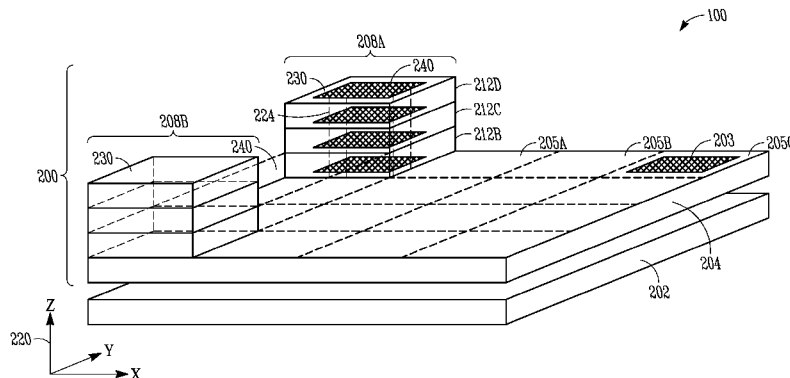


FIG. 2

(57) **Abstract:** Electronic apparatus, systems, and methods to construct and operate the electronic apparatus and/or systems include a stack of memory dies with user data and/or first level error correction data stored in a stripe across the memory dies. One such stack can include a second level error correction vault, such as a parity vault, to store parity data corresponding to the user data and/or first level error correction data. Additional apparatus, systems, and methods are disclosed.

WO 2011/082070 A3

A. CLASSIFICATION OF SUBJECT MATTER**G06F 11/16(2006.01)i, G11C 29/42(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: memory, stack, error correct, parity

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2007-0058410 A1 (SURESH N. RAJAN) 15 March 2007 See abstract; paragraph 51 - paragraph 78 and figures 6-9	1-35
A	US 2006-0164882 A1 (ROBERT NORMAN) 27 July 2006 See abstract; paragraph 19 - paragraph 27; claims 1-10 and figure 1	1-35
A	US 2008-0010435 A1 (MICHAEL JOHN SEBASTIAN SMITH et al.) 10 January 2008 See abstract; paragraph 36 - paragraph 43, paragraph 58 - paragraph 85 and figure 2	1-35
A	US 2002-0083390 A1 (THOMAS H. LEE et al.) 27 June 2002 See abstract; paragraph 17 - paragraph 23 and figures 2,3	1-35

 Further documents are listed in the continuation of Box C. See patent family annex.

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