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(54) Overspeed sensing system

(57) In an overspeed sensor for a gas turbine, a symmetrical pulse signal B of frequency proportional to rotational speed of a rotor is compared initially at 18 with a first reference period of a non-symmetrical pulse signal A for indicating existence of an overspeed condition, and subsequently, with a second greater reference period of signal A for indicating absence of overspeed. An output signal C is produced for correcting the overspeed, e.g. by restricting fuel flow to the turbine at 21. The two reference periods (ON and OFF) can be independently adjusted by reference data generator 24.

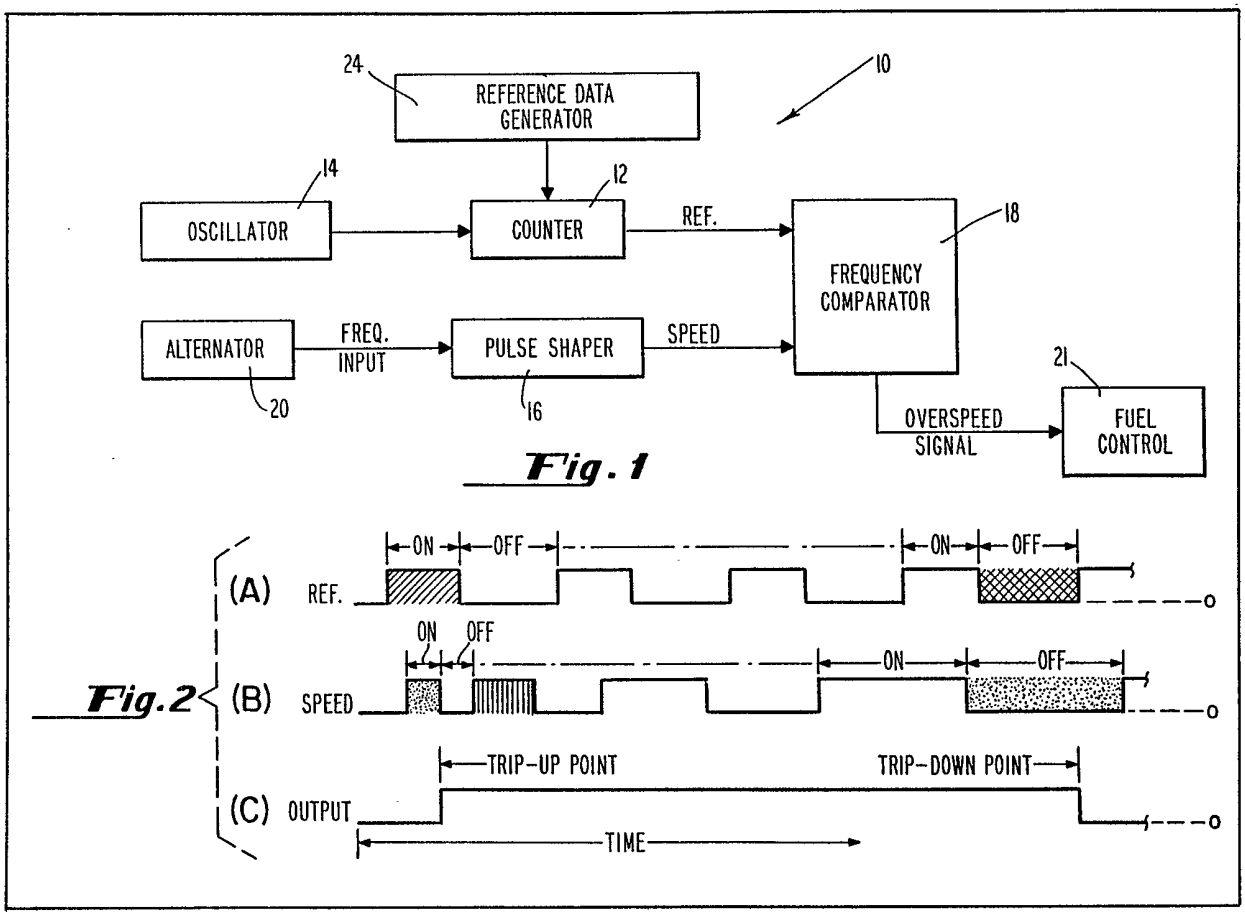

Fig. 1

Fig. 2

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The mathematical diagrams appearing in the printed specification were submitted after the date of filing, the diagrams originally submitted being incapable of being satisfactorily reproduced.

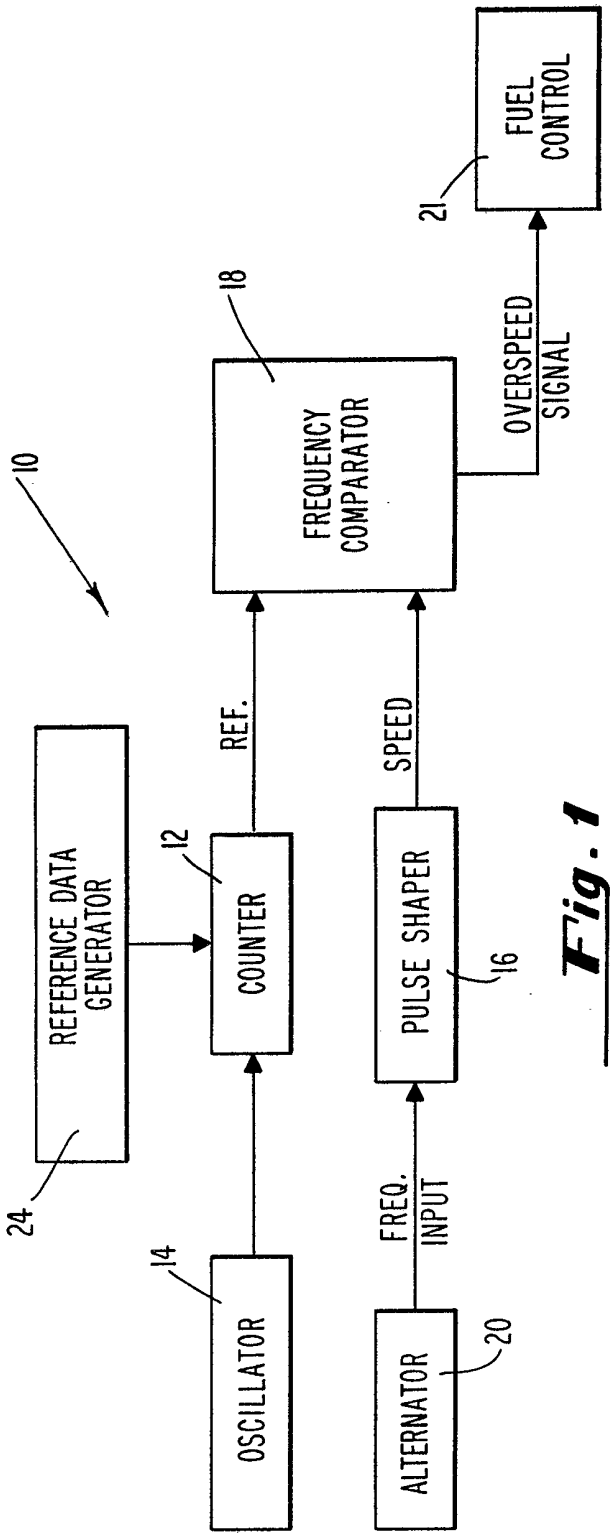
10
REFERENCE DATA GENERATOR
24
COUNTER
12
OSCILLATOR
14
REF.
FREQUENCY COMPARATOR
18
SPEED
PULSE SHAPER
16
FREQ. INPUT
ALTERNATOR
20
OVERSPEED SIGNAL
FUEL CONTROL
21

Fig. 1

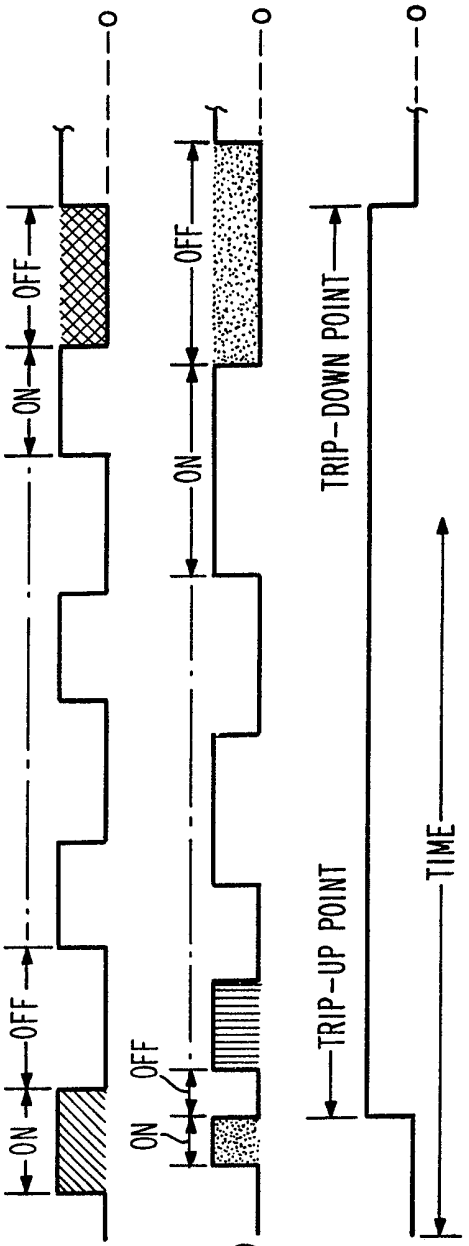
(A)
REF.
ON
OFF
ON
OFF
(B)
SPEED
ON
OFF
ON
OFF
(C)
OUTPUT
TRIP-UP POINT
TRIP-DOWN POINT
TIME

Fig. 2

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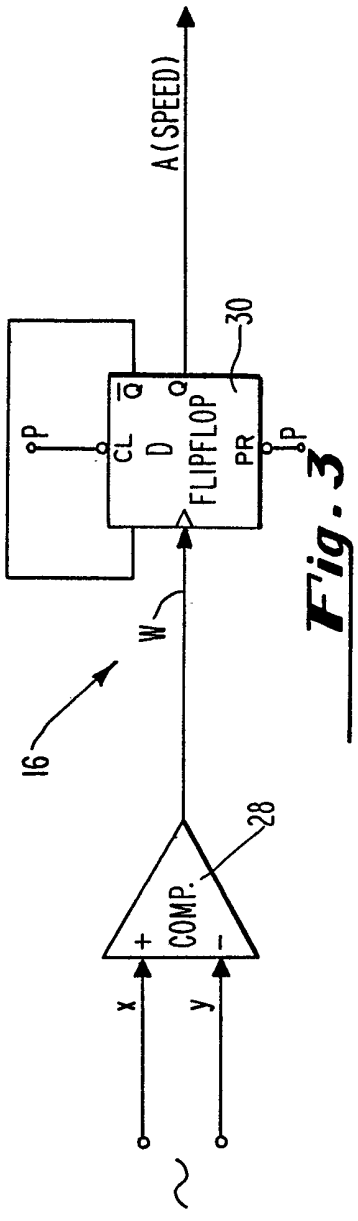

Fig. 3

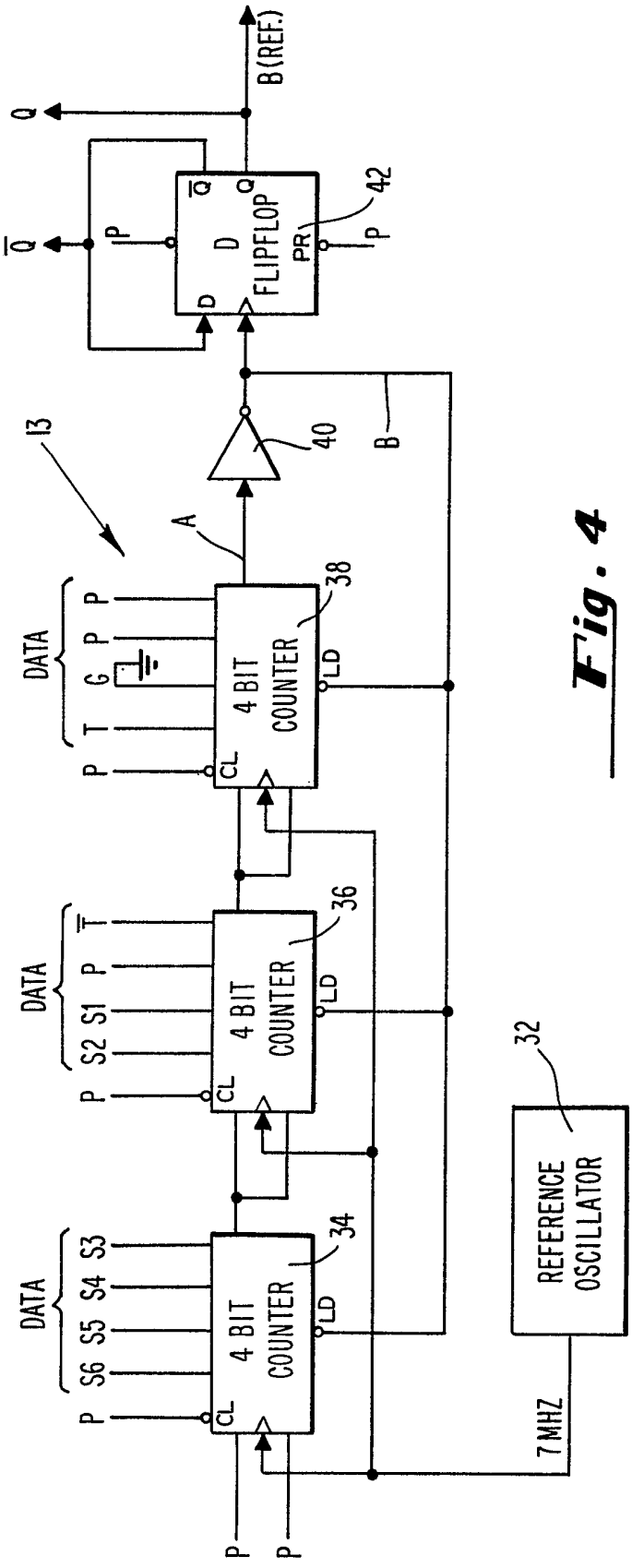

Fig. 4

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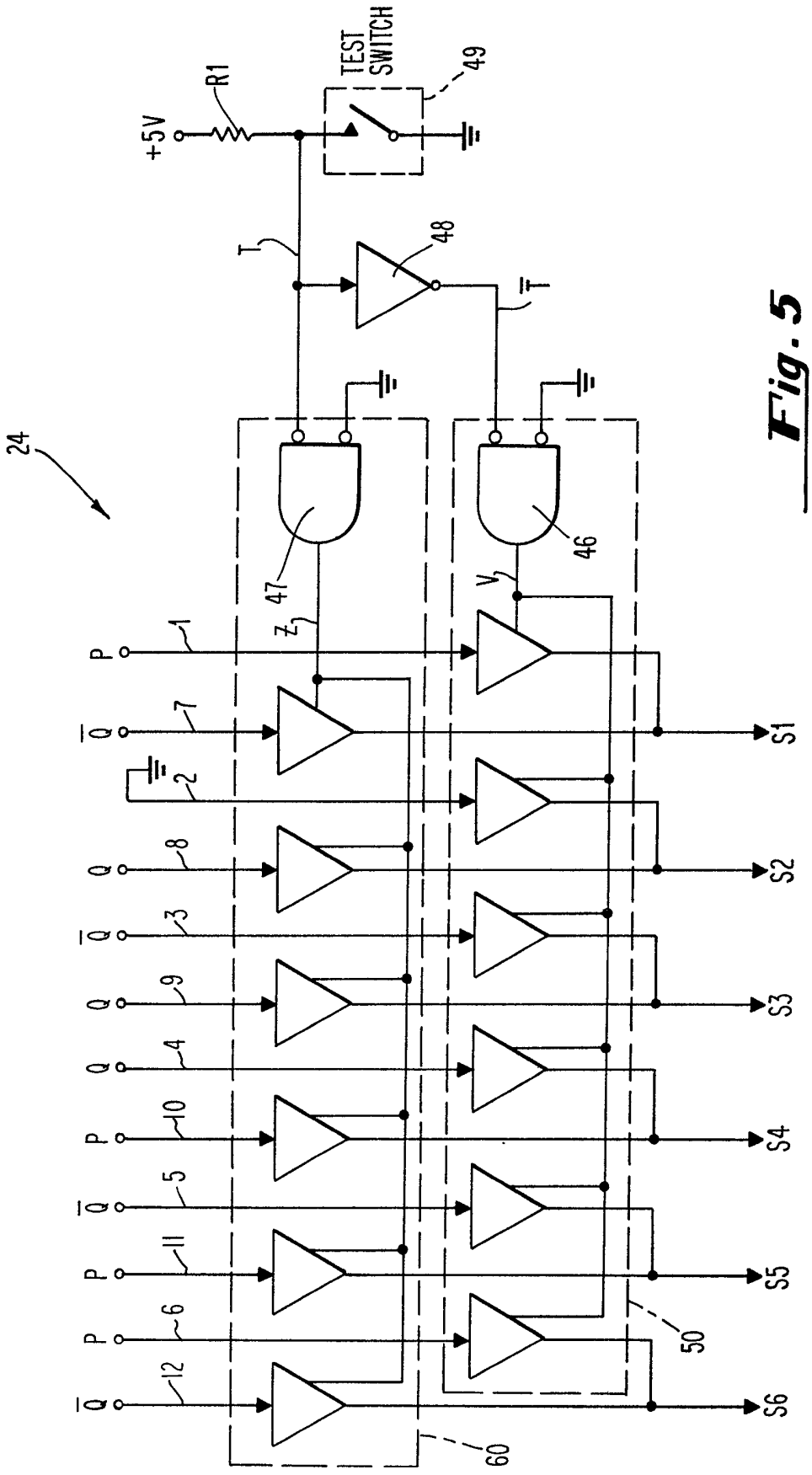

Fig. 5

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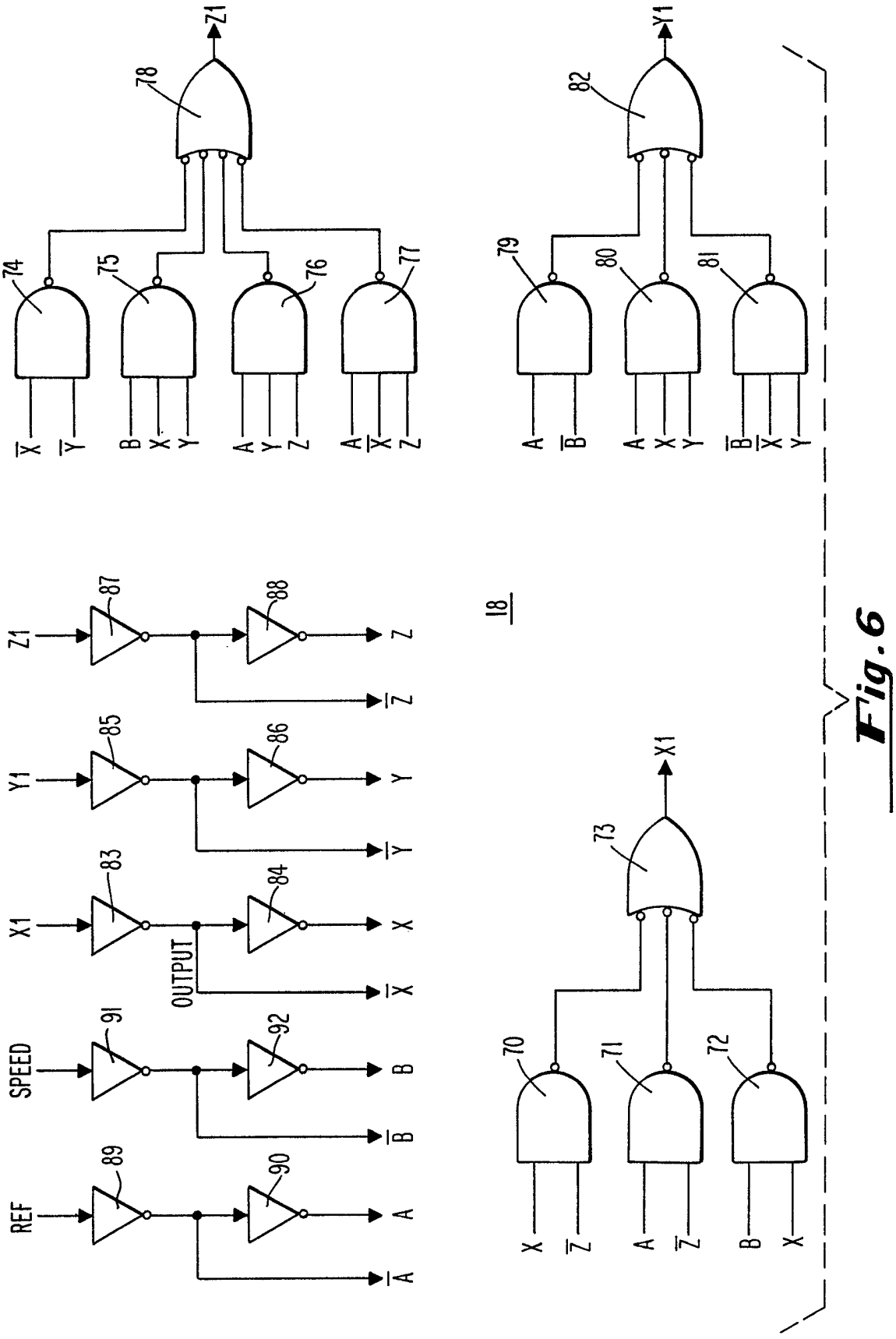


Fig. 6

SPECIFICATION

Overspeed sensing system

BACKGROUND OF THE INVENTION

The present invention relates to gas turbine engines, and more particularly to detection of an overspeed condition in such engines.

A current problem existing in gas turbine overspeed detection equipment is that it is typically based upon an analogue system with its accompanying inability to achieve a high accuracy standard. Precise accuracy is difficult to attain in these systems since they are based on a detection of voltage levels using circuitry that lacks immunity to noise interference, and is subject to component drift over time and temperature variations. Such analogue circuitry prevents a trip-point (a frequency at which overspeed is detected) and a trip-down point (a frequency at which overspeed disappears) from being accurately defined, and therefore is not particularly well suited for use in modern day aircraft.

Accordingly, it is an object of the present invention to provide an improved overspeed sensing system for a gas turbine engine.

It is another object of the present invention to provide an overspeed sensing system in a gas turbine engine with accurately defined trip points.

It is also an object of the present invention to provide an overspeed sensing system where its trip points are adjustable to achieve desired degrees of hysteresis.

It is another object of the invention to provide an overspeed detector for a gas turbine which is based upon a system for sensing signal transitions.

It is a further object of the invention to include a test function for determining proper operation in an overspeed sensing system.

It is an additional object of the invention to provide a digital overspeed sensing system for a gas turbine employing a finite-state asynchronous sequential machine.

SUMMARY OF THE INVENTION

In one form of the invention, there is provided a method for detecting overspeed in a rotating member by generating a substantially symmetrical signal corresponding to the speed of the rotating member, as well as generating an asymmetrical reference signal, and comparing the speed and reference signals to indicate overspeed and absence thereof. Apparatus is also provided for detecting rotational overspeed.

DETAILED DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of an overspeed detection system embodying one form of the present invention.

Figure 2 is a comparison of reference and speed signals shown in Figure 1.

Figure 3 is a block diagram of the pulse shaper circuit of Figure 1 which is utilized with a speed signal from a gas turbine rotor.

Figure 4 is a block diagram of a counter chain for producing reference frequencies.

Figure 5 is a block diagram of a data generator utilized with the counter of Figure 4.

Figure 6 is a schematic of an asynchronous sequential machine used a frequency comparator.

DETAILED DESCRIPTION OF THE INVENTION

In Figure 1 there is depicted one form of an overspeed sensor 10 for detecting overspeed in a rotating member such as a gas turbine rotor. The sensor 10 compares asynchronously a 50% duty cycle speed frequency signal with respect to a reference signal, which signal provides an ON period and an OFF period of unequal durations. The ON and OFF periods define two different frequency references.

In a gas turbine rotor, the speed signal is shaped sinusoidally and is derived from an A.C. generator 20 geared to an engine rotor. The sinusoidal speed signal is modified by a pulse shaper circuit 16 into a square wave to provide one input to a frequency comparator 18. The reference signal originates with an oscillator 14 whose output provides a clock for counting by a binary counter 12. Two different binary numbers related to the ON and OFF periods emanate from a reference data generator 24 and are consecutively loaded into the counter 12 from which a full count is made to produce the ON, OFF reference periods, enabling trip-up and trip down points to be determined. Two test periods, which are lower than the previous two reference periods, are also provided by the data generator 24 in order to move the trip points into a normal operating range to insure proper operation of sensor 10 prior to in-flight use.

The comparator 18 includes digital logic which alternately compares the speed signal with the reference signal or alternatively, the test signal, and provides a logic output that indicates which is the higher frequency. A logic one output of the comparator 18 indicates that an overspeed condition is present in the turbine rotor and the speed signal frequency exceeds the higher reference frequency, or has not dropped below the lower reference frequency, whereas a logic zero indicates an absence of such condition and the speed signal frequency is below the lower reference frequency, or has not exceeded the higher reference frequency. The logic output is applied to a solenoid operated value in fuel

control 21 for modulating fuel flow to a turbine combustor (not shown), such that when the output of the comparator 18 is a logic one, the fuel flow is relatively restricted, and when a logic zero, the fuel flows relatively unimpeded.

Exemplary speed and reference signals are illustrated in Figure 2 where the unequal periods of the hatched ON signal and cross-hatched OFF signal of Figure 2A are compared with the stippled speed signal of Figure 2B. To test for an overspeed condition starting with both signals zero or low in Figures 2A, B, the ON reference first undergoes a low to high transition after which the speed signal undergoes the same transition. When the speed signal returns to zero, while the reference signal remains high, the circuitry of Figure 1 trips to a high output signal to indicate that an overspeed condition is present. When the reference signal returns to zero, the speed signal is enclosed within the ON reference, and the frequency of the speed signal exceeds the frequency of the ON reference. The period of the positive ON reference, which is the reciprocal of its frequency, determines the trip-up points represented by a transition to a logic one output. The logic one output is applied to a fuel control to cause the turbine to reduce speed and this signal will remain high until the overspeed condition is eliminated. Figure 2B depicts an immediate decrease in engine speed from the trip-up point by a decrease of its frequency as indicated by an increase of the speed period. To determine when the overspeed condition has disappeared, the cross-hatched OFF signal is compared with the stippled negative speed signal. The output becomes a logic zero if the reference makes a high to low transition followed by a low to high transition in a period where the speed signal is continuously low. This indicates that the frequency of the speed signal is below the frequency of the OFF reference and the trip-down point is determined, which allows the fuel to the turbine to flow normally to the engine.

The periods of the ON, OFF references can be altered by changing the reference data applied to the counter 12. Thus, to raise the speed at which the trip-up point is established, the period of the ON reference is narrowed by increasing its frequency, whereas to lower the speed at which the trip-down point occurs, the period of the OFF reference is increased and its frequency is decreased. The ON, OFF reference frequencies can be shaped independently of each other to achieve sufficient hysteresis or separation to prevent chatter in the circuit of Figure 1. The signals of Figure 2A indicate that the reference signals remain constant, whereas the speed signal in Figure 2B varies depending upon its speed but with a 50% duty factor. This establishes an asynchronous relationship between the reference and speed signals which is accommodated by a frequency comparator 18 utilizing a finite-state asynchronous sequential machine.

In a preferred embodiment, the pulse shaper circuit 16 of Figure 1 for receiving the sinusoidal speed signal is depicted schematically in Figure 3. This signal is applied to inputs x,y of a LM111D zero crossing detector 28 for transforming the sinusoidal signal into a square wave. The square wave output of detector 28 is fed to input w of a 54LS74 D flip flop 30. The flip flop 30 changes state each time a positive pulse is received at input w which is transferred to its Q, $\overline{Q}$ output terminals. The output signal of flip flop 30 produces a square wave with a 50% duty cycle and reduces by one-half the frequency of the sinusoidal input speed signal.

A 12 bit counter 13 from which the reference signal is derived is shown schematically in Figure 4 and comprises three 54LS163 interconnected 4-bit counters 34, 36 and 38. The counter 13 is clocked by a 7 megahertz frequency which emanates from a Vectron CO238A stable, crystal controlled oscillator 32. The counter is loaded in its six least significant bits at its inputs with a number S1—S6 emanating from a data generator 24 in Figure 5. The remaining six signals loaded as most significant bits into the counter 13 comprising permanent high and low signals, P and ground G representing a binary one and zero, together with signals T and $\overline{T}$ from the data generator 24 which are high and low signals when test switch 49 is open. The high signal P is applied to each of the counter clear terminals. The number S1—S6 assumes a high and low value for loading into counter 13 to provide different durations for the ON, OFF reference periods. Outputs Q and $\overline{Q}$ of flip flop 42 are applied to inputs 3, 4 and 5 of the data generator 24 such that the state of flip flop 42 varies the number S1—S6 to determine the two shapes of the ON, OFF reference signals.

The data generator 24 comprises a plurality of 54LS365 gated buffers included in one group as 50 with control gate 47, and in a second group as 60 with control gate 47. The data generator 24 operates either in a normal or a test mode depending upon whether test switch 49 is respectively opened or closed. In a conventional mode of operation with the test switch 49 open, buffer group 50 is activated by a high or positive control signal V emanating from NOR gate 46. The gate 46 produces a high output signal when both input signals are low. One such input is permanently connected to ground, and its second input at T is derived from a +5 volt supply which is transmitted through resistor R1 to an input of a 54LS04 inverter 48 that transforms the +5 volts to a low output signal at $\overline{T}$. When both inputs to NOR gat 46 are low, its output is high to thereby cause the activation of buffer group 50.

The activation of buffer group 50 permits binary signals which are present on input terminals 1—6 to be transferred to output terminals S1—S6. The signals on inputs 1—6 include P, which is always high, ground which is low, Q and $\overline{Q}$ as determined by the state of flip flop 42. When flip flop 42 is in a state where output Q is high and $\overline{Q}$ is low, it indicates that a high number was previously loaded into counter 13 to provide the ON reference, and number S1—S6 was subsequently changed by the state of flip flop 42 to represent a low number in preparation for the next loading cycle. To provide the period of

the ON reference, a number 110101101011 is loaded inter counter 13 where the six most significant bits are predetermined by the high and low signals from P, G, T and $\overline{T}$, whereas the remaining six bits are provided by S1—S6. A decimal equivalent of the binary number is 3,435, which when subtracted from 4,095, the maximum count of counter 13, gives 660. Accordingly, the period of the ON reference is obtained by loading in the decimal number 3,435 from which counter 13 counts to 4,095. The counter 13 counts 660 pulses from oscillator 32 plus one additional pulse required for loading the next number therein. When the count 661 is multiplied by the period of oscillator 32, which is 94.43 microseconds, the period of the ON reference is obtained which corresponds to a frequency of 10,590 Hertz. The remaining reference signals are obtained in a similar manner. When the maximum count of 4,095 is reached by counter 13, signal A goes high and B goes low to allow S1—S6 corresponding to the lower number to be loaded into the counter data inputs. At the next available clock received by counter 13, signal A goes low by making signal B high to toggle flip flop 42 to change stage making $\overline{Q}$ high and Q low. This again changes the number S1—S6 so as to enable the high number to be again generated for loading into counter 13. The low number in the counter 13 requires a longer period to reach the maximum count of 4,095 thereby enabling a longer duration OFF reference signal to be produced which occurs at a frequency of 10,494 Hertz.

The normal operating trips points may be replaced by test trip-up and trip-down points in order to ascertain that the overspeed sensing circuit is operating properly when a turbine is rotating at ground level. This is achieved by closing the test switch 49 to ground one end of resistor R1. This grounding enables NOR gate 47 to activate the buffers within group 60 with signal Z and disable NOR 46 to deactivate the buffers within group 50. By enabling the buffers within group 60, the binary information present on inputs 7 to 12 is transferred to the outputs S1—S6 to change the data produced by generator 24. The binary number S1—S6 is loaded into inputs of the 12-bit binary counter 13 to provide two reference signals depending upon the state of flip flop 42. The counter is loaded with one number corresponding to a trip-up frequency at 8,824 Hertz and a trip-down frequency of 8,728 Hertz, where the lower frequencies are used because the rotor is operating at lower speeds.

The speed and reference signals of Figures 2A, B, are applied to a digital frequency comparator 18 incorporating a finite-state asynchronous sequential machine. The machine comprises a group of electrically interconnected combinational logic circuits as shown in Figure 6 and is able to process all possible combinations of the asynchronously occurring reference and speed signals in order to produce the required trip points. Sequential machines comprise circuits whose output depends not only on the inputs at a given period of time, but also on the prior sequence of inputs, and it follows a programmed sequence that is dependent on the output as well as the inputs. All of the possible combinations of speed and reference input signals, some of which are delineated in Figure 2, are accommodated by comparator 18, and are set forth below in a Primitive Flow Table.

AB	00	01	11	10	Output
a	①	7	–	2	0
b	1	–	3	②	0
c	–	7	③	4	0
d	6	–	5	④	1
e	–	9	⑤	4	1
f	⑥	9	–	2	1
g	1	⑦	8	–	0
h	–	7	⑧	2	0
i	10	⑨	5	–	1
j	⑩	9	–	4	1

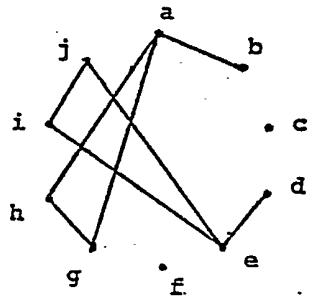
Beginning at the left in Figure 2, when the reference A and speed B signals are both zero, as indicated in column 00 in the Table, a stable state ① is defined and the output is a zero in row a and Figure 2c. As the A signal goes high by a negative to positive transition and B remains low as indicated by the 10 column, an unstable state 2 is identified because by definition there can only be one stable state in each row. Stable ② is established in a new row b with a zero output. The next event is for speed signal B to go high while reference A is high causing a transition to the 11 column in the table. This sequence is identified by an unstable state 3 and a new row c containing stable state ③, and the output signal remains zero.

The next event is for the speed B to go low while the reference signal B remains high causing a transfer from the 11 column to the 10 column in the Table creating an unstable state 4. The output signal changes to a one from a zero and thereby conforms to the characteristic previously defined for the sequential machine where a logic one signal is produced if the speed signal makes a low to high transition followed by a high to low transition in a period where the reference is continuously high, and stable state ④ is provided in row d. From state ④ there are two possibilities that can occur, namely, the reference can go low, or the speed can again go high. If the speed again goes high as indicated by a transfer from the 10 to the 11 columns, a new unstable 5 is created which becomes stable ⑤ in a new row e. The output signal does not change under state ⑤ because the previously defined characteristic for the machine is still satisfied. If the reference goes low with a corresponding transfer from the 10 to 00 columns, an unstable state 6 is produced in row d which becomes state ⑥ in row f with a one output.

From stable ⑥ there are two possibilities that can occur: the reference can go high, or the speed can go high. If the reference rises before the speed as by transferring from the 00 to the 10 columns, no new state is assigned for the above possibility since the original hatched condition is being repeated, and therefore the sequence transfers to unstable 2 and thence to stable ② where the output is zero. If from stable ⑥ the speed undergoes a low to high transition as exemplified by the straight-hatching without the reference rising first from the zero condition as in a transfer from the 00 to the 01 columns, the output remains a one as in Figure 2, and an unstable 9 is created for which a new row i is assigned for stable ⑨. Stable ⑨ represents a holding state, since the speed rises without the reference rising first so that there is no positive closure test in progress. From stable ⑨ there can be a return to stable ⑤ or, the speed may return to zero as indicated by a transfer from the 01 to the 00 columns. The output remains a logic one since no closure test is in progress, and an unstable 10 is assigned which becomes a stable ⑩ in a newly created row j. Therefore, stable ⑩ like ⑨ describes a holding position since no test is in progress and both outputs are a logic one. Stable ⑦ and ⑧ for which new rows g and h have been assigned parallel stable ⑨ and ⑩ except that the outputs produced are both logic zeroes.

Various dashes positioned within the Table indicate a "don't care" possibility and a transition from columns 00 to 11 from stable ①, ⑥ and ⑩ is not viable, because a likelihood of both the speed and reference going positive simultaneously is not considered in an asynchronous machine. Sequences for defining the characteristic shown by the cross-hatched OFF reference with respect to a stippled negative speed signal where an overspeed condition is no longer present are also contained within the Primitive Table. With the speed and reference appearing as shown in Figures 2A, B, the signal transitions just prior to the negative cross-hatched and stippled signals place the machine in state ⑤ with both the reference and speed high. The first transition from state ⑤ is for the speed to return to zero so there is a transfer to unstable state 4 in row e, and thence to stable ④ in row d. The next sequence is for the reference to drop to zero, and there is a transition from the 10 column to the 00 column to unstable 6 in row d, and thence to stable ⑥ in row f. The next transition in the closure test occurs in a transfer from the 00 to the 10 columns indicating that the reference rises before the speed, and there is a transfer to unstable 2 in row f and thence to state ② in row b. The output is a logic zero in this sequence and the frequency of the speed signal is below the reference frequency to determine the trip-down point indicating that the overspeed condition is obviated. When the speed signal rises after the reference signal rises, there is a transition from the 10 column to the 11 column to unstable 3 in row b and thence to row c and stable ③ to complete the negative closure test. All the remaining transitions in the Table indicate other possible signal sequences that may arise in the operation of the frequency switch that are accommodated by the sequential machine. The various sequences of the reference and speed signals indicate that the machine must have a memory of its previous sequence to accommodate the next sequence.

The machine based on the ten stable states of the Table is complex, since it requires $2^4 = 16$ or four feedback loops to defin ten states. To simplify design and operation, the various stable states are merged whereby any two rows are combined independent of output provided the state in a column are identical. A Merger Diagram assists in combining of the various rows each of which contains a stable state of the Primitive Table

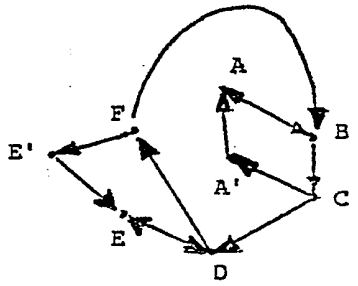


The Diagram indicates by a straight line that two rows of the Primitive Table may be merged, whereas three are indicated by a triangle. The vertices of the triangle a-g-h indicate a merger of states ①, ⑦ and ⑧ and e-i-j a merger of ⑩, ⑨ and ⑤. Merger of rows a-b and e-d after the merger of e-i-j and a-g-h are not utilized because it does not aid the reduction. By merging the states of the Primitive Table, a Merged Flow Table results where an upper case letter assigned the left-hand column references six states that the machine must accommodate, whereas identifiers placed atop each column refers to various combinations of the reference and speed signals.

AB	00	01	11	10
A	①	⑦	⑧	2
B	1	–	3	②
C	–	7	③	4
D	6	–	5	④
E	⑩	⑨	⑤	4
F	⑥	9	–	2

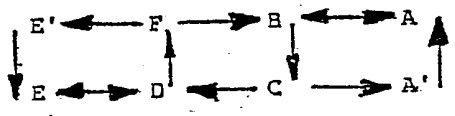
The Merged Table indicates that the ten states of the Primitive Table has been reduced to six states whereby the machine can process the sequences of Figure 2 with three, $2^3 = 8$, feedback loops.

In asynchronous machines, an oscillation or race condition due to a simultaneous change of two variables is not desirable. In order to avoid such a race condition, an adjacency diagram determines which rows of the Merged Table are adjacent to each other wherein a later assignment of variables to the states A to F produce only a one variable time change at a time as the machine transitions between adjacent states.



The adjacency diagram indicates by a double arrow that state A is contiguous to B and B to A through stable ① of the Merged Table which transitions to stable ② in state B via unstable 2, and from state B, a horizontal movement from stable ② to unstable 1 resulting in a vertical transition to stable ① in state A. State B is adjacent to C by a horizontal shift to unstable 3 ending in stable ③ in state C resulting in an arrow from B to C. A horizontal shift within state C to unstable 4 from stable ③ results in movement to stable ④ in D, and an arrow is provided from C to D. In state D, a horizontal shift from stable ④ to unstable 5 provides a vertical transition to stable ⑤ in state E and to stable ⑥ in state F as indicated by the two arrows extending from D. State E is adjacent to D by a horizontal movement to unstable 4 from stable ⑤, and a resulting vertical transition to stable ④ with an arrow from E to D. A horizontal movement from stable ⑥ to unstable 2 and a vertical transition to stable ② in state B indicates adjacency which allows an arrow from states F to B. A horizontal movement from stable ③ to unstable 7 in state C with a vertical transition to stable ⑦ in state A is required, but because state A cannot be adjacent to state B, B to C and C to A all at the same time, a quasi-stable state A′ is used to break the chain.

State A′ is adjacent to both A and C and therefore a transition from state A to C is achieved by first transitioning to A′. A quasi-state E′ is also provided because state F cannot be adjacent to B, D to F, and F to E at the identical time. The six states of the Merged Table have been increased to eight by an addition of the two quasi-states A′ and E′, which are within the limit of eight required for the three feed back signals and the states have been arranged whereby only one stage variable can be changed at a time as required for asynchronous operation. The adjacency diagrams may be conveniently rearranged ake in block 3 folio 16



The rearranged adjacency diagram allows an assignment of variable X, Y Z in binary form to be made by a State Assignment in a 3-variable Karnaugh map. The state variables X, Y, Z provide memory in the machine by defining its present state. Variables are identified in the State Assignment with each state whereby there is only a one variable change in transferring between adjacent states as shown below.

Z \ X Y	00	01	11	10
0	E′	F	B	A
1	E	D	C	A′

Since the asynchronous machine utilizes the speed and reference signals in addition to state variables X, Y, Z, a 5-variable Karnaugh map is required for its design in the form of an Excitation Matrix as shown below.

$\overline{Z}$

A B \ X Y	00	01	11	10
00	xxx	010	100	100
10	001	000	xxx	100
11	xxx	xxx	111	100
10	xxx	110	110	110

Z

A B \ X Y	00	01	11	10
00	001	010	xxx	xxx
01	001	xxx	101	100
11	001	001	111	xxx
10	011	011	011	xxx

The state variables X, Y, Z corresponding to those of the State Assignment are listed along the top of the Matrix, wherein binary sequences of the reference A and speed B signals are listed along the sides and correspond to the sequences of the columns in the Merged Table. The state assignment of variables X, Y, Z for state E is 001 as in the State Assignment and corresponds to a first column of the right Excitation Matrix having the same variable 001 for variables X, Y, Z. Therefore each one of eight states listed in the State Assignments is identified with a column in the Matrix which embraces four cells.

Once the state of the machine is defined in the Excitation Matrix by variables X, Y, Z and four cells, a particular one of the four is selected by any of the four reference and speed sequences listed in its left column. Contents of each cell represent a next state of the machine after the speed and reference sequence is changed, and are indentified by variables X1, Y1, Z1. To indicate the contents of state E in the first column of the right Matrix, the State Assignments and Merged Table are referenced. In state E of the Table, three stable states ⑩, ⑨, ⑤ and one unstable 4, which becomes stable in state D, are listed. Stable ⑩ relates to column 00 in the Table and the first row of the Matrix, and corresponds to variables 001 from the State Assignments. The binary representation of 001 or X1, Y1, Z1 is contained in the first cell in state E of the matrix, and indicates that it is the same as the state variable X, Y, Z listed by the outside identifiers 001 of the Excitation Matrix. If the current state of machine represented by variables X, Y, Z are equal to variables X1, Y1, Z1, the next state of machine, it is stable, which represents stable ⑩. For stable ⑨ in state E the speed, reference sequences 01, which identifies the second row, first column of the Matrix. The cell contents remain 001, since the machine remains unchanged when transitioning from stable ⑩ to ⑨. In the third cell of the Matrix, the contents remain 001 because the machine remains unchanged in transferring between stable ⑨ to ⑤. By referring to the State Assignments, the contents of the fourth cell in state E change to 011 from 001 because in transferring to unstable 4 from stable ⑨ or ⑤ the machine becomes unstable and the variables X, Y, Z do not match X1, Y1, Z1. The machine becomes stable in state D as indicated by the Merged Table in an adjacent cell of the second column, fourth row, where the contents are also 011. Stability is indicated in state D of the Matrix by the current state of the machine represented by column identifiers 011 (X, Y, Z) being equal to contents 011 (X1, Y1, Z1) of the cell. The remaining cell contents are derived in a similar manner.

The Excitation Matrix allows Boolean equations to be written from which the hardware for the asynchronous sequential machine is implemented and are:

$$X1 = X\overline{Z} + A\overline{Z} + BX$$

$$Y1 = A\overline{B} + AXY + \overline{B}\overline{X}Y$$

$$Z1 = \overline{X}\overline{Y} + BXY + AYZ + A\overline{X}Z$$

$$OUTPUT = \overline{X}$$

The variable X_1 which is the first bit of the group of three bits in a cell, is obtained by searching for a largest contiguous cell group pattern in both Excitation blocks where its value is a one in the first or X position. In the left block, the largest group of one's in the first bit position is in two right columns where seven one's are found. One cell has an x or "don't care" in the first bit position indicating that this bit can be a one or zero, so a block of eight continguous cells have a one in the first bit position. A minimum

Boolean equation describing this block is $X\overline{Z}$, since X and $\overline{Z}$ are the only common identifiers of this group. This expression represents a logic AND gate so that when X is a binary one and Z is a binary zero, the function X1 will be a binary one. Another group of eight one's is found in the first bit position on the left Excitation block in rows three and four wherein x's are considered as one's, and the minimum Boolean expression is written as $A\overline{Z}$ since A and $\overline{Z}$ are common to this group. In the right Excitation block, a group of four cells having a one in the first bit position is located at the intersection of the third and fourth columns with the second and third rows. Another similar grouping of one's in the same location is found in the same location of the left block. Since the Karnaugh map includes five variables, the left and right blocks may be superimposed upon each other and a minimum Boolean expression BX may be written. The function X1 is equivalent to a logical OR function and is equal to a binary one if any of the AND functions $X\overline{Z}$, $A\overline{Z}$ or BX is equal to one. The variables Y1 and Z1 are similarly obtained.

The expression for an output signal corresponding to the output of Figure 2C is derived by noting in the Primitive Flow Table that a one output is obtained for stable ④, ⑤, ⑥, ⑨ and ⑩, and these states correspond to states D, E and F in the Merged Table. A zero output is obtained for stable ①, ②, ③, ⑦ and ⑧ and correspond to states A, B and C. Referring to the State Assignments, States D, E and F occur in the left portion, whereas states A, B and C occur in the right portion. By inspection of the variables X, Y, Z the output becomes a one for $\overline{X}$.

Figure 6 depicts an asynchronous sequential machine using gating circuitry to implement the derived Boolean equations for X1, Y1, and Z1. To generate the variable X1, the logic terms A, B, X and $\overline{Z}$ are provided as inputs to 54LS00 NAND gates 70, 71, 72, and their respective outputs become inputs to a 54LS10 NAND gate 73 shown in an alternate representation. A circled output of gate 70 applied to a circled input to gate 73 negates their effect and therefore, if both variables of terms $X\overline{Z}$, $A\overline{Z}$ or BX are high, a low output is produced by either gates 70, 71, or 72 which is applied to gate 73. When any of the inputs to gate 73 is low, its output is high. A high X1 signal fed back to serial inverters 83, 84 causes variable X to become high, the output $\overline{X}$ low after passing through inverter 83. The logic terms A, $\overline{B}$, X, $\overline{X}$ and Y are applied to NAND gates 79, 80, 81, where gates 80, 81 are 54LS10 models, whose outputs are applied to NAND gate 82 to produce the variable Y1. The logic terms A, B, X, $\overline{X}$, Y, $\overline{Y}$ and Z are applied to NAND gates 74, 75, 76 and 77 whose outputs are applied as inputs to a 54LS20 NAND gate 78 to produce variable Z1. The variables Y1, Z1 are fed back as input signals to respective chains comprising inverters 85, 86, and 87, 88. The inverter chains are used as buffers and produce output signals X, $\overline{X}$, Y, $\overline{Y}$ Z and $\overline{Z}$ representing the current state of machine. The signals X1, Y1 and Z1 are fed back with a propagation delay of approximately forty nanoseconds.

The reference A and speed B signals generated in accordance with the circuitry of Figures 3, 4 are respectively applied to inverter chain 89, 90, and 91, 92 and output signals A, $\overline{A}$, B and $\overline{B}$ are applied as inputs to the NAND gates to produce variables X1, Y1 and Z1. The sequential machine operates like it was defined in the Primitive Flow Table and in conformance with the speed and reference sequences of Figure 2.

It will be understood that the foregoing suggested apparatus and method as exemplified by the Figures, is intended to be illustrative of a preferred embodiment of the subject invention and that many options will readily occur to those skilled in the art without departure from the spirit or the scope of the principles of the subject invention.

CLAIMS

1. A method for detecting overspeed in a rotating member, comprising the steps of:

a) generating a substantially symmetrical signal corresponding to speed of said rotating member;

b) generating an asymmetrical reference signal; and

d) comparing said speed and reference signals to indicate overspeed and absence thereof.

2. A method for detecting overspeed in a rotating member, comprising the steps of:

a) shaping a speed signal produced by said rotating member to obtain substantially equal ON and OFF periods;

b) shaping a reference signal to obtain unequal ON and OFF periods wherein the OFF period is of longer duration than the ON period; and

c) comparing the ON, OFF periods of the speed and reference signals to determine a presence of an overspeed condition by the ON reference enclosing the ON speed period, and a discontinuance of an overspeed condition by the OFF speed enclosing the OFF reference period.

3. A method of claim 2 wherein said comparing step is performed asynchronously.

4. A method of claim 3 comprising a step of producing a first level signal to indicate a trip-up point when the ON reference encloses the ON speed period, and a second level signal to indicate a trip-down point when the OFF speed encloses the OFF reference period.,

5. A method of claim 4 including a step wherein said first and second trip point level signals are applied to a fuel control of a turbomachine for reducing the overspeed condition.

6. A method of claim 5 including a step wherein the trip points may be independently varied by adjusting the duration of the reference ON, OFF periods to achieve hysteresis.

7. A method of claim 6 including a step wherein a higher trip-up point is obtained by shortening

the duration of the ON reference and a lower trip-up point is obtained by lengthening the ON reference period.

8. A method of Claim 7 including the step of moving the trip points to test for proper operation prior to normal use.

9. A method of detecting overspeed in a rotating member, comprising the steps of:

a) generating a symmetrical signal whose frequency is a function of speed in said rotating member and having ON, OFF periods of equal durations;

b) generating predetermined non-symmetrical first and second reference period signals;

c) asynchronously comparing said speed signal with said first and second reference period signals;

d) producing a trip-up point when the first reference period signal incurs a positive transition prior to a positive transition of said speed ON period, and a negative transition after a negative transition of said speed ON period; and

e) producing a trip-down point when the speed OFF period makes a negative transition prior to a negative transition of the second reference period signal, and a positive transition after a positive transition of the reference period signal, said trip-up and trip-down points being separated from one another to provide hysteresis

10. The method of claim 9 wherein the generating of said symmetrical speed signal is produced by shaping a sinusoidal signal representative of rotation speed into a substantially 50% duty cycle square wave.

11. The method of claim 10 wherein trip-up and trip-down frequency points may be determined independently by shaping the first and second reference period signals.

12. An overspeed detection system for a rotating member, comprising:

a) means for generating a frequency signal corresponding to a speed of the rotating member;

b) means for generating first and second reference period signals wherein said first period is shorter than said second period;

c) an asynchronous frequency comparator for receiving both said reference period signals and rotational speed frequency signal; and

d) said frequency comparator producing a first output level signal to indicate rotational overspeed when the speed signal is compared with said first reference period signal, and producing a second output level signal when the speed signal is compared to said second reference period signal indicating an absence of said overspeed condition.

13. An overspeed system in accordance with claim 12 wherein said frequency comparator comprises a finite-state asynchronous sequential machine.

14. An overspeed system in accordance with claim 12 wherein said first and second output level signals are applied to a means for correcting and controlling said overspeed condition.

15. An overspeed system in accordance with claim 12 wherein said rotating member comprises a turbomachine rotor.

16. An overspeed system in accordance with claim 15 wherein said first and second output level signals are applied to a turbomachine fuel control for reducing said overspeed condition.

17. The overspeed system of claim 12 wherein said means for generating said reference period signals comprises a digital counter.

18. The overspeed system of claim 17 comprising generator means for producing first and second datum for loading into said counter to produce said first and second reference period signals.

19. An overspeed system of claim 18 wherein flip flop means having first and second states are coupled to said generator means to alter its output for producing said first and second datum.

20. An overspeed system in accordance with claim 19 wherein means are coupled to said generator for producing third and fourth reference period signals which are respectively longer than said first and second reference period signals for testing said system.

21. A method of detecting overspeed or an overspeed detecting system substantially as hereinbefore described with reference to the drawings.

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